R&D towards a Si-W ECAL

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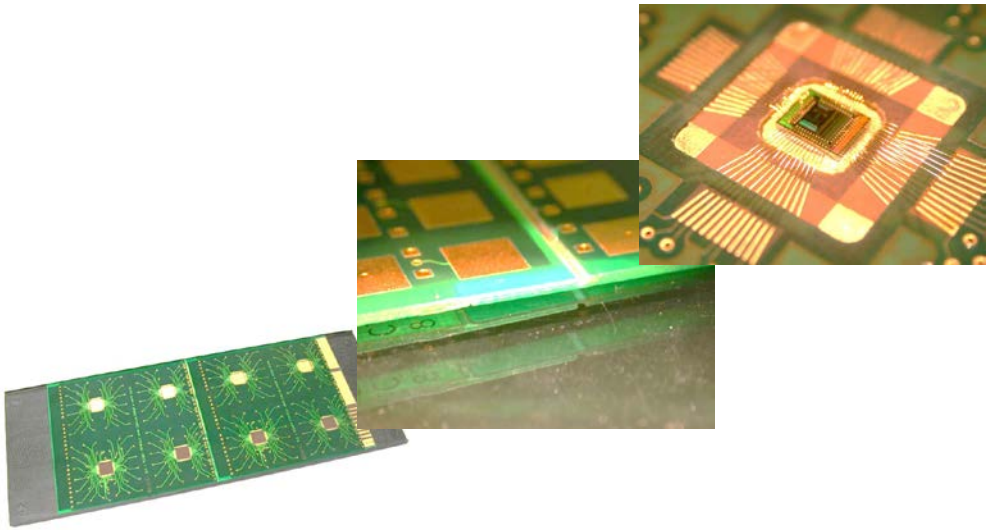
From Physics prototype…to technological prototype

Pixel density increased by a factor 10 while S/N target gained a factor 1.5

Global optimization needed :

- Sensors
- Chips
- integration
- Powering & cooling
- DAQ & software



Extremely constrained design

- Large sensors : uniformity, Si purity, integration
- Chips : mixed signal, channel nb., naked die bonded into pcb
- State of the art pcb processing : flatness, non homogeneous stack-up
- composite structure : manufacturing, mechanical & thermal characteristics

Technological prototype : a first build

A small detector of intermediate technicity that can be easily tested in beam

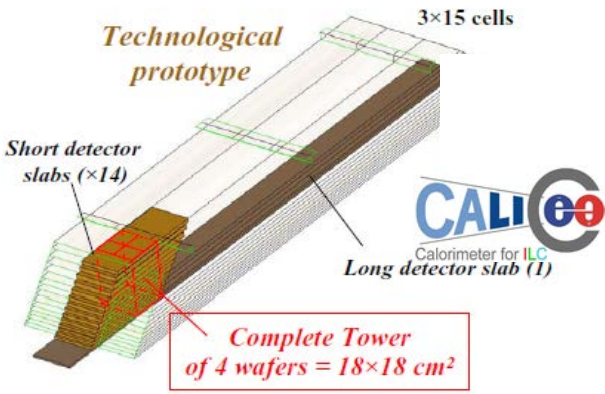
- Slabs with a single detection layer (aka 'U' slab)
- ¼ instrumented channels : 4 chips per slabs
- Nominal sensor, SKIROC2 prototype chip

Environment setting up : DAQ, power, grounding, software

- Will remain the similar for next development steps
- Good experience to further enlarge the scale

Rehearsal of integration process

- Gluing, stitching, costing
- Team organization



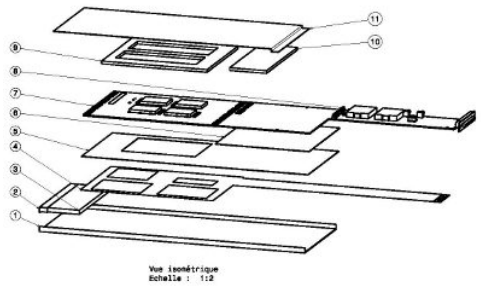
‘U’ technological prototype

Validation of concept in test beams : March & July’12

- S/N always better than 10 w.r.t gain & location, typ. ~15
- Good uniformity
- Traces and showers seen
- Quasi nominal analog part chips & DAQ

First signals seen from 9cm sensors (HPK)

Validation of the measurement & DAQ chain



Vue isométrique
Echelle : 1:2

Nomenclature de slab U court

Quantité	Référence	Type	Nomenclature	Révision
1	short_structure_U	Assemblage	1	
1	FEV8_CIPB	Pièce	7	
1	butee U	Pièce	2	
1	capton plateau test	Pièce	4	
1	adaptatrice card SMBV3	Pièce	6	
1	calle wafer	Pièce	5	
1	calle CHIP	Pièce	9	
1	capot SLAB U	Pièce	11	
1	BUTEE ASU	Pièce	3	
1	calle SMBV3	Pièce	8	
1	CALLE SMBV3 SUP	Pièce	10	

Nomenclature de short_structure_U

Quantité	Référence	Type	Nomenclature	Révision
1	short_C	Pièce	1.1	
1	short_comp_couche1	Pièce	1.2	
1	short_comp_couche2	Pièce	1.3	

How to do better ?

Physics simulations : optimize number of layers, pixel size, overall thickness ; impact of dead zones… (see tomorrow)

Instrumentation of every pixels in a slab : 16 chips base pcb (FEVx)

Long SLAB (7 to 10 FEVx in a row) : signal integrity ?

Set-up power pulsing features, design of power supplies

Alveolar structure : check mechanical properties and integration

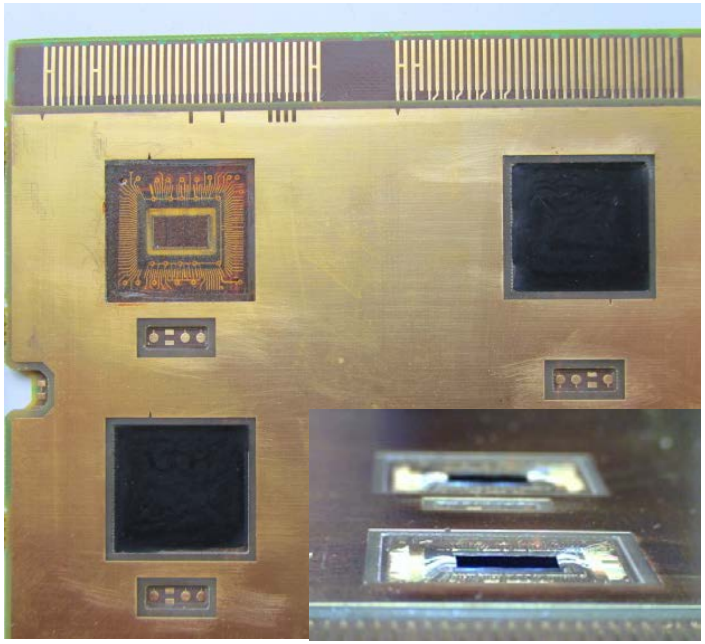
Validation in magnetic field & radiations (powering stages)

Costing, mass production processes…

Next steps : fully instrumented ASU

Base option : Chip On Board (COB)

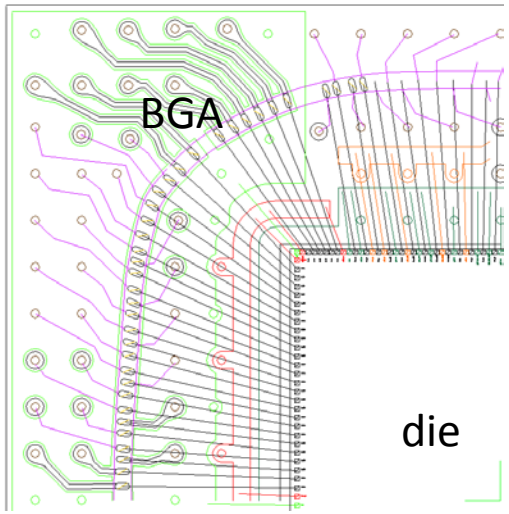
- Allow single or double layer slabs
  - Best optimization of traces length
- Flatness issue : integration, gluing of sensors
- Very few manufacturers ; testability (dies covered by resin) ?



Alternate option : Chip In Package (CIP)

- Classical PQFP used for first build : too thick
- Ultra thin BGA under study : promising
  - Feasibility of leadframe
  - Impact on Xtalk, noise
  - Length of pixel-chip traces divided by 2-3

  w.r.t. PQFP design

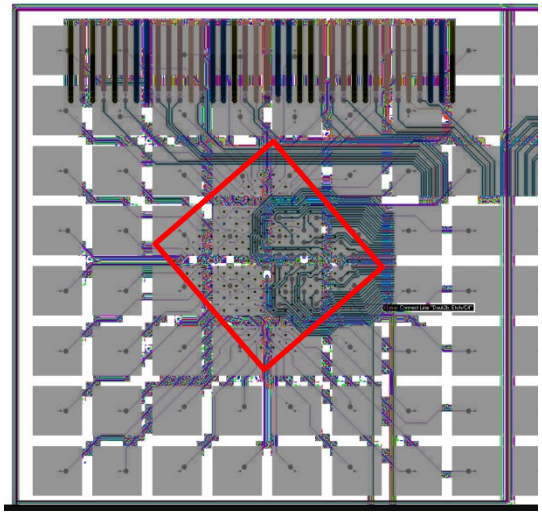


Next steps : design of SLAB

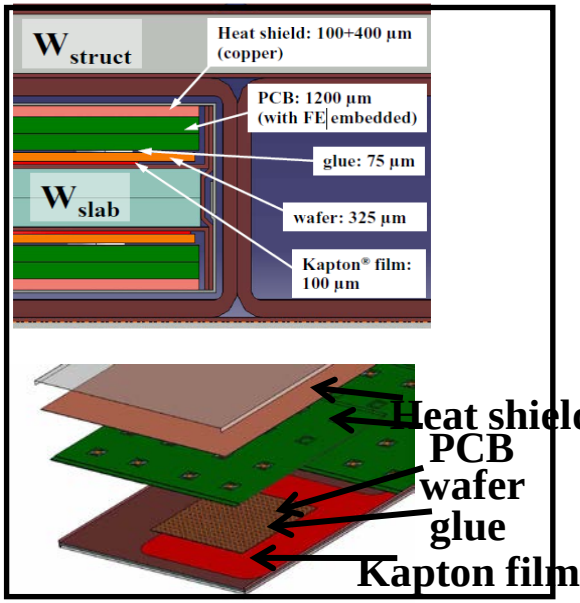
Single layer ‘U’ : BGA : ~5 mm thick alveoli

Double layer ‘H’ : COB (7 mm) or BGA (10mm)

- COB is being manufactured
- BGA design has started
  - Longest analog trace is ~2 cm



BGA pattern : 1/16th of the PCB



Advanced package technologies

- Thicknesses as low as 0.5mm
- Ball bonded Flip chip
- Less risky 1.2 mm thick very thin

“classical” BGA

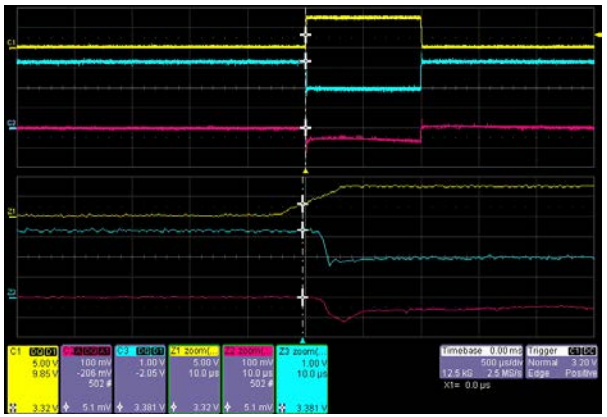
- Allow efficient routing of pcb traces and digital/analog separation

Next steps : power pulsing

Current pulses from few 100 mA to several A (~10 A), Voltage remains constant (hopefuly)

- 1st option : Battery or huge capacitance : few mF to few 100 mF, regulator (current design)
- 2nd option : current source (charge pump) with regulated voltage output (~mobile phone charger)
  - Allow poor power distribution network
  - Power pulsing only

Command : 1% duty cycle
Vin= 3.3 V
Load : 1 A on 1 Ohm, 1 ms, rise=1 us
Vin undershoot : 100 mV



Specific setup being build

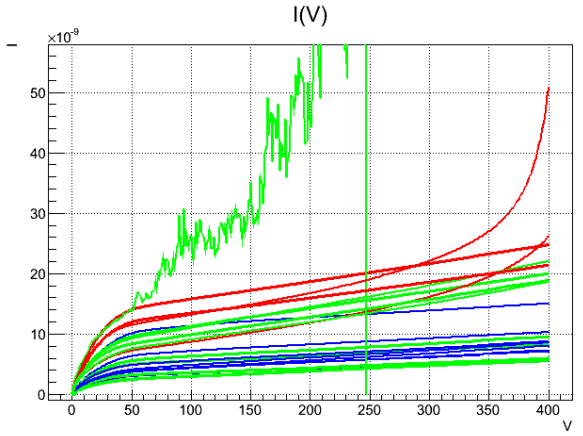
- Test in B field (~next ECAL test beam)
- Power distribution through connectors
- December Test beam : FEV w/o decoupling caps

Next steps : sensors optimization

Optimization w.r.t. Crosstalk (aka. “Square events”), Dead area, size (=cost)

HPK sensors (in collab. with JP institutes)

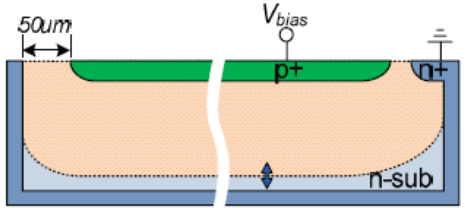
- Laser cut allow to lower dead area down to 700 µm : OK
- Option without guard rings or segmented GR (R&D from LLR)
  - Laser cut : blue
  - No GR : red
  - Segmented GR :green
- Will need more tests : Xtalk measurement



Determine optimal size : yield, cost, integration

R&D : New edgeless sensors from VTT

- No guard rings : no crosstalk
- Dead area ~ 50 µm
- Cost++ (prototyping)
- Samples received last month

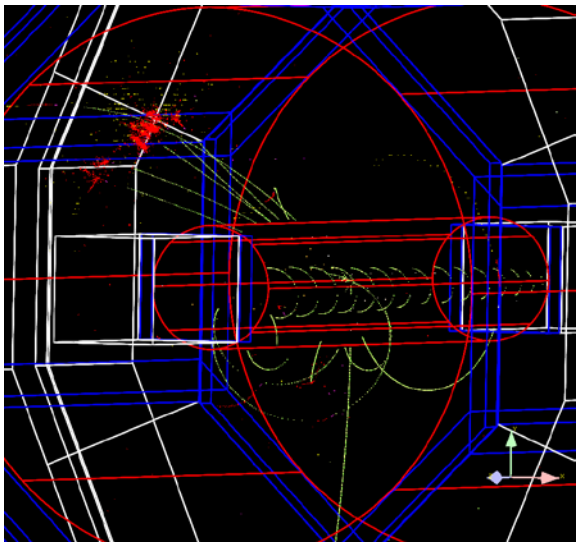


Need to enlarge manufacturer pool : OnSemi, …

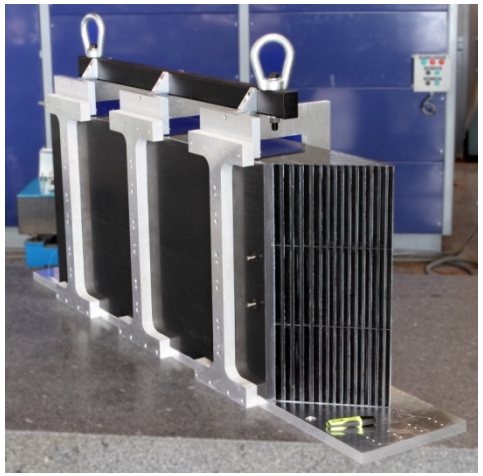
Toward a module #0

Long SLAB : 7-10 ASU, up to 2m

- Signal integrity along the SLAB
- Integration of fragile units
- Part of the current prototyping effort

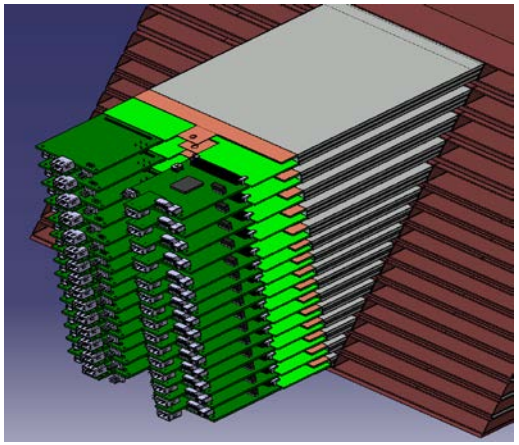


Ongoing work will lead to guidelines for the detector design for an ILC experiment



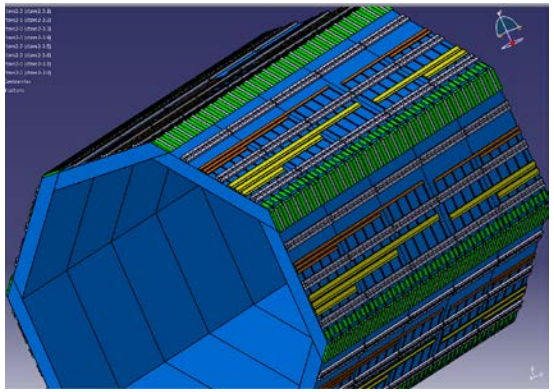
Versions of technological prototype will help to choose the best design option validated by test beams at system level.

Questions ?



Going step by step through R&D, “final” (EUDET) design should be reached within a year (at least few slabs).

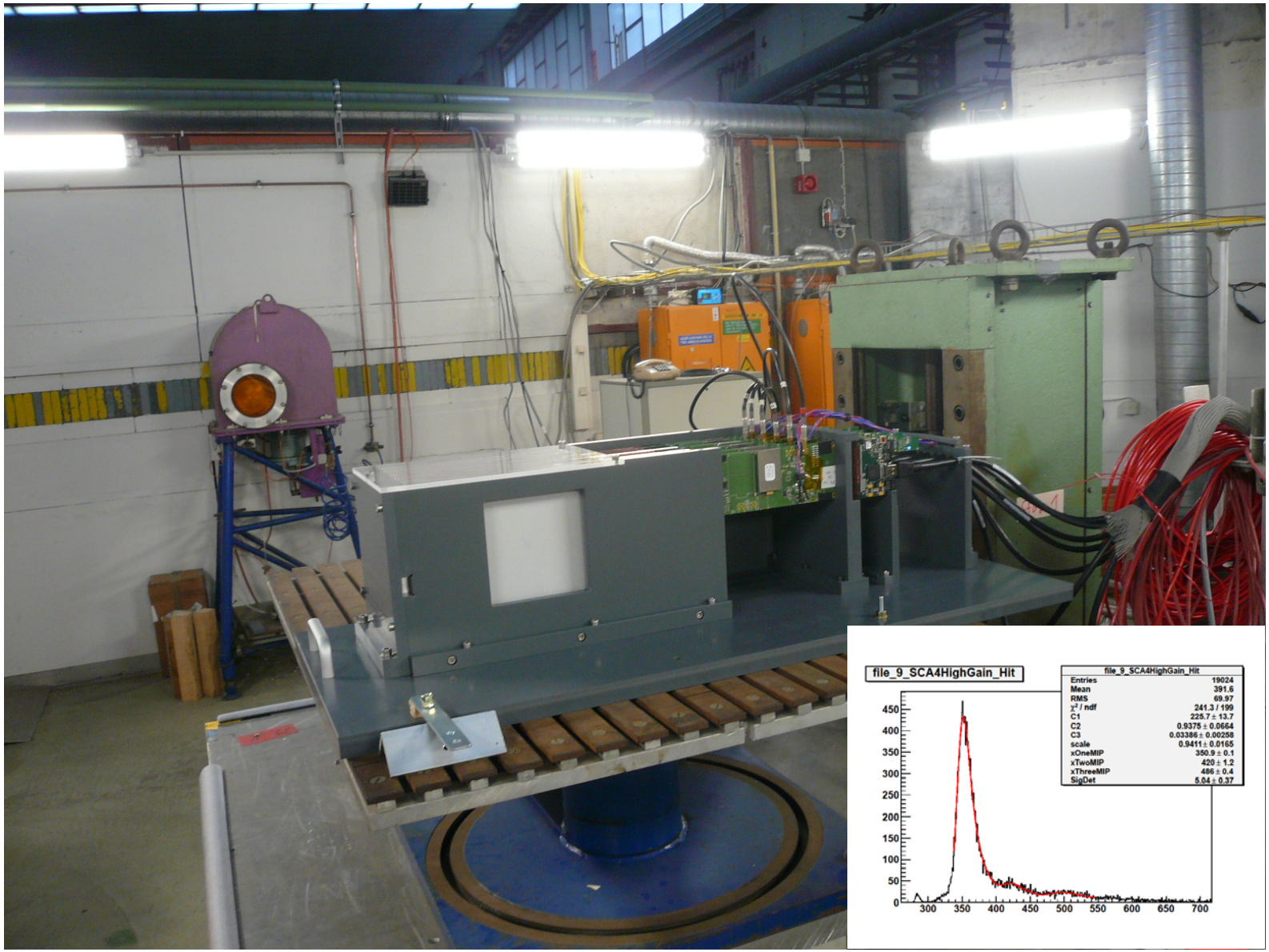
Up-scaling studies have started since few years and will be refined following prototyping steps.



Major forthcoming steps :

- Integration into structure
- DAQ & SW
- SKIROC3

Project funded by Agence National pour la Recherche under contract ANR-BLANC-2010-0429-01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C2 0.9375 ± 0.0664
C3 0.03386 ± 0.00258
scale 0.9411 ± 0.0165
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xTwoMIP 420 ± 1.2
xThreeMIP 486 ± 0.4
SigDet 5.04 ± 0.37
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