SiD Workshop
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Electronics and DAQ Editors Report

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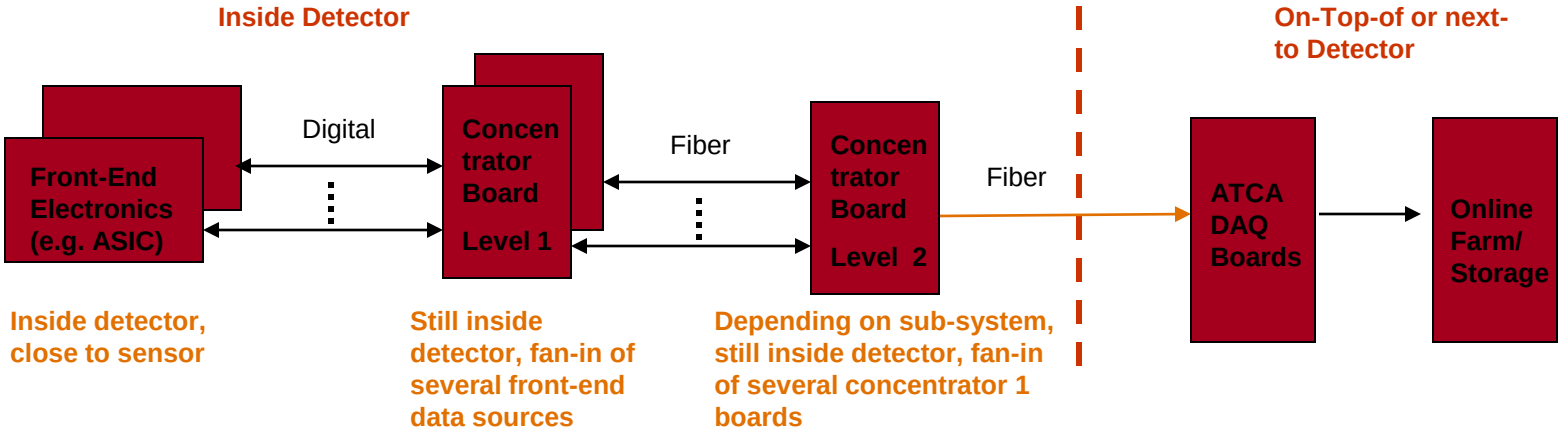
Overview

In report:

- Electronics Architecture
- KPIX readout
- DAQ Hardware

Electronics Architecture



Total data rate from each front-end relatively small, thus can combine data from several front-ends to reduce number of connections to the outside of the detector

Front-End ASICs/electronics transmit event data to concentrator 1 boards

- **Digital interface (optical or electrical, e.g. LVDS)**
- **Concentrator 1 boards close to front-end, combining data-streams from several front-end ASICs**
- **Zero-suppression either at front-end or on concentrator 1 boards**
  - **No additional processing needed at this stage**

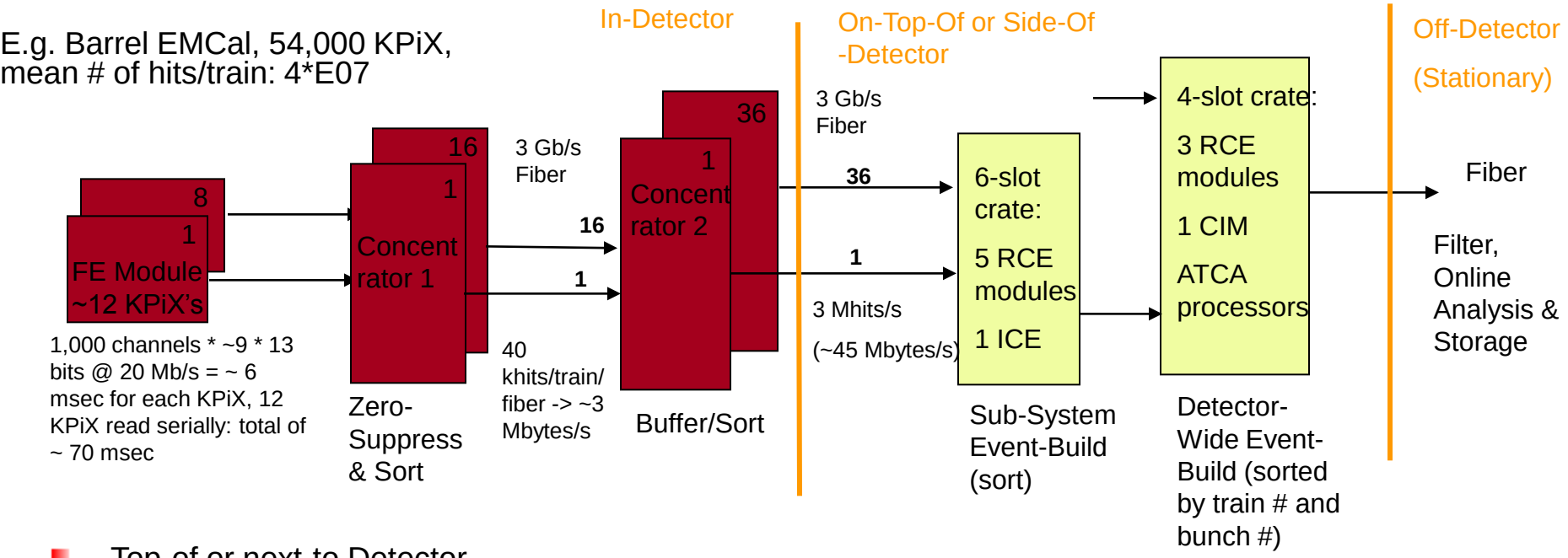
Event data from concentrator 1 boards are combined in concentrator 2 boards

- **Multiplexing of concentrator 1 board event data onto fewer fibers**

Event data is transmitted to top or side of detector

- **ATCA crate (see later) to process and switch data packets**
- **Online farm for filtering (if necessary)**

EM Barrel Example

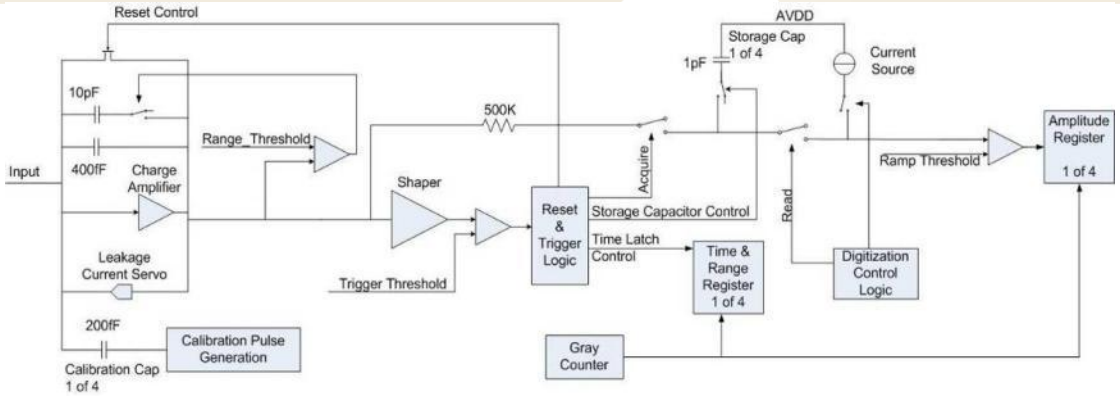


- Top-of or next-to Detector
  - Readout to outside-Detector crates via 3 Gbit/s fibers
    - Single 6-slot crate to receive 36 fibers: 5 RCE modules
  - Total out of EM Barrel partition: 1.6 Gbytes/s
    - Available bandwidth: > 144 Gbit/s/module (and is scalable)
  - Sorting, data reduction
- Can be switched into ATCA processors for data-filtering/reduction or online farm
  - A few 10-G Ethernet fibers off detector

KPiX ASIC: generic R&D toward system-on-chip designs

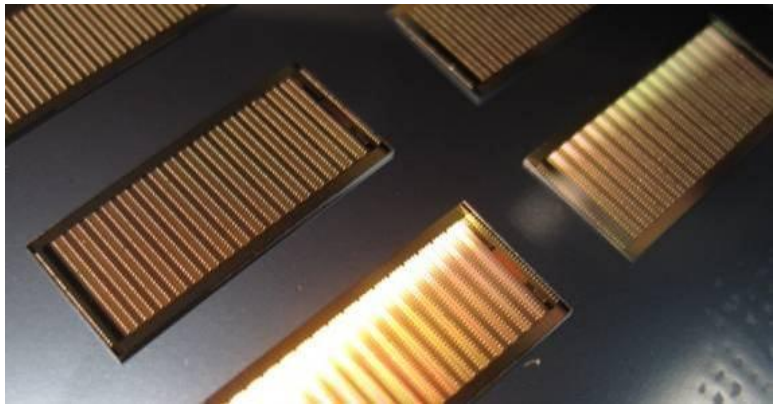
32×32 array = 1024 channels
Designed to be

- bump-bonded to a Si sensor, or
- bumped to a hybrid for large area detectors (RPC's, GEM's, etc)



Block diagram of a single channel

- For each channel of the system-on-chip
  - 4 samples per train with individual timestamps
  - auto-triggering
  - internal per-channel 13-bit ADC
  - automatic range switching for large charge depositions (10pC)
  - bias current servo for DC coupled sensors
  - power cycling: power down during inter-train gaps (20 uW avg for ILC time structure)
  - built-in calibration
  - nearest neighbor trigger ability
  - high-gain feedback capacitor for tracker application
  - dual polarity for GEM and RPC applications
  - external trigger for test beam
- Digital IP core with serial data IO (only 4 signals)
- 0.25µm TSMC

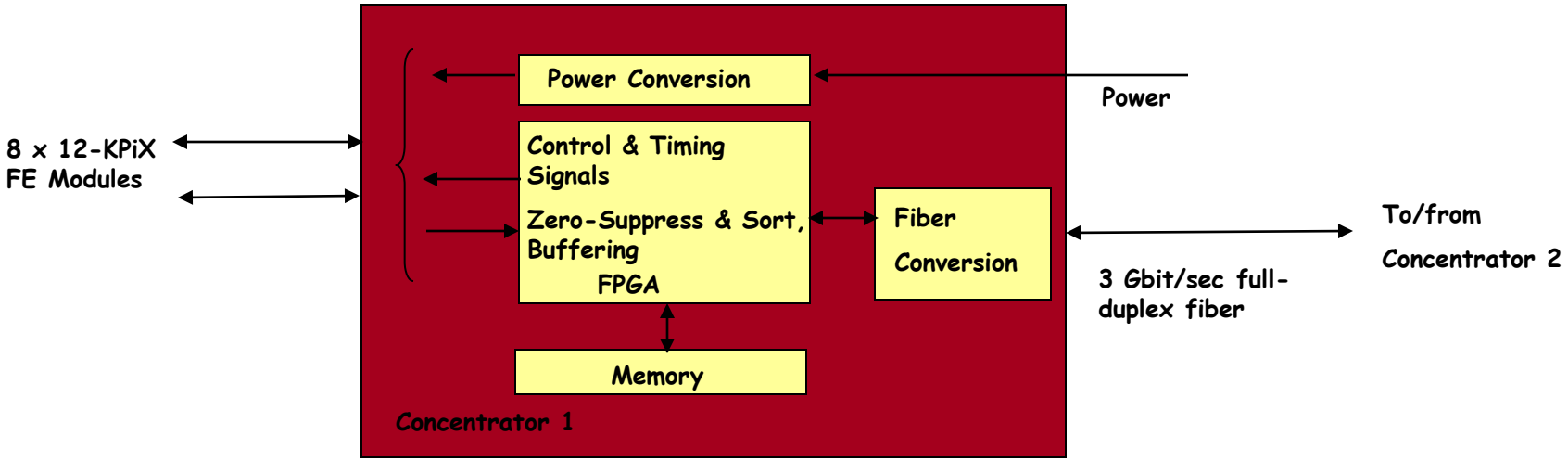


1024-channel KPiX

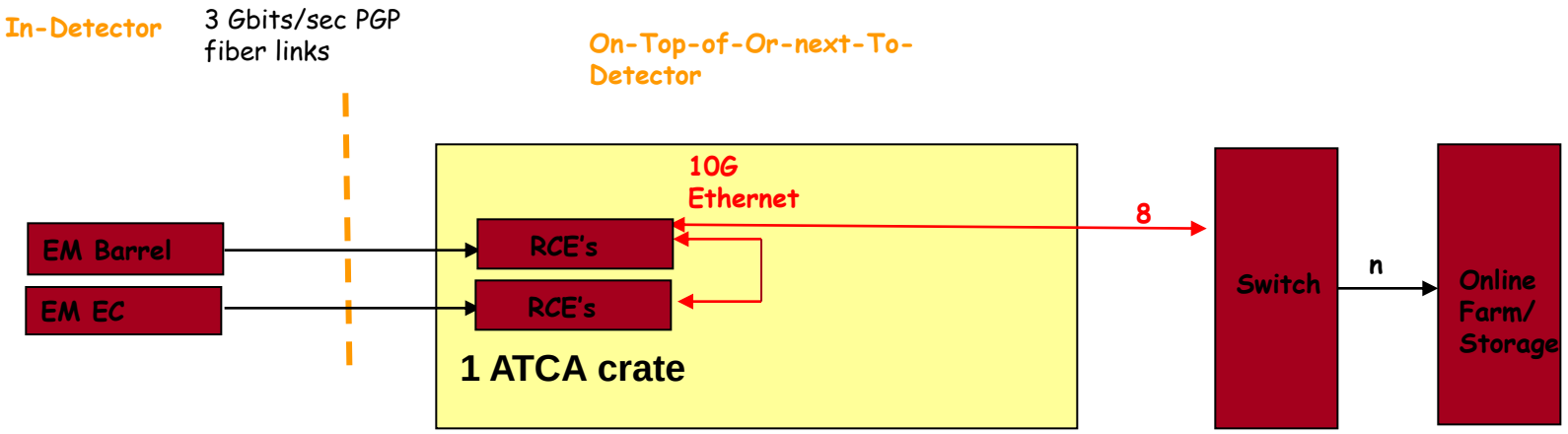
Collaboration: SLAC, UCSC, U. of Oregon, UC Davis

KPiX, An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information", D. Freytag. G. Haller, et al. SLAC-PUB-13462, 2008. 4pp (IEEE NSS Oct 2008)
KPiX, an 1,024 cell ASIC, Design and Performance, accepted for presentation at NSS 2012

Concentrator-1



DAQ Architecture



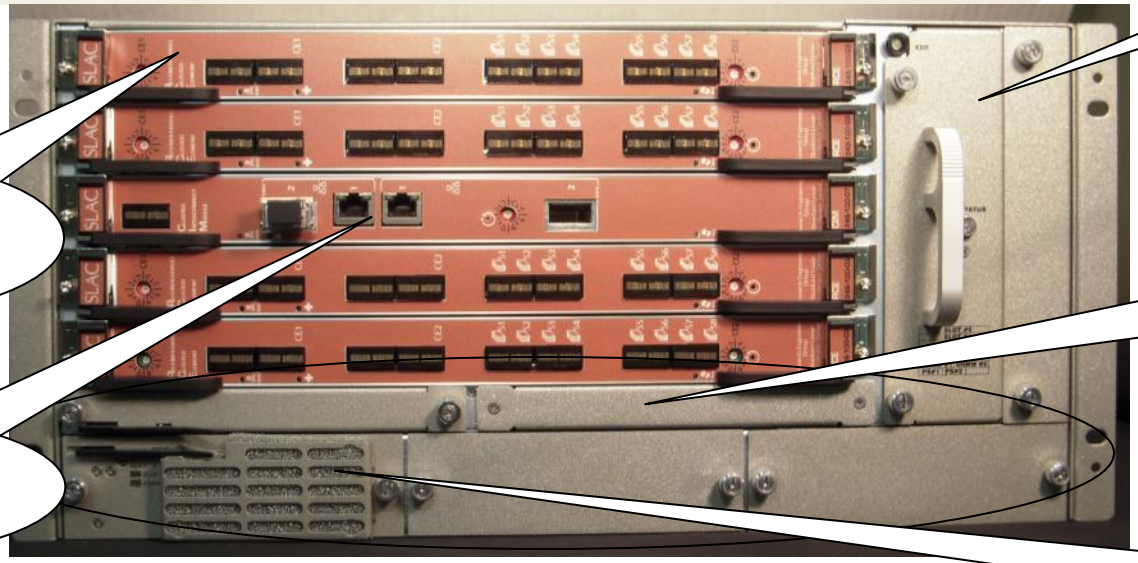
- 1 ATCA crate for each sub-system for partitioning reasons
  - One custom ATCA module type
    - RCE: Reconfigurable Cluster Element, full-mesh topology

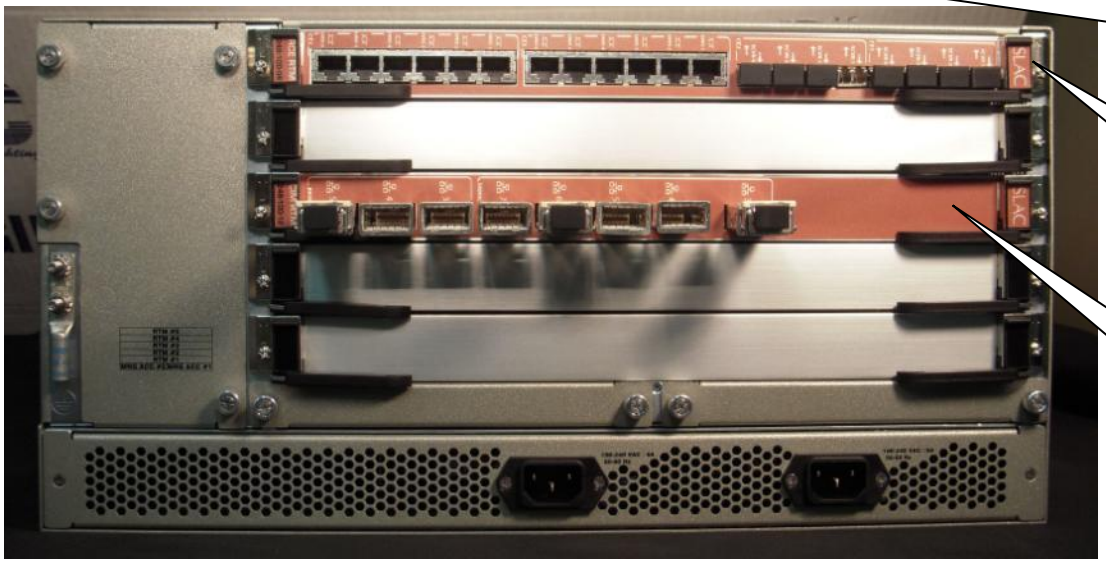
DAQ Sub-System

Based on ATCA (Advanced Telecommunications Computing Architecture)

- Next generation of “carrier grade” communication equipment
- Driven by telecom industry
- Incorporates latest trends in high speed interconnect, next generation processors and improved Reliability, Availability, and Serviceability (RAS)
- Essentially instead of parallel bus backplanes, uses high-speed serial communication and advanced switch technology within and between modules, plus redundant power, etc

Intro: Typical (5 slot) ATCA shelf (i.e. crate)





Front

Back

fans

front board

Shelf manager

front board

Power supplies

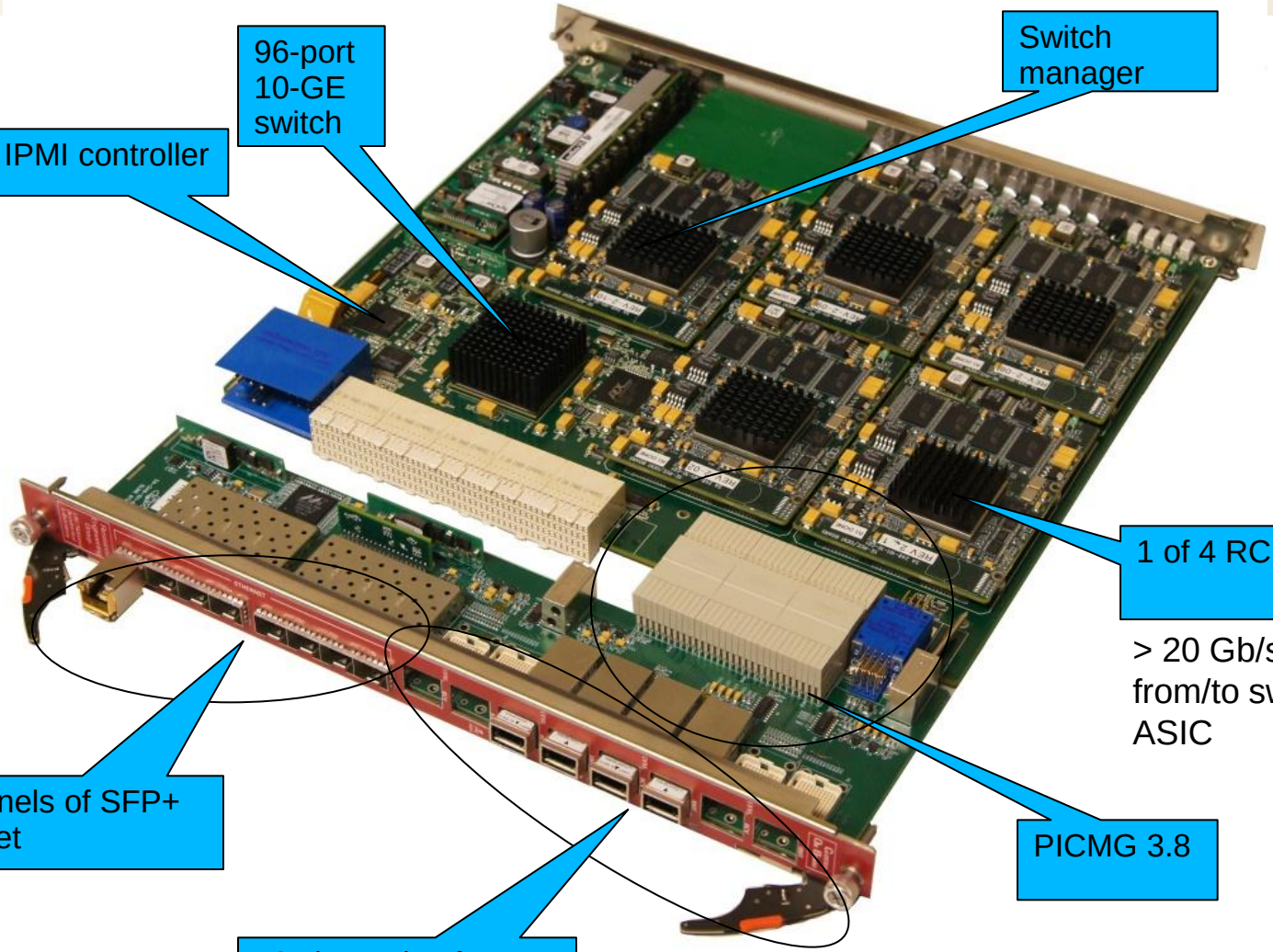
RTM

RTM

RTM: Rear Transition Module

COB + 48 channel R/O + 80 Gbits/sec Ethernet RTM

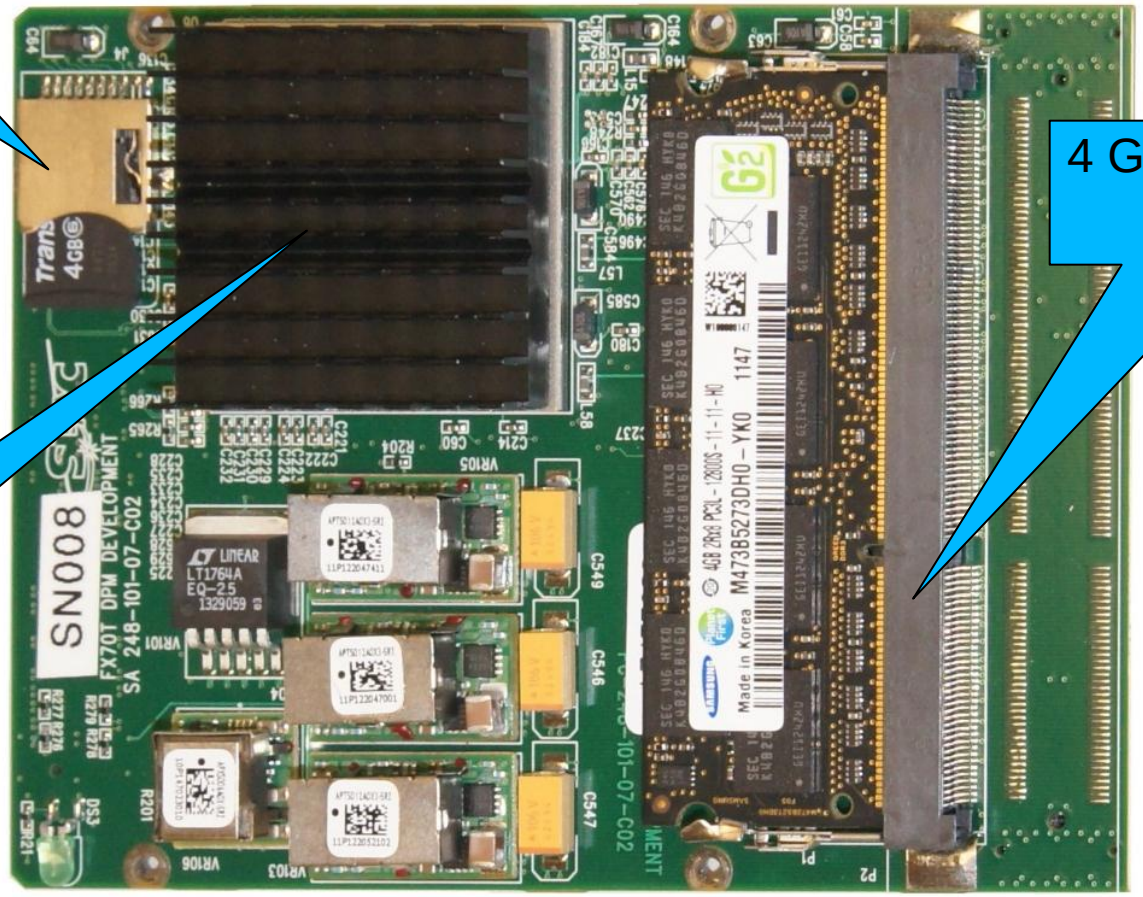
- Is ported and bundled with operating system and real-time kernel so users can easily use system and tailor functionality and performance to their processing needs



Single-element (GEN-II) mezzanine board

SD configuration flash

System-On-Chip



4 GBytes (DDR3)

System is flexible: current and future deployments

SLAC

- Deployed currently:
  - For the LCLS experiment detector readout DAQ
  - For the Heavy Photon Search test-beam DAQ
  - As readout technology for IBL stave testing (for example CERN's SR1 & U Geneva IBL stave loading site)
  - For the pixel planar sensor test beam readout
  - As the test-stand for LSST Camera CCD read-out

- Chosen as the core technology for:
  - The LSST camera's DAQ system
  - The alternative final readout scheme for IBL as well as the AFP (ATLAS Forward Proton) silicon readout
  - The pixel beam telescope readout for an upcoming SLAC test beam
  - The ATLAS CSC ROD replacement in 2014
  - The AFP timing detector readout for 2014

Summary

SLAC

- KPIX ASIC can be used in several sub-systems, see detector sub-system talks for applications
- SiD data rate dominated by noise & background hits
- Event data rate for SiD can be handled by current technology, e.g. ATCA system being built for LCLS, LHC, etc
- No filtering required in DAQ. Could move event data to online farm/off-line for further filtering/analysis
- Still: investigate filtering in ATCA processors