

Vertex DBD and 3D Status

Ronald Lipton, Fermilab

R&D on components of the sensor design:

- 3D Submission - VICTR and VIP testing
- Thinning
- Active edge devices

Vertex DBD chapter

Vertex Sensor Development

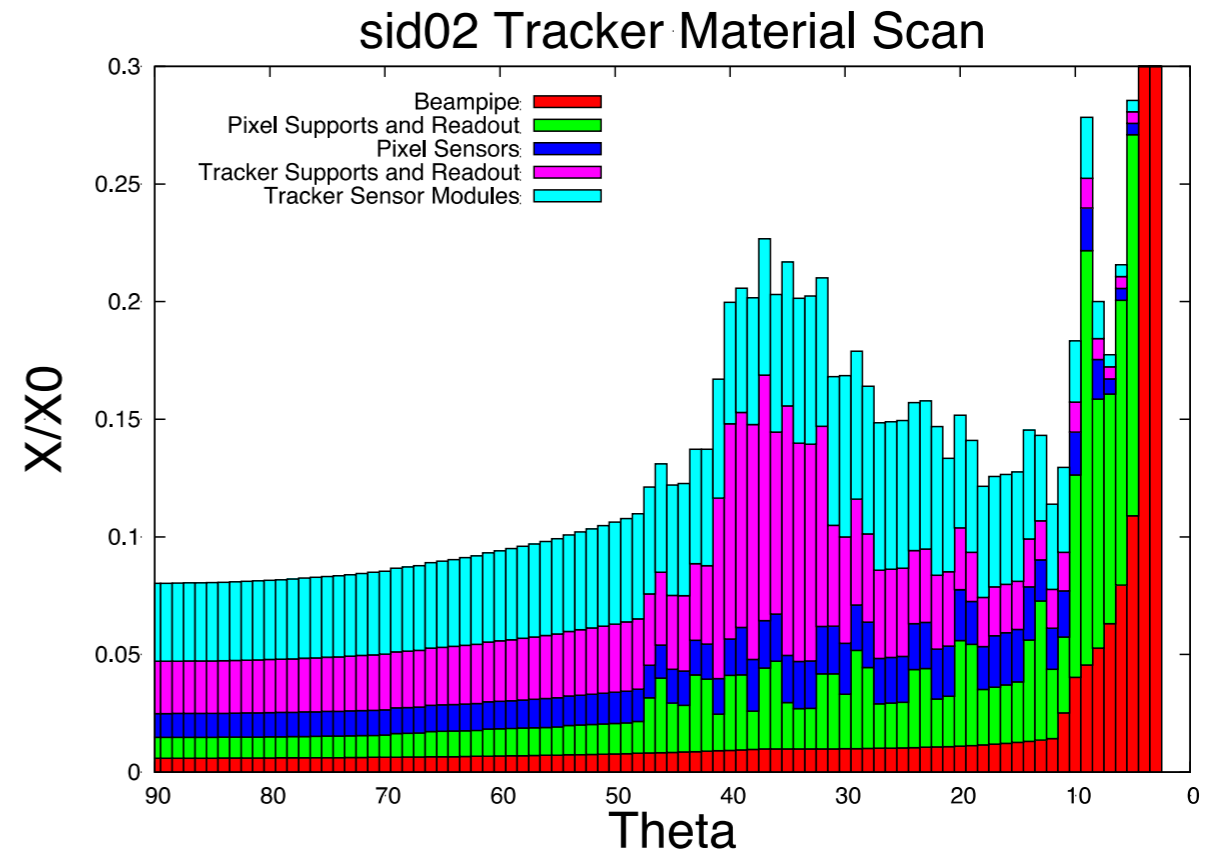
Our initial work on 3D electronics was motivated by the extraordinary requirements for ILC vertex detectors

- ~0.1% radiation length/layer
- time stamping
- 5 micron resolution

We realized that emerging IC technologies which offer a high density of electronics, fine pitch interconnects, and wafer thinning could offer a solution to the ILC vertex problem.

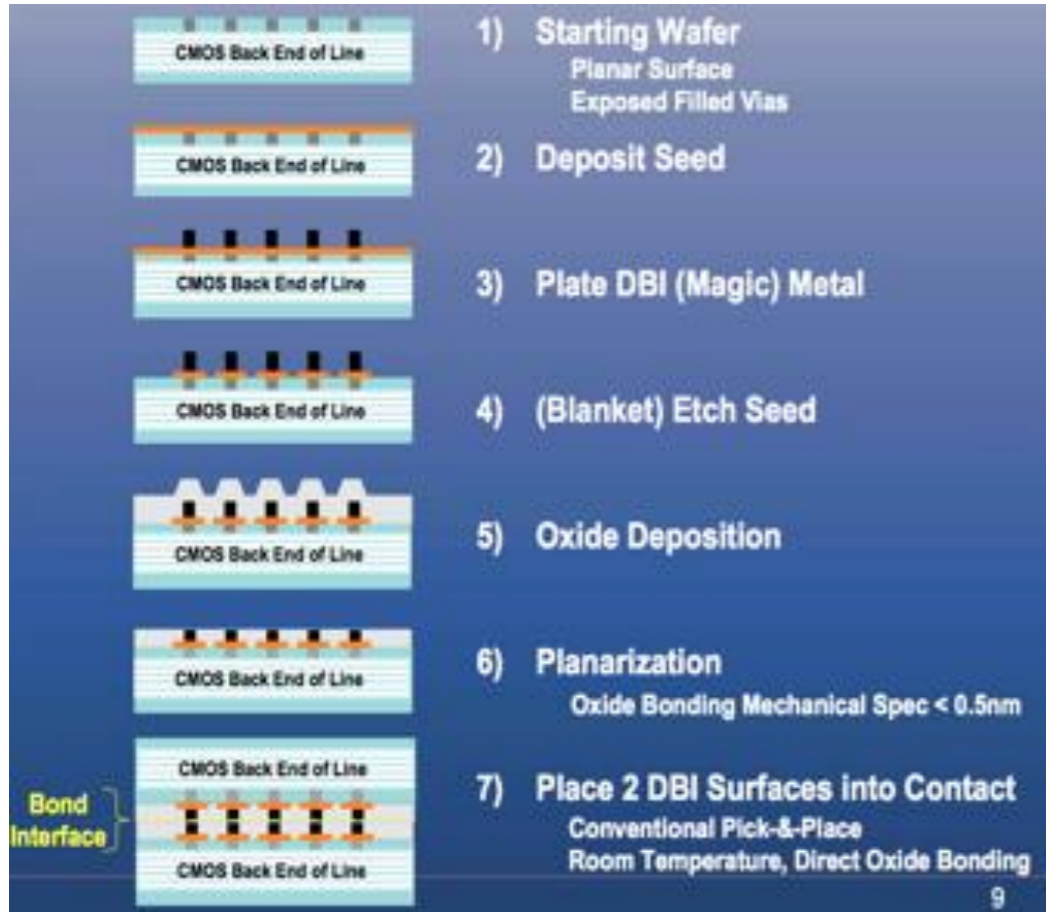
This led to work with:

- MIT-LL on SOI based 3D ICs
- Tezzaron on bulk CMOS based 3D ICs
- Ziptronix on detector/sensor integration with oxide bonding
- Cornell on thinning and laser annealing



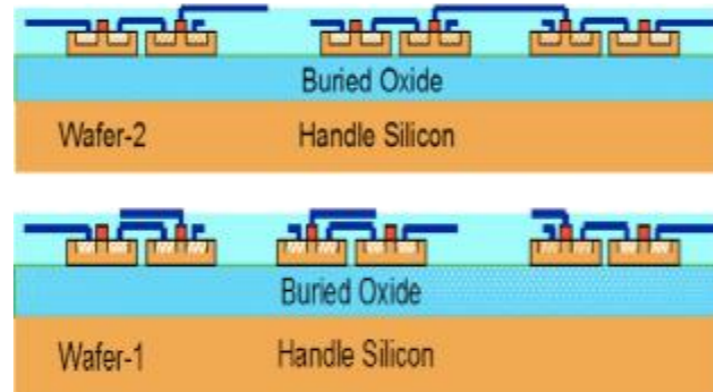
Processes Explored

Ziptronix Oxide Bonding

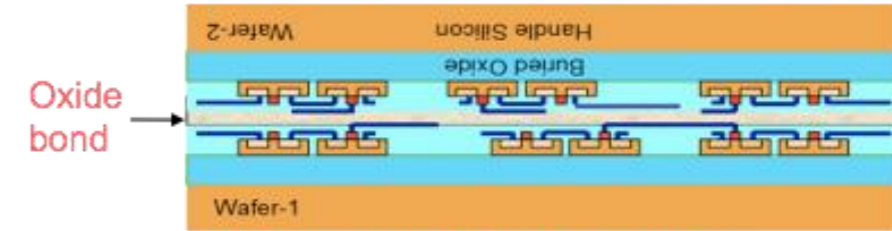


MIT-LL Oxide wafer bonding

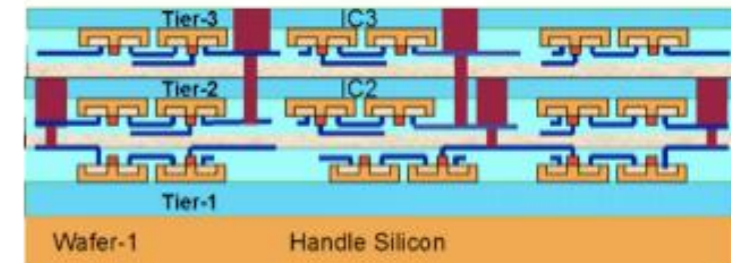
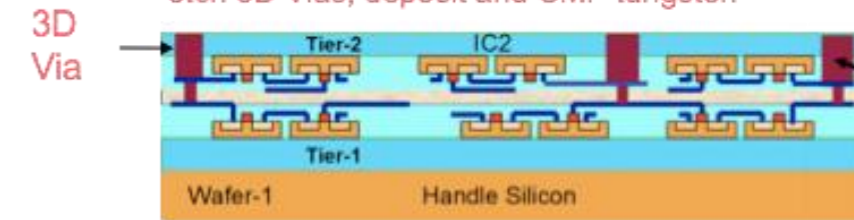
1) Fabricate individual tiers



2) Invert, align, and bond wafer 2 to wafer 1

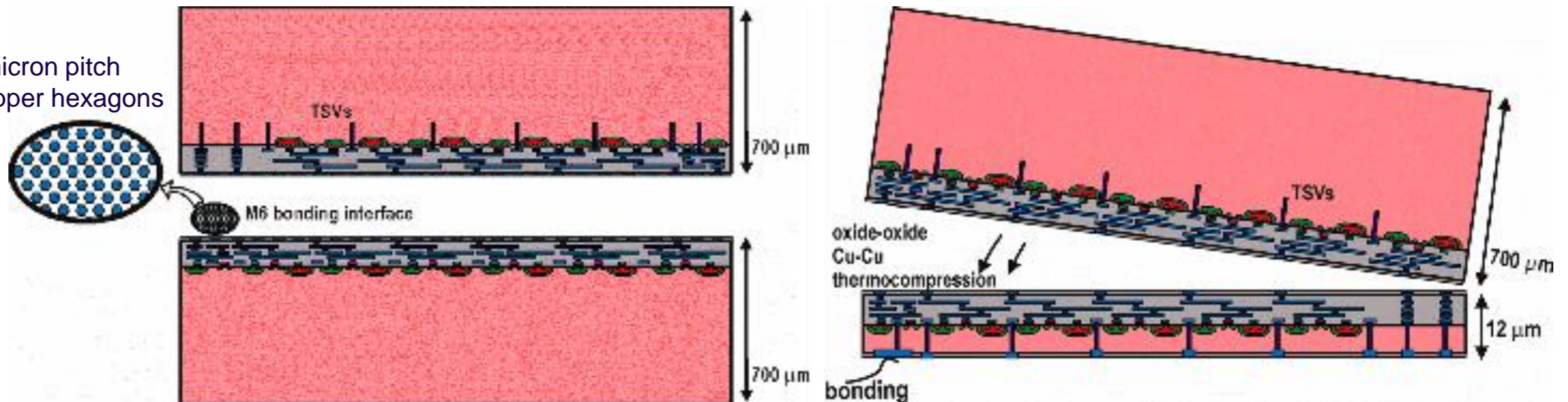


3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



Tezzaron cu-cu bonding

4 micron pitch
Copper hexagons



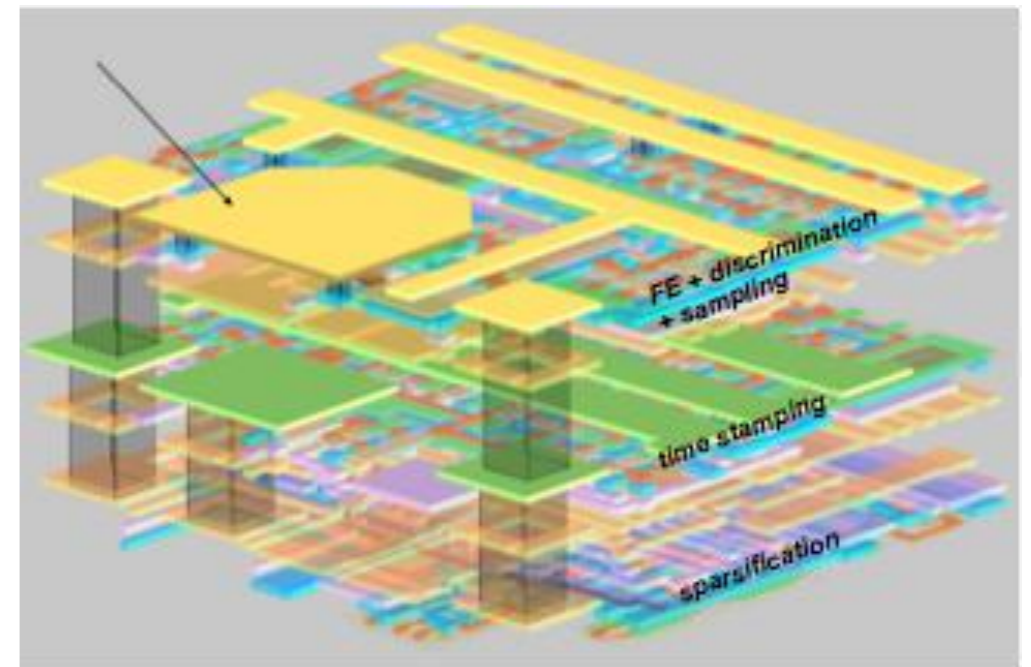
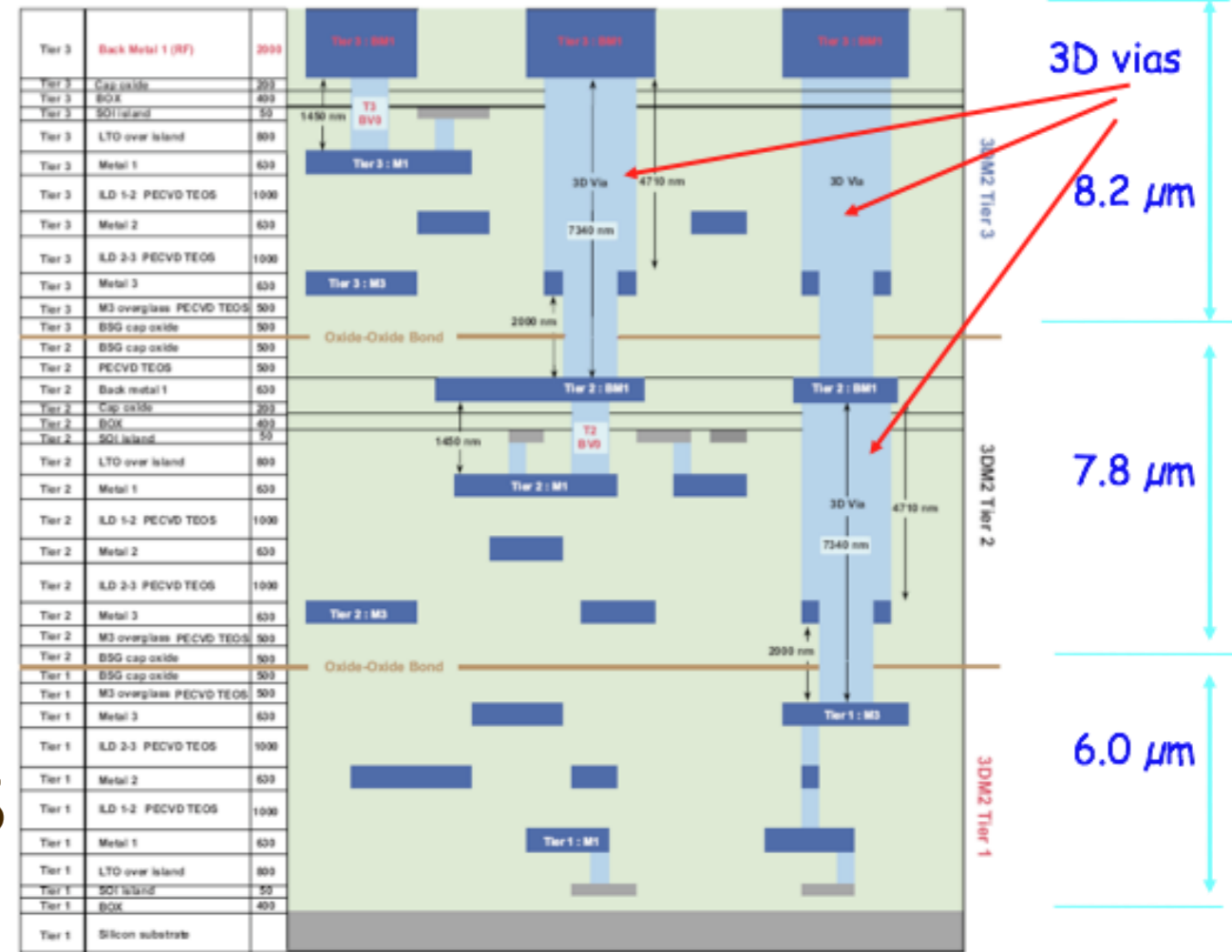
MIT-LL 3D Technology

MIT-LL had developed a 3D technology which seemed an excellent match to ILC needs.

- Demonstrated 50 micron thick bonded sensor/readout
- 3 Tiers of 0.18 micron SOI CMOS
- Bonding, thinning and detector laser anneal technology

We were invited to participate in 2 DARPA-sponsored 3D runs.

Submitted the VIP ILC Vertex chip.
Made significant contributions to the submission debugging ...



VIP Chip

Chip designed for ILC Vertex

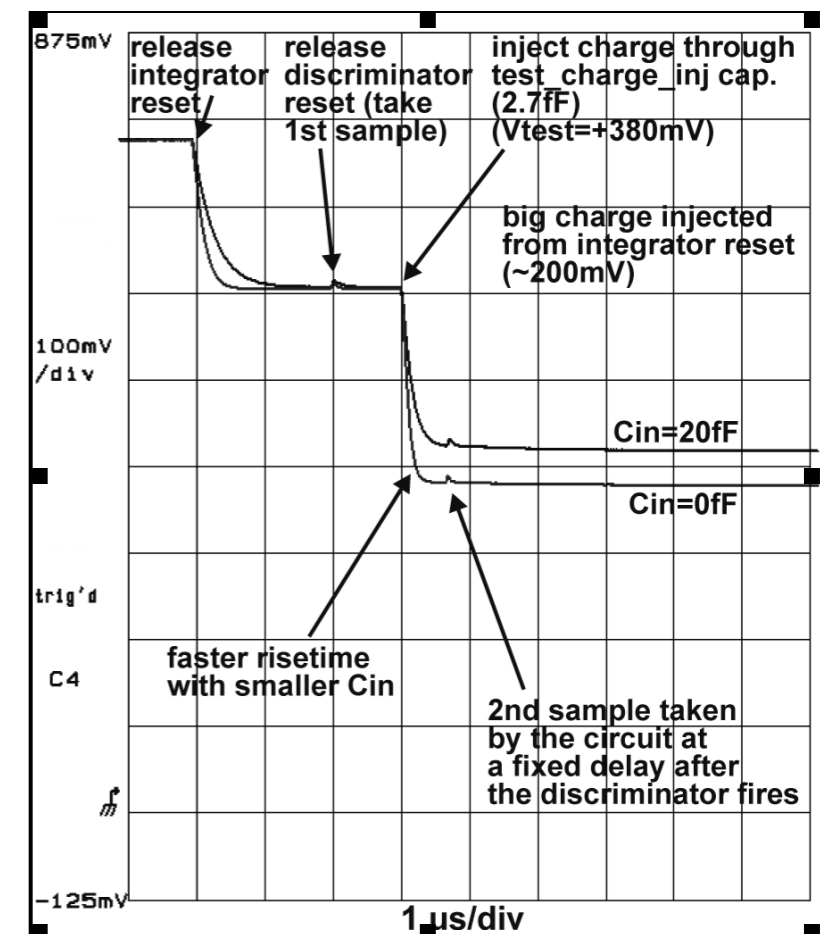
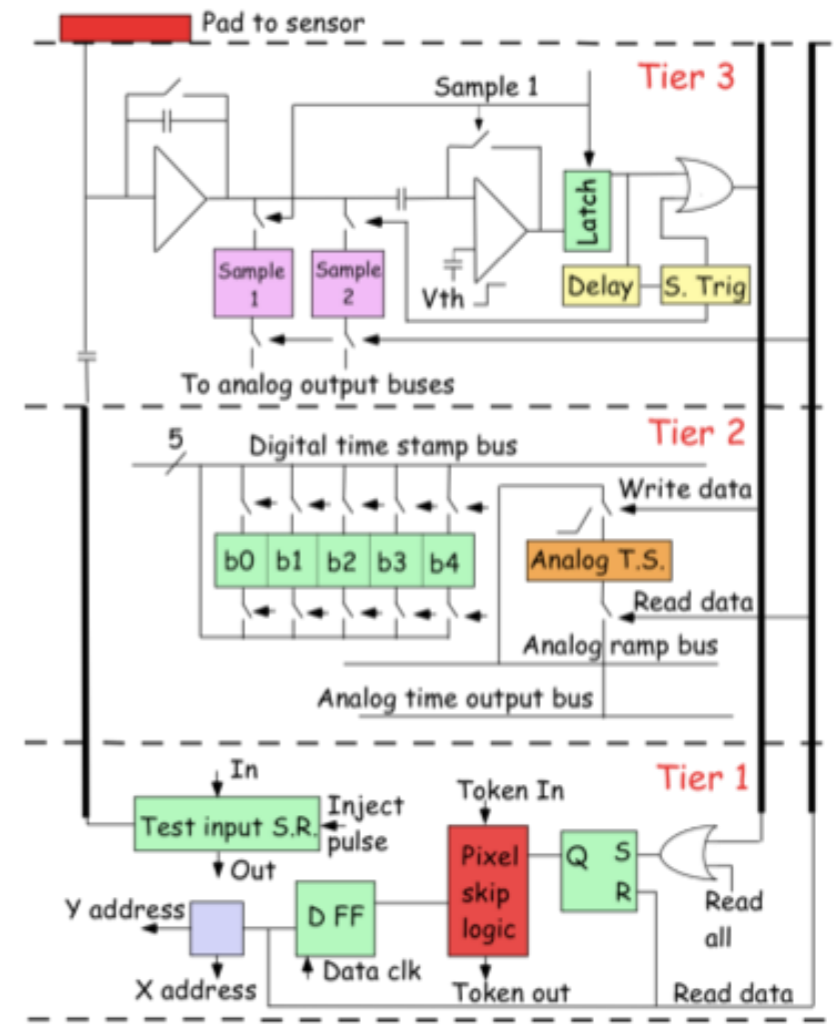
- Low power front end
- Digital and analog time stamp
- Sparse scan readout
- 20(VIP1), 24(VIP2a) micron pitch

Initial submission had low yield and marginal functionality due to MIT-LL process issues.

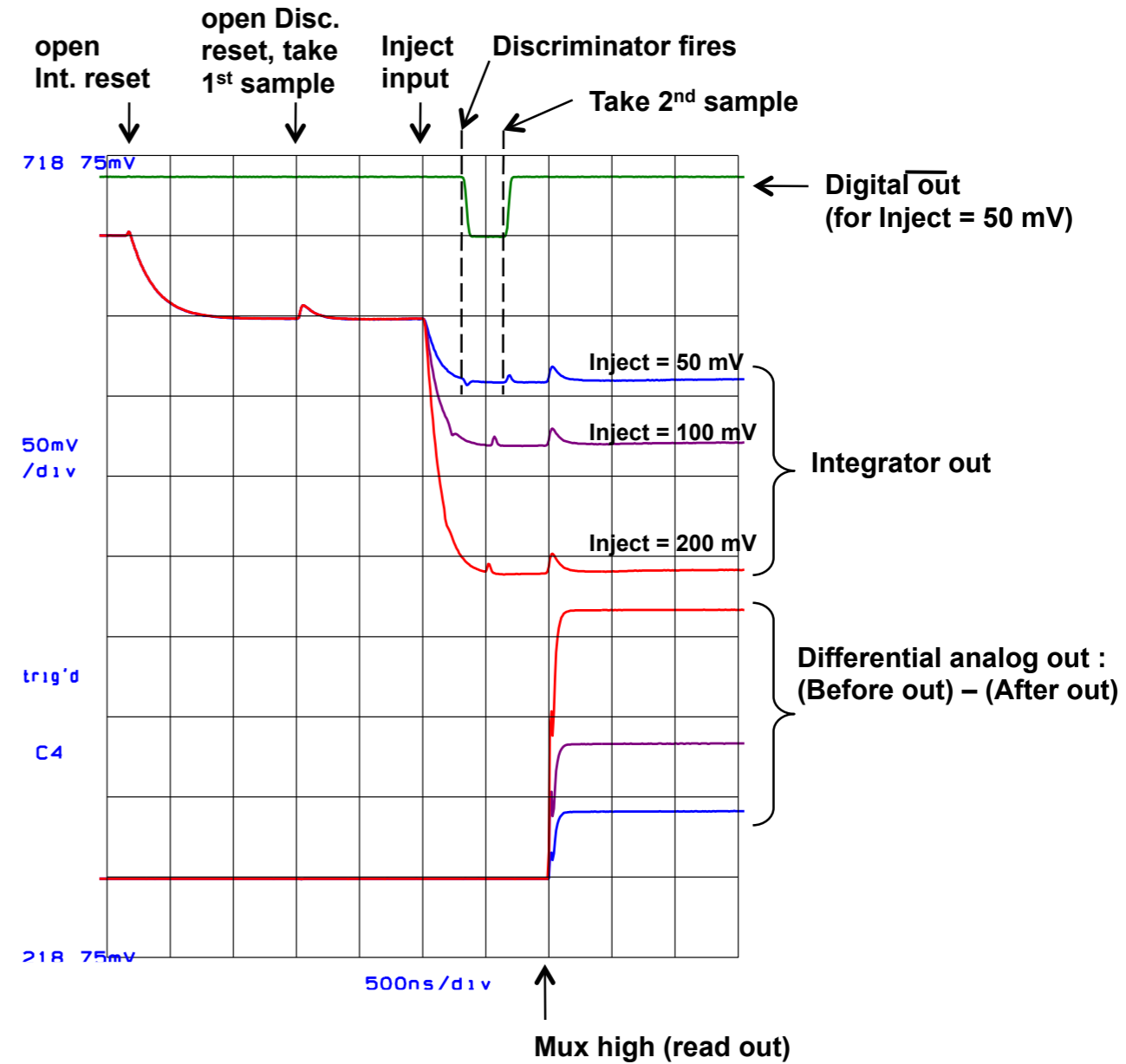
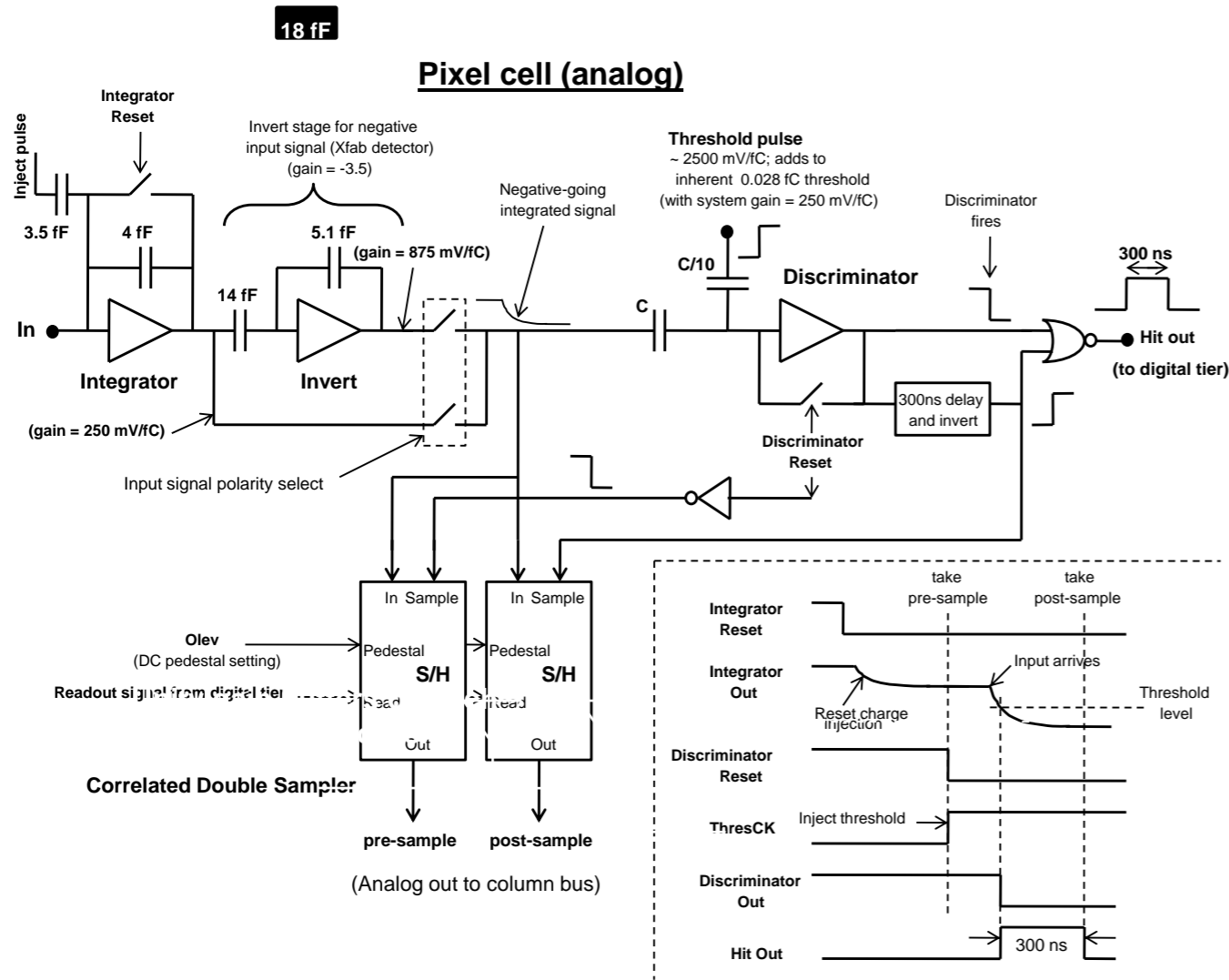
Second submission with a more conservative design worked well. Converted to 0.18 micron CMOS for 3D Tezzaron run VIP2b. Analog performance of the 2D VIP was tested and reported last year.

Full 3D VIP2b is received at Fermilab – we expect to begin testing in September.

We have tested the VICTR CMS 3D chip – which works!



VIP2b tests



Measured response with charge injection

Measured noise (DCS)

Csel	Cin added	Cin + Cinstray	Noise at Inv. Out (mV)	Noise at Inv. Out (e)	Noise at Int. Out (mV)	Noise at Int. Out (e)
111	0	12.5 fF	2.26 mV	16 e	0.74 mV	19 e
110	4 fF	17 fF	2.58	18	0.79	20
101	8	21.5	2.84	20	0.82	21
100	12	26	3.11	22	0.87	22
011	16	30.5	3.38	24	0.93	23
000	28	44	4.09	29	1.04	26

Bandwidth not very sensitive to Cin

Bandwidth varies with Cin

$$8e + 0.5 e/fF$$

Measured speed

(T = one RC time constant)

Both sample caps on the output
One sample cap on the output

Csel	Cin added	Cin + Cinstray	T _{before} Int. out	T _{after} Int. out	T _{before} Inv. out	T _{after} Inv. out
111	0	12.5 fF	115 ns	73 ns	135 ns	65 ns
000	28 fF	44 fF	215 ns	125 ns	140 ns	80 ns

At integrator out; speed varies due to varying C_{sample} and varying Cin.

At invert stage out; varying Cin has much less effect on bandwidth.

We will perform testing of the full readout and chip performance in September. Given the good analog performance we have hopes that the chips will be fully operational. We have tested VICTR, on the same wafer with similar technology.

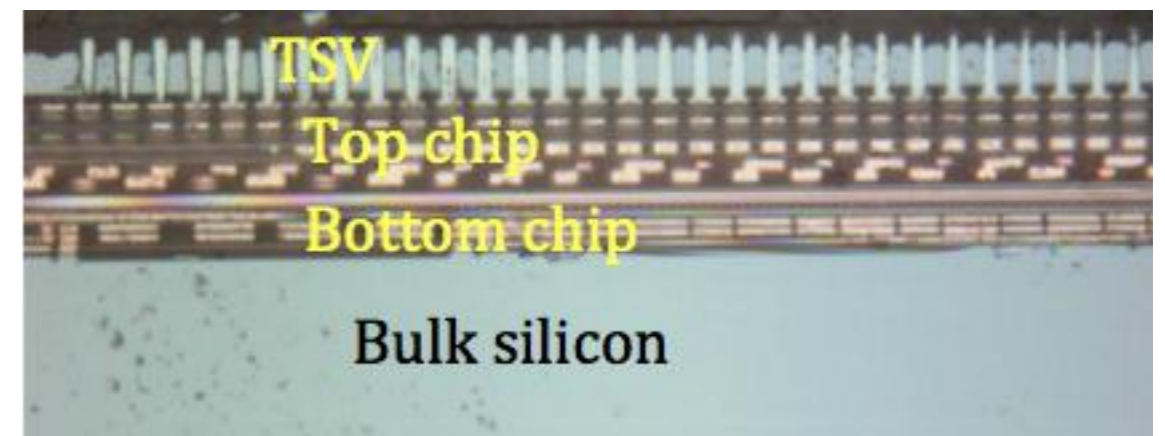
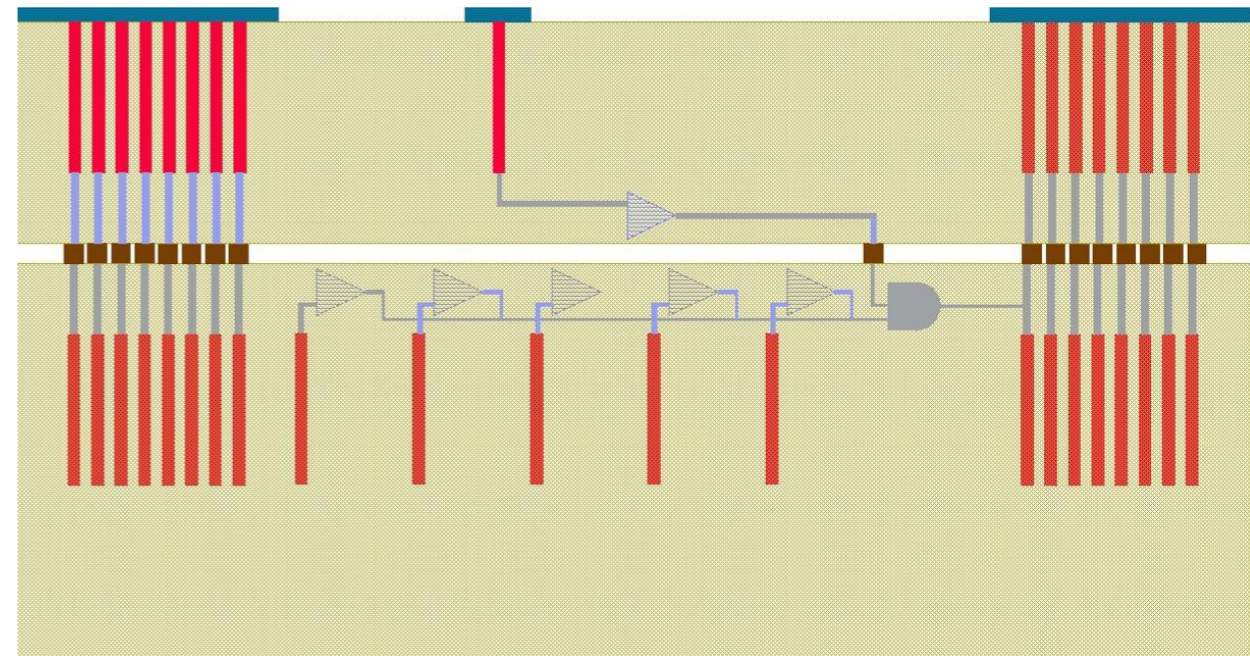
Measured speed is somewhat slower than simulated – probably due to somewhat lower gm and ?

VICTR Chip

(Cornell, Brown)

The VICTR chip is designed to demonstrate the principles of a track trigger integrated sensor/ROIC

- Part of Fermilab 3DIC run
- Modified FEI4 (Atlas) front end
- First chips delivered last Sept had alignment problems but other processes worked well.
 - backside thinning
 - TSV contact
 - Backside metalization
- We now have well-aligned functioning chips from wafers delivered in June Communication of hits from top to bottom tier on all channels
 - Detailed testing of several chips in progress
 - 9/11 functional after visual inspection
- 18 “recovery” wafers received at Tezzaron
 - Bonding at EVG, Ziptronix this summer

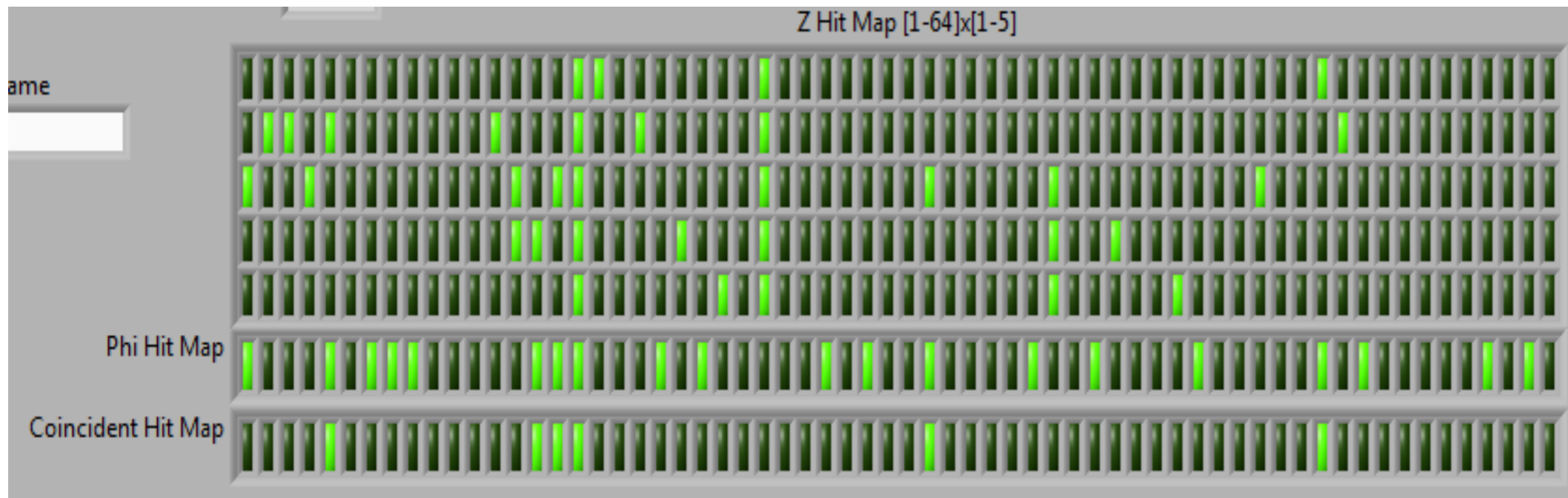


VICTR Test results



See top and bottom tier fast and slow outputs as well as coincidences between tiers – indicates good 3D bonding

Random hits



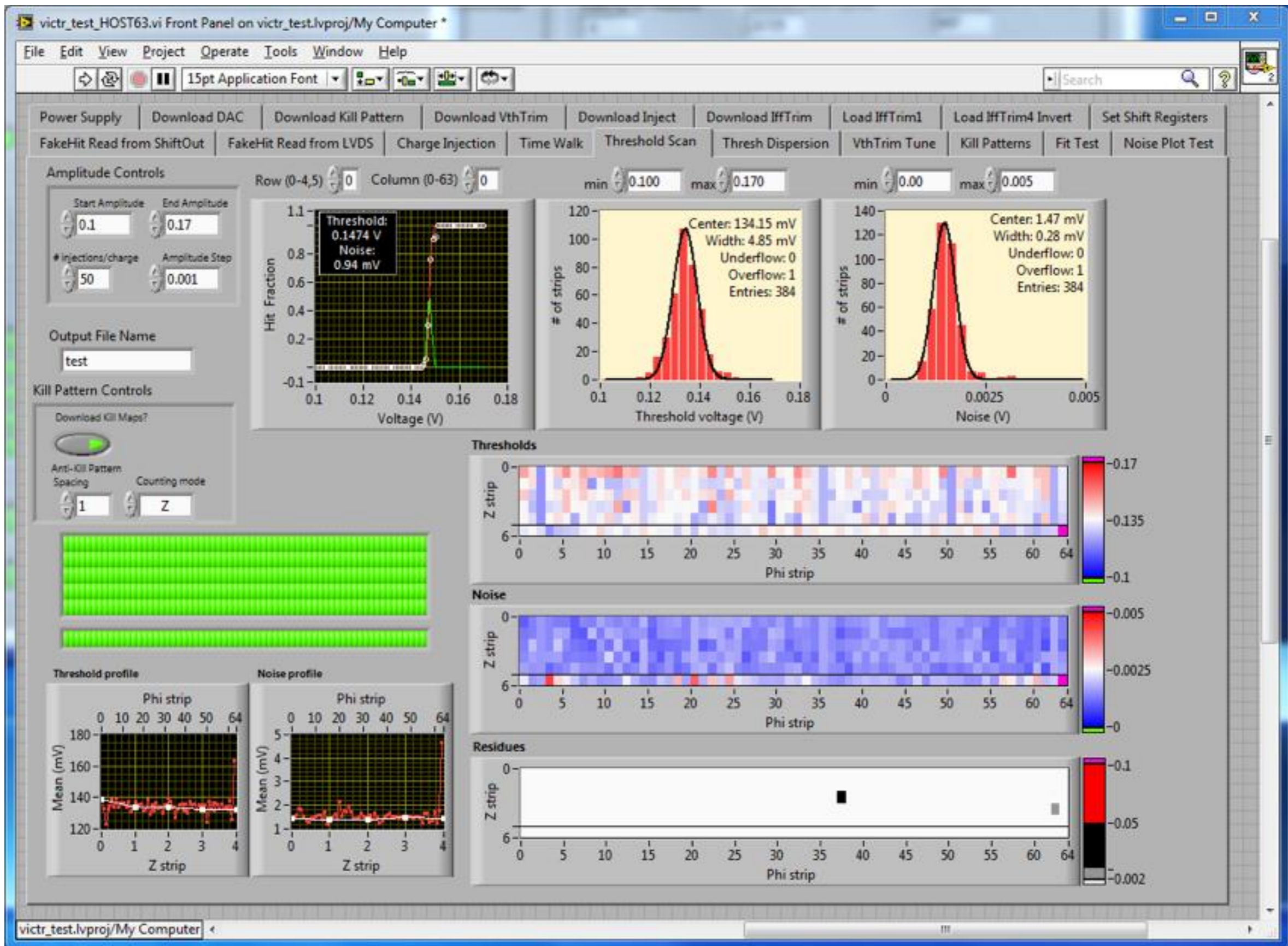
Short strip tier

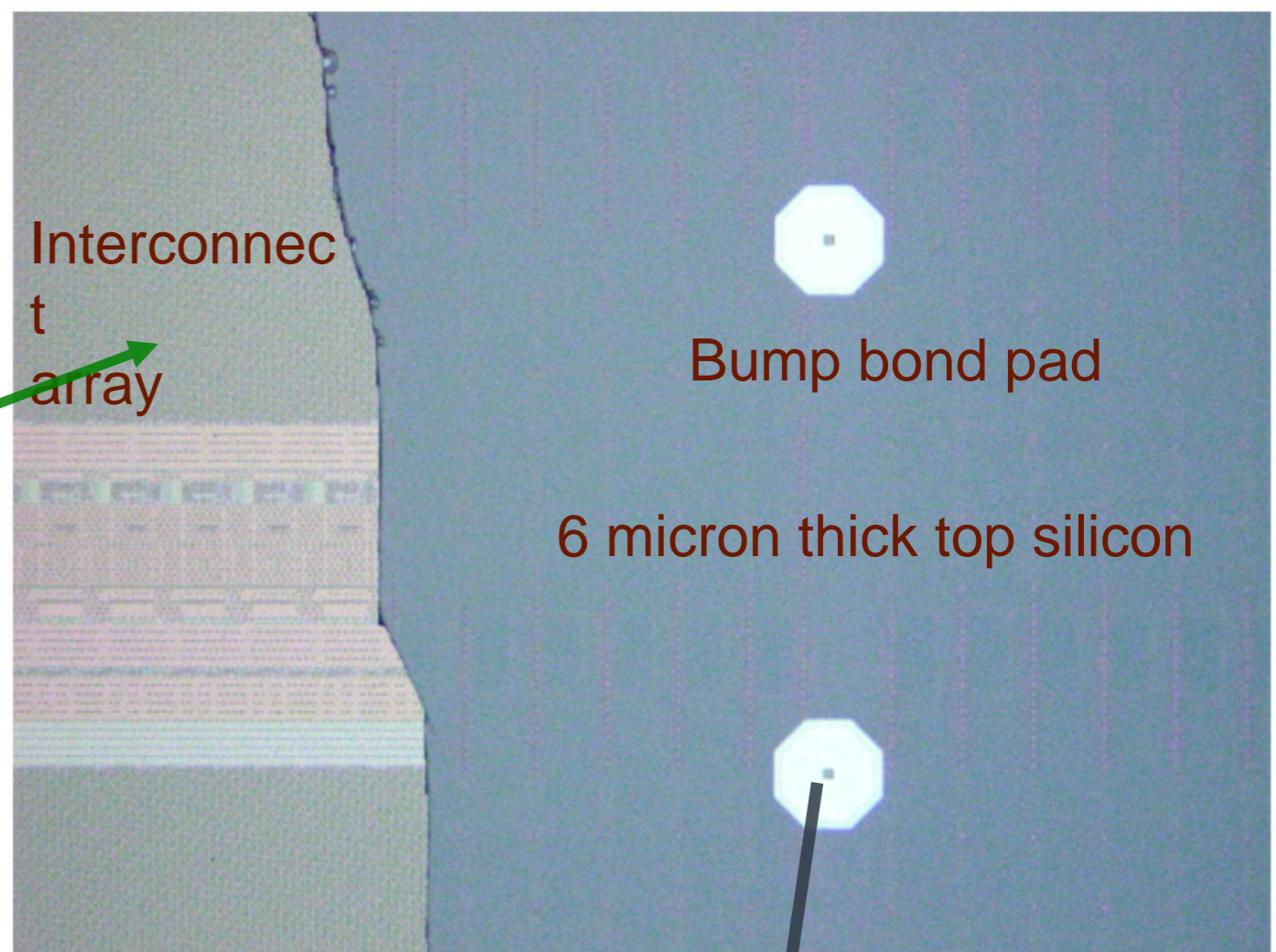
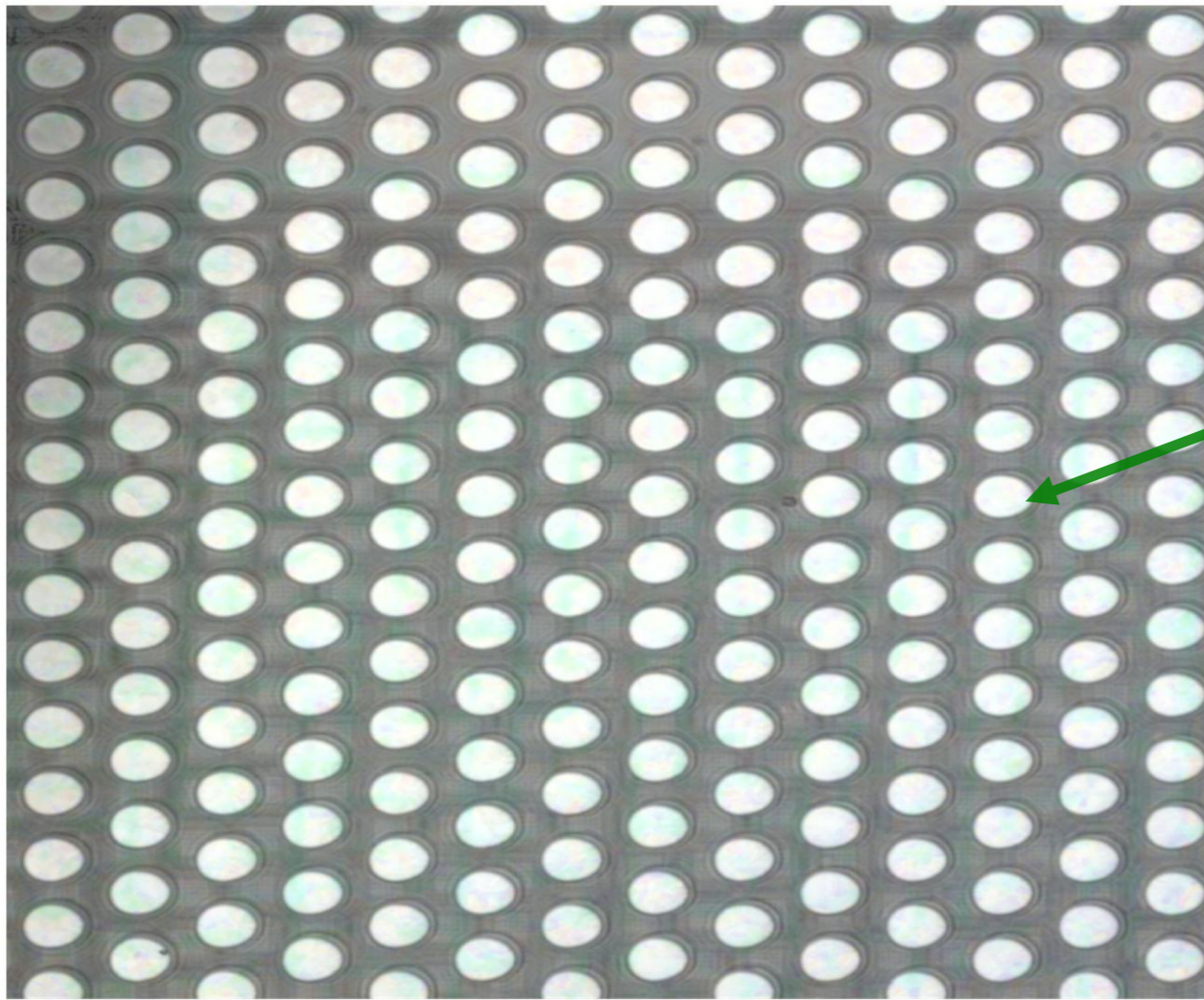
Long strip tier

Coincidence

Test Results

Threshold scan





Interconnect array

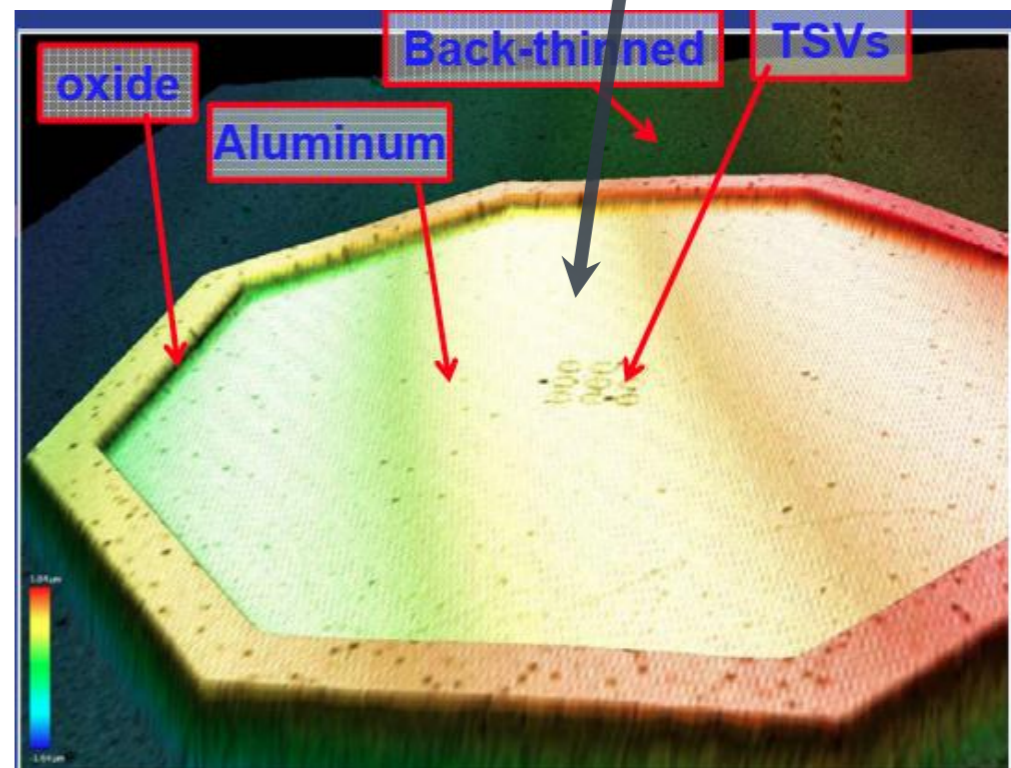
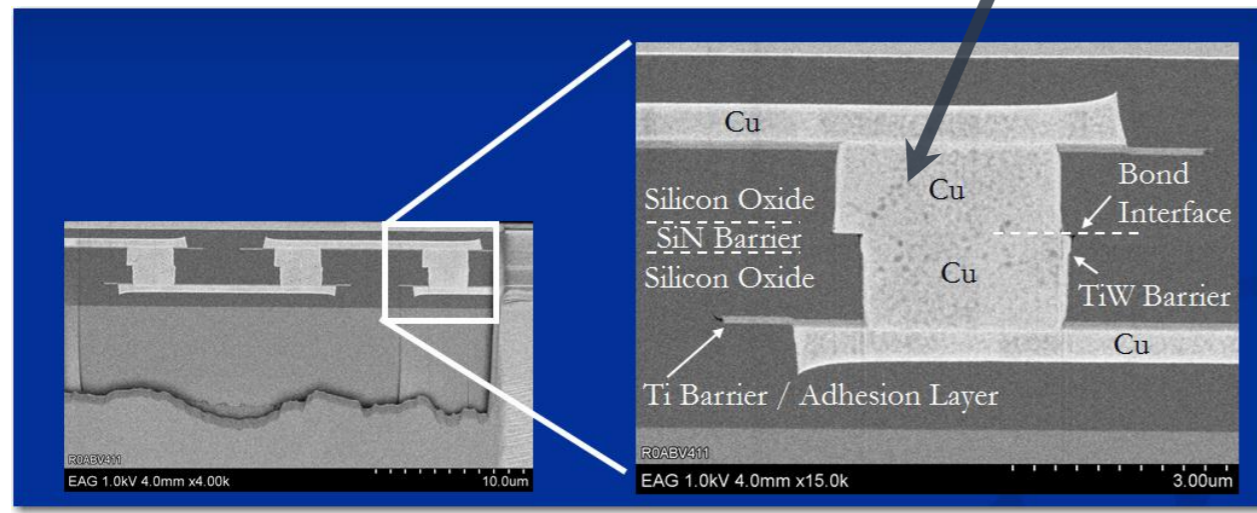
Bump bond pad

6 micron thick top silicon



4 micron pitch

DBI Copper pillars

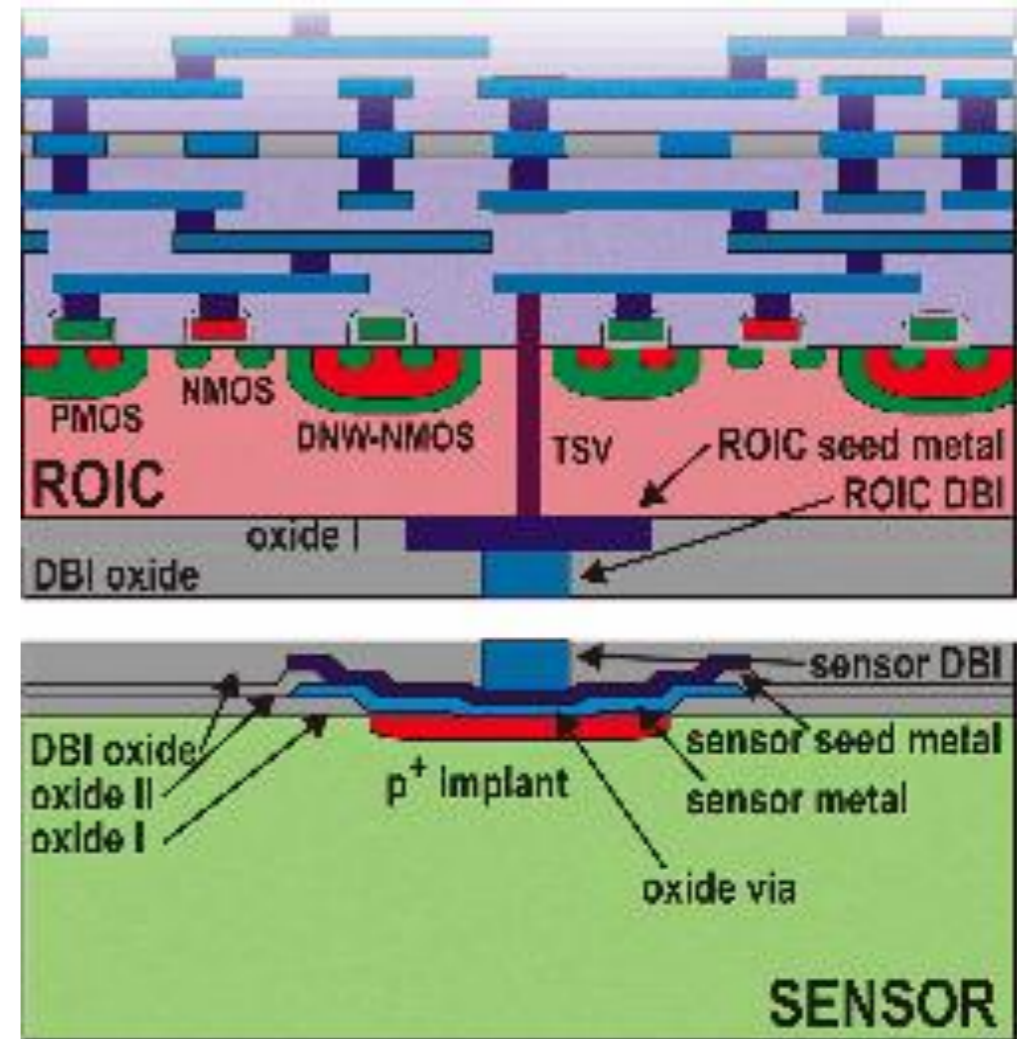


Oxide Bonding

In our studies the most promising fine pitch bonding technology was (and is) the direct bond interconnect (DBI) process from Ziptronix

- No bump bonds -
- Very fine pitch - 4 microns used for 3D Tezzaron wafers
- Mechanical strength enables aggressive post-bond thinning
- Uses standard IC processes - CMP and metalization
- Can withstand high temp.

In principal can be low cost

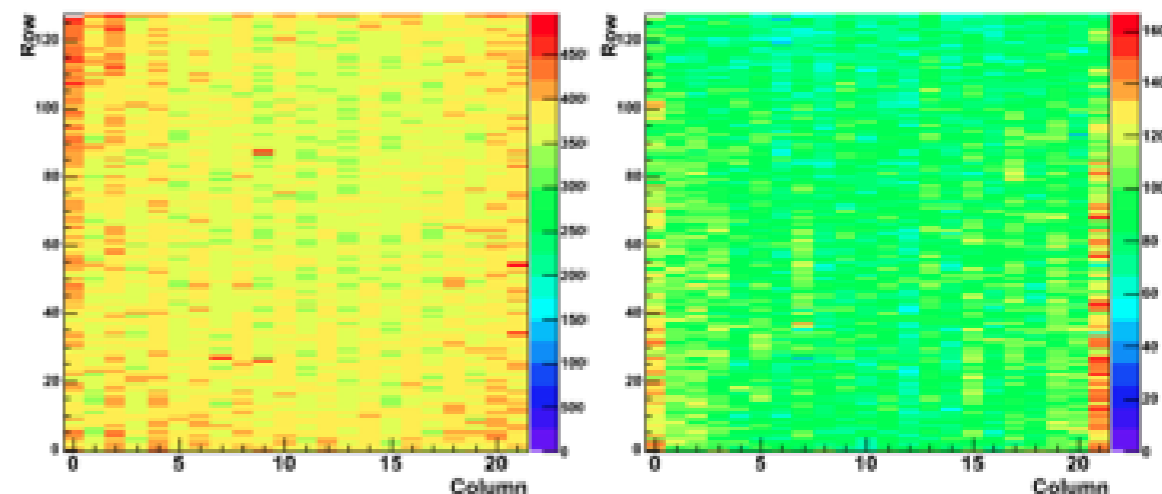
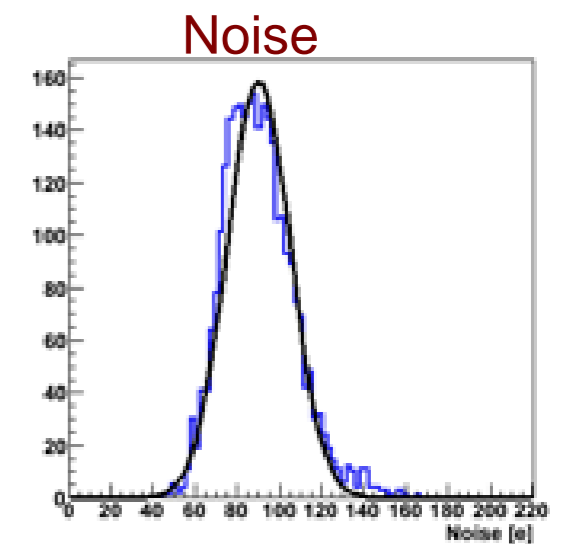
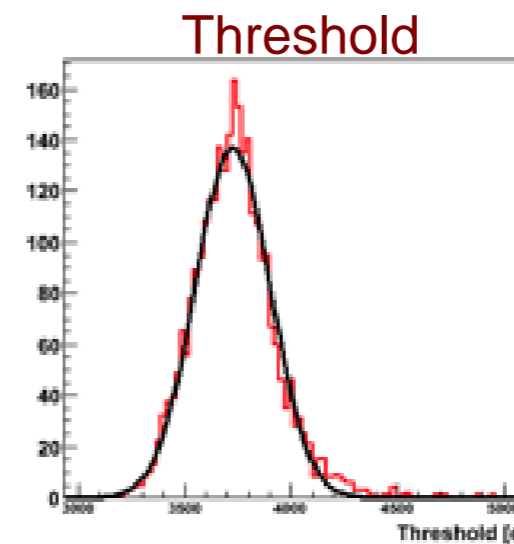
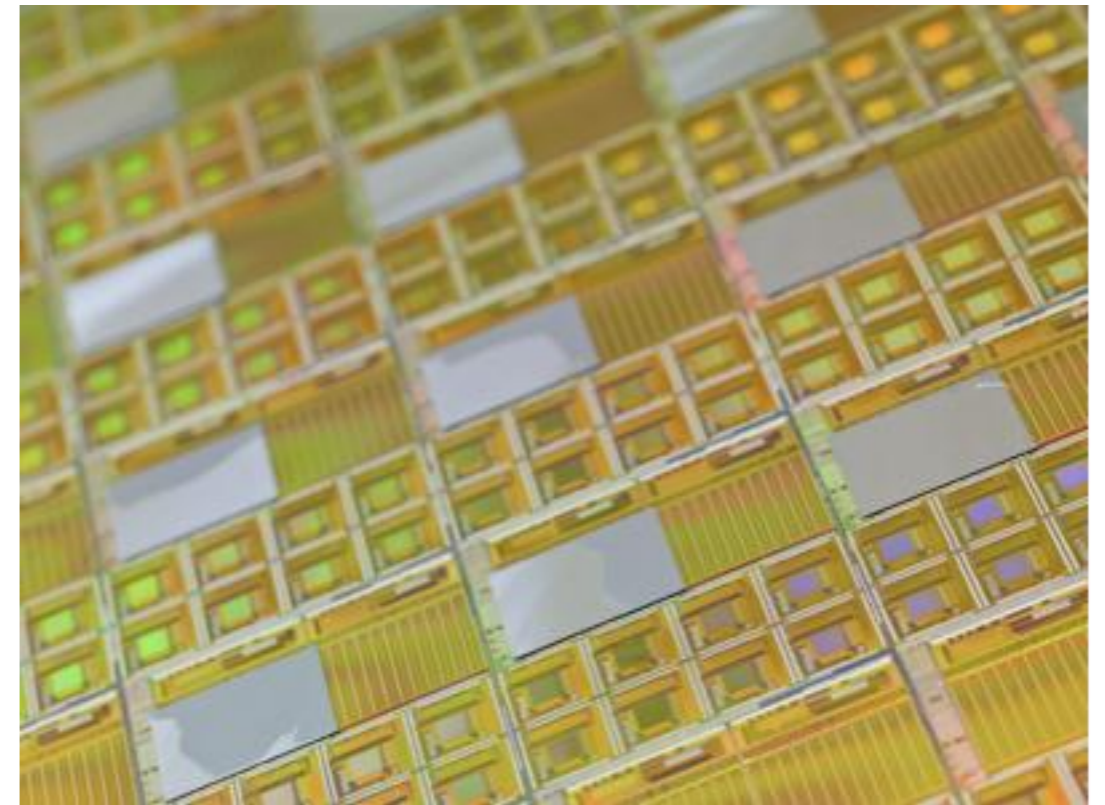


Oxide Bond Testing

Initial work was based on existing ROIC wafers from BTeV and sensor wafers from MIT-LL.

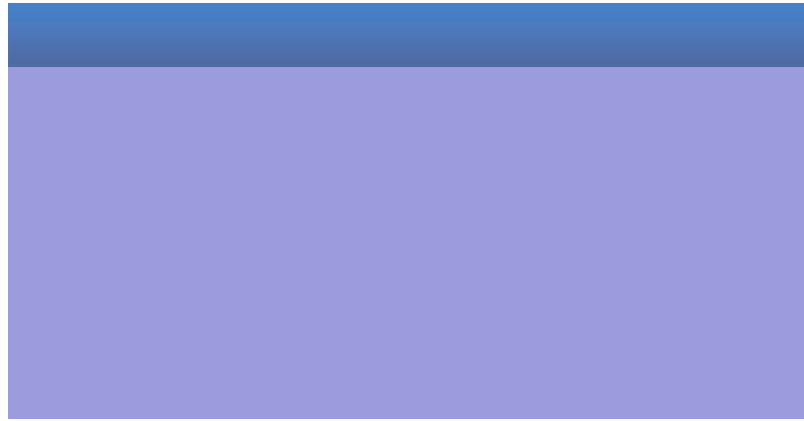
- Sensor chip to FPIX wafer bond
- Sensors ground to 100 microns - 8 V depletion
- 100% connectivity on sensors without obvious bond voids
- No degradation in s/n
- Radiation hard to >10 MRad

Process used for 3D wafers (iphone camera), planned for track trigger, active edge, x-ray imaging work



Thinning

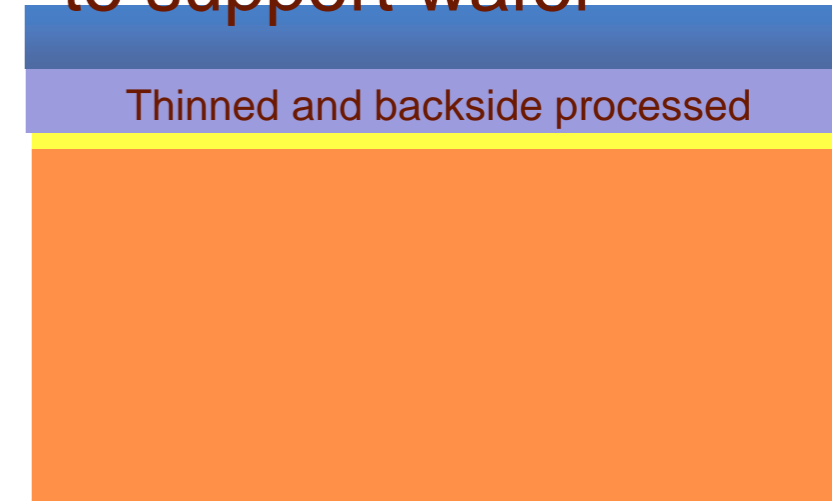
Bulk CMOS/SOI
bonded to sensor



CMOS MAPS
epitaxial layer



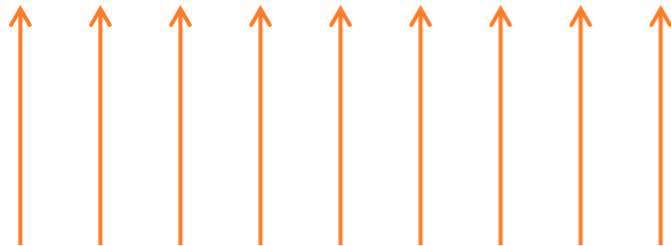
Sensor oxide
bonded
to support wafer



Backgrind



Polish, implant and
Laser anneal



Etch backside silicon



Thinning and Laser Anneal

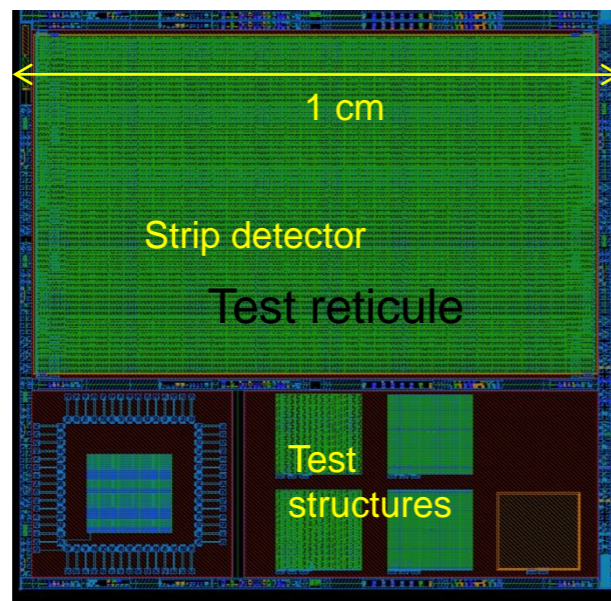
(Cornell, ASI)

To be useable for HEP the bonded detectors need to be thinned and we need to provide a backside ohmic contact to the thinned wafer.

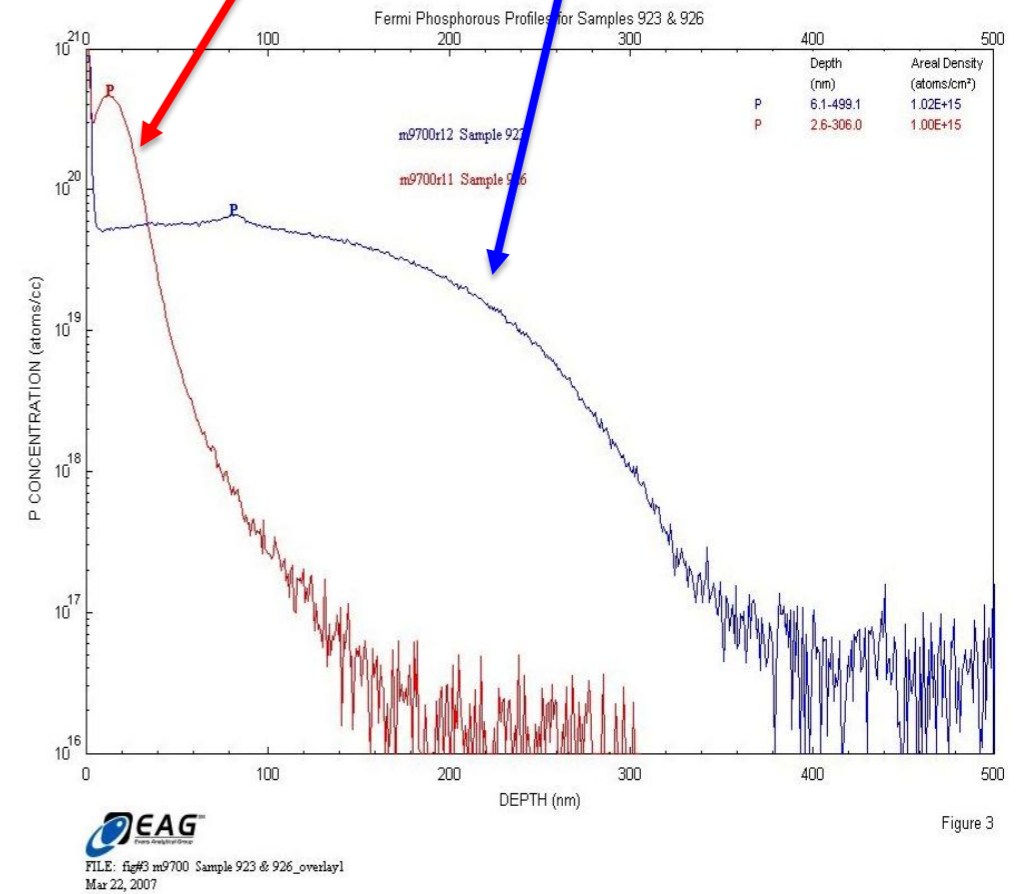
- Normally done by ion implantation activated using furnace anneal at ~ 1000 deg C.
- But the topside has been fully processed and we need to keep the top below ~ 500 deg C to protect topside metal

Use a raster scanned eximer laser at Cornell to melt the silicon backside locally – this activates the ohmic implant and repairs the implantation damage by recrystallizing the silicon

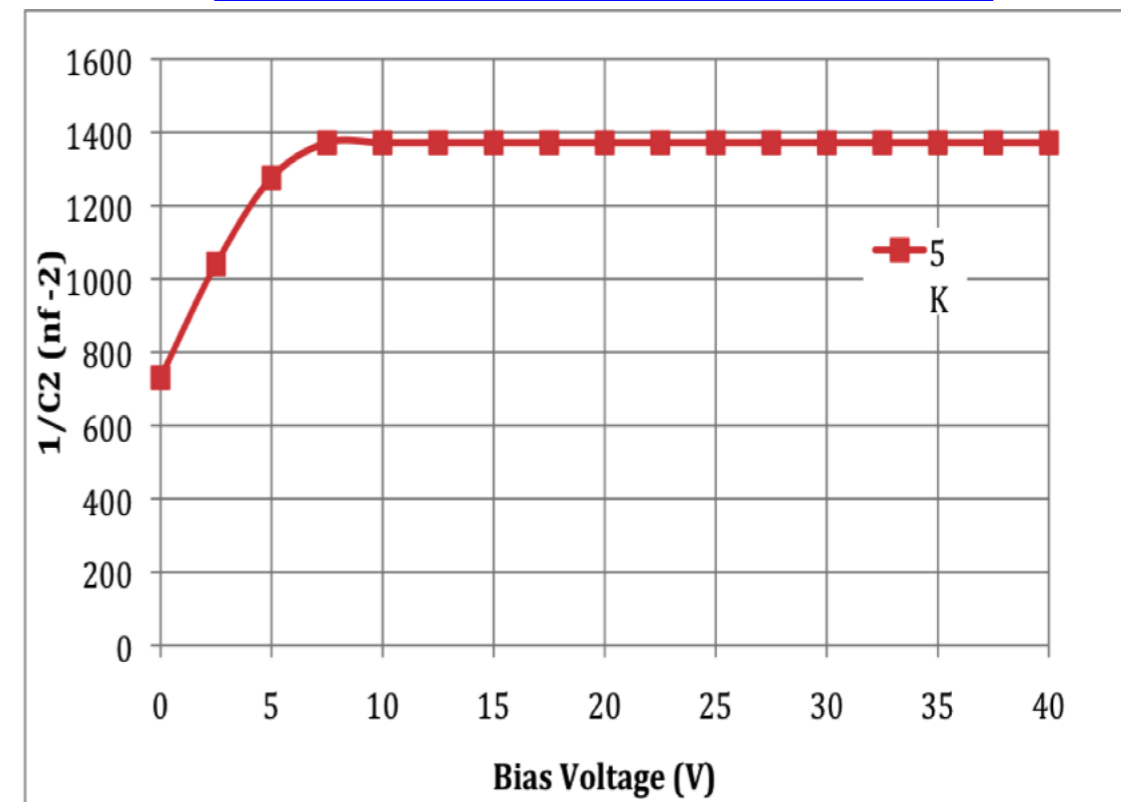
Done for Micron, MIT, OKI/Lapis and American Semiconductor (SBIR) test wafers



Implant before anneal Implant after anneal



Sensor thinned to 50 μm Depletion at 6V

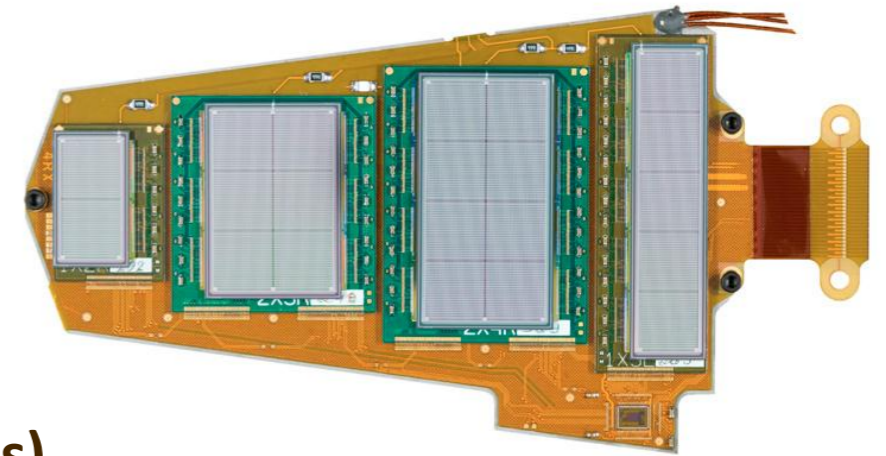


Combining the Two 3Ds

The Problem: Build large area arrays of highly pixelated detectors with minimal dead area and reasonable cost

Current pixel detectors have dead areas arising from:

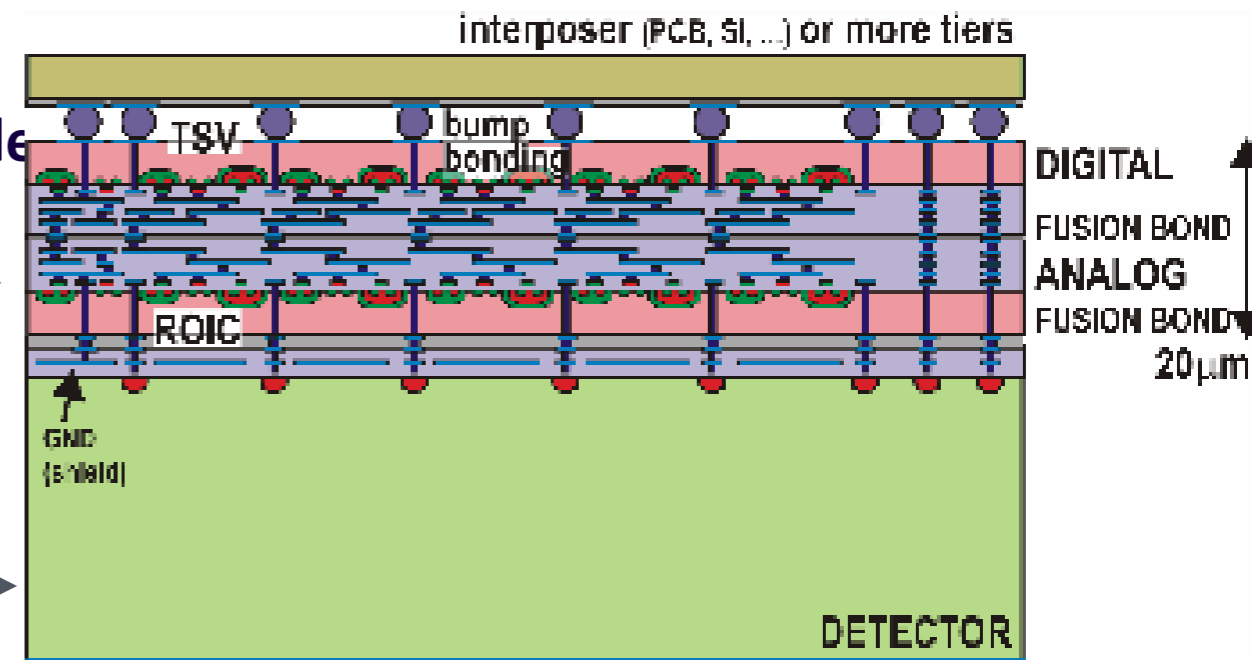
- **Sensor Edges**
- **Wirebond connections for Readout Integrated Circuits (ROICs)**



The fabrication of a large area pixelated array yield with bonding efficiency ϵ is ϵ^n , for $n \sim 25$ (CMS) ϵ must be ~ 1 - typical placement yields are unacceptable

A solution:

- **3D #2 - 3D or vertically integrated electronics provides a backside path for extraction of signals**
- **3D #1 - Active edge sensors remove dead area at the edges**



Combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.

- **These tiles can be used to build large area pixelated arrays with good yield and reasonable cost**
- **Tiles can populate SiD forward disks with optimal tiling and low dead area**
- **Only bump bonds are large pitch backside interconnects**
- **The density and geometrical flexibility means this is exactly what is needed for forward disks at SiD**

Costs and Yields

Component	Current or projected cost	Yield	Comment
Readout IC	\$8/cm ² [6]	65-70% [7]	Current 3D wafers and FEI4 prototype yield
Active Edge Sensors	\$53/cm ²	-	Current cost for prototype 150 mm wafers
Silicon Strip Sensors	\$10/cm ²	100%	CMS tracker costs
Bump bonding	\$213/cm ²	98%[8]	CMS forward pixel costs (2007) Yield \equiv <20 bad bumps/chip
DBI bonding	\$0.04/cm ²	90%	Projected by Yole Development [9] for high volume production
Target Costs (2020s)	\$10/cm ²	90%	Assuming 200 mm sensor wafers and batch active edge process

Current and projected costs and yields for sensor/readout integration technologies

Active Edge Project

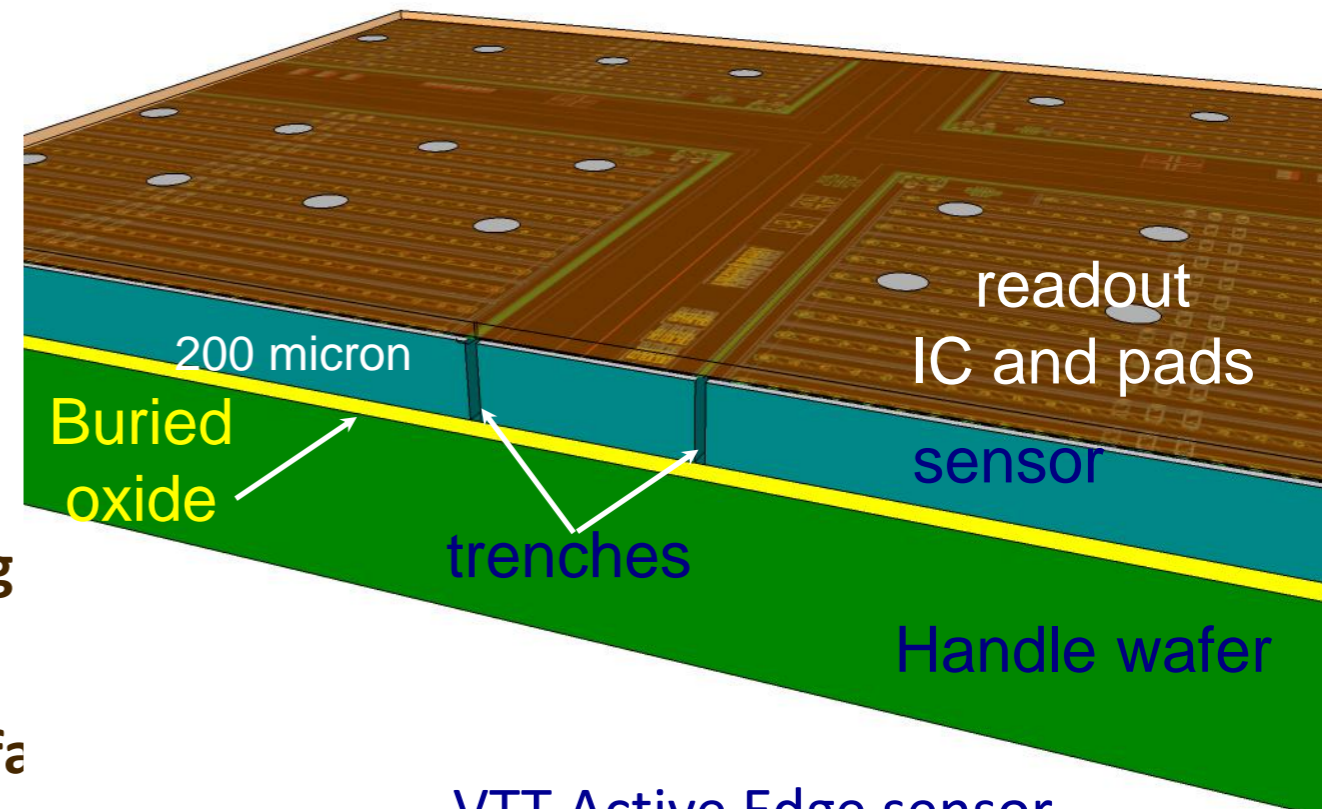
(Cornell, SLAC, Hawaii, Brown, UCSC, NRL)

We are building a demonstration array including active edge sensors, oxide bonded wafers, and “damascene” dummy readout wafers

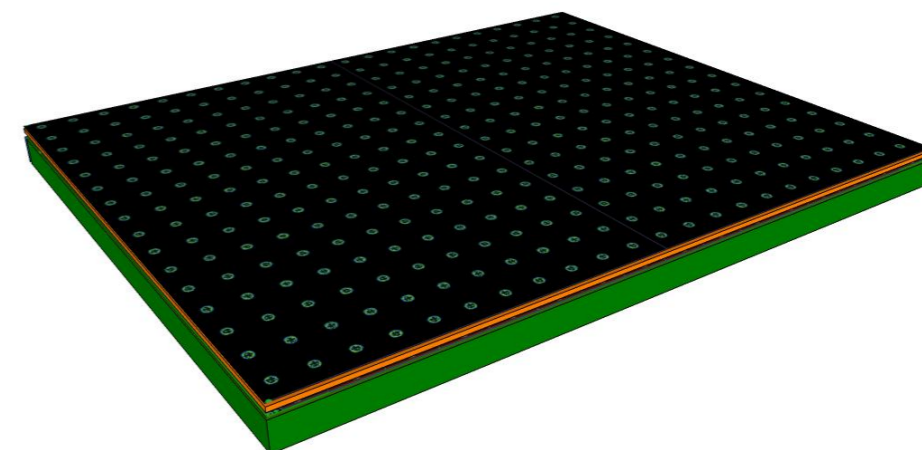
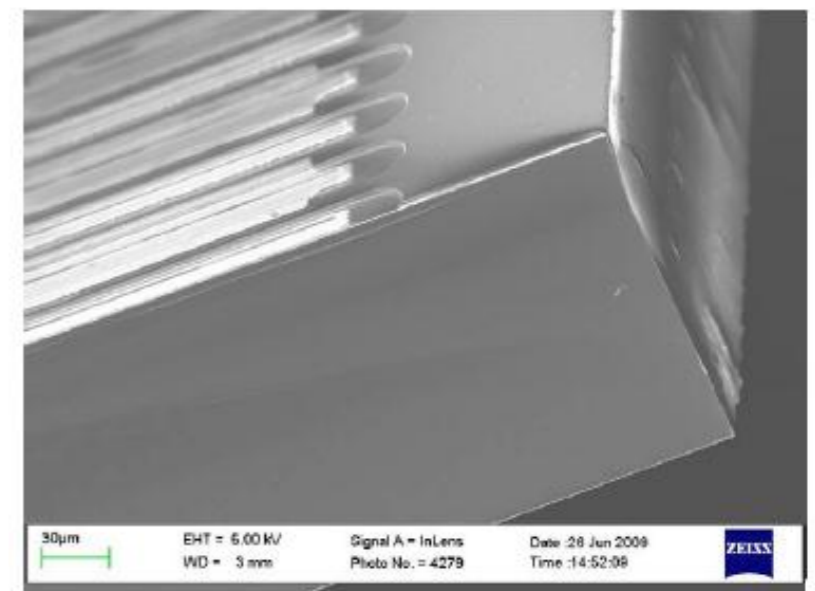
- Sensors (being fabricated at VTT) match the geometry envisioned for CMS track trigger long (1 cm) and short (1.25 mm) strip sensors.
- Top tungsten plug “damascene” wafer is being fabricated at Cornell - designed to readout either long or short strips with single reticule.
- Wafer bonding top thinning and etch and interconnect at Ziptronix
- Singulation and handle wafer removal will be done at Stanford in collaboration with SLAC
- There are no trenches on the edge reticules to allow test of the UCSC/NRL “slim edge” process

Processing of the VTT and Cornell wafers is underway. Ziptronix interface design is complete - should get results next year.

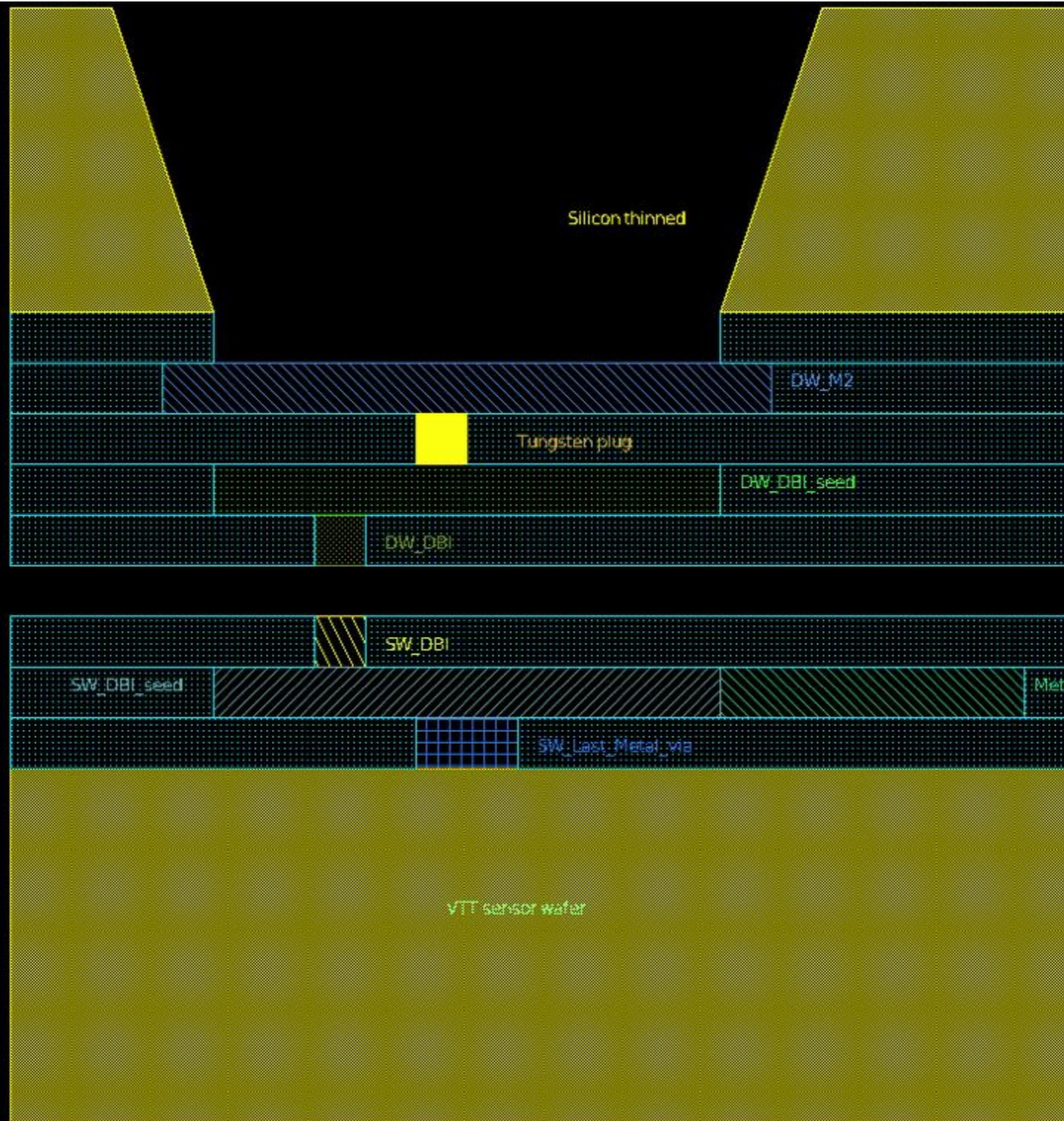
- Next step - move to 8” sensor wafers similar to material in Lapis and American Semiconductor SOI work.



VTT Active Edge sensor



Layer Stack



Vertex DBD

Current status:

- Draft of introductory and sensor sections are done
 - I have assumed 3D sensor technology because that is what I have been thinking about.
 - It is included as an example for definiteness, not a choice.
- I have not included mechanics hoping Bill might contribute, if not it will primarily be copied from the LOI
- Already 9 pages (big figures, 2 pages of placeholders)

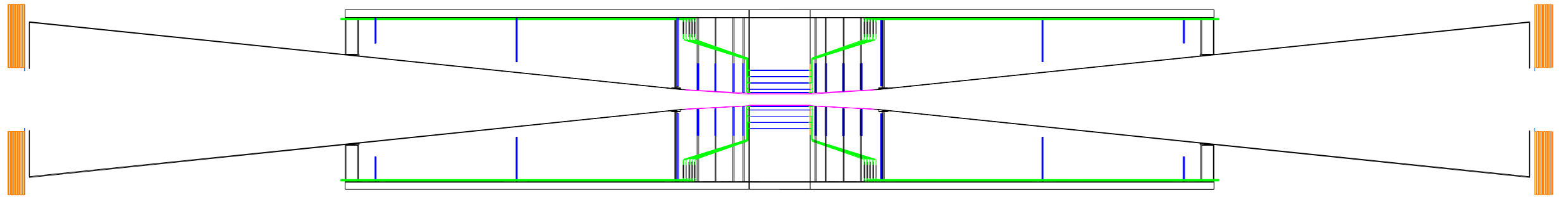
Basic Parameters

The variety of inner radii is awkward, requiring many reticule designs

Barrel	R		
Layer 1	14		
Layer 2	22		
Layer 3	35		
Layer 4	48		
Layer 5	60		
Disk	R_{inner}	R_{outer}	Z_{center}
Disk 1	14	71	72
Disk 2	16	71	92
Disk 3	18	71	123
Disk 4	20	71	172
Forward Disk	R_{inner}	R_{outer}	Z_{center}
Disk 1	28	166	207
Disk 2	76	166	541
Disk 3	117	166	832

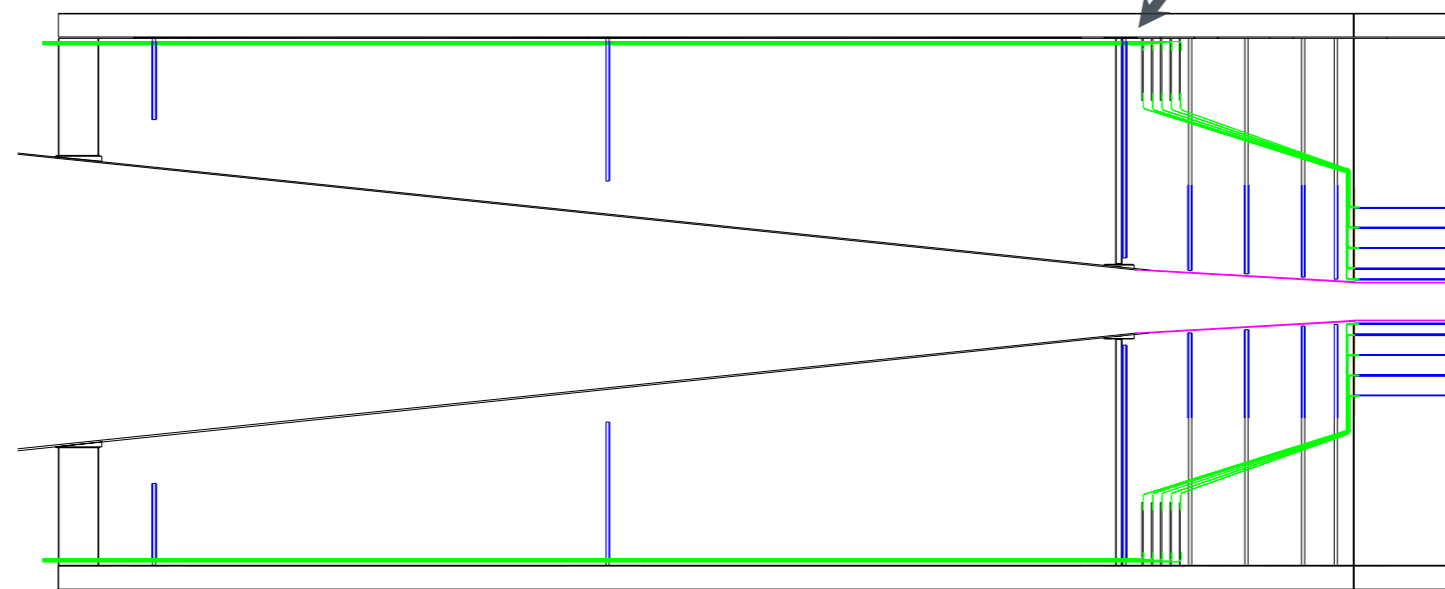
This is OK (later Slide)

Overall Layout



Full Barrel

DC-DC converters

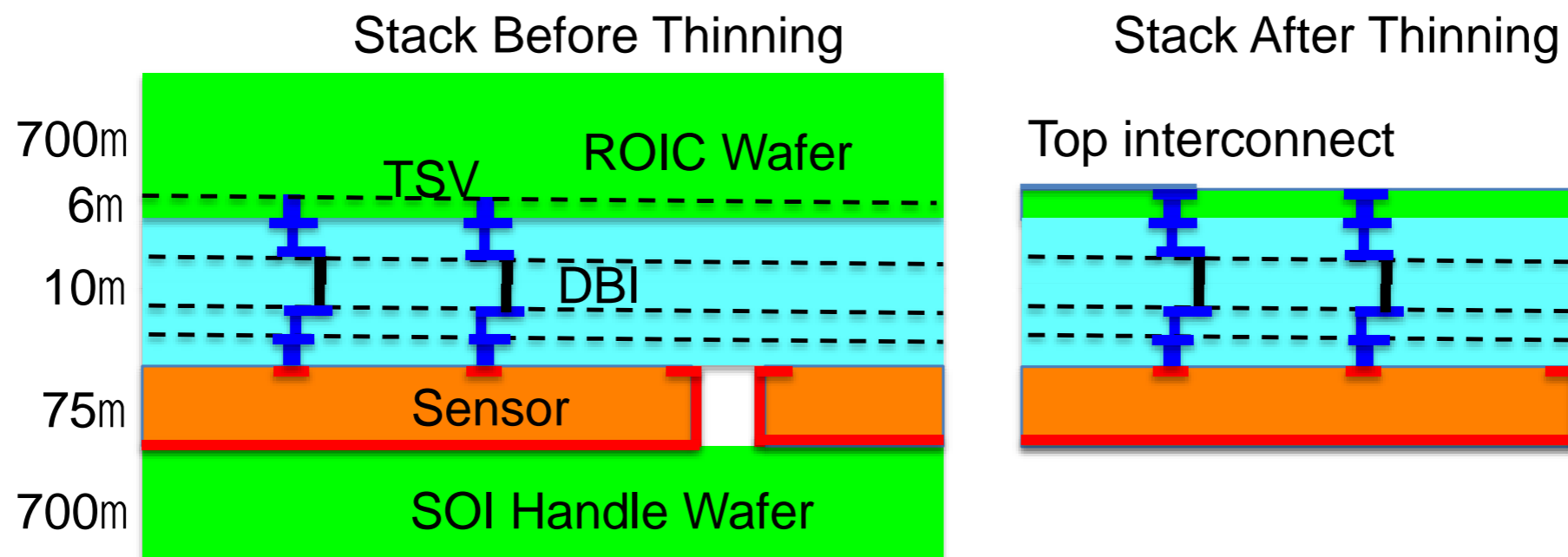


Half Barrel showing
disks, cables and DC-DC
converters

Barrel Tiling

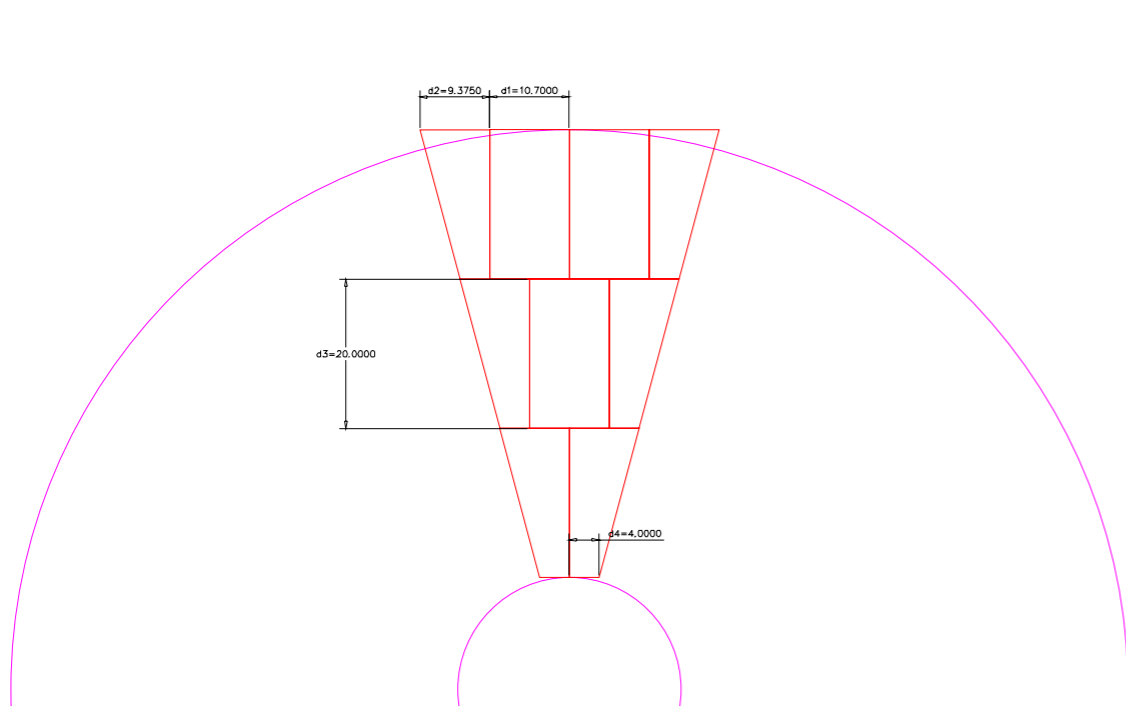
I have kept the all silicon mechanical design. This is difficult to achieve in pixel detectors (other than CCDs) because the natural size unit is the reticule (2.5x2.5 cm)

With a 3D process this can be achieved by matching the sensor spacing to reticules and taking the yield loss requiring 6 working chips. A nice feature is that all of the top interconnect can be done in the final topside aluminum patterning with low mass. Cables are bump bonded to the ends of the ladders.

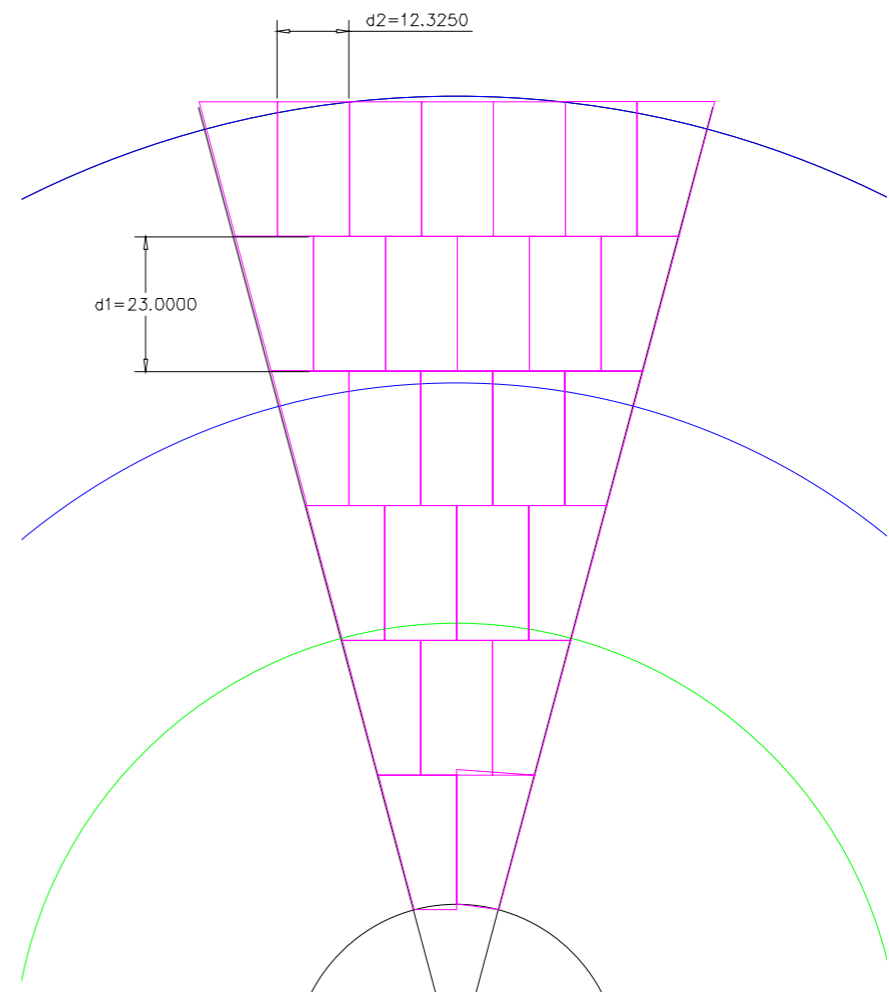


Disk Tiling

The active edge devices are a natural fit for pixelated disks. Only two reticule shapes are needed for the forward disks. More are needed for the inner disks if they keep the small step in radius.



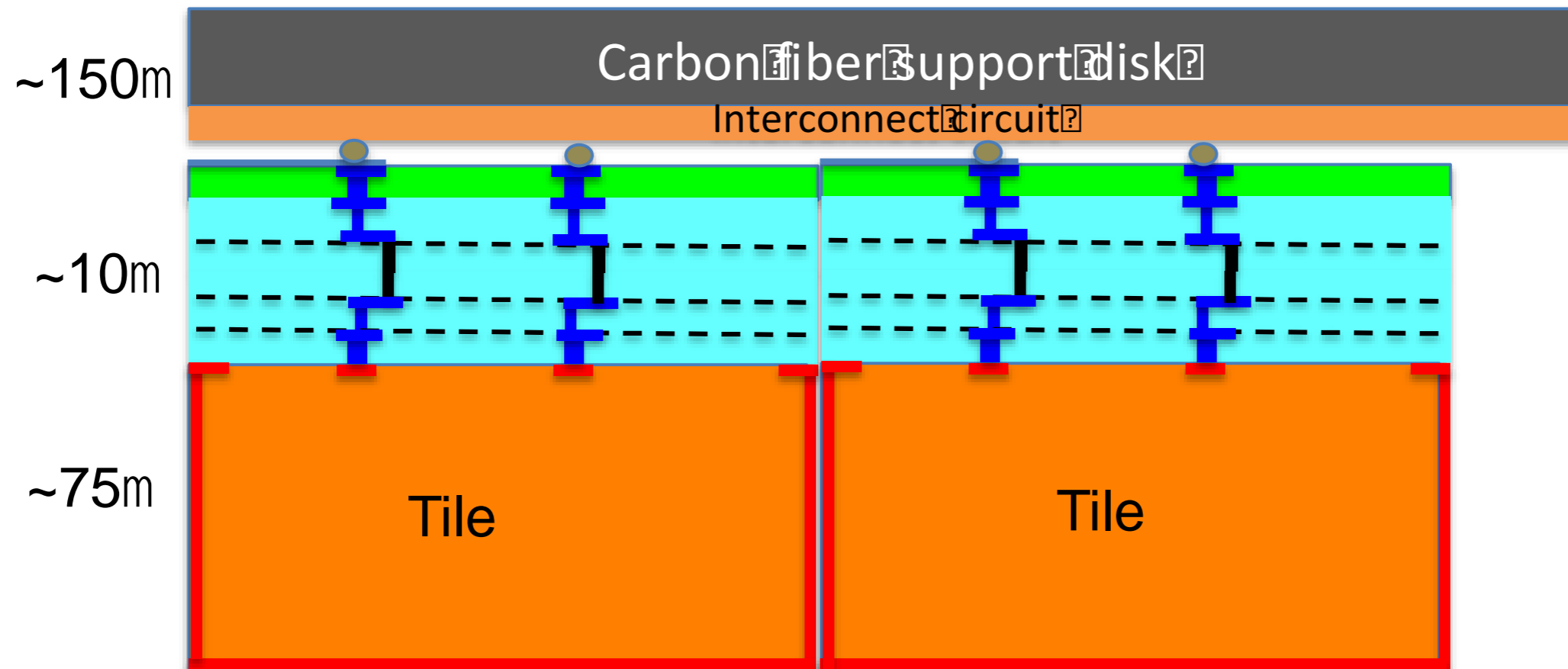
Inner pixel disk



Outer pixel disk radii

Disk Assembly

I assume a slightly higher mass budget for the disks, which allows for carbon fiber supports, still only $\sim 0.35\%$ RL assuming 10 micron average copper trace thickness



This technique can be used for the barrel ladders at some cost in mass.

Missing on DBD

- Text on power delivery and power pulsing
 - Satish will provide some in coming weeks
- Text on cooling
- Text on support structures
- Alignment and vibrations
- Integration and cabling
- Summary of R&D status(?)
- Overall summary

Plans

In progress:

- Test VIP2b (September) – can resubmit to MOSIS 3D run if a problem is found.
- Integrate VIP2b with BNL sensors using Ziptronix oxide bonding – depends on success of backup wafer processing (Fall 2012)
- Demonstrate active edge processes with VTT/Cornell wafers and Ziptronix processing

Next Steps:

- Develop 8” wafer active edge process using SOI wafers from American Semiconductor or Lapis
- Demonstrate fabrication of arrays of tiled sensors

No plans to pursue SiD vertex-specific full reticule design unless motivated by immediate needs. “Generic” work will continue