Tracking DBD Editors' Report

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Tracking DBD Status

- First draft of document, a lightly edited version of the SiD LOI, is in SVN.
- In the coming weeks, the sections need to be updated/replaced.
- Meanwhile, any new work must be completed, summarized and added.
- First tasks:
  - assess scope of changes
  - identify and summarize status of ongoing work we would like to include
  - ➡ These are my goals for this talk

Scope and Key Components

In terms of *content*, DBD is a modest evolution of the LOI. Key points are still...

- Explanation SiD tracking philosophy
- Description of detector layout and design
- Discussion of technologies and implementation
- Status of R&D
- Tracking performance estimates

Task: better organize/streamline, better focus on critical details, and update with most recent developments

Reorganization

LOI Outline

DBD Outline

More formal separation between tracker and vertex detector and more structure in tracker section

Introduction

3.1 Introduction

- Overall geometry
- Silicon tracker requirements and the basis for each (point resolution, momentum resolution, material budget, occupancy)
- Integration of tracker, vertex detector, and calorimetry

Nothing new here:

- SiD tracker is an integrated system, including the vertex detector and ECal
- SiD baseline uses mostly well-established technologies to instrument a large tracking volume with excellent performance at low risk and cost.

LOI text does a fine job of describing and explaining these points:

➡*Only minor editing required. Wonder whether "Tracker" should be renamed "Outer Tracker" in recognition of extent of integration with VXD (Inner Tracker)?*

Baseline Design - Layout

Nothing new here:

- Outer tracker uses silicon microstrips, axial in barrel and stereo in endcaps. Interplay with vertex detector design is critical!
- Outer tracker slides over VXD and beamline elements to allow access to VXD and beampipe
- A detailed concept of the layout, including positions of all sensors and mounting/support concept has been in place since LOI.

LOI text does an adequate job of describing and explaining these:

➡ *Reorganize and rewrite existing material to fit new outline.*

Technologies and Implementation

(Almost) nothing new: baseline utilizes relatively conventional technologies

- Single-sided silicon microstrips with double-metal readout
- KPiX readout ASIC *and cable* bump-bonded to sensor to reduce material and complexity of in-house assembly.
- Sensors glued to CF/Rohacell frames with PEEK mounts to form modules.
- Modules attached to PEEK mounting clips on CF/Rohacell support cylinders (barrel) and cones (endcaps) to complete a layer.
- Layers are nested, supported by rings and endcap interfaces that host power/ readout distribution boards.

LOI text does a fine job of describing and explaining these:

➡ *Text will benefit from some tightening along with required reorganization*

Status of R&D - KPiX / Sensors

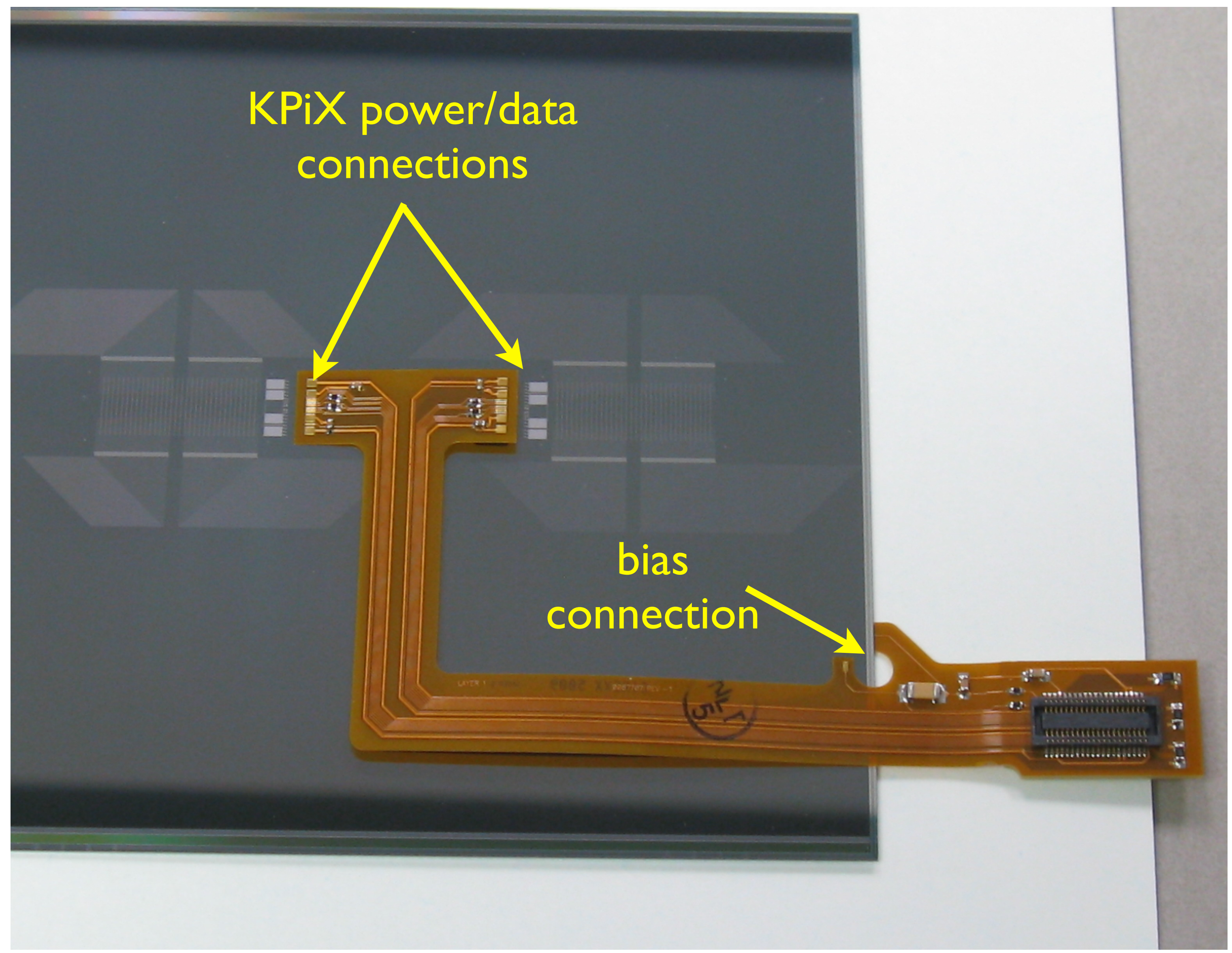
- Significant progress by the KPiX group (SLAC, Oregon, Davis, *UCSC*, ...)
  - Full 1024 channel KPiX now bonded to ECal sensor
  - Solder bonded readout cable
  - This work applies directly to the tracker as well: same interconnection problem...
- Prototype sensors suffered same defect as ECal sensors (similar design and identical vendor/process.)
  - weak inter-metal dielectric damaged by wire bonding and some bumping processes
  - has precluded planned assembly of prototype module for tracker
  - HPK has acknowledged the defect with new process (thicker dielectric). However, quoted cost for new prototypes reflects no price break.

Fortunately, bonding progress for ECal allows R&D to progress with existing sensors.
Will discuss progress on KPiX and interconnection in context of tracker.

Status of R&D - Readout Cable

- UNM *(Seidel, Hoeferkamp)* has produced a nice pigtail prototype
- ... but designed for wirebonding
- Putting together setup to allow testing with bare KPiX now
- planning redesign accommodate solder bonding (like ECal)
- Considering other modifications to improve resistance to Lorentz effects, minimize signal coupling to KPiX input nodes.

An example of ongoing work.

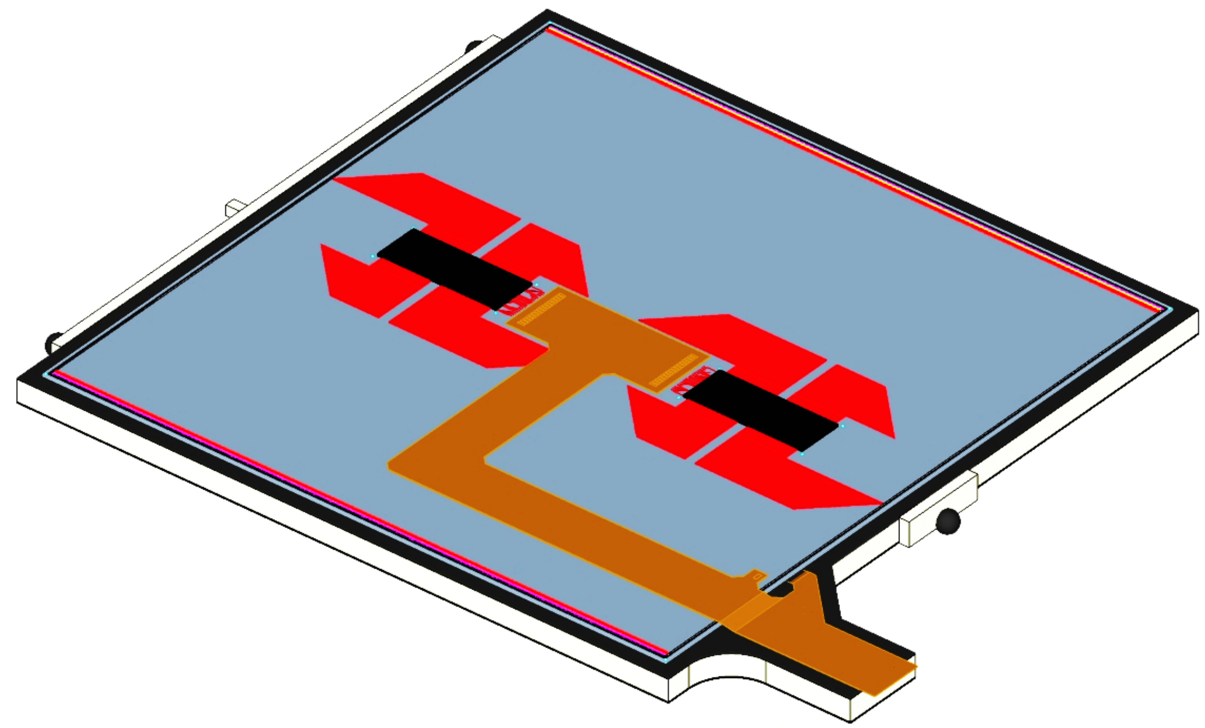


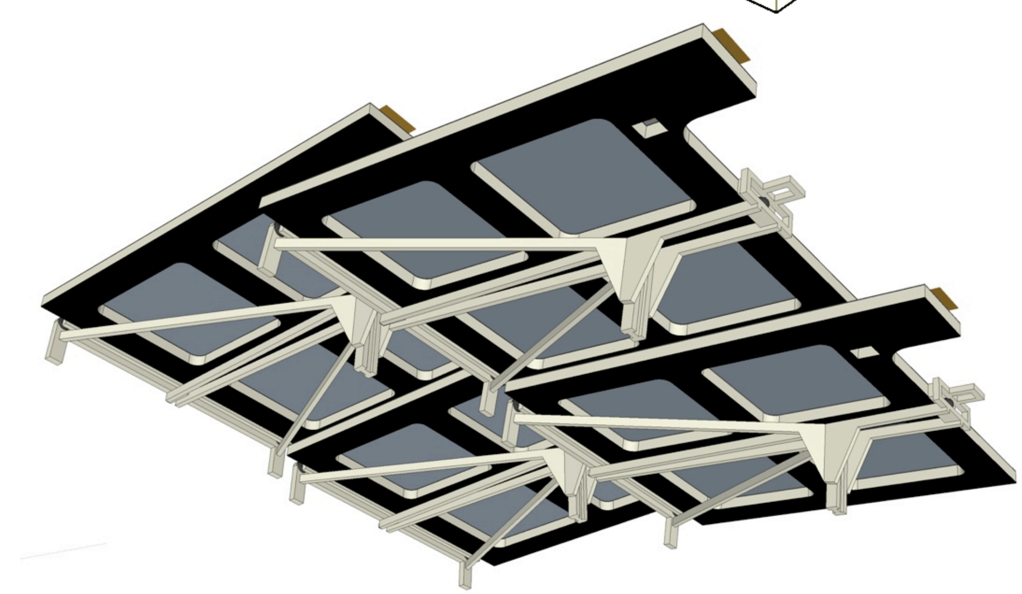
Status of R&D - Power Issues

- Power distribution (DC/DC conversion or serial power)
  - Common issue with ECal and VXD (and also LHC upgrades!)
  - No need for tracker-specific work at this stage, but work at Yale is certainly relevant.
- Power pulsing
  - Lorentz forces/vibration.
  - Nothing yet, but planning to pursue testing as part of cable design/testing effort.
- Gas cooling and vibration.
  - Not aware of any plans, but would be nice to refer to some specific R&D.
  - Interesting work done for other experiments. For example, LBL is building an air-cooled, two-layer, 0.37% X_0/layer, 350 MPixel, MAPS-based pixel detector that generates 240W in about 0.1 m^3 for the STAR HFT.

Status of R&D - Support/Mounting

- The designs for both module supports and large scale support elements are quite conventional and carry little risk.
- Aside from non-essential details, the same is true for module mounting
- However, it is nice to have something to hold in your hand.
- Would also like a prototype that could be placed in test beam.
- This is still something we plan to do with 3d printing in the near future.





Status of R&D - Other Items

Decide how to treat/update

- upgrades to baseline
  - pixels (what flavor?)
  - strips with resistive charge sharing (UCSC)
- other R&D
  - FSI alignment monitoring (UMich)

3.3 Critical R&D

- Development of KPIX chips and associated sensors
- Studies of alternative sensors and readout to provide z information
- Development of designs and fabrication techniques for barrel sensor modules
- Design and development of sensors and modules for the disks
- Studies of signal to noise and crosstalk
- Studies of pulsed power, power delivery, and associated vibrations
- Development of cabling
- Studies of heat removal
- Studies of alignment precision and monitoring

Tracking Performance

Simulation infrastructure has seen many improvements:

- LOI used approximate geometry for performance studies, even though simulation of detailed "planar" geometry was already available.
- CLIC-SiD implemented full planar geometry for CLIC CDR.
- For DBD, we should be presenting results using detailed geometry. Much of this work has already been done (Rich Partridge / CLIC-SiD)
- In addition to SiD work, work for ATLAS and CLIC CDR uncovered several bugs and resulted in a number of improvements to org.lcsim tracking. Further improvements have resulted from use of lcsim for the HPS experiment.

Performance studies must be updated for DBD.

Tracking Performance

Updating performance estimates is an involved task:

- CLIC-SiD worked hard to identify key performance measures beyond those in SiD LOI. We should examine those and assess their inclusion in SiD DBD.
- During work for CLIC CDR, some corner cases were identified where performance suffered. Some of these were addressed for CLIC-SiD, but not clear whether some tuning of layout/strategies will be required for SiD.
- We need to be ready to make small perturbations to the design/tracking.
- A significant amount of computing time is required even for a single pass: we need to move quickly if we want to be able to respond to surprises.

We need to push hard on this if we want to finish in time.

Conclusions

- The task of reorganizing the content of the LOI to suit the DBD can be completed relatively quickly.
- We need more discussion with those who have been working on the key R&D efforts to decide what should be said about each.
- We need to decide how to refer to and discuss R&D that is not tracking specific but is directly relevant to tracker (e.g. KPiX, powering). Requires some coordination with editors of other sections.
- The most critical task is updating the performance studies. Quick action is required to make this happen in a timely way.