



Status and plans of the CALICE AHCAL

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LCWS 2013,
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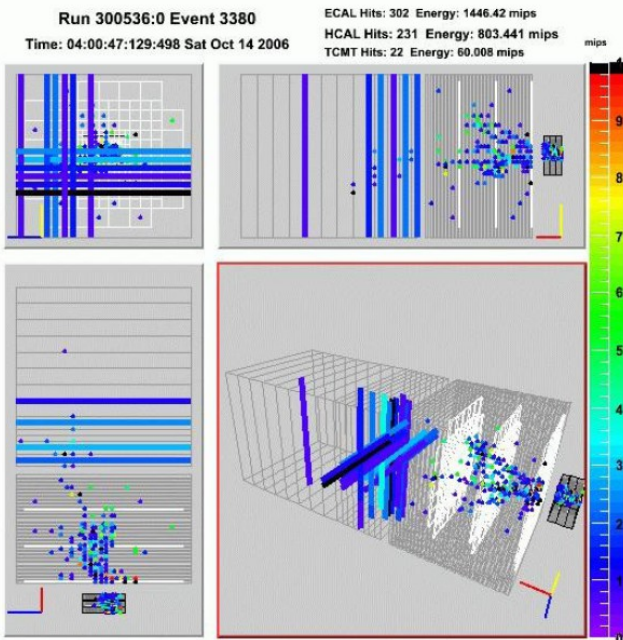
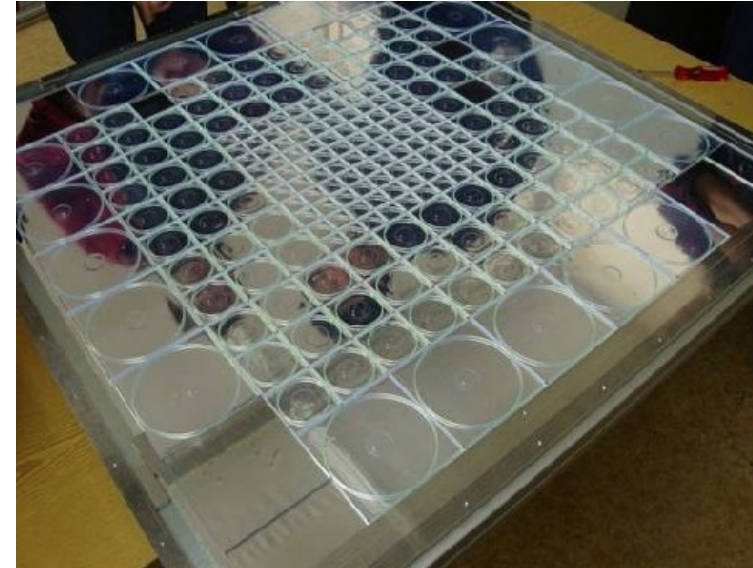
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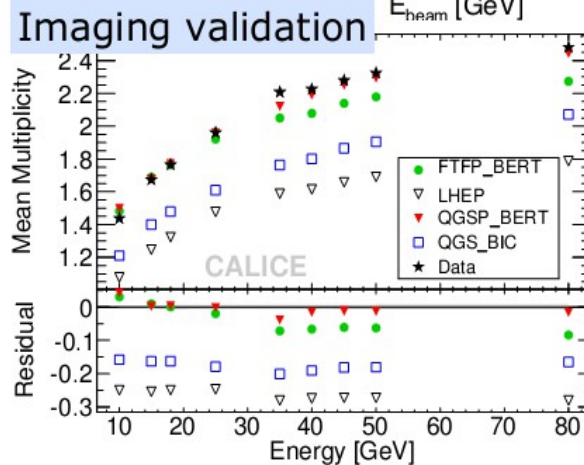
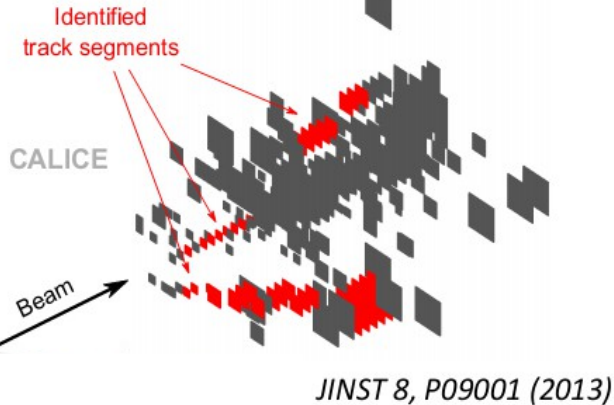
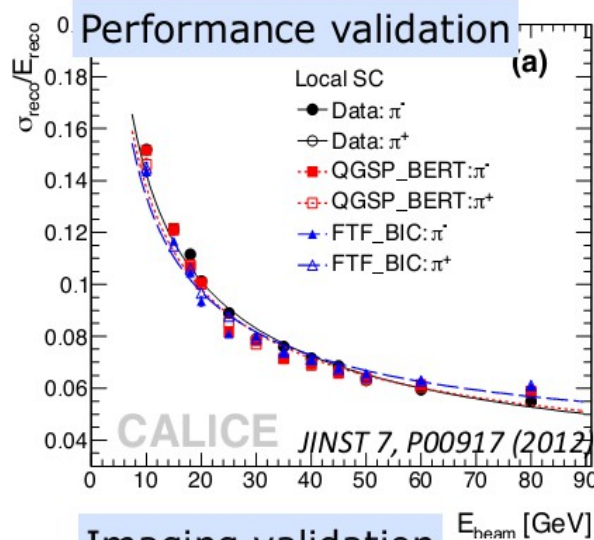
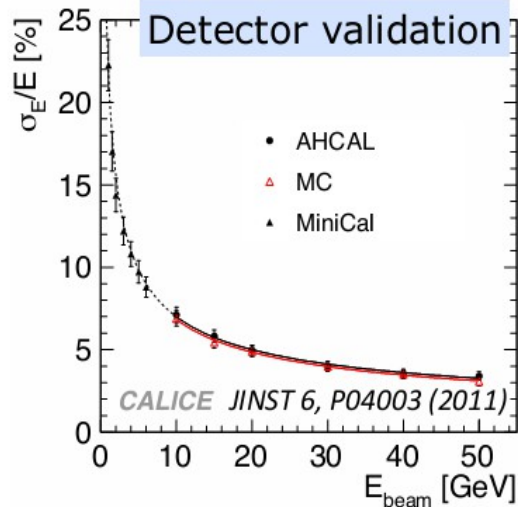
CALICE AHCAL

- ◆ CALICE **A**nalog **H**adronic **C**ALorimeter (AHCAL)
- ◆ Based on Scintillator tiles ($3 \times 3 \text{cm}^2$)
 - ◆ Individual Silicon Photomultiplier (SiPM) per cell
- ◆ 1m^3 physics prototype used in different testbeams 2006-2012

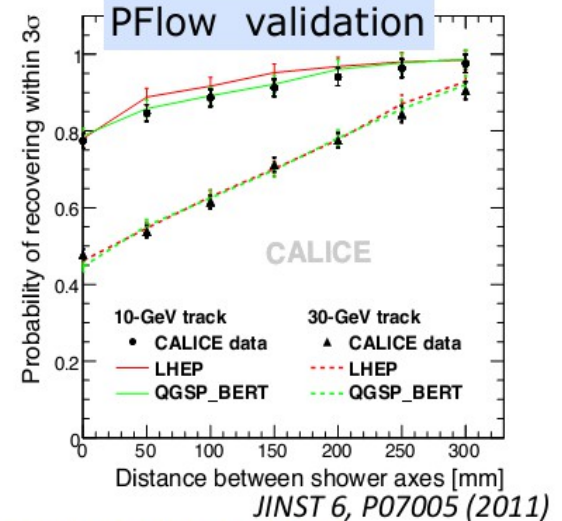
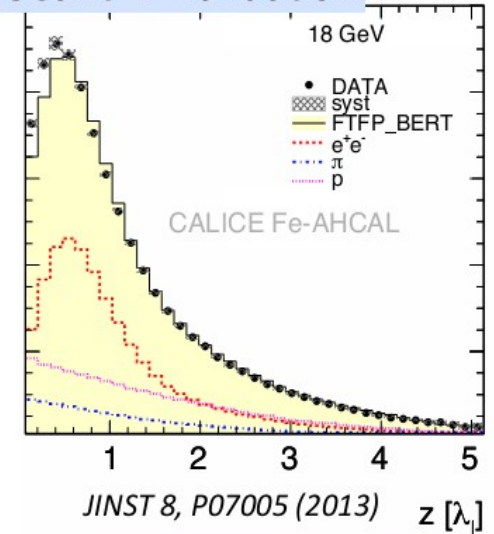


AHCAL Performance

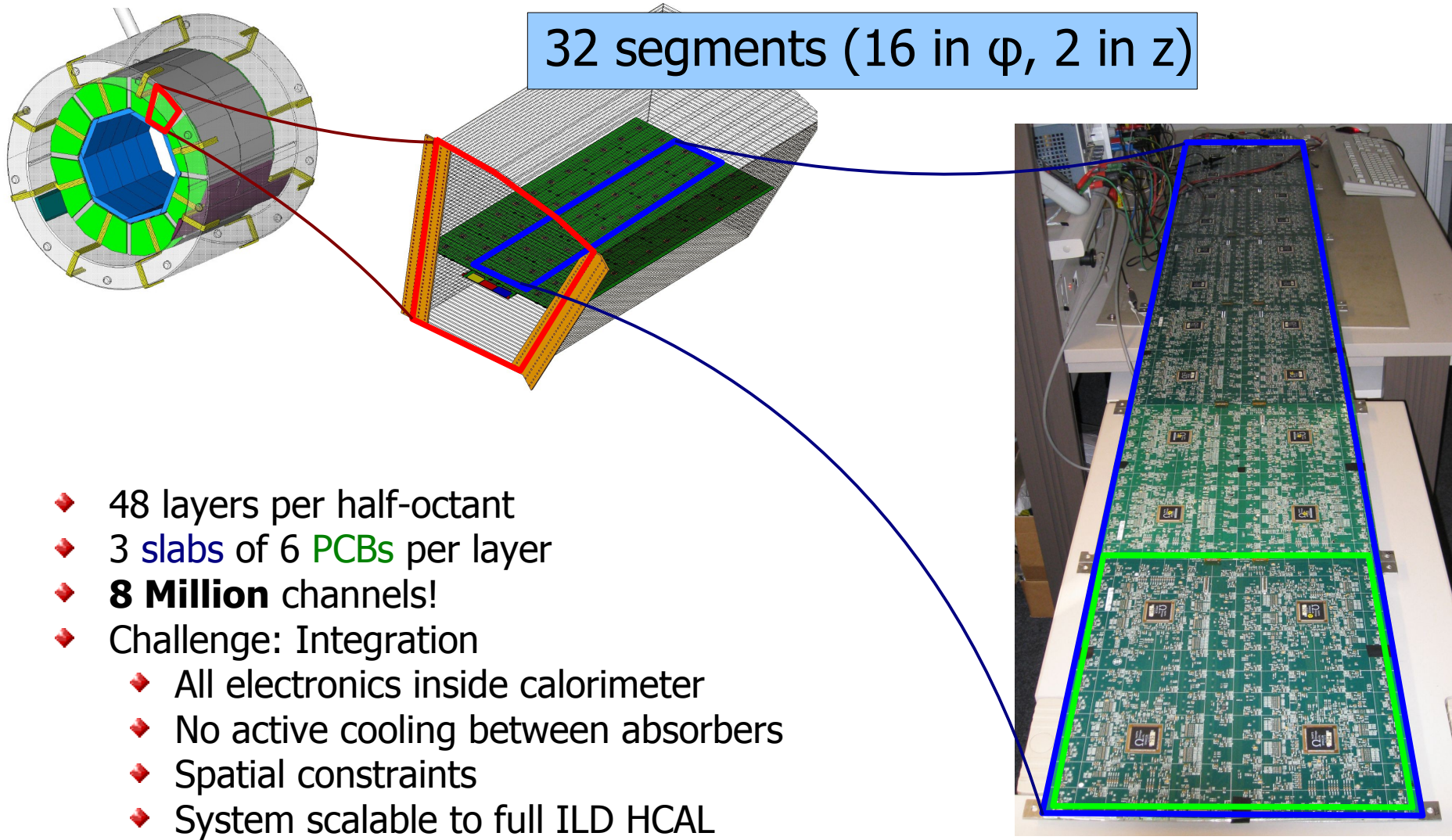
- ◆ Performance of concept validated with prototype
→ Various published results



Geant 4 validation

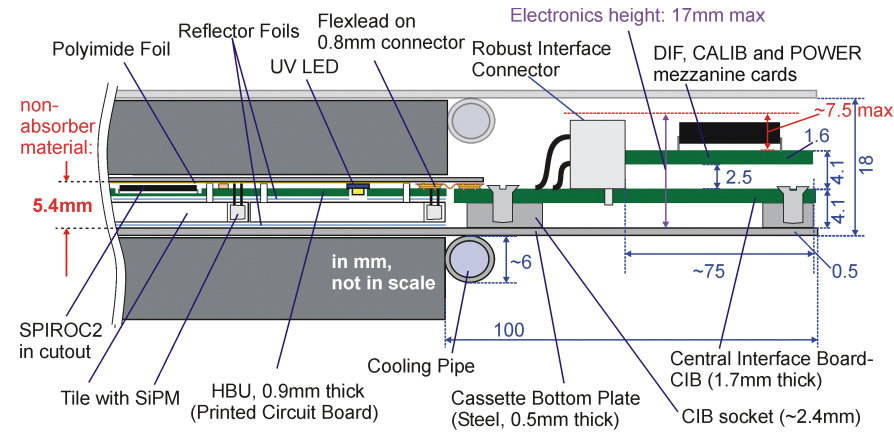


The AHCAL Engineering Prototype



The HCAL Base Unit (HBU)

- ◆ 4 ASICs, 144 channels per PCB
- ◆ Designed within ILD constraints
 - ◆ Extra thin PCB, cutouts for ASICs
- ◆ SPIROC2b frontend ASIC (OMEGA, France)
 - ◆ Specifically designed for AHCAL/ScECAL
 - ◆ Full self triggered operation
 - ◆ Hitwise time stamping (<1ns resolution)
 - ◆ Power pulsing capable
- ◆ See next talk (A. Ebrahimi) about electronics



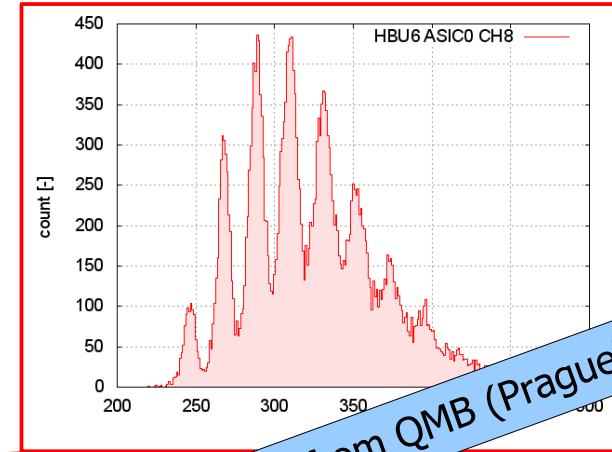
The road to a full prototype

Operation modes to be tested:

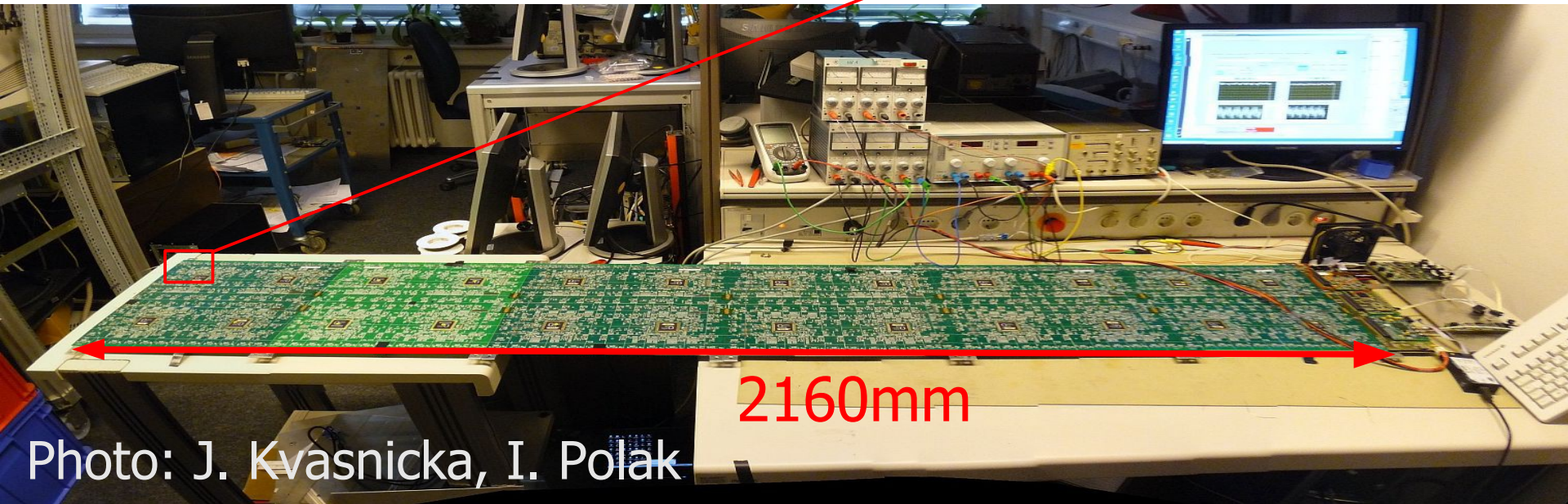
- ◆ Single boards in the lab ✓
- ◆ Single boards in testbeam ✓
- ◆ Multiple boards in one slab (1D extension)
- ◆ Multiple HBUs in one layer (2D extension)
- ◆ Multiple layers in one detector (3D extension)

Full Slab Test

- ◆ Full slab assembled in lab
 - ◆ 6 serial HBUs
- ◆ Readout, calibration, power pulsing tests
- ◆ Excellent data quality via 2.2m signal path
- ◆ 1D extension established ✓

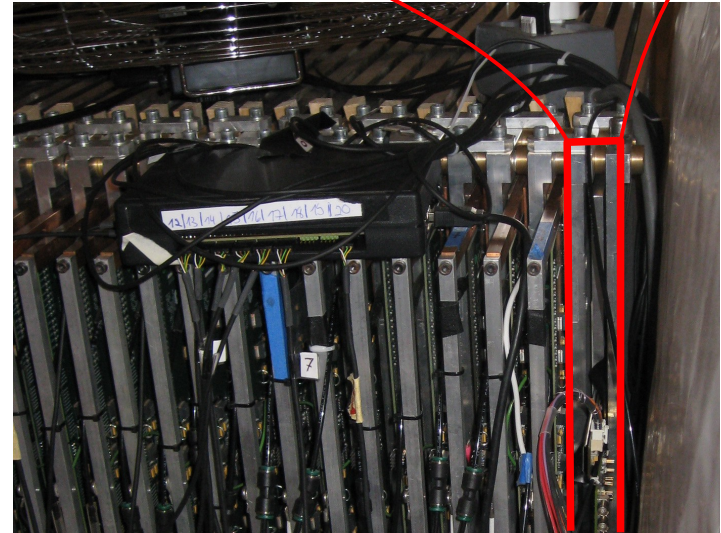
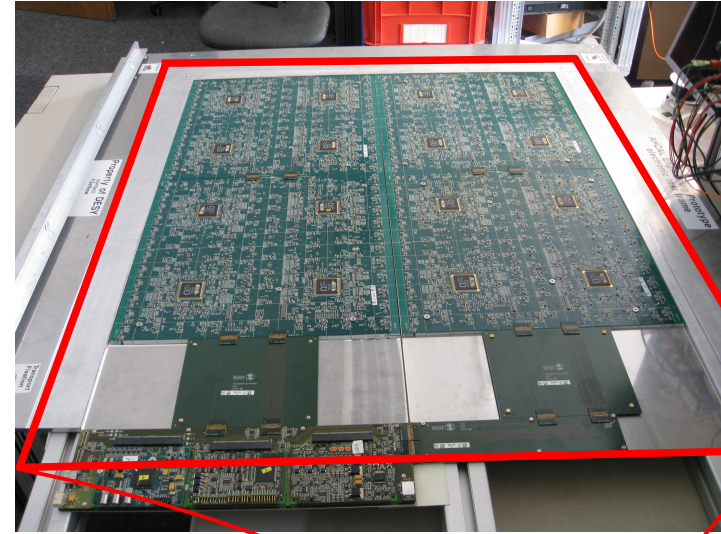


SPS from QMB (Prague)



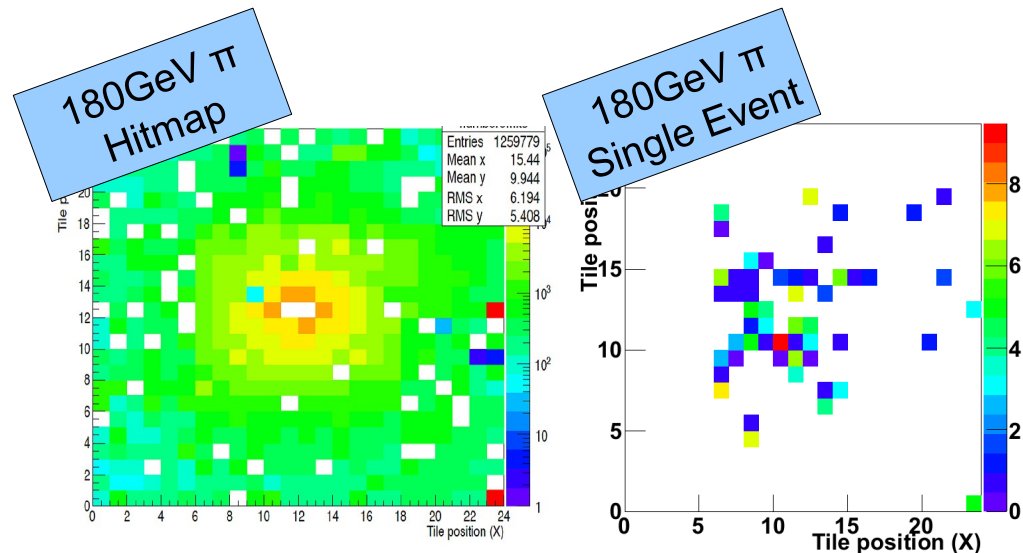
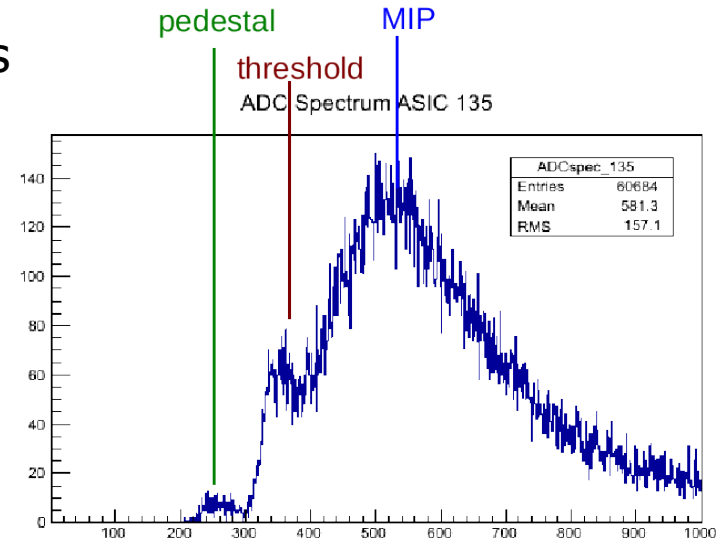
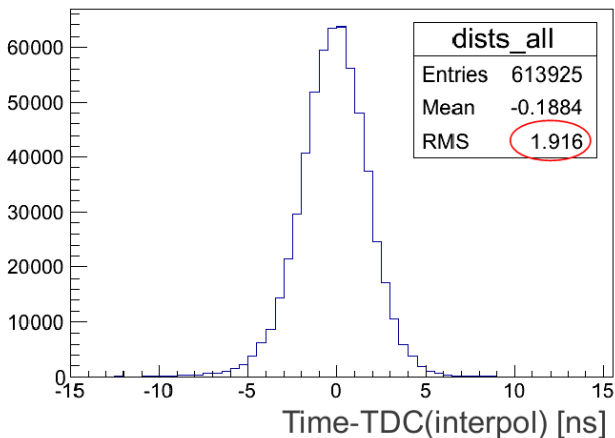
CERN Layer

- ◆ 2012 CERN hadron beam
 - ◆ 4 HBUs ($72 \times 72 \text{cm}^2$), 576 channels
 - ◆ Measurement of hadron shower hit timings
 - ◆ Operation in last layer of CALICE W-DHCAL
 - ◆ Parasitic data taking
 - ◆ Fully autotriggered, low beam rates (20-2000Hz)
 - ◆ Stable operation
- 2D extension established ✓



CERN Layer: current results

- ◆ Various runs: 180GeV Muons, 50-180GeV Pions
- ◆ Critical threshold setup
 - ◆ MIP response equalised channelwise
→ Single threshold per chip
- ◆ Hit timing needs precise TDC calibration
 - ◆ Work in progress
 - ◆ ~2ns time resolution for **electronics only**

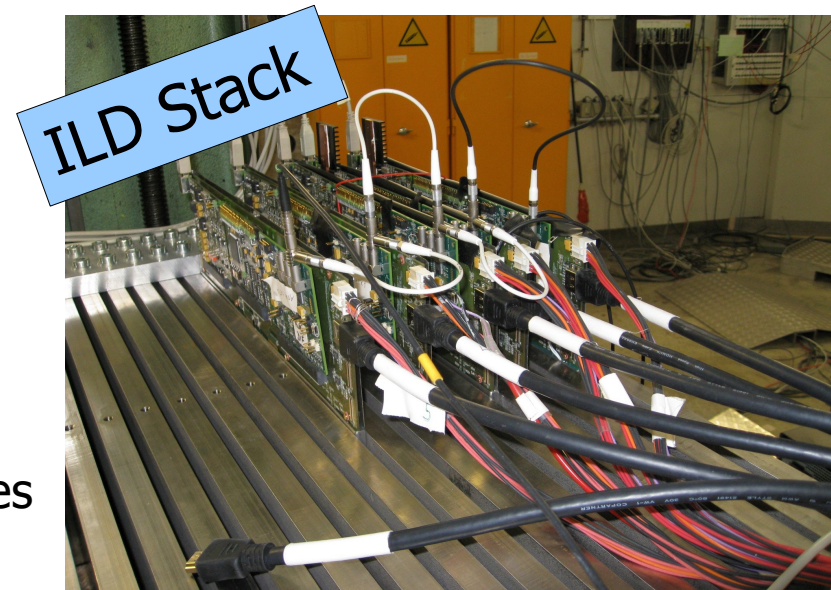
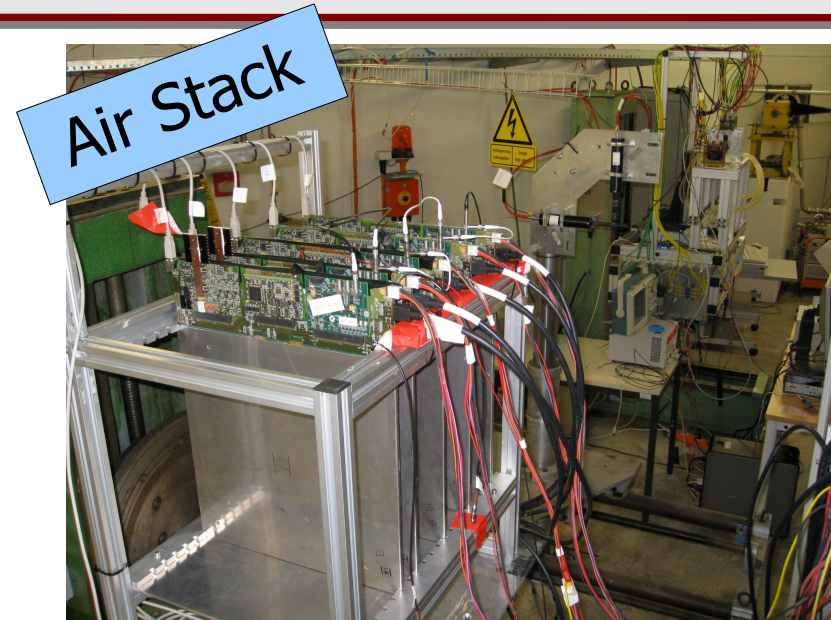


Towards a small HBU stack

Intermediate goal: Small stack for DESY electron beam

- ◆ System tests
- ◆ Performance validation
- ◆ Calibration strategy
- ◆ ILD Mechanics test

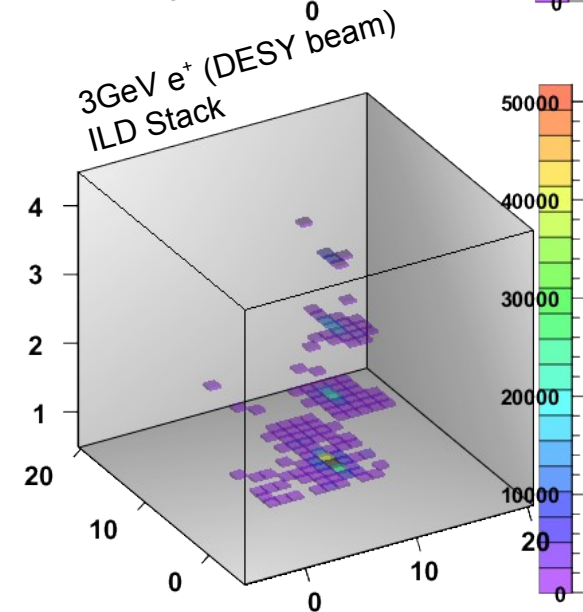
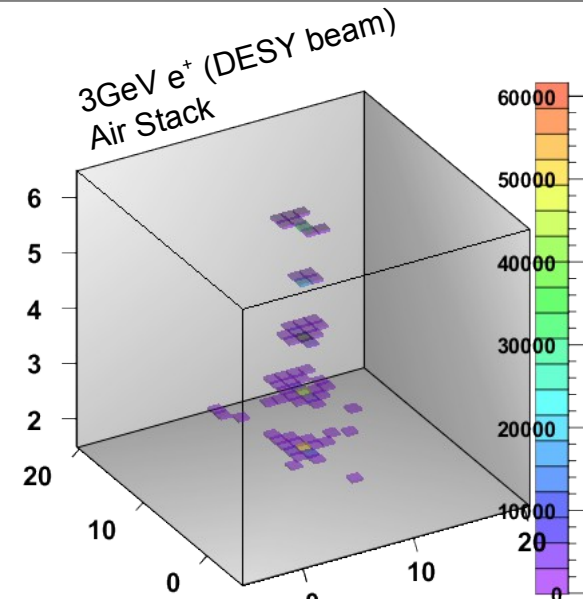
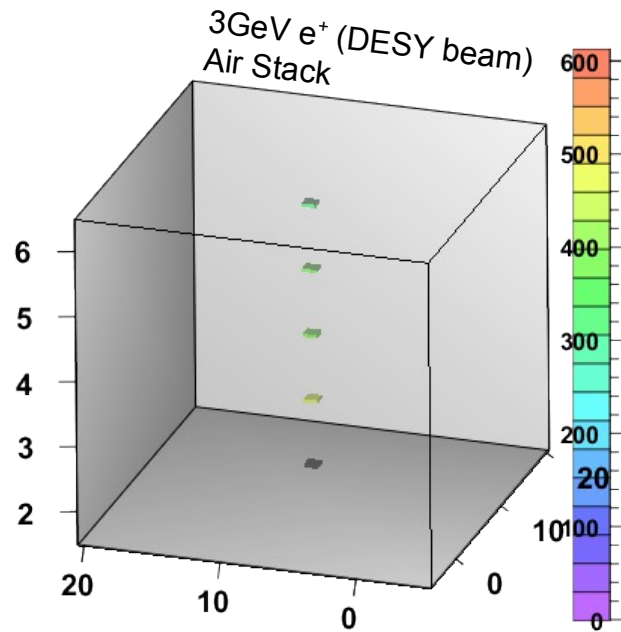
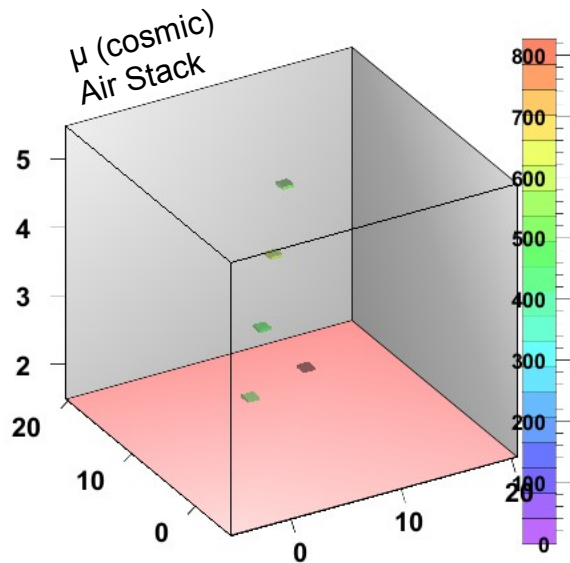
→ Flexible test bench for tile/SiPM options



- ◆ Air stack for cosmics/MIP calibration
- ◆ ILD absorber prototype (Fe) for EM showers
 - ◆ Permanent installation in DESY TB22
- ◆ Mechanics in final ILD dimensions & tolerances

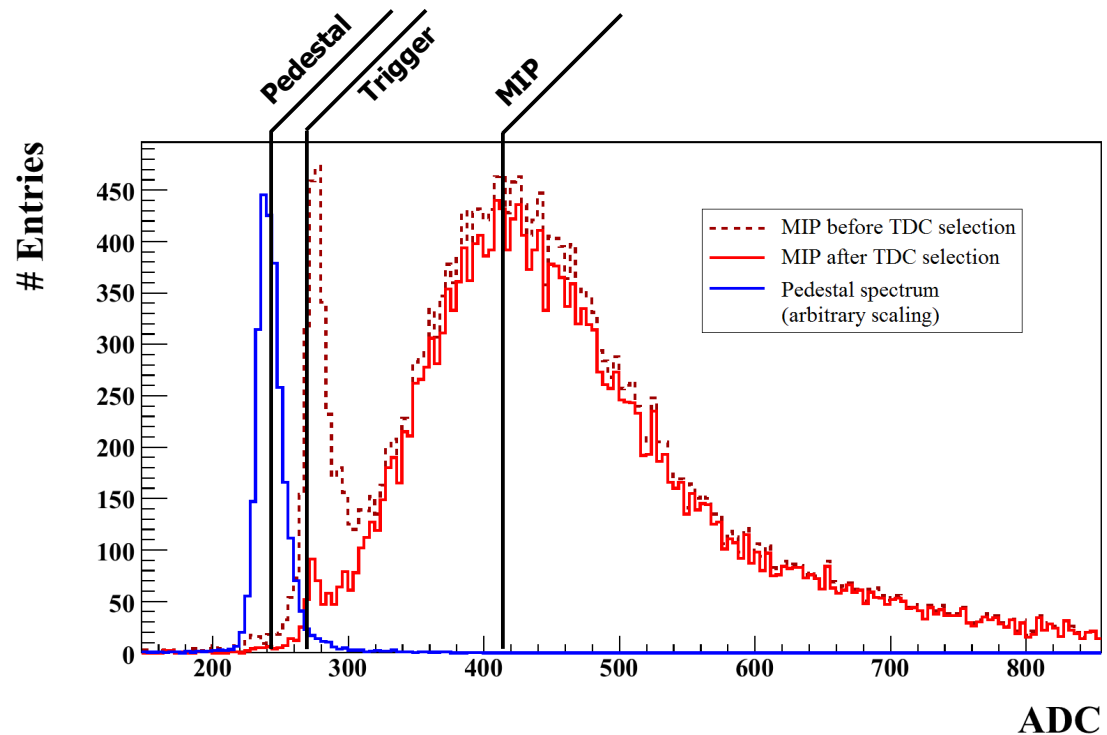
Multilayer Test Beam

- ◆ Operation of up to 5 synchronous layers
 - ◆ Parallel runs with ScECAL layers
- ◆ Fully self-triggered
- ◆ MIPs and showers taken
 - ◆ 1-5 GeV positrons



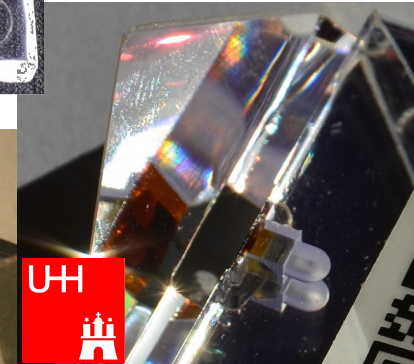
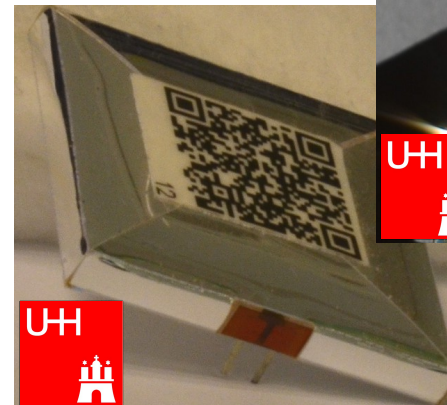
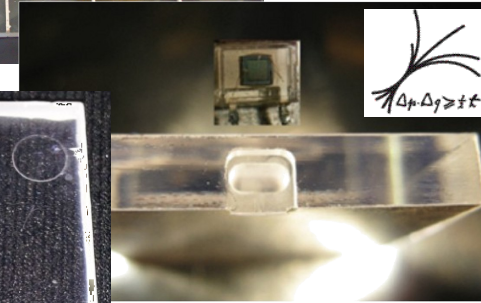
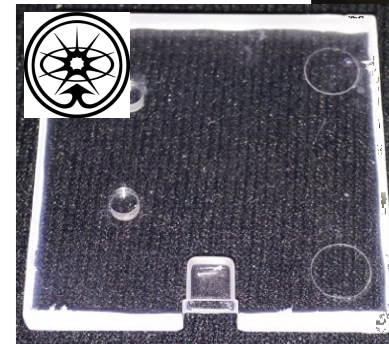
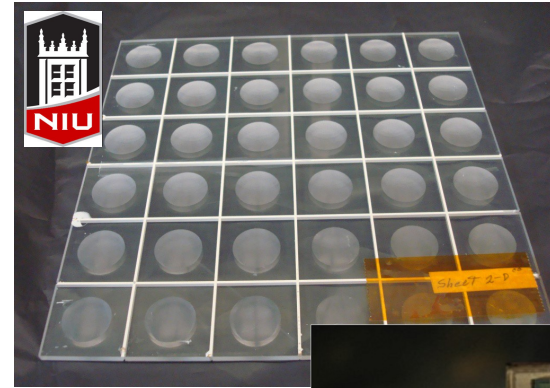
Multilayer MIP calibration

- ◆ MIP calibration through 4 layers
- ◆ Noise suppression
 - ◆ Online: External trigger validation
 - ◆ Offline: Hit timing correlations
- ◆ **0.1MIP** threshold
 - ◆ Minimum noise fraction
 - ◆ Minimum signal loss
- ◆ Multi layer operation: ✓



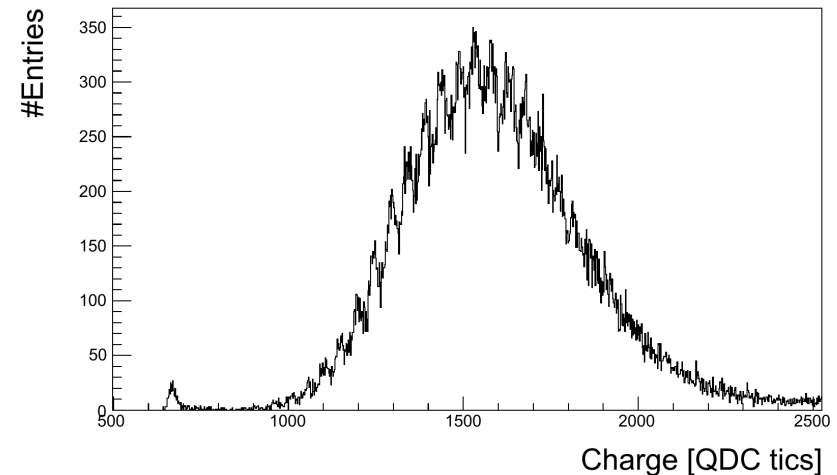
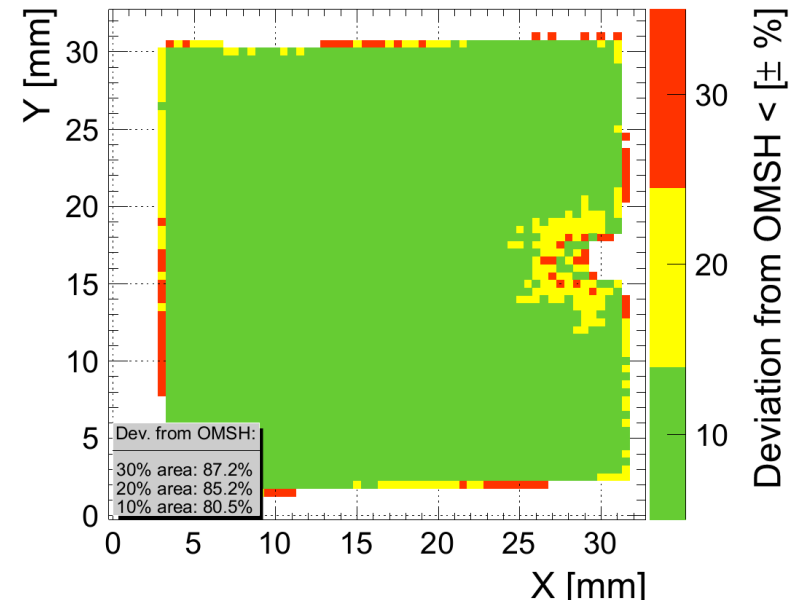
Fiberless Tiles

- ◆ Optimising tile design for mass production
- ◆ SiPMs now blue sensitive, no WLS fiber needed
 - ◆ Need to ensure uniformity without fiber
- ◆ Idea: Dimple around SiPM for uniform response
- ◆ Top mounted SiPM:
 - ◆ NIU: Surface mounted SiPMs
 - ◆ *Megatile* for assembly in larger units
- ◆ Side mounted SiPM:
 - ◆ MPI: first concepts, machined dimple
 - ◆ ITEP: injection moulded fiberless tiles
 - ◆ UHH: improved shape → easier machining



UHH Tiles

- ◆ Machined tiles, individually wrapped
 - ◆ Homogenous tile response across area
- ◆ New commercial SiPM (KETEK)
 - ◆ Lower device by device variation (gain, bias, etc.)
- ◆ First batch of >40 tiles characterised
 - ◆ Full bias/temperature scan w/ particles
- ◆ ~300 tiles assembled
 - ◆ Mass characterization at KIP Heidelberg
- ◆ Material for 1200 tiles available (8 HBUs)
- ◆ Process geared towards automation
 - ◆ Laser cut reflective foil
 - ◆ Tile wrapping



Testbeam plans

Short term:

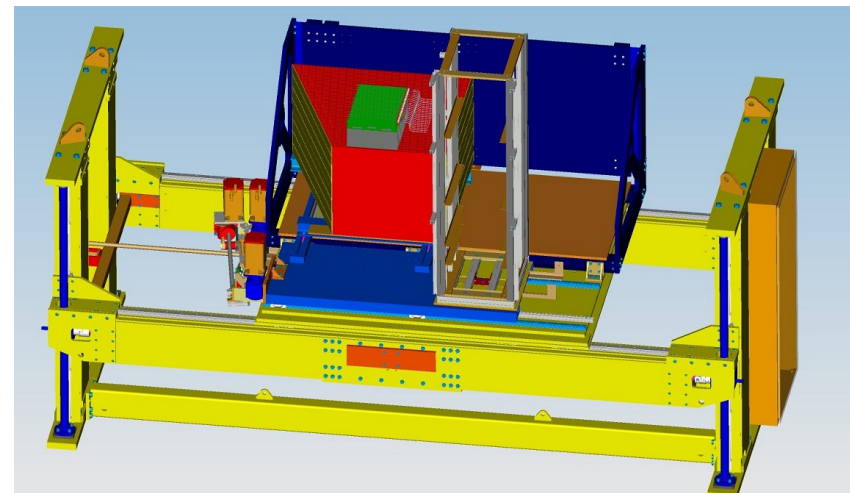
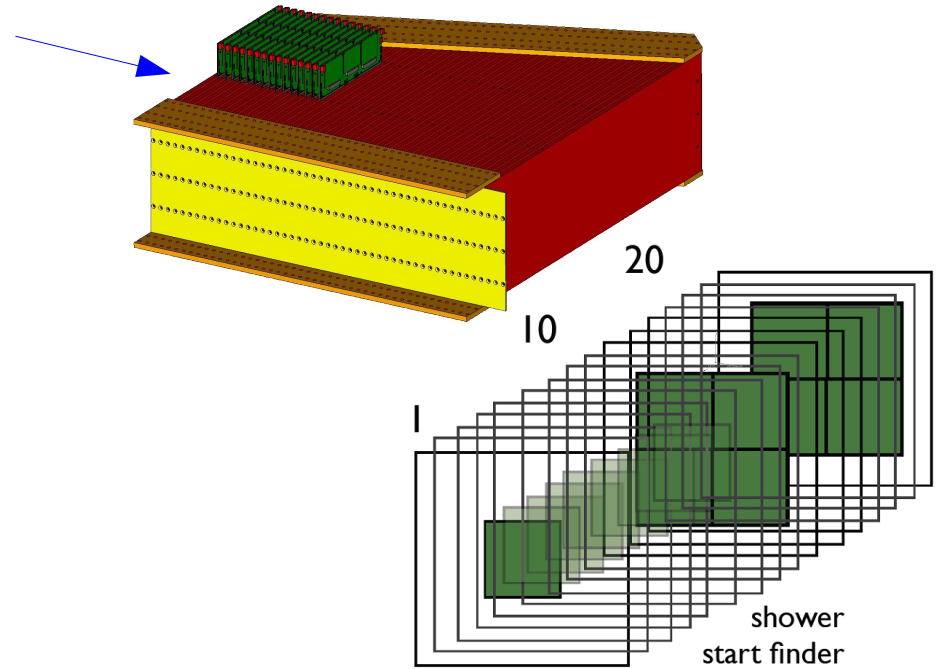
- ◆ 5 equipped boards available, 4+ to be equipped with UHH tiles
 - ◆ EM performance in DESY beam
 - ◆ 4 weeks beam time end of 2013

Medium term:

- ◆ Timed hadron shower imaging
 - ◆ ~10 single HBU layers (interaction finder)
 - ◆ ~2 full (2*2 HBUs) layers

Long term:

- ◆ Full 1m³ technical prototype
 - ◆ ~40 full layers
 - ◆ Demonstrate full integration, production automation



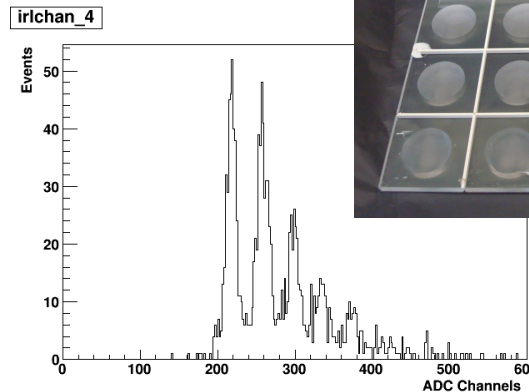
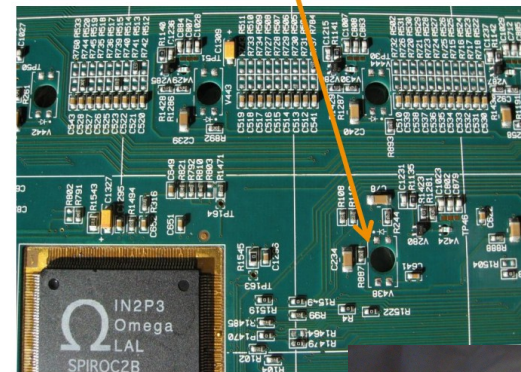
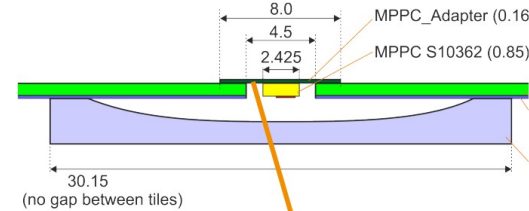
Summary

- ◆ The AHCAL is a scintillator-SiPM based concept for a hadronic calorimeter
 - ◆ Physics performance has been proven in various testbeam campaigns
- ◆ Now developing a prototype that is scalable to a full detector
 - ◆ Mechanical integration within ILD constraints is well advanced
 - ◆ The first multilayer setups have and will be tested in the DESY beams
- ◆ Various options for scintillator tiles under development
 - ◆ Focus on scalability of production and assembly
- ◆ Strong synergies with Scintillator ECAL effort

Backup

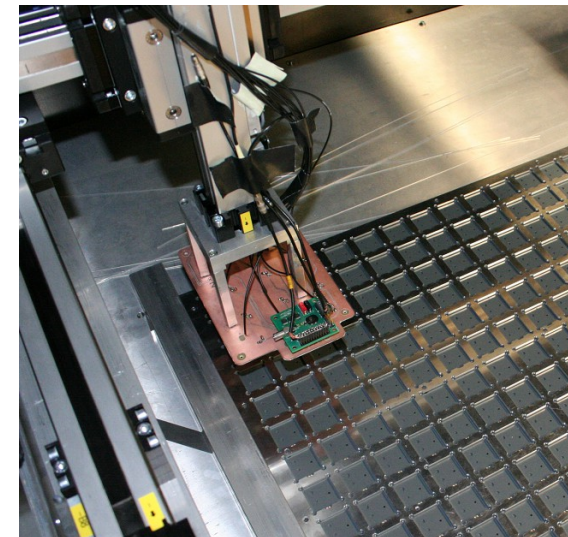
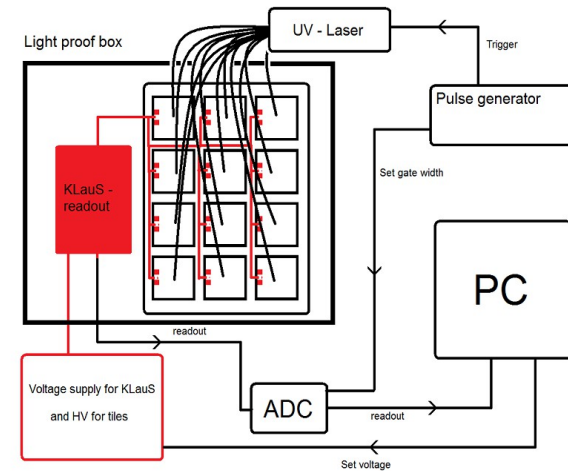
NIU Megatile

- ◆ NIU concept: Surface mounted SiPMs
 - ◆ SiPMs mounted on top of tile
 - ◆ Concave dimple in tile for uniformity
- ◆ *Megatile* scintillator
 - ◆ 18*18cm² divided into 3*3cm² cells
 - ◆ Optical isolation by white epoxy
- ◆ Easy assembly
 - ◆ SiPMs assembled like standard components
 - ◆ Scintillator is equipped in larger components
- ◆ Modified HBU designed and produced at DESY
 - ◆ First calibration spectra obtained by NIU



Mass Tile Characterisation

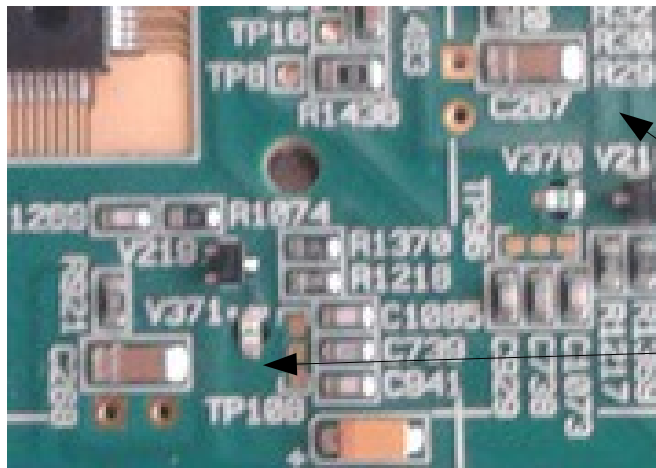
- ◆ Studies for automated mass tile characterisation by Uni Heidelberg
- ◆ Goal: Simultaneous full characterisation of 12 tiles at once, 216 tiles per run
- ◆ Readout by KlauS ASIC
- ◆ System commissioning and test runs with first 12 UHH tiles



Mass Tile Assembly

Studies by Uni Mainz:

- ❖ Mechanical connection tile ↔ HBU
 - ❖ Detailed study of glueing tiles to HBU as an alternative to alignment pins
- ❖ Electric connection tile ↔ HBU
 - ❖ Soldering SiPMs to the HBU is fastest with commercial wave soldering
 - ❖ Needs to be reflected in PCB design



good

bad

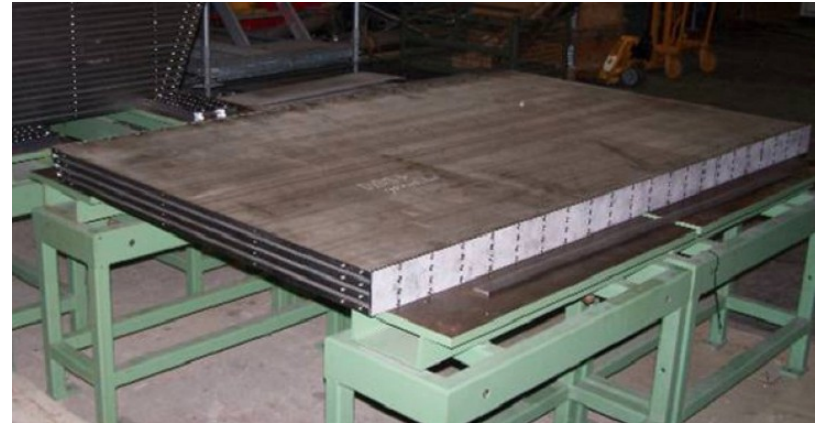


Mechanical Integration – Absorbers



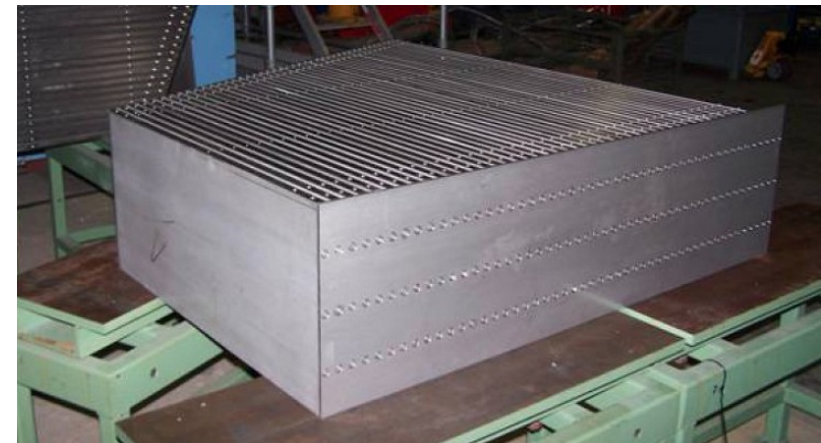
Full layer test stack

- ◆ 4 layers of ILD HCAL absorber
 - ◆ Largest plates in ILD stack
 - ◆ Full layer dimensions (6*3 HBUs)
- ◆ Heat dissipation and power pulsing



Half octant test stack

- ◆ 1/6 HCAL segment (1 HBU depth)
 - ◆ 2pcs available, stackable
- ◆ Current and future testbeam setups
- ◆ Integration of infrastructure
 - ◆ Power supplies
 - ◆ Cooling systems
- ◆ Stress tests (earthquake safety!)



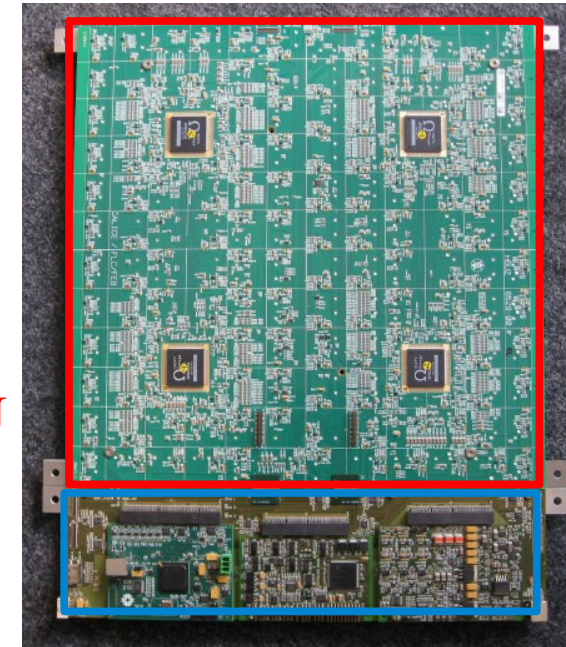
Electronic Integration - HBU

- ◆ 4 ASICs, 144 channels per PCB
 - ◆ SPIROC chip family by Omega, France
 - ◆ Full digitisation on chip
 - ◆ <1ns time stamping
 - ◆ Power pulsing
 - ◆ Separate developments for analog part by Uni Heidelberg: KlauS ASIC
- ◆ One Central Interface Board (CIB) per layer
 - ◆ Power board
 - ◆ Calibration and trigger controller
 - ◆ DAQ interface
- ◆ 5 HBUs equipped and calibrated in DESY electron beam
 - ◆ 8 fresh HBUs to be equipped with tiles



HBU

CIB



Multilayer Setup

- ◆ At the moment: no hadron beams available
- ◆ Start in DESY beam (EM showers)
 - ◆ Using available ILD prototype absorber
- ◆ Synchronous operation of multiple layers requires DAQ rework
 - ◆ Single layer operated via USB and Labview
 - ◆ Local clock generated on CIB
 - ◆ Multilayer needs central clock generation
 - ◆ Needs distribution of fast signals
 - ◆ Hardware from Uni Mainz
 - ◆ First step: data via USB, fast signals via HDMI
 - ◆ Next step: Data also via HDMI, dedicated data aggregation hardware
 - ◆ New DAQ software
 - ◆ Still Labview, but modular and faster

Beam

