Summary of Tracking, Vertex

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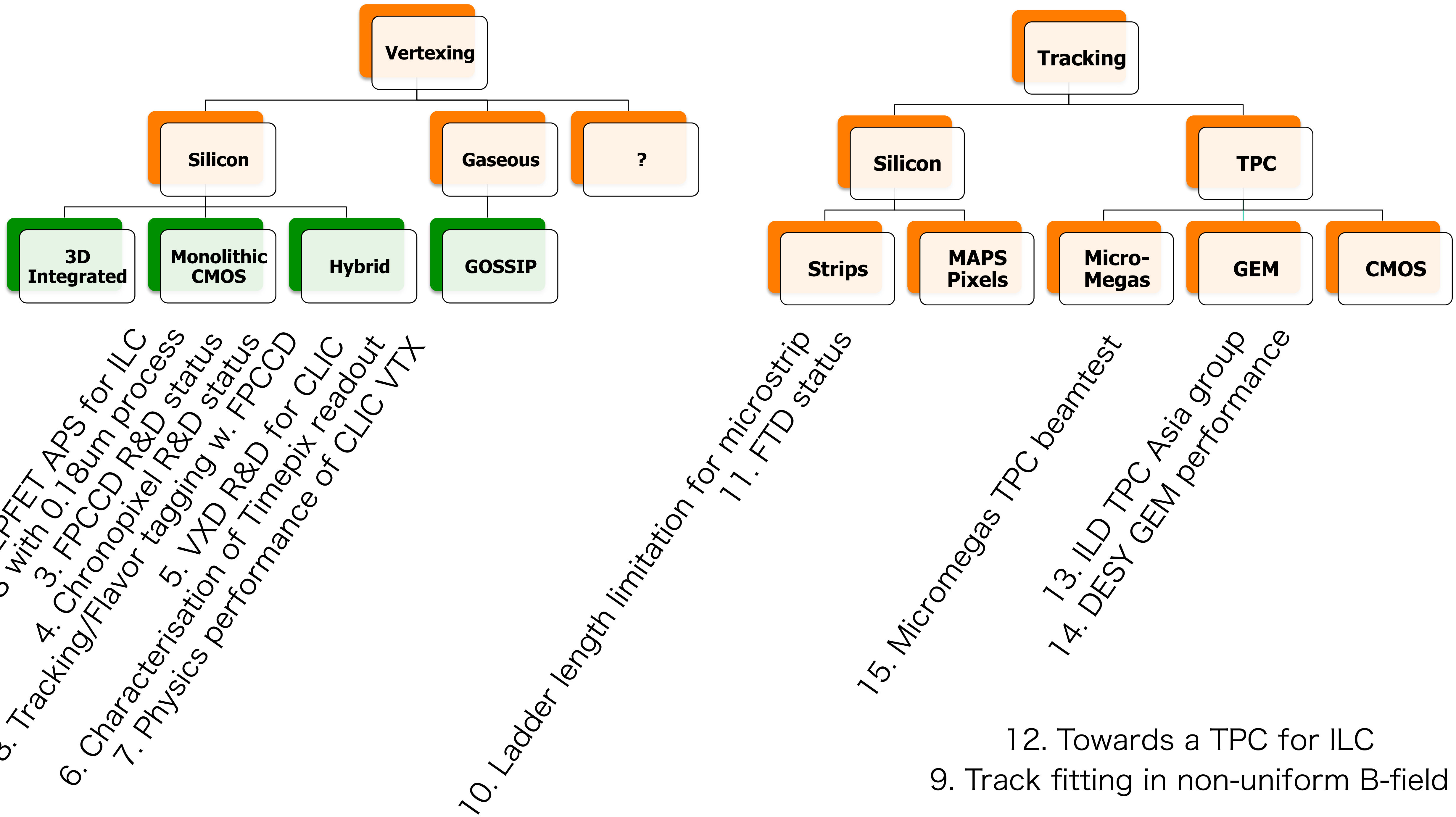
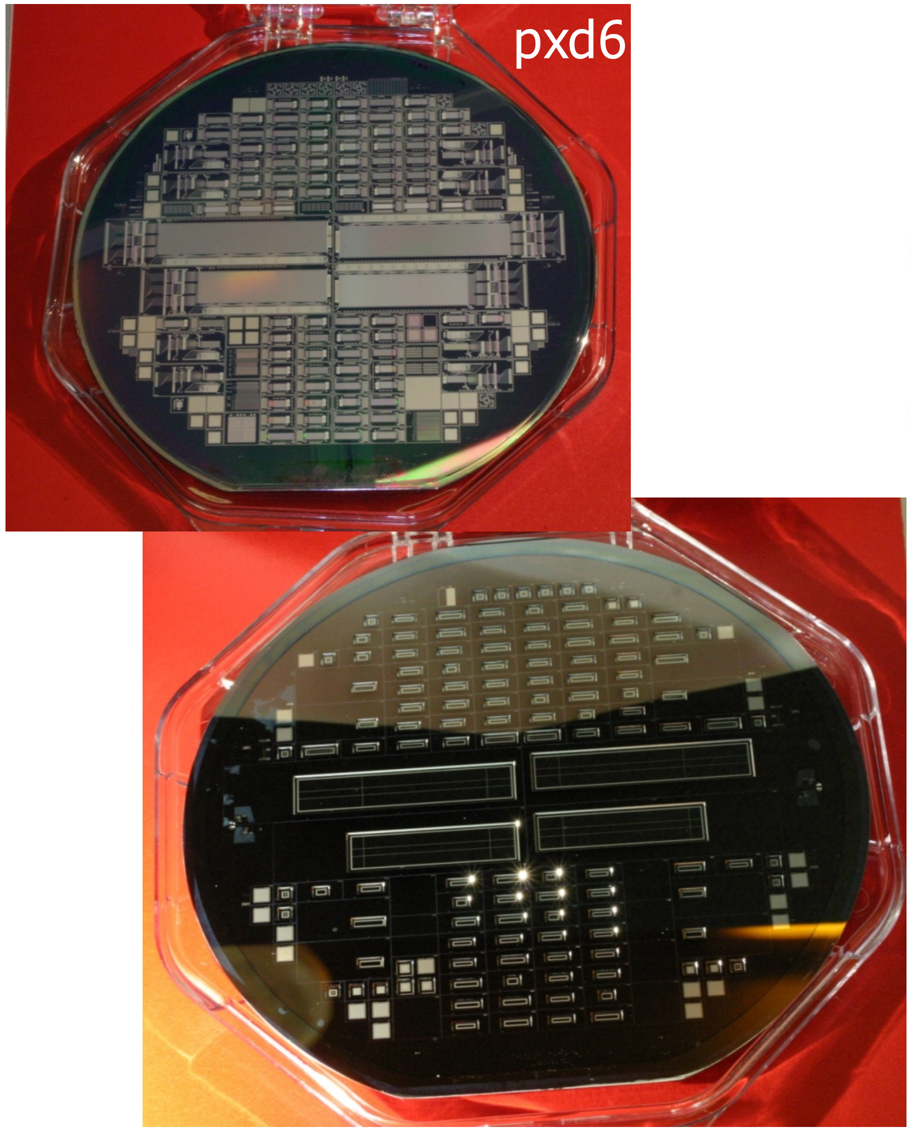
Contribution Map

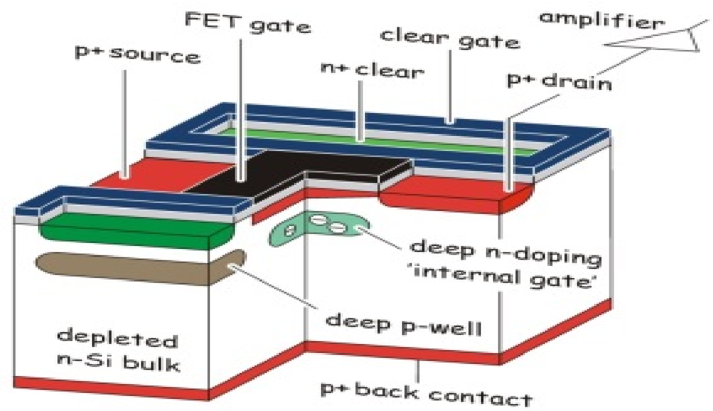


(Technology map from “LC Detector R&D Status and Overview” by Marcel Demarteau)

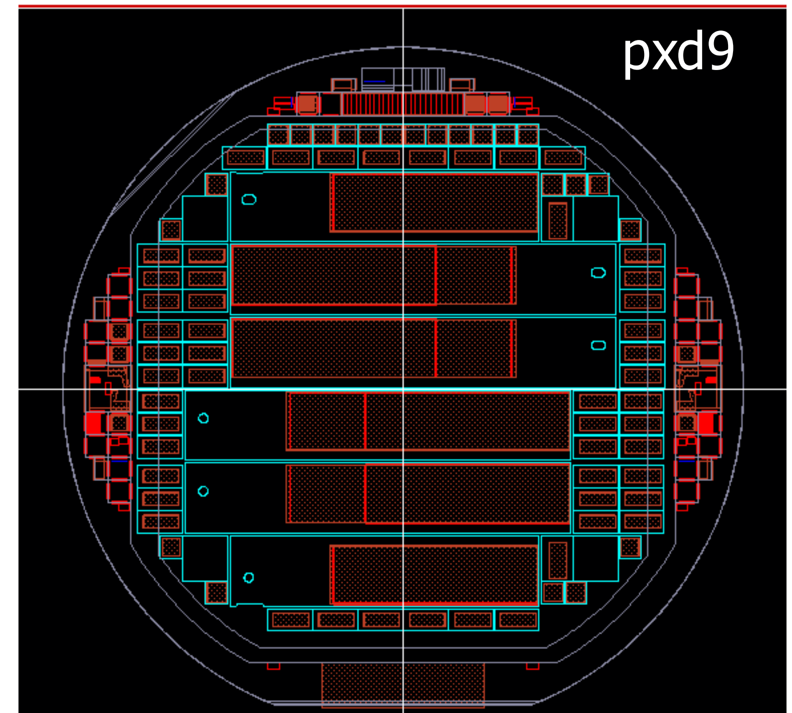
Vertex

Thin DEPFETs for vertexing – production status





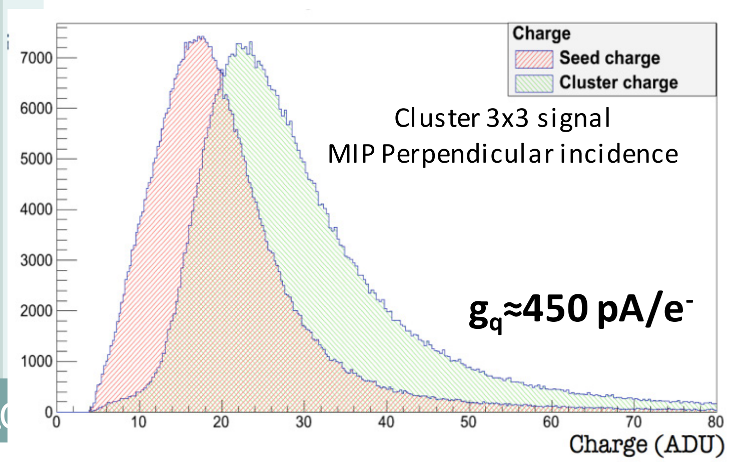
FET amplifiers are incorporated into a fully depleted sensor substrate

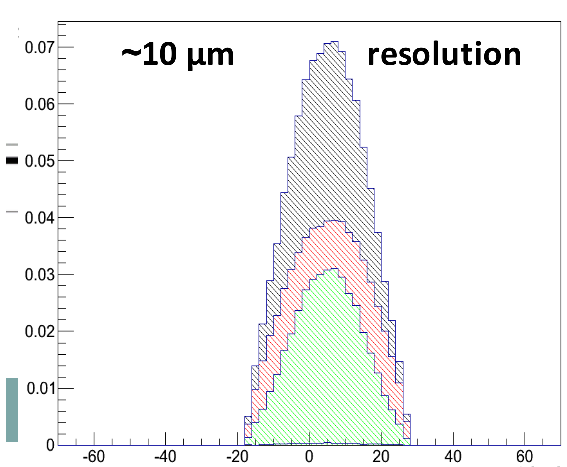


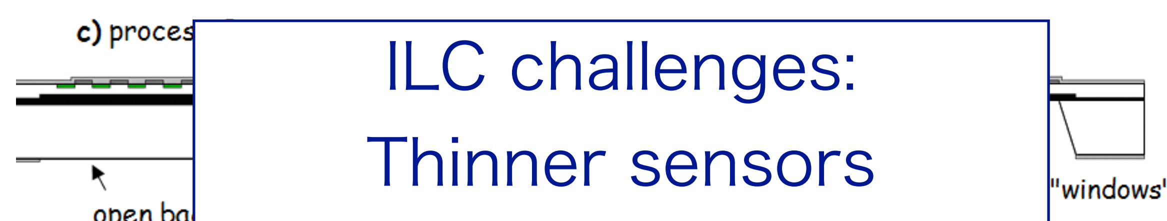
- **pxd6 finished and extensively tested : 50 µm DEPFETs**
- **pxd9 (75 µm DEPFETs) for Belle II**
  - **Three batches in production (10 wafers each)**
  - **FEOL of first batch done (next: metal system)**
  - **2nd and 3rd batch following**

Prototype for ILC!

PXD6 test results



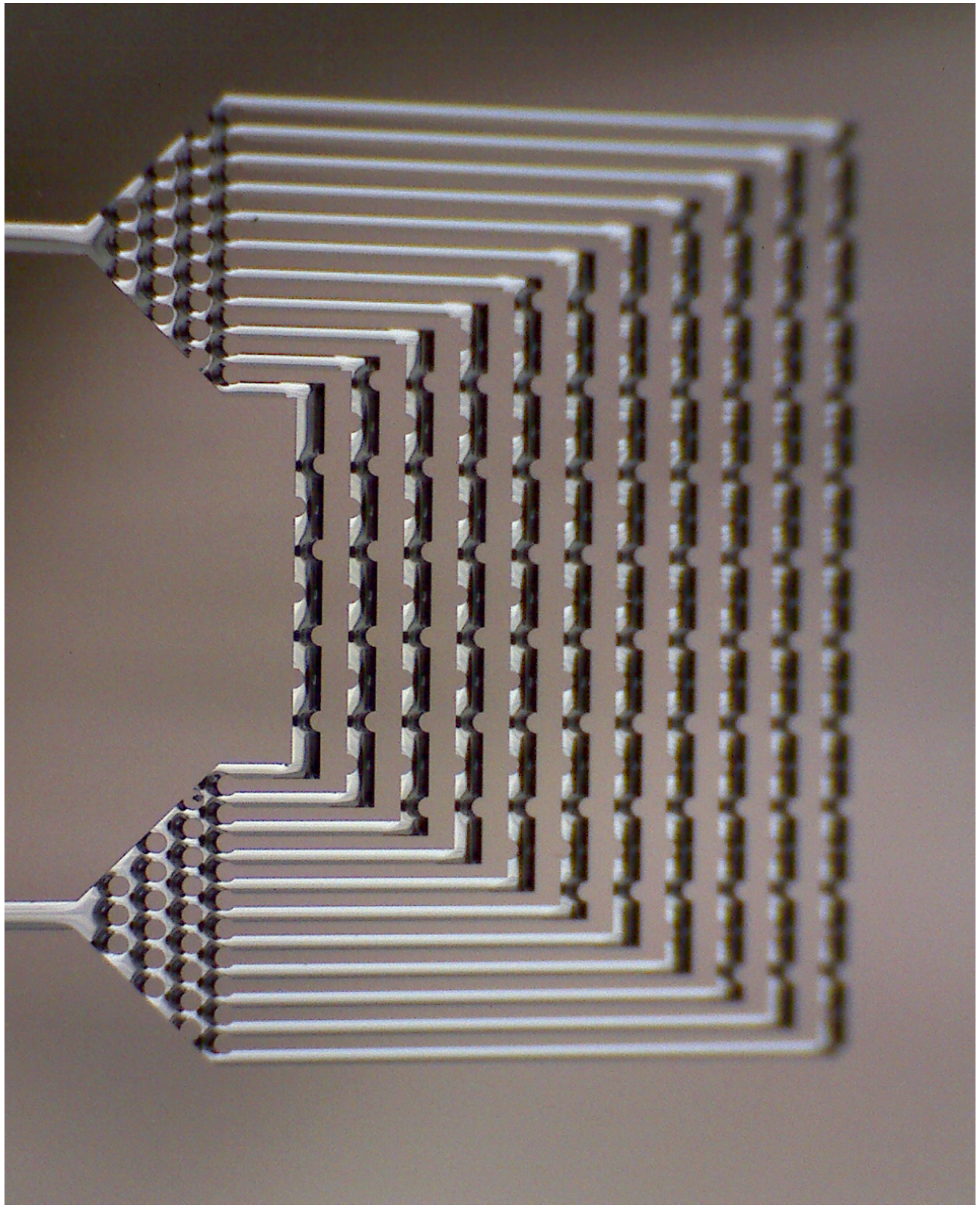


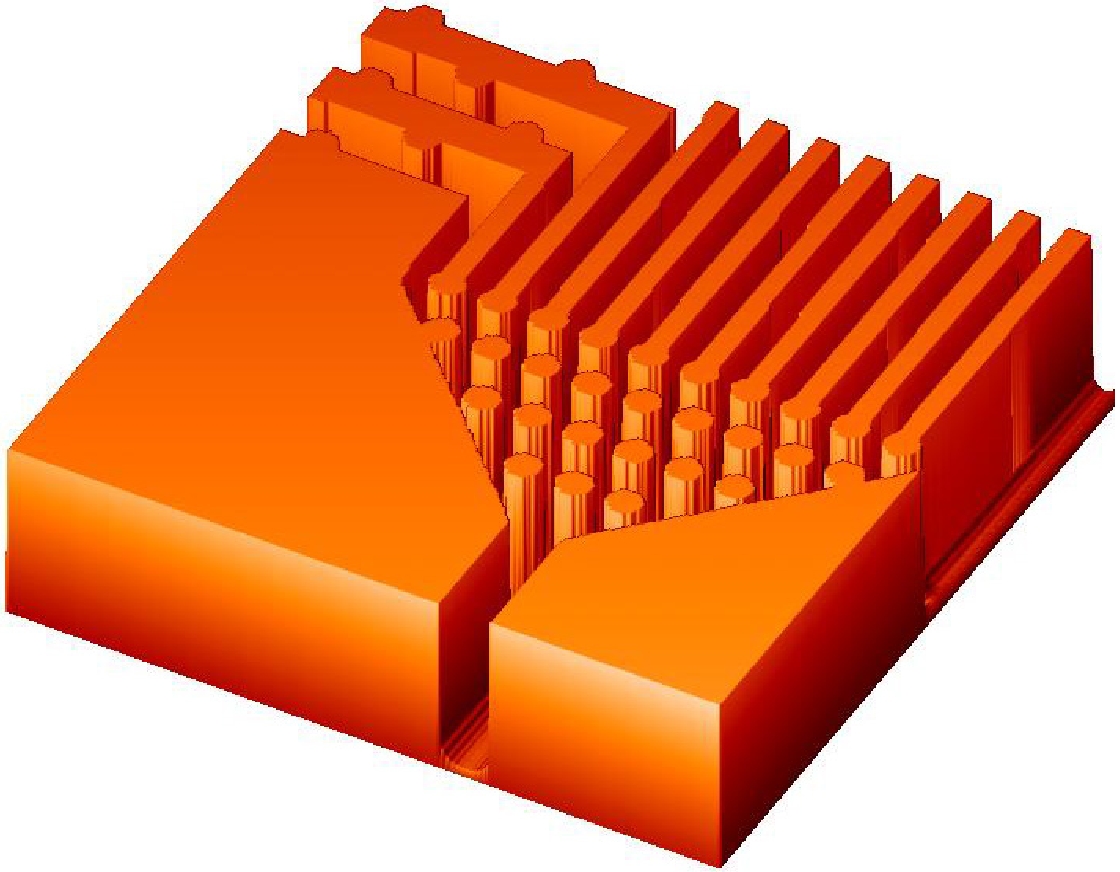


ILC challenges:
Thinner sensors
with smaller pixels (20um)

Micro-channel device for effective air cooling being developed (DEPFET)

Handle wafer before bonding





Inlet and outlet is ~350 µm deep, 400µm wide
Cavity etch and SOI done at Icemos, Belfast

Status:
- ✓ CSOI finished
- ✓ first oxidation done ….

CMOS pixel sensors

SUMMARY

- **CPS are getting validated in subatomic physics experiments**
  $\hookrightarrow$ *STAR-PXL: 400 sensors in 0.35 μm process, 350 Mpixels, 0.37 % X_0, 190 μs, 3.7 μm, 160 mW/cm^2*
- **Recently addressed 0.18 μm CMOS process offers perspective of faster read-out suited to :**
  - 1 TeV ILC running conditions
  - standalone Si tracking based on track seeds in VXD
  - Added value : substantial improvement of radiation tolerance
- **Preliminary test results of 0.18 μm CMOS technology indicate that it is the 1st CMOS process allowing to come close to the real CPS potential :**
  - innermost layer : $<$ 3 μm and $\lesssim$ 2 μs
  - outer layers : $<$ 4 μm and $\lesssim$ 10 μs
  - VXD power consumption : $<$ 600 W (inst.) / $<$ 12 W (average)
- **0.18 μm CPS development sustained by ALICE-ITS, CBM-MVD, AIDA-BT :**
  - 2012: validation of charge sensing properties ✓
    - 2013: validation of upstream and downstream sensor elements ✓
      - 2014/15: validation of complete sensor architecture with "1 cm^2" MISTRAL/ASTRAL prototype
        - 2015/16: pre-production of MISTRAL/ASTRAL sensor for ALICE and CBM

  $\hookrightarrow$ **2017-19: adapt MISTRAL/ASTRAL to ILC vertex detector** $\rightarrowtail$ BUNCH TAGGING ?
- **Experience getting accumulated on system integration aspects within STAR & ALICE environments**

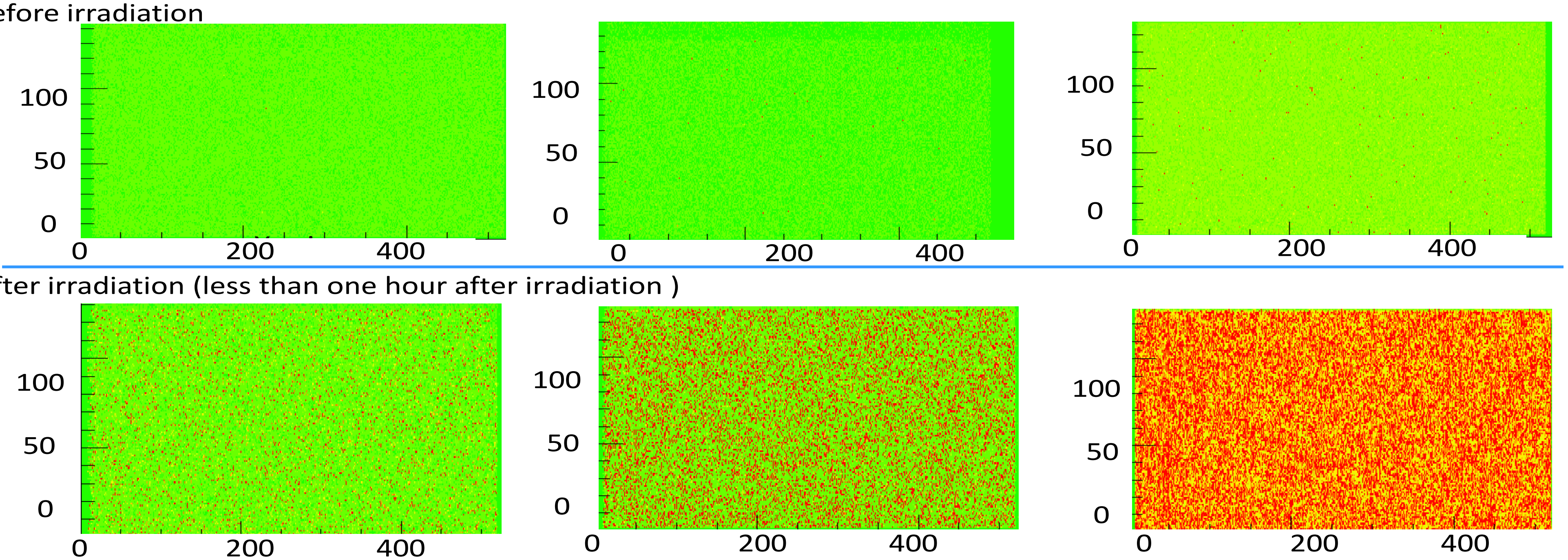
Neutron irradiation test of FPCCD

- Hot pixels

After irradiation, we saw many hot pixels.

Before irradiation

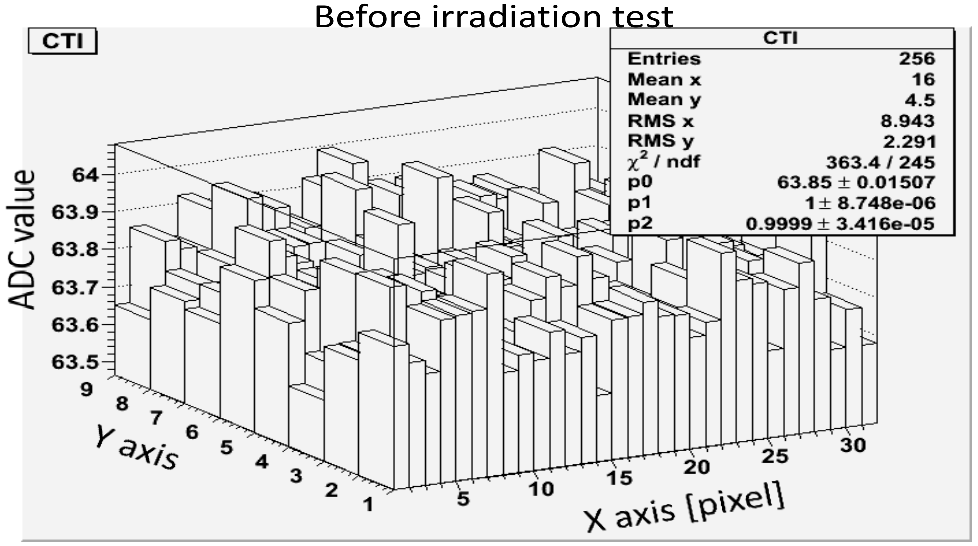
After irradiation (less than one hour after irradiation)



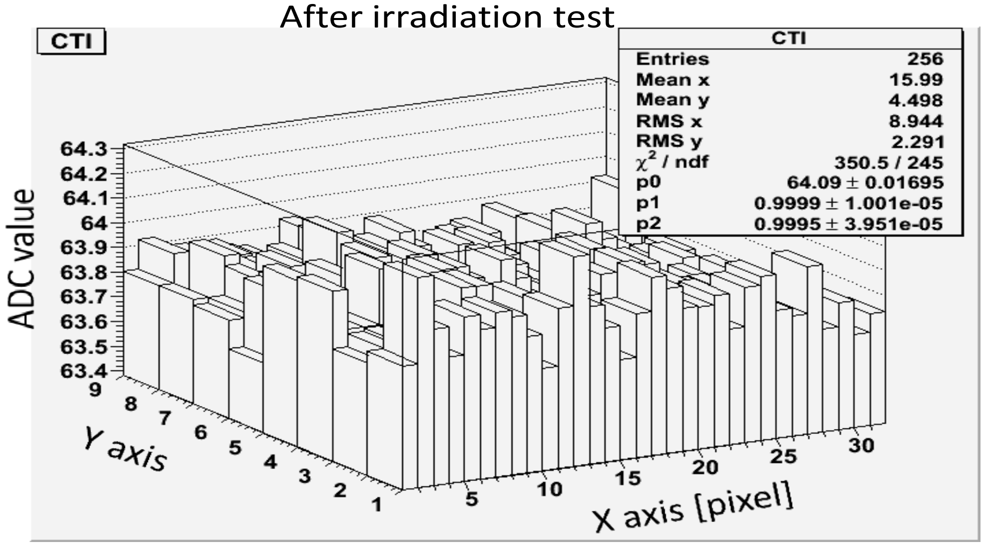
-20°C　　0°C　　+20°C

- CTI (charge transfer inefficiency)

Before irradiation test



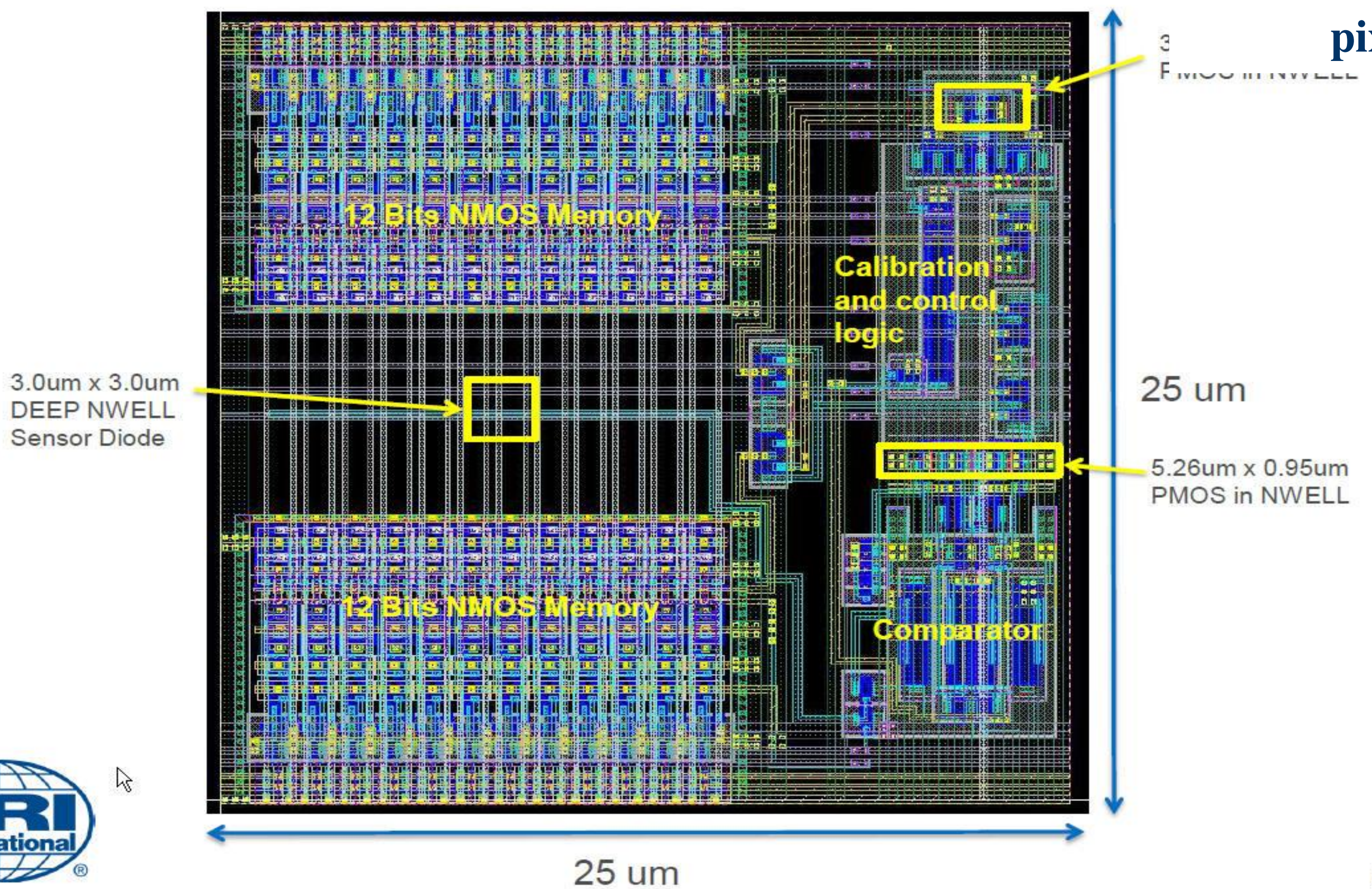
After irradiation test



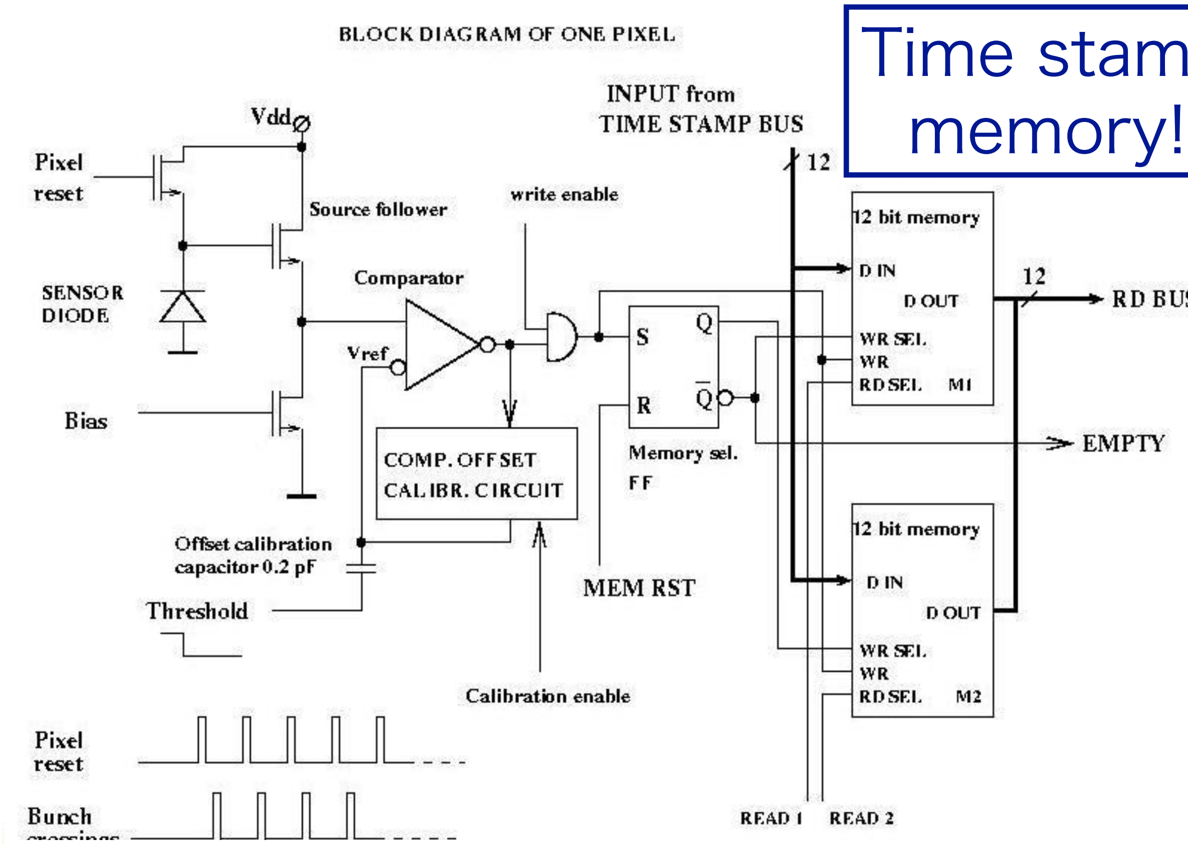
CTI / pixel was ...

Before irradiation	After irradiation
X direction : $(1.844 \pm 0.547) \times 10^{-6}$	X direction : $(6.392 \pm 0.626) \times 10^{-6}$
Y direction : $(4.660 \pm 2.135) \times 10^{-6}$	Y direction : $(2.834 \pm 0.247) \times 10^{-5}$

Chronopixel prototype 2



- **Very brief reminder of Chronopixel concept:**
  - **Chronopixel is a monolithic CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.**

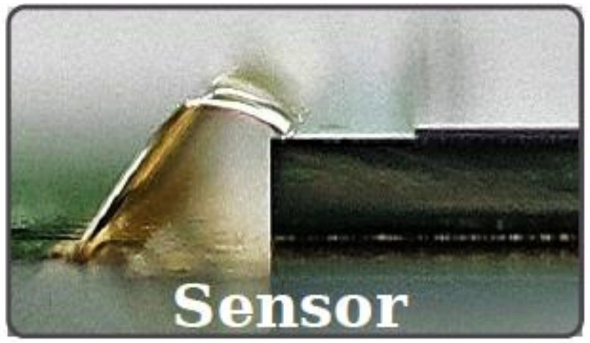


Time stamp memory!

- **From both, first and second prototype tests we have learned:**
  - **1. We can build pixels which can record time stamps with 300 ns period (1 BC interval) - prototype 1**
  - **2.We can build readout system, allowing to read all hit pixels during interval between bunch trains (by implementing sparse readout) - prototype 1**
  - **3.We can implement pulsed power with 2 ms ON and 200 ms OFF, and this will not ruin comparator performance - both prototype 1 and 2**
  - **4. We can implement all NMOS electronics without unacceptable power consumption - prototype 2. We don't know yet if all NMOS electronics is a good alternative solution to deep P-well option.**
  - **5. We can achieve comparators offset calibration with virtually any required precision using analog calibration circuit.**
  - **6. Going down to smaller feature size is not as strait forward process as we thought.**

CLIC Vertex

Hybrid Pixel Sensor R&D

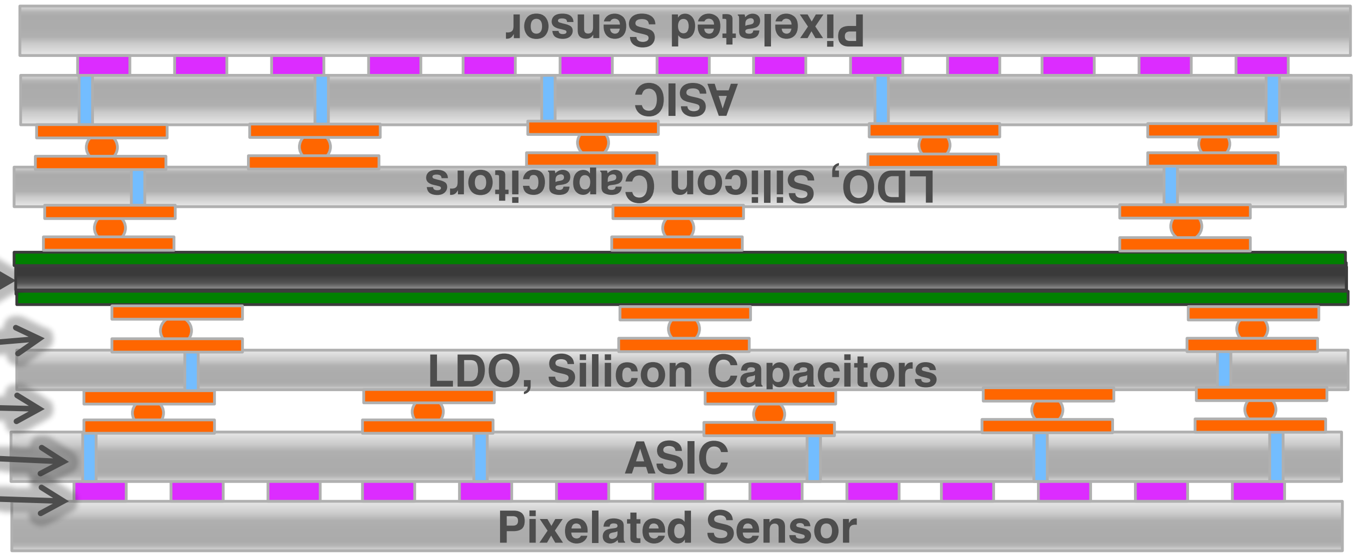


CLIC Vertex detector will take advantage of :

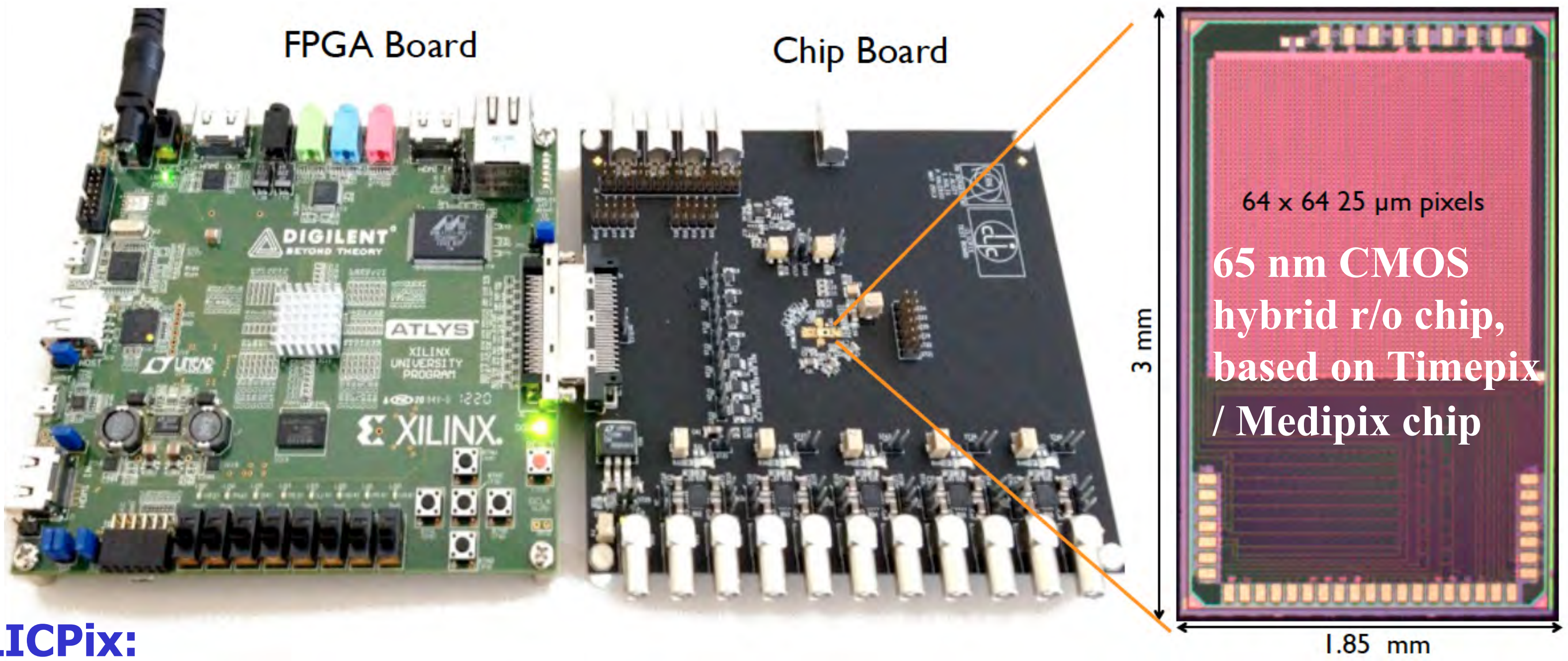
- **4-side buttable single chip assemblies**
  - **Through-Silicon Vias,**
  - **Active edge sensors**
- **Air cooling**
  - **High-Density (pF/µm^3) Silicon capacitors**
  - **Low mass LDO**

CLIC Hybrid Pixel Assembly

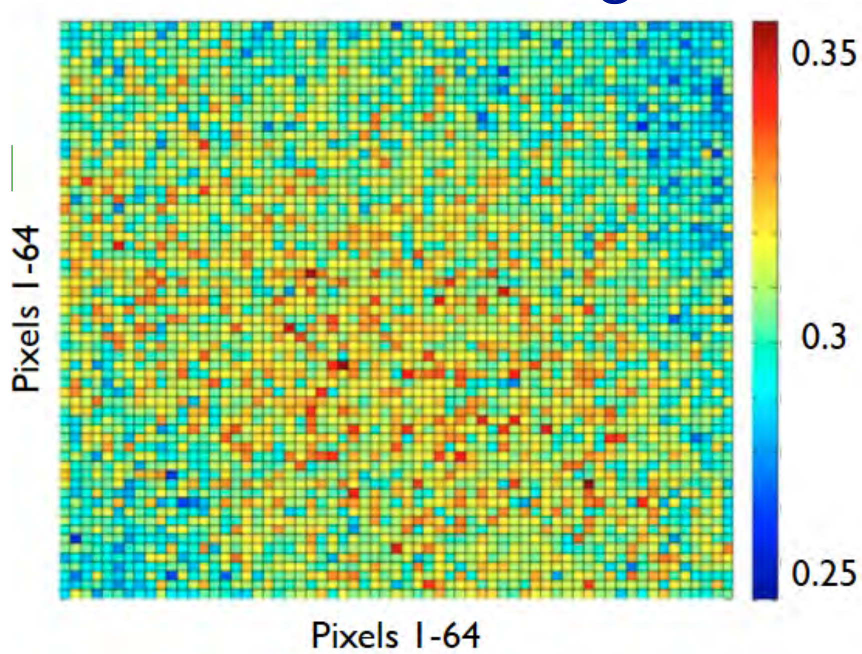
Carbon fiber Ladder
Flex (Power IN, Data)
BGA Interconnect
Through-Silicon Vias (TSV)
Pixel Interconnect
- **Bumps,**
- **Copper Pillar,**
- **Oxide-Oxide bonding**



- **CLICPix:**



Uniform TOT gain



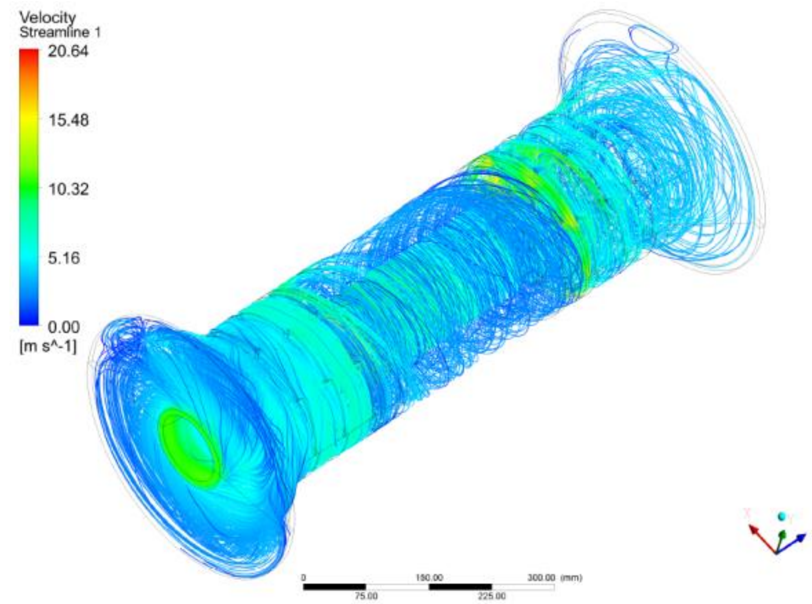
Air cooling studies

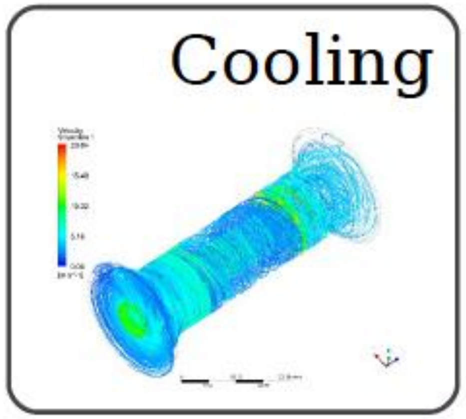
Challenges:

- Low material budget
- ~470 W heat load to extract (50mW/cm^2)
- High dimensional stability
- Assembly and cabling integration

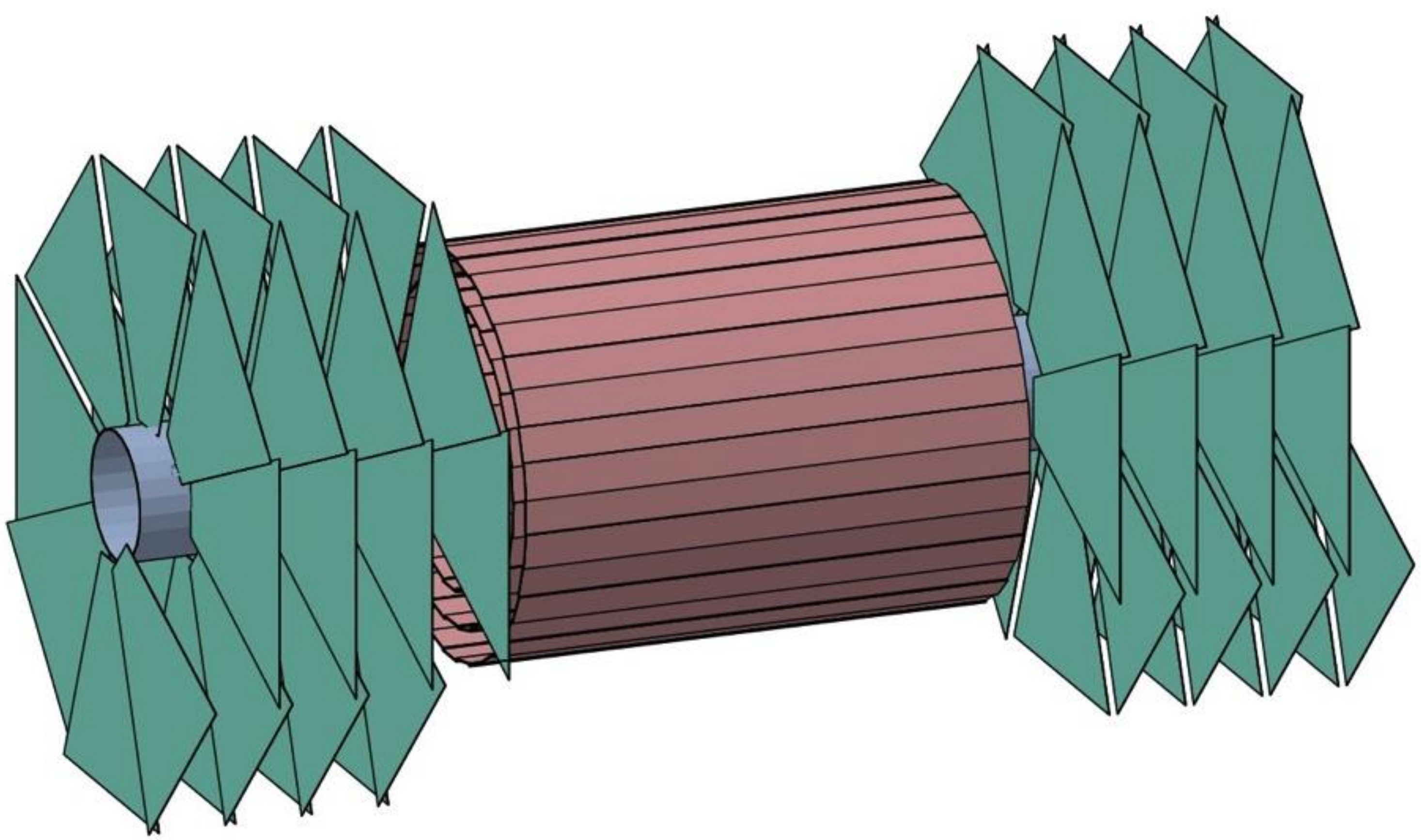
Solution:

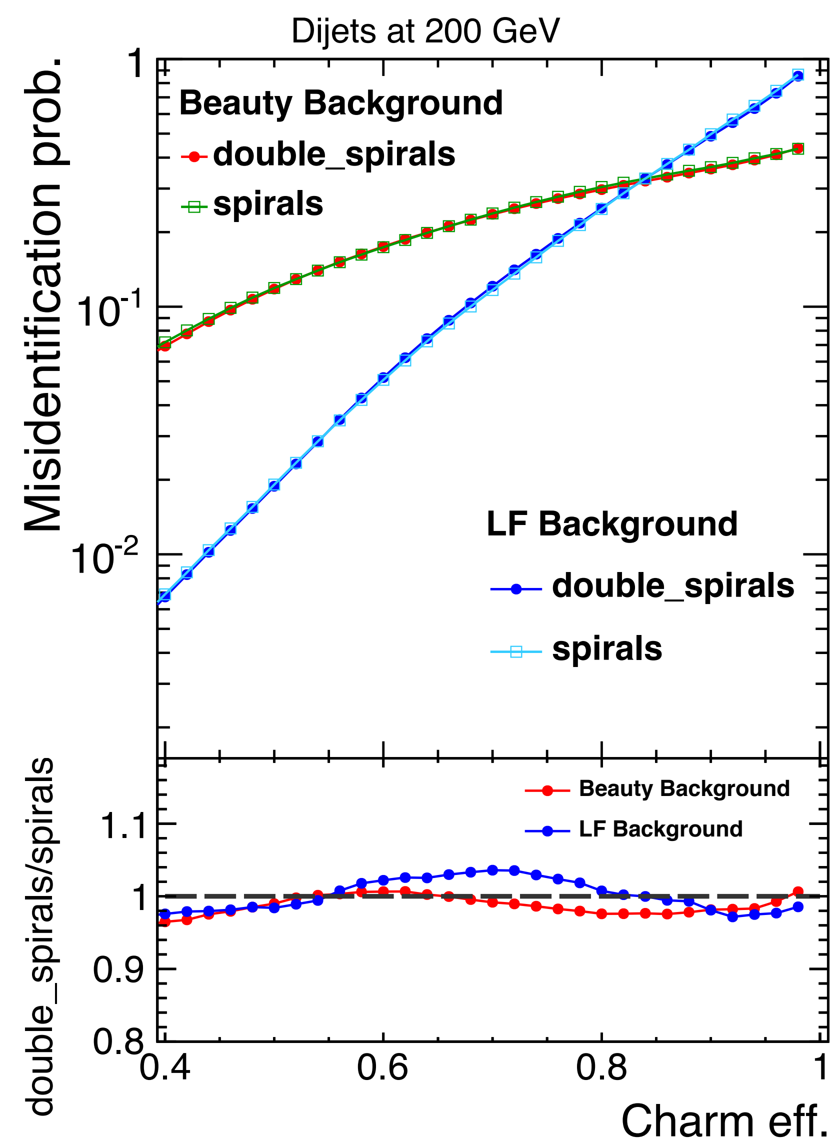
- Forced air-flow cooling, spiral endcap geometry





- Mass flow: **19.9 g/s**
- Avg. velocity in barrel: **6.3 m/s**





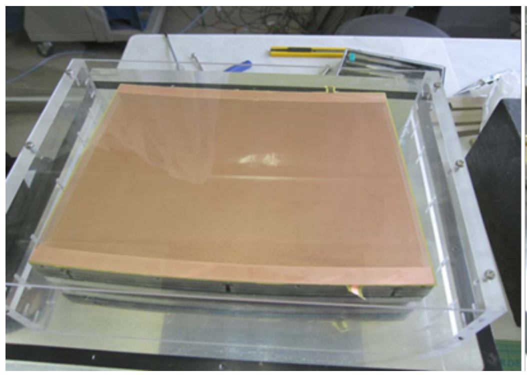
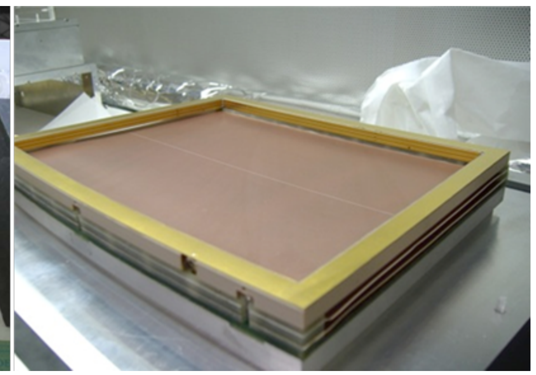
Physics performance studies for different CLIC vertex detector geometries, Niloufar Alipour Tehrani

Tracking
(from TPC studies)

GEMs with Pads

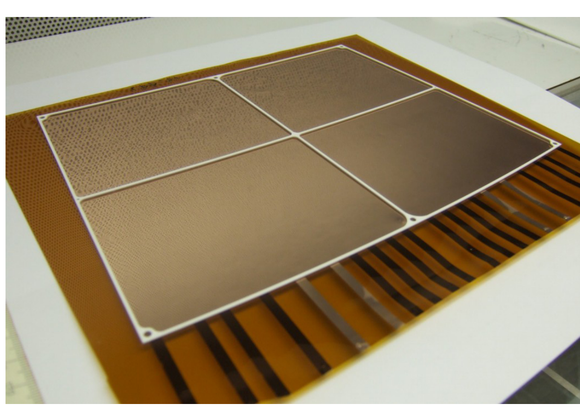
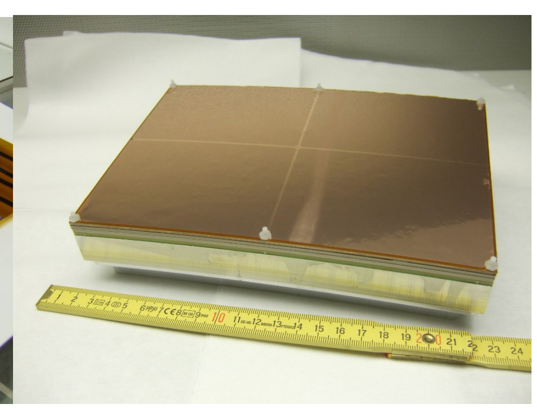
Asian GEM module:

- 2 GEMs, 100 µm thick, without side support
- 1.2×5.4 mm^2 pads, 28 pad rows

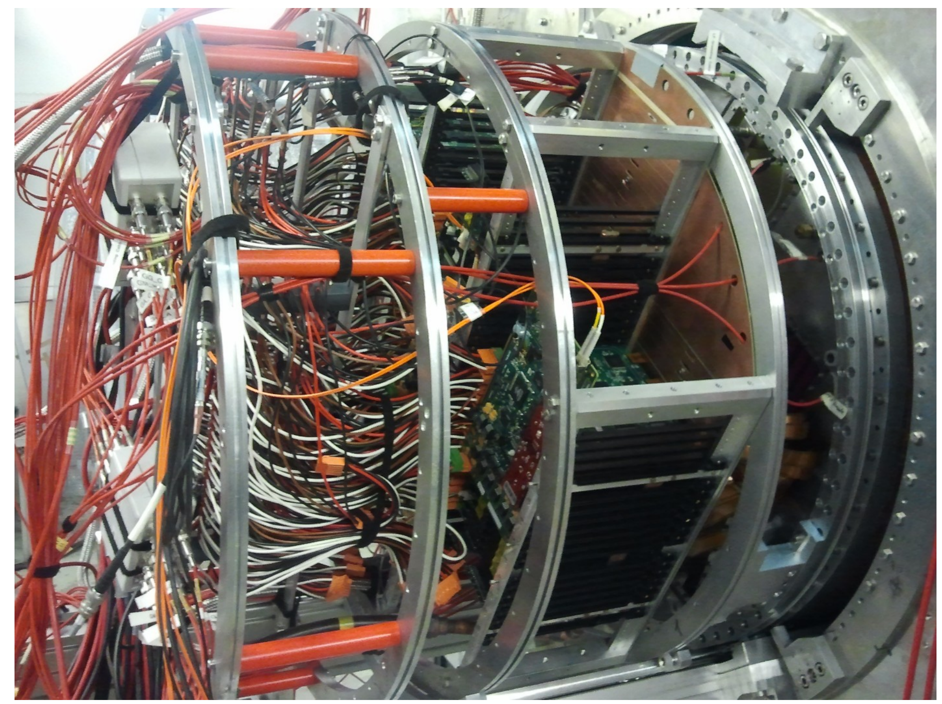
DESY GEM module:

- Triple CERN GEM with thin ceramic frame
- 1.26×5.85 mm^2 pads, 28 rows

About 5000 pads per module for both module types

ALTRO readout electronics
$\approx$ 10000 channels



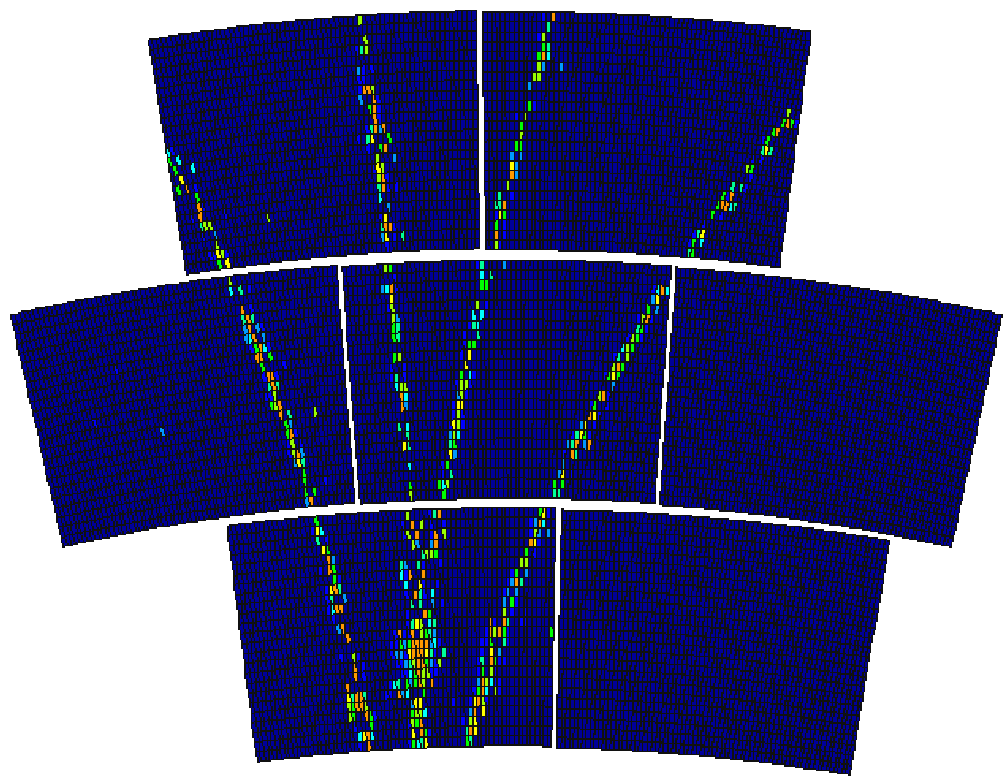
Next step: SALTRO (improved integration)

More details by Yukihiro Kato "Activity report of ILD-TPC Asia group"

and Astrid Münnich "Performance of DESY GEM Module in Testbeam Measurements"

MicroMegas with Pads

Compact T2K electronics mounted directly on the back side of each MicroMegas module



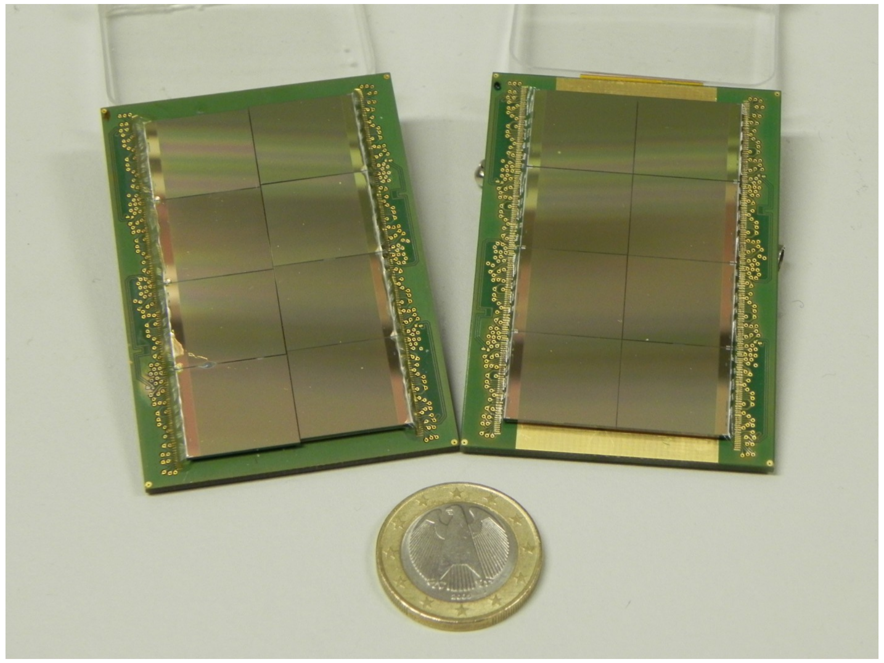
- 3×7 mm^2 large pads
- 24 rows with 72 pads
- 1728 pads per module
- Resistive foil to spread charge

Fully equipped endplate with 7 modules with 12k channels

Pixel Readout

Bump bond pads for Si-pixel detectors serve as charge collection pads

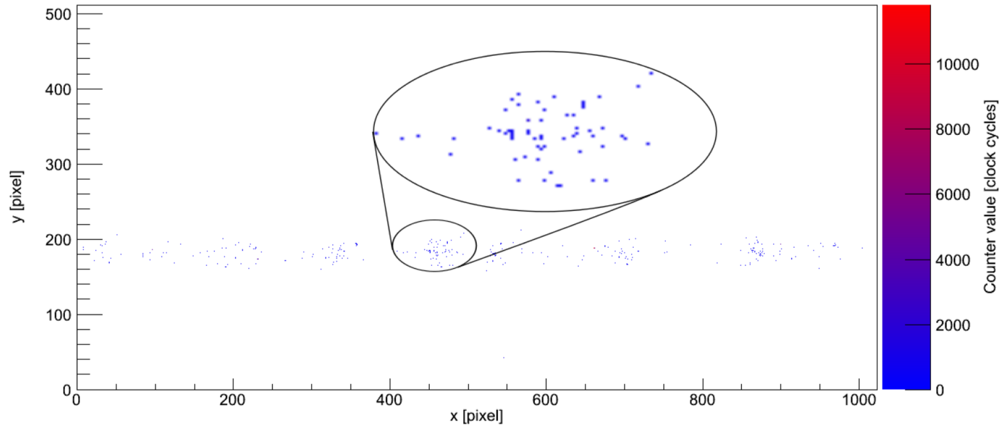
2 Octoboards with bare Timepix chips:



256×256 pixel of size 55×55 μm^2
Each pixel can be set to:

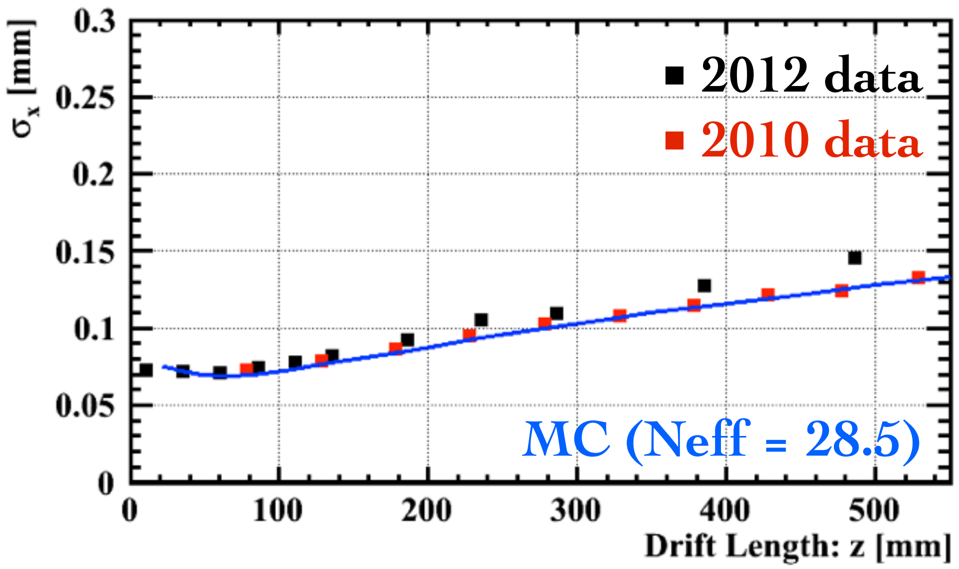
- Hit counting
- Charge measurement
- Time measurement

InGrid: Pixel + Micromega

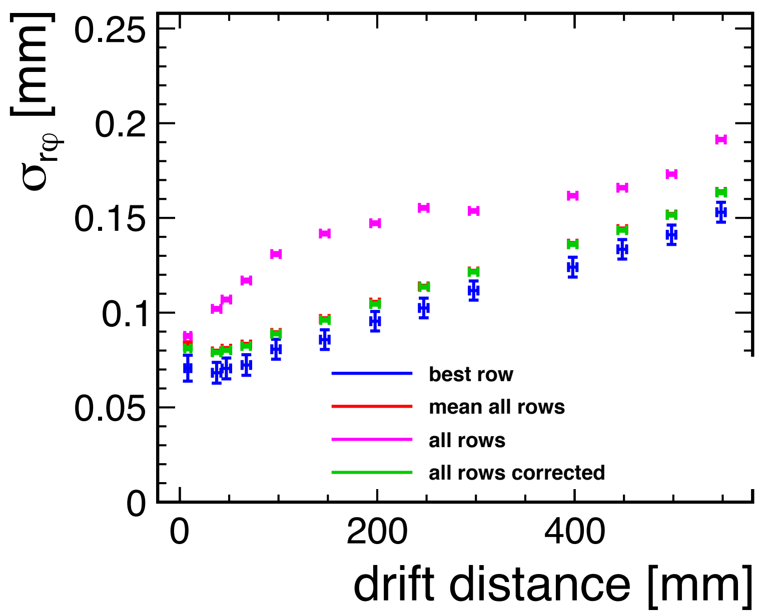


Spatial resolution vs. drift length

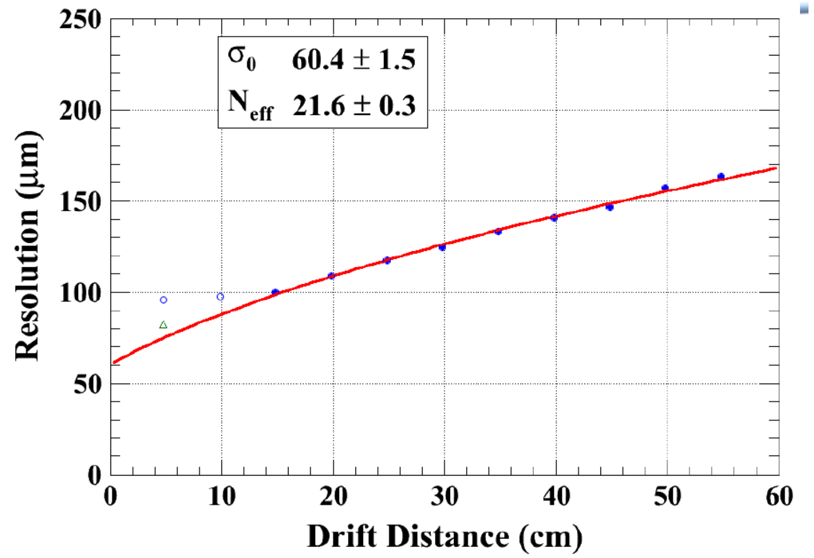
Asian GEM

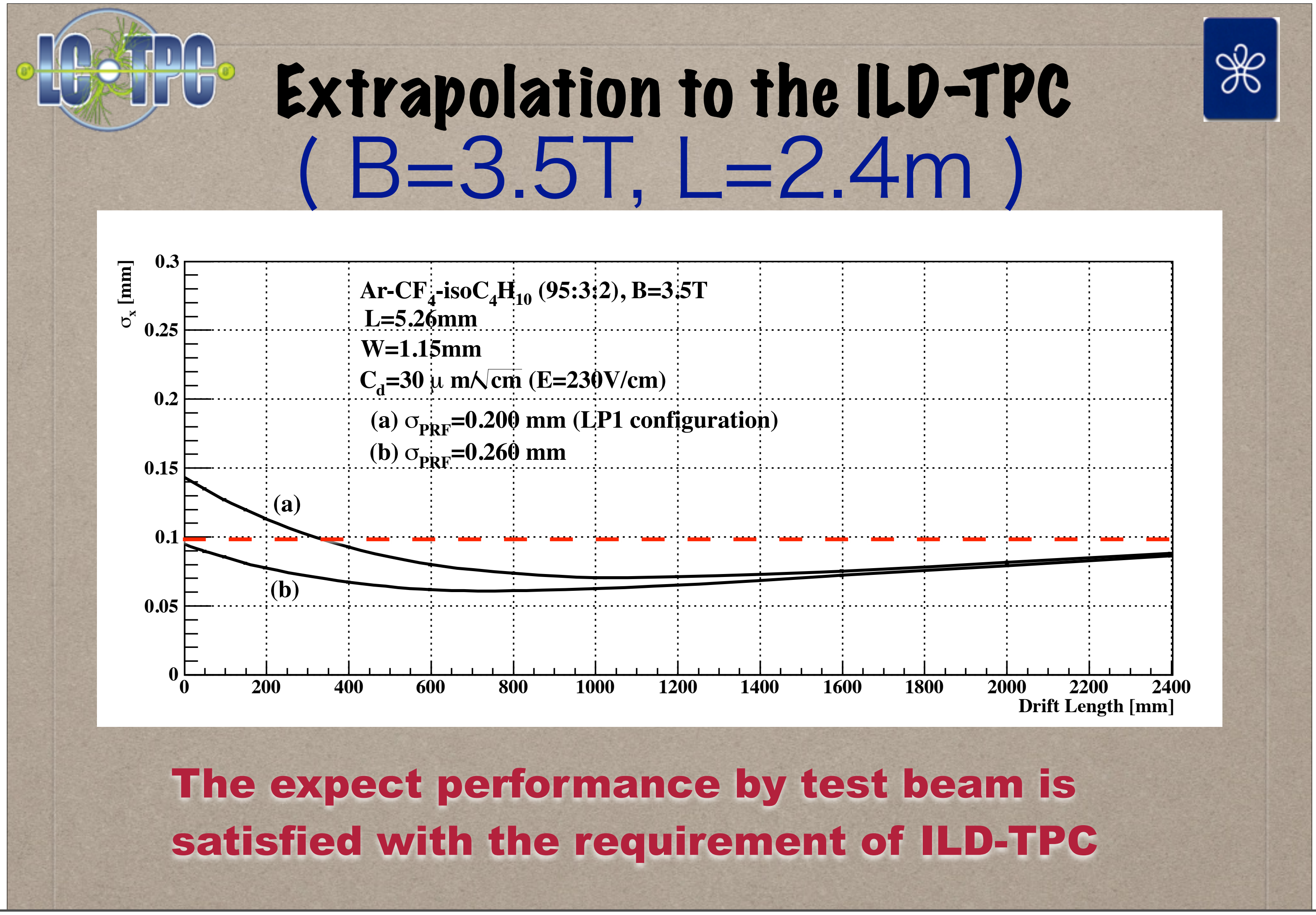


DESY GEM



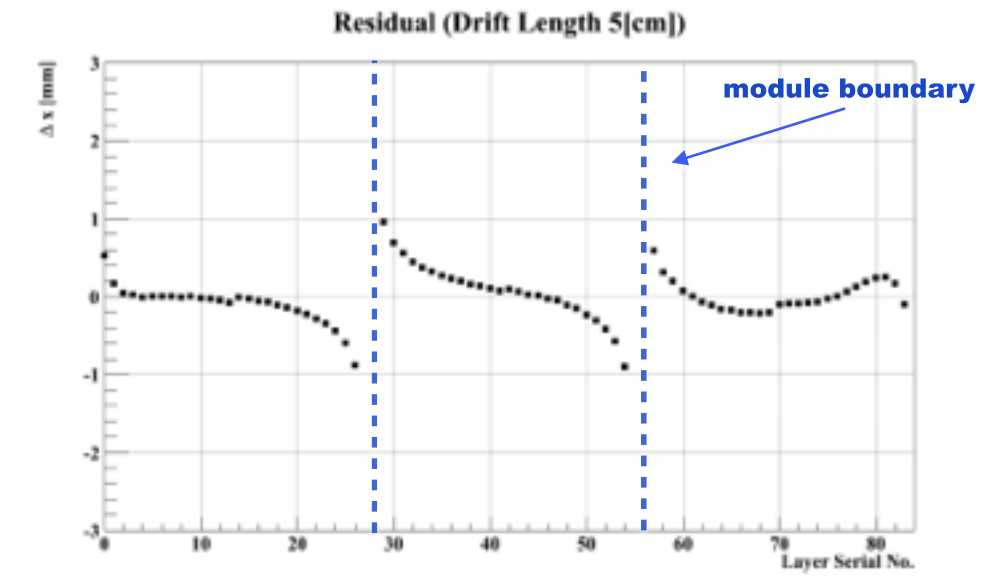
Micromegas





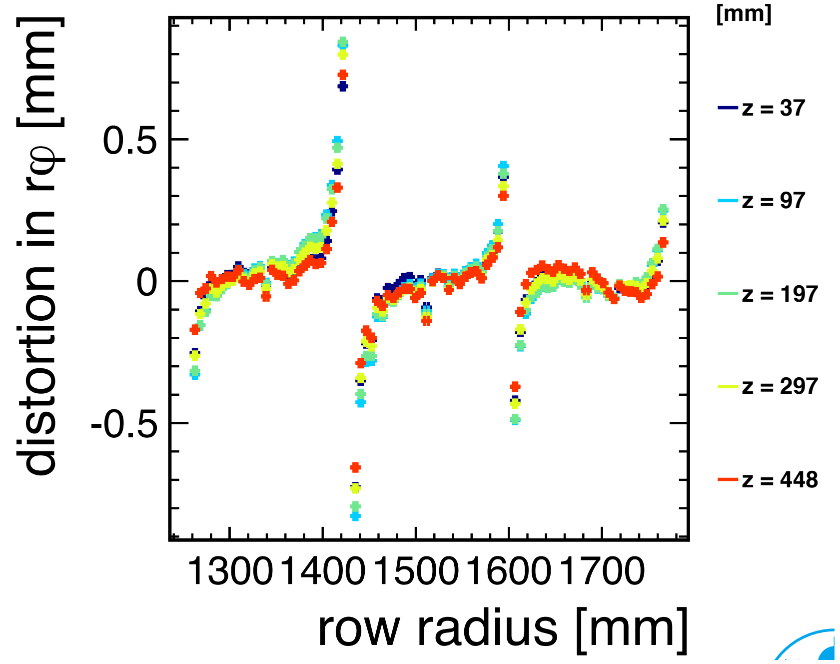
Field Distortion

Asian GEM

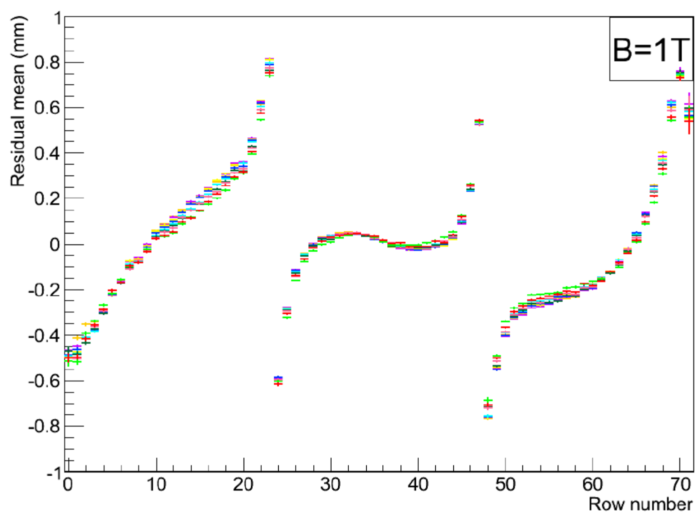


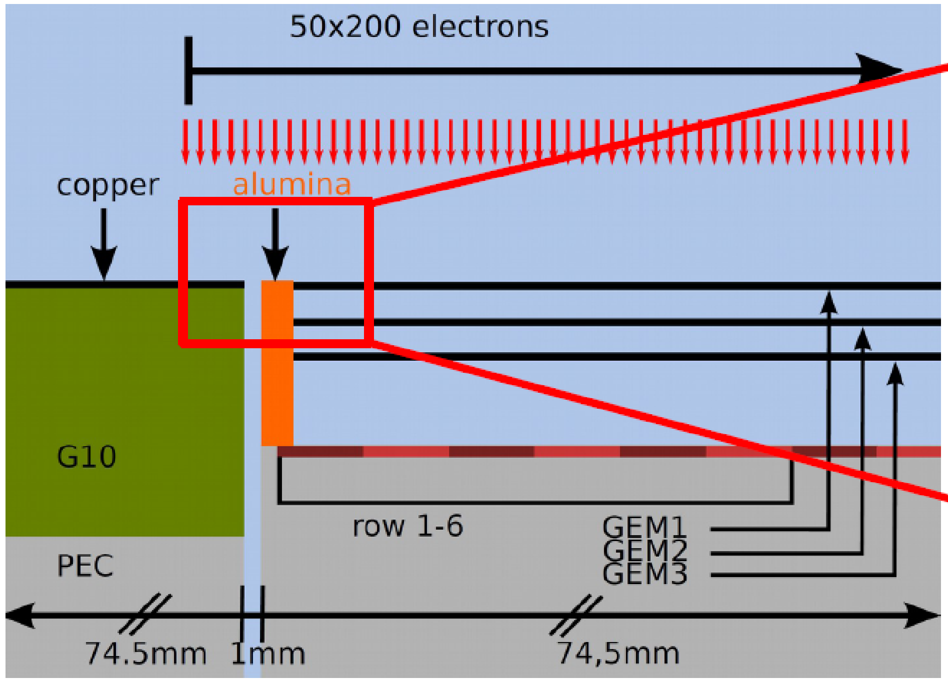
DESY GEM

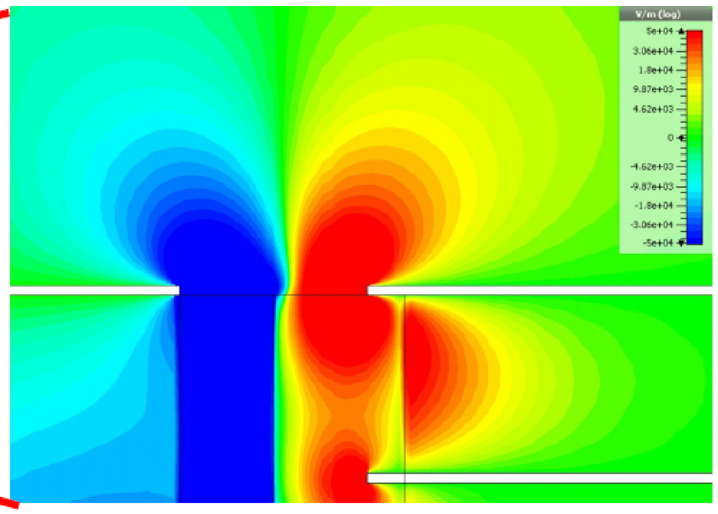
B = 1 T



Micromegas







Simulation (DESY module)

Current Topics

- Field distortions:
  - Improve module designs to limit distortion at the borders
  - Apply corrections for electric and magnetic field distortions
  - Needs field maps and dedicated software
- Ion back flow:
  - Study intrinsic suppression of ion back flow inside amplification structure
  - Design and test gating schemes
  - Evaluate effect of remaining ions on field homogeneity
- External reference for momentum resolution
  - Several layers of silicon detectors between the magnet and the TPC
  - Alignment of the two systems
- Electronics development
- Cooling system (CO_2 system close to being installed)
- Endplate integration
- Calibration: drift velocity, temperature, gain
- Software development

Summary (Vertex/Tracking)

- We have choices of advanced detector technologies.

- Should be ready to go into the system design phase in the near future.

Many thanks to all contributors

1. DEPFET APS for future collider applications - a status report, Ladislav ANDRICEK.
2. Detection Performances of CMOS Pixel Sensors Designed in a 0.18 micrometer Process for an ILC Vertex Detector, Marc WINTER.
3. R&D status of FPCCD vertex detector, Shuhei ITO.
4. Status of the Chronopixel project, Nick SINEV.
5. Vertex-detector R&D for CLIC, Mathieu BENOIT.
6. Calibration, Simulation and test-beam characterization for Timepix hybrid-pixel readout assemblies with ultra-thin sensors, Samir ARFAOUI.
7. Physics performance studies for different CLIC vertex detector geometries, Niloufar TEHRANI.
8. Study of tracking and flavor tagging with Fine Pixel CCD vertex, Tatsuya MORI
9. Track fitting in non-uniform magnetic field for ILC tracking detector, Bo LI.
10. Ladder Length Limitations for Microstrip Detectors, Bruce Andrew SCHUMM.
11. FTD status at ILD, Alberto RUIZ JIMENO.
12. Towards a TPC for ILC, Astrid MUENNICH.
13. Activity report of ILD-TPC Asia group, Yukihiro KATO.
14. Perfomance of DESY GEM Module in Testbeam Measurements, Astrid MUENNICH.
15. Recent results from test bench and beam tests of Micromegas TPC modules, Paul COLAS.