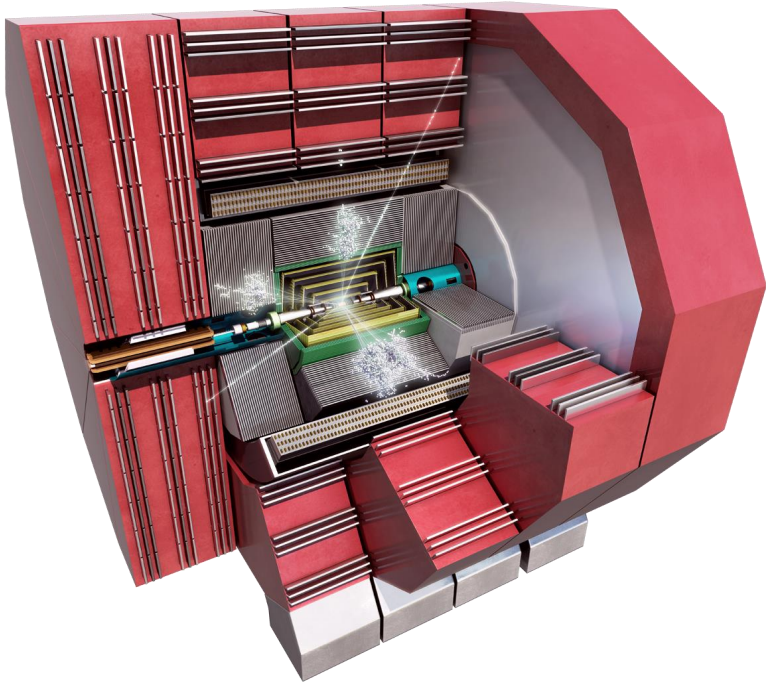
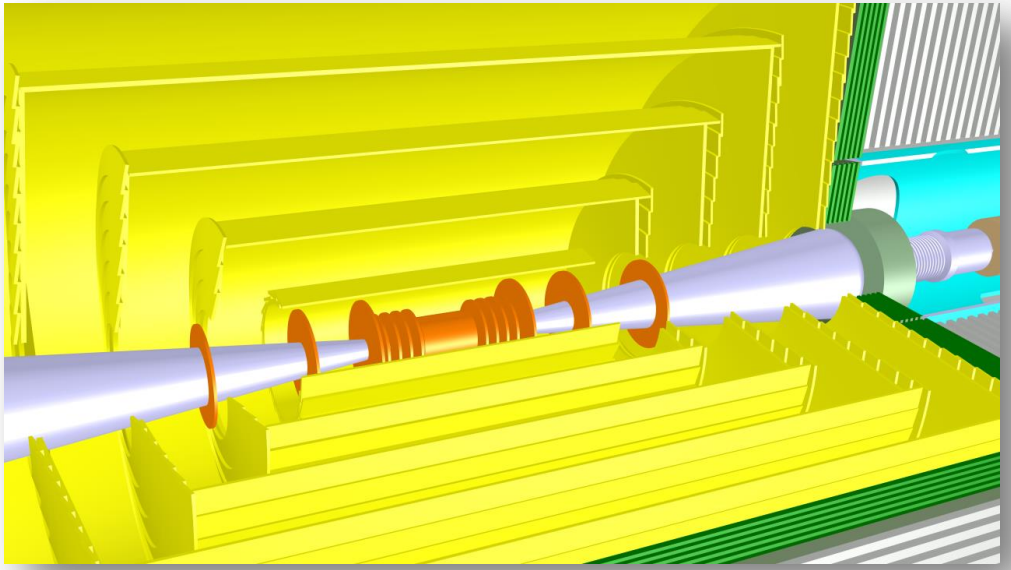


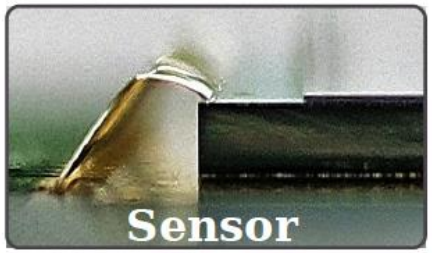


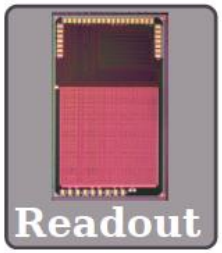
Vertex-detector R&D for CLIC

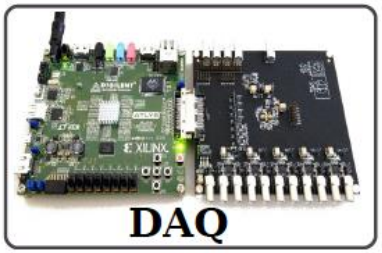
Mathieu Benoit, PH-LCD, CERN ,

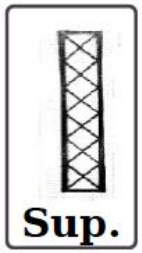
On behalf of the CLIC Detector and Physics Study

Outline

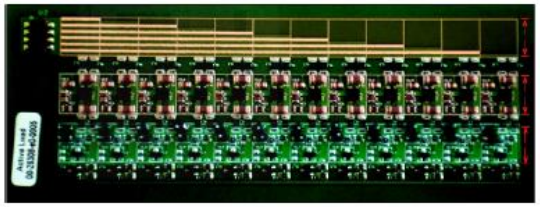




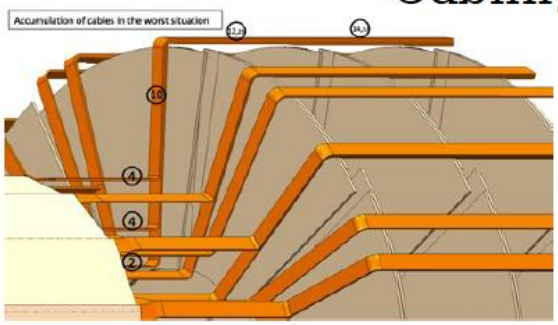




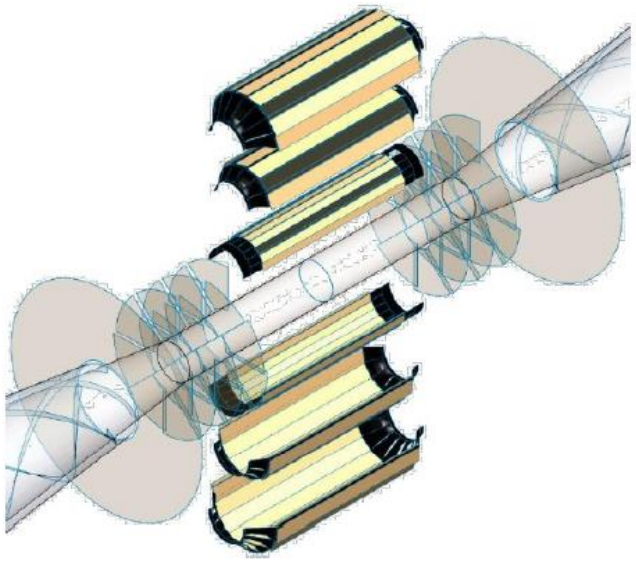
Powering



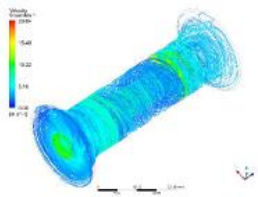
Cabling



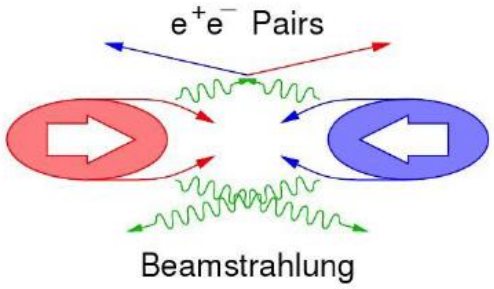
Assembly scenarios



Cooling

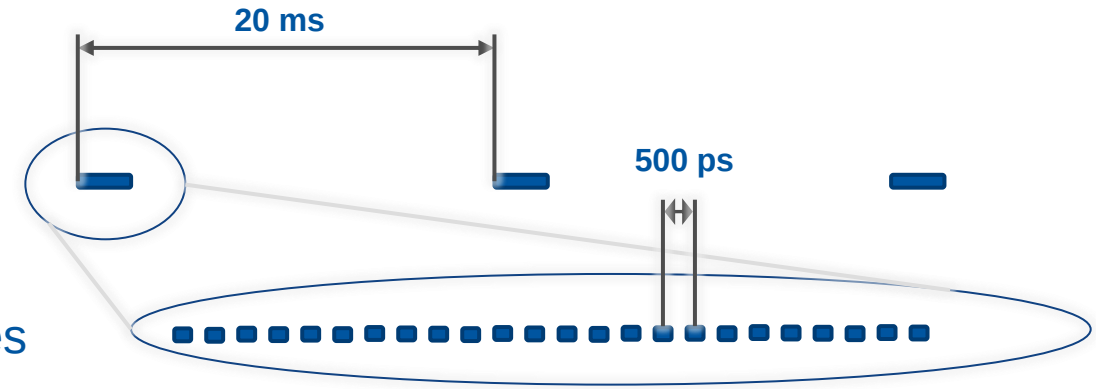


CLIC Machine environnent



	ILC at 500 GeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	$2x10^{34}$	$6x10^{34}$
BX separation	554 ns	0.5 ns
#BX / train	1312	312
Train duration	727 µs	156 ns
Train repetition rate	5 Hz	50 Hz
Duty cycle	0.36%	0.00078%
σ_x / σ_y (nm)	474 / 6	≈ 45 / 1
σ_z (µm)	300	44

Small bunch size will generate a high e+ e- and hadronic background. The small time separation between bunches put a stringent requirement on timing resolution for the vertex detector, (10 ns slicing required)



CLIC Vertex detector requirements

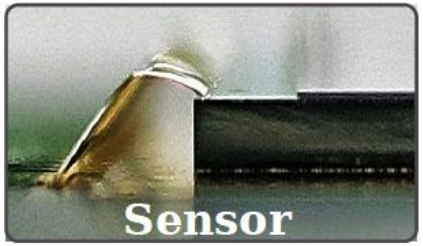
- For the physics measurements foreseen at CLIC we require an efficient tagging of heavy quarks through precise determination of displaced vertices :

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

a~5 μm, b~10-15 μm

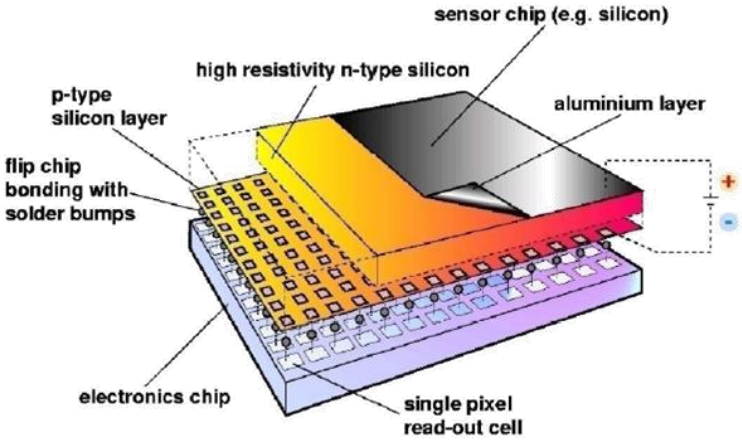
- To meet these requirements, we need :
  - **Good single point resolution**: σ_{sp} ~ 3 μm
    - Small pixels < 25x25 μm^2 , analog readout
  - **Low material budget**: X_0 < 0.2% per single layer
    - Equivalent to 200 μm in Silicon, including support, cabling and cooling
    - Low power ASICs (~50mW/cm^2) -> Power Pulsing
    - Air Flow Cooling

Hybrid Pixel Sensor R&D



Hybrid Silicon Pixel sensors area good candidate to meet CLIC requirements :

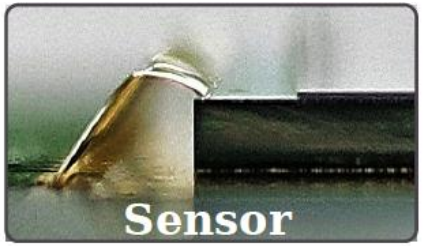
- **Mature Technology,** widely used in LHC experiments
- **Fast and strong signal** due to high resistivity substrate and full depletion (Timing, Single Point Resolution)
- **Commercial CMOS Process** allow for complex electronics, fast clock , large throughput , clock-gating and power pulsing
- **Interconnect technology** (Bump-Bonding, Wire-Bonding) costly, bonding method for pitch < 50 µm needs R&D
- **Material budget** for State-of-the-art Hybrid Pixel sensor is on the way to reach CLIC requirements (~100um equivalent Silicon for Sensor + ASIC)



CLIC Vertex Detector R&D Focus on demonstrating the feasibility of using Hybrid Pixel detector :

- Demonstrate production capabilities of Ultra-Thin Sensor and ASIC
- Evaluate tracking performance of Ultra-Thin Hybrid pixel assemblies
- Develop a readout electronic meeting CLIC requirement and demonstrate the possibility to produce modules on large scale

Hybrid Pixel Sensor R&D

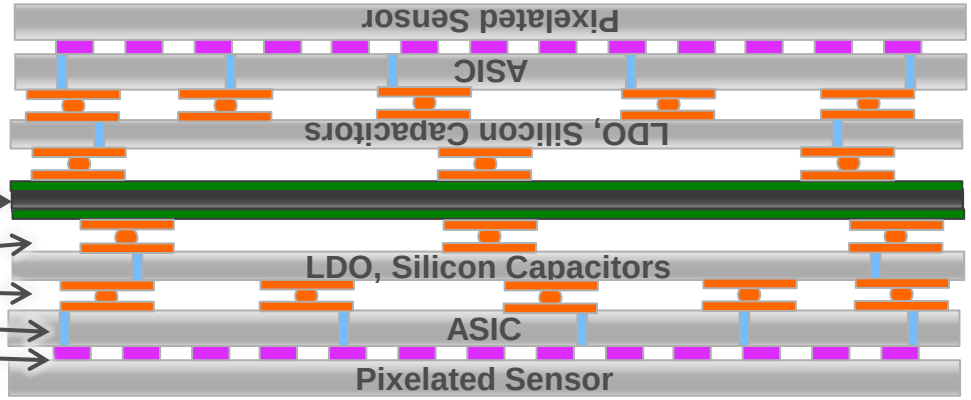


CLIC Vertex detector will take advantage of :

- **4-side buttable single chip assemblies**
  - **Through-Silicon Vias,**
  - **Active edge sensors**
- **Air cooling**
  - **High-Density (pF/μm^3) Silicon capacitors**
  - **Low mass LDO**

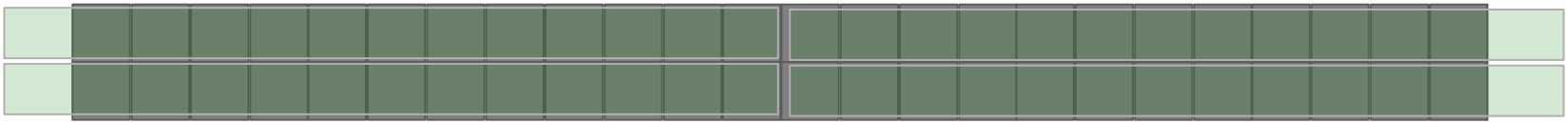
Carbon fiber Ladder
Flex (Power IN, Data)
BGA Interconnect
Through-Silicon Vias (TSV)
Pixel Interconnect
- **Bumps,**
- **Copper Pillar,**
- **Oxide-Oxide bonding**

CLIC Hybrid Pixel Assembly

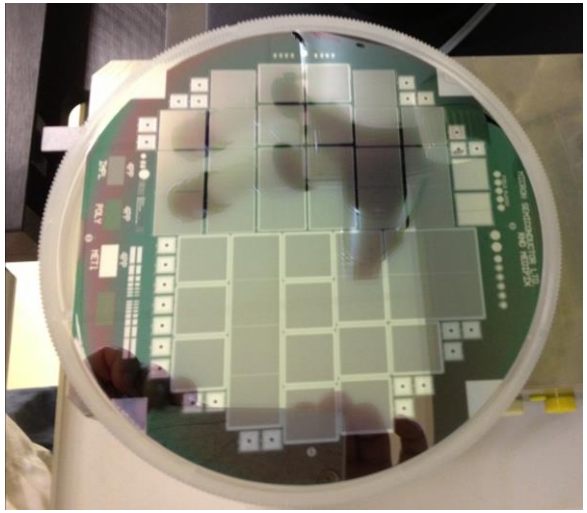


Single Ladder

Double Ladder

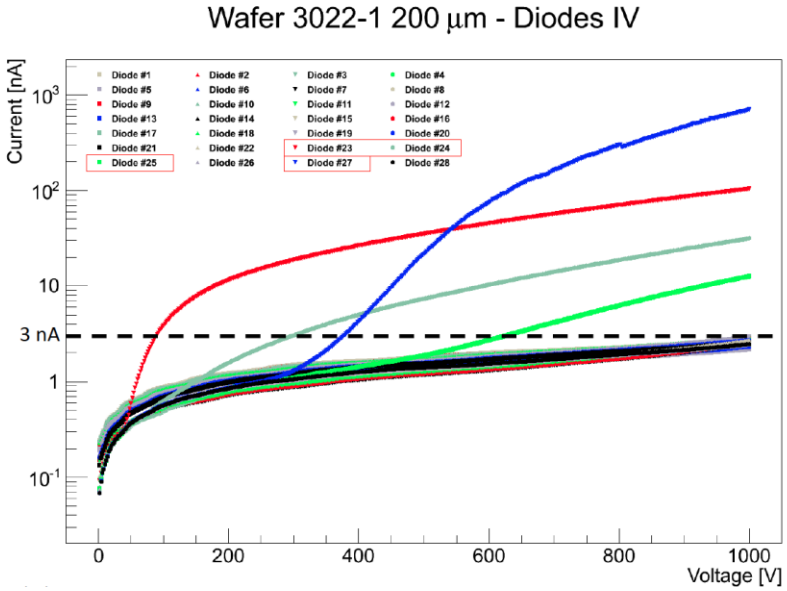


Sensor production and procurement : Micron Semiconductor Ltd

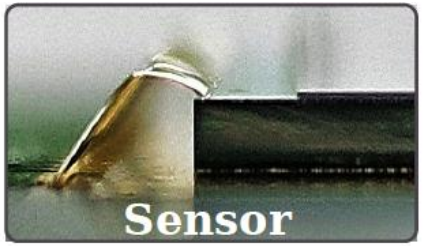


A first sensor production was launched in 2012 to investigate with manufacturers the possibility to process very thin sensor wafer.

- First delivery from Micron Semiconductor Ltd. (UK) of 10 Timepix Sensor wafer end of 2012
  - 4 N-in-P, 6 P-in-N wafers
  - Thickness between 100 um and 300 um
- Very good sensor quality
  - Visual inspection OK!
  - Current-Voltage curve on test diode show very good leakage properties and no breakdown up to 1000V

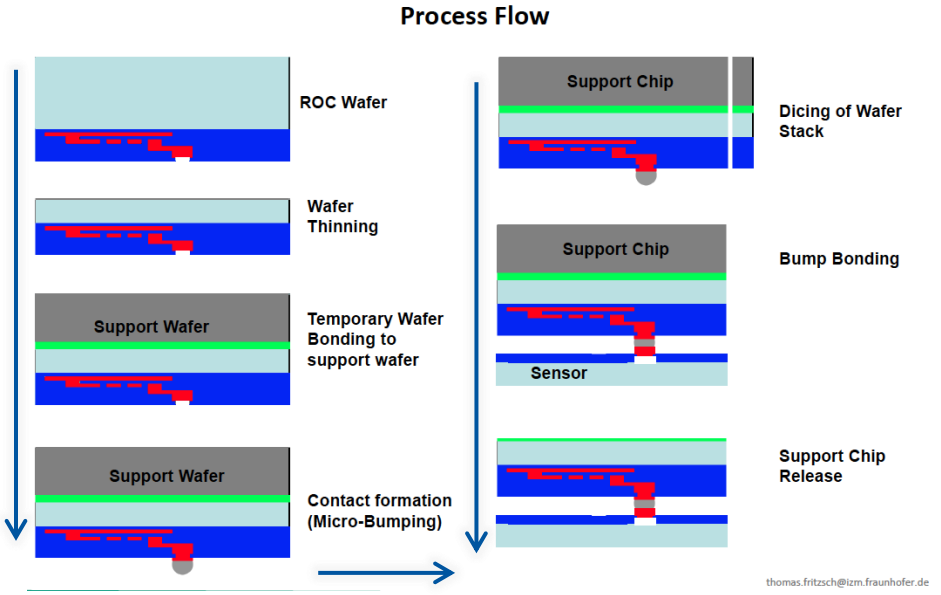


Sensor production and procurement : Bumping at IZM



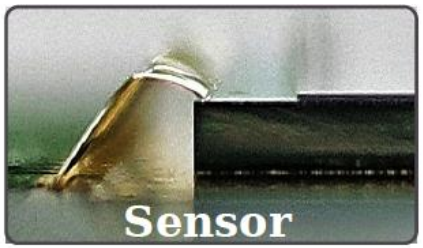
Micron Sensor Wafer were sent to IZM for Under-Bump Metallization and assembly to Timepix and Medipix3RX ASIC

- 6 Sensor wafers processed by IZM
  - wafer < 200 um thickness attached to handle wafer for processing
- 2 Timepix ASIC wafer processed with bumps for attachment to Micron sensors .
  - 2nd wafer thinned down to 100um and attached to handle wafer for production of very thin sensor assemblies
    - Target : 100 um Sensor on 100 um Timepix ASIC
- First Assemblies return to CERN and tested in August DESY Test beam
- 100um Sensor wafer broke during handle wafer removal -> Most sensors OK !
- 100um ASIC wafer processed , now testing quality of the assemblies



Sensor production and procurement : Advacam

For Test Beam results, see Samir Arfaoui in next talk



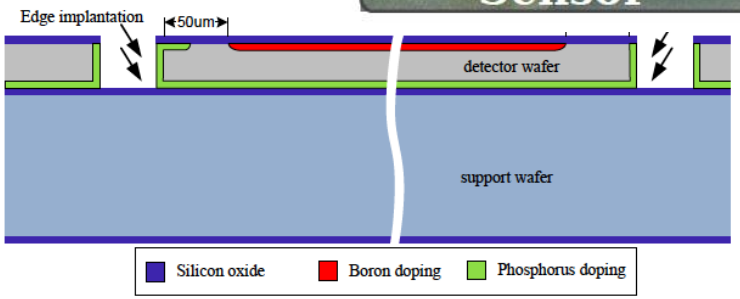
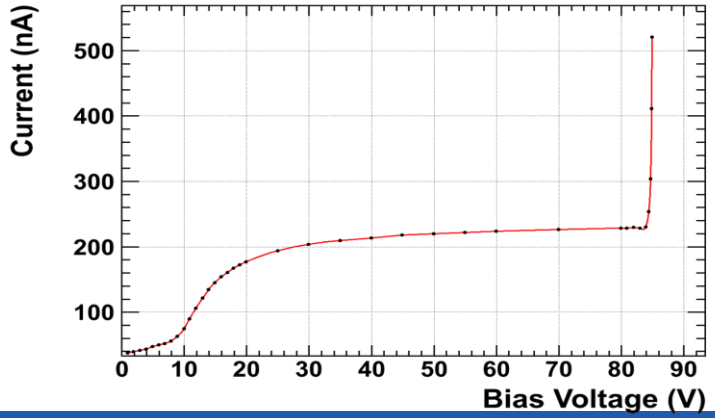
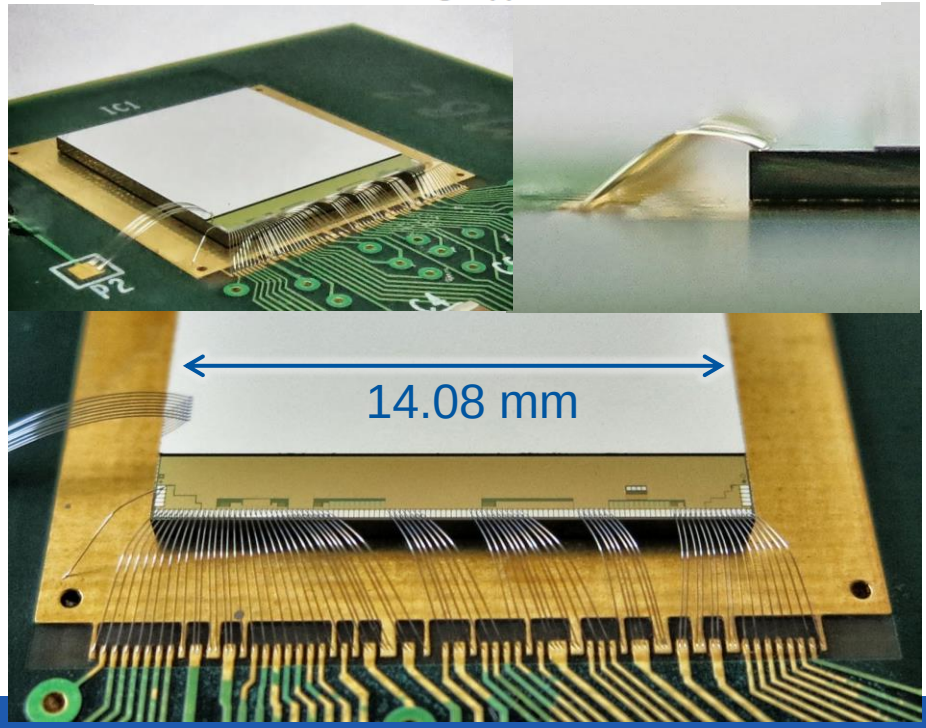


Illustration of the active edge approach with P-on-N structure

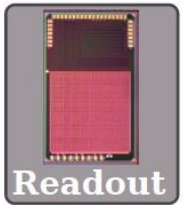
Production of assemblies with very thin sensors has also been investigated with Advacam (Finland)

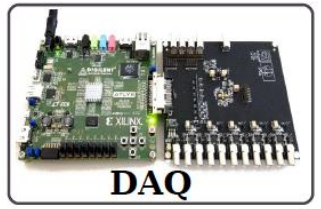
- 50 um p-in-n Timepix thin assemblies with 20/50um active edges delivered to CERN in July 2013
- Very good bump quality, only a few merged/unconnected bumps
- Depletion at 15V, good leakage current properties (~100nA @ 15V) , uniform on all tested chips , Breakdown @ ~85V
- 5 assemblies tested in August 2013 DESY Test beam





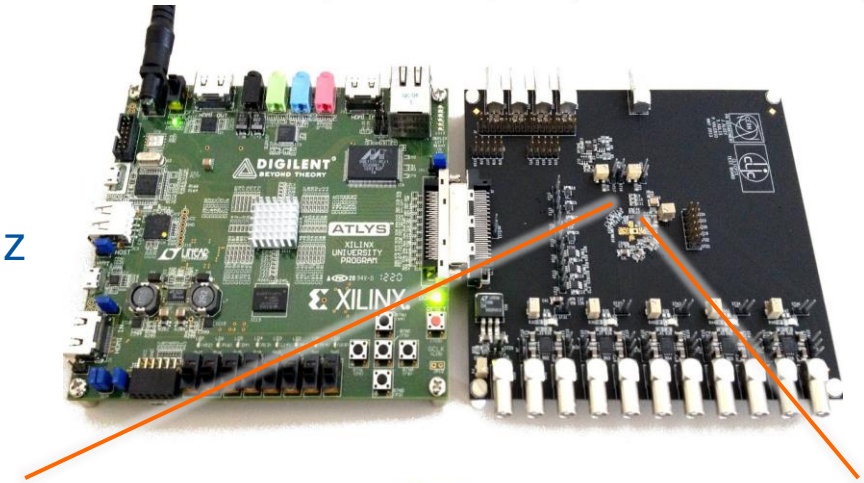
ASIC Development : CLICpix





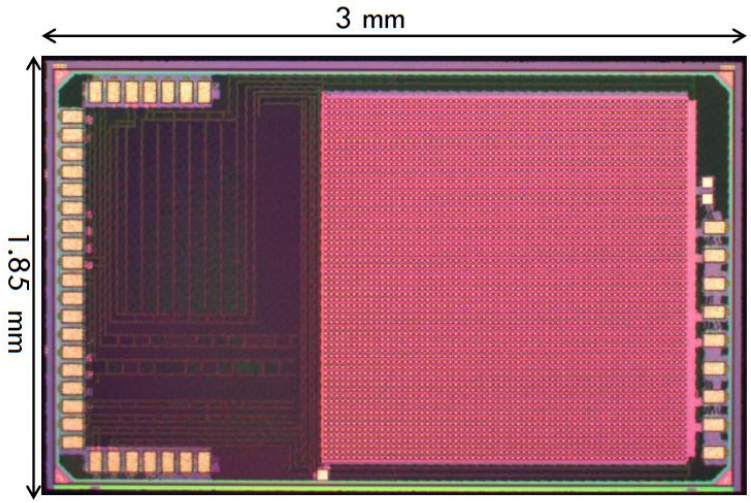
Main features:

- Small pixel pitch (**25 µm**),
- **Simultaneous TOA** (4 bits) &**TOT** (4 bits) measurements
- **100MHz measurement clock** and 320 MHz readout clock
- **Power pulsing**
- **Data compression**
- Both pulse polarities can be handled

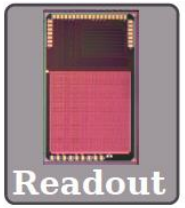


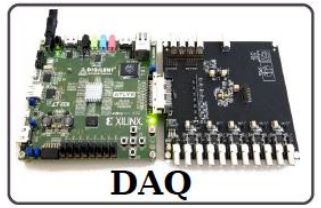
Demonstrator CHIP:

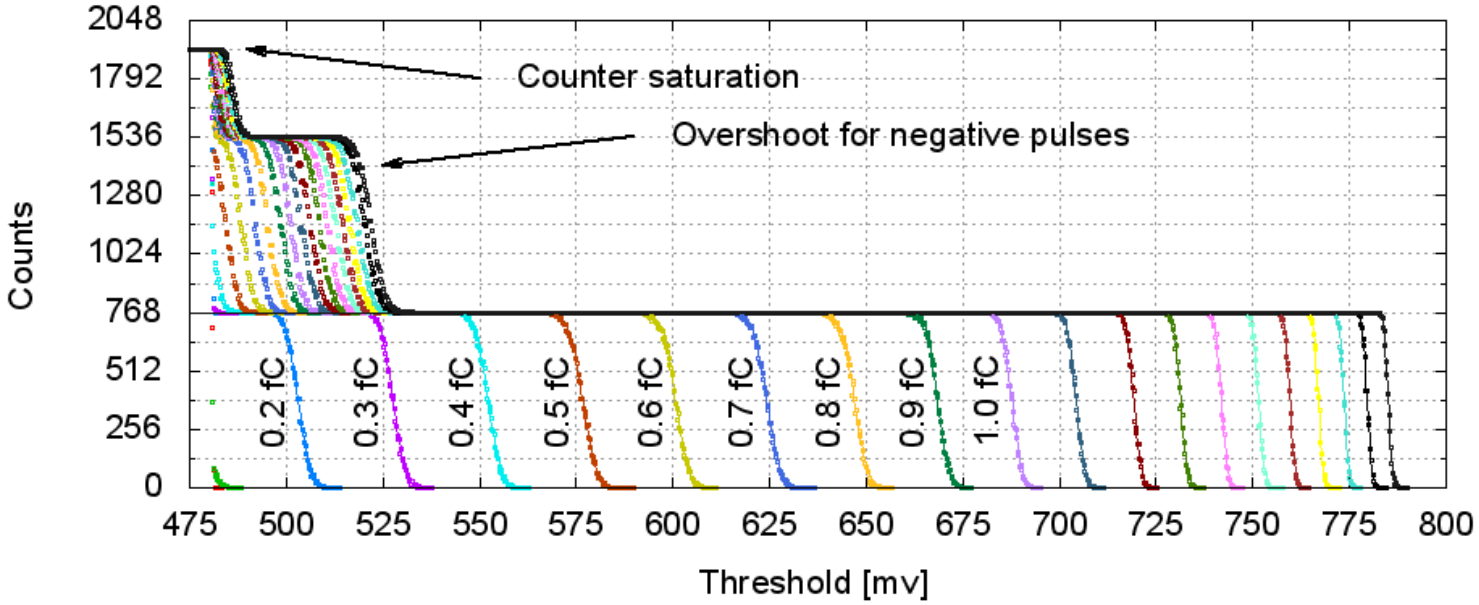
- commercial **65 nm CMOS technology** (proven to be radiation resistant)
- **array of 64x64** pixels
- The **Krummenacher architecture**, with a single ended preamp, a two stage discriminator and a 4-bit DAC

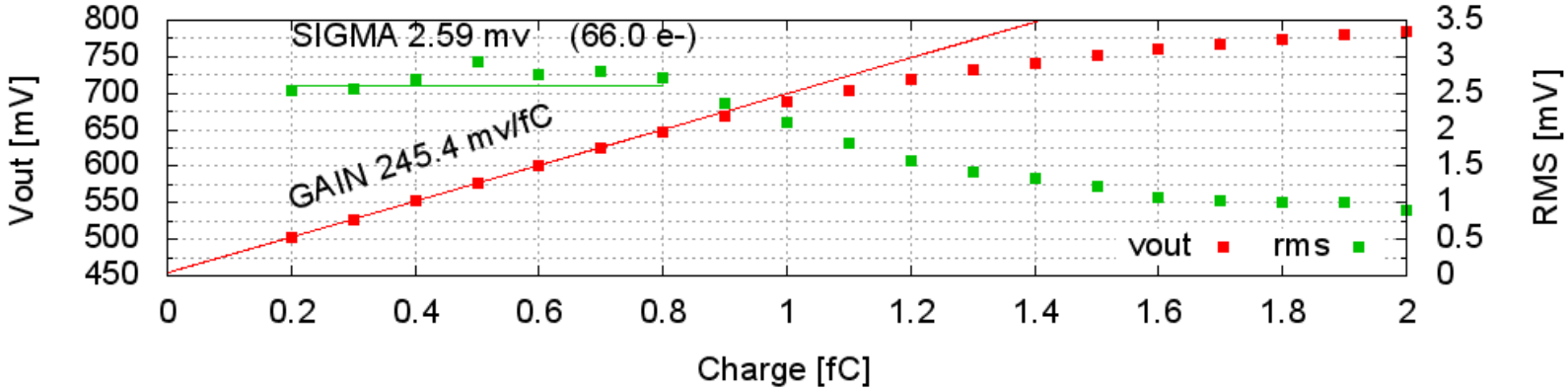


ASIC Development : CLICpix

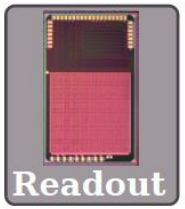


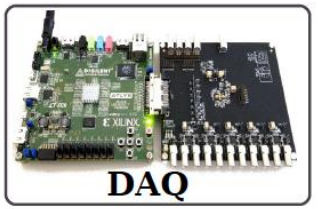


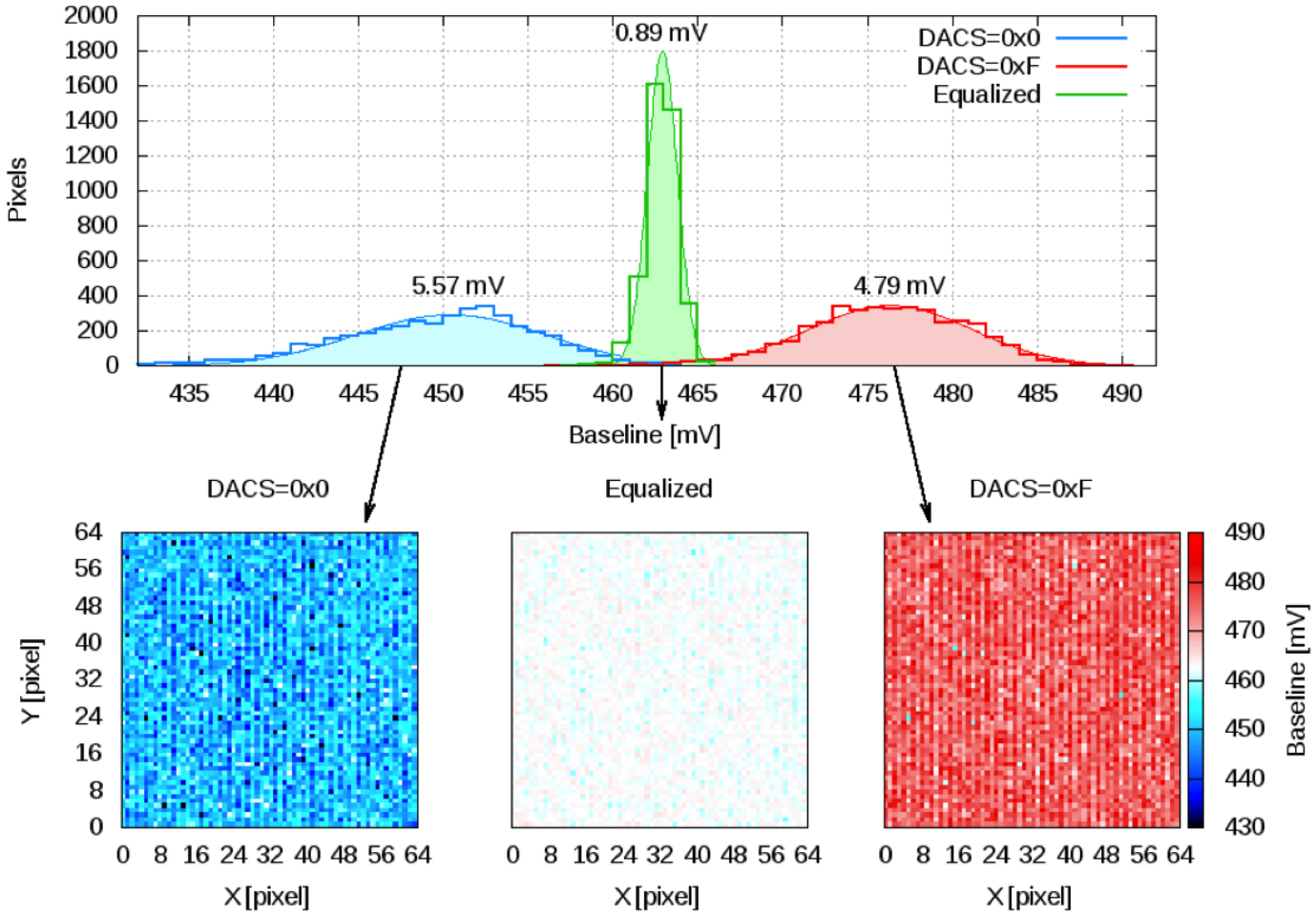




ASIC Development : CLICpix

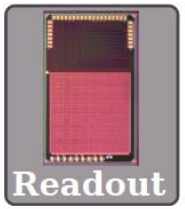


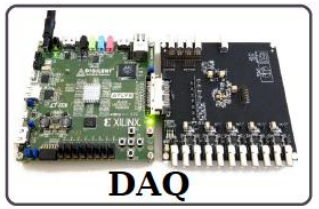




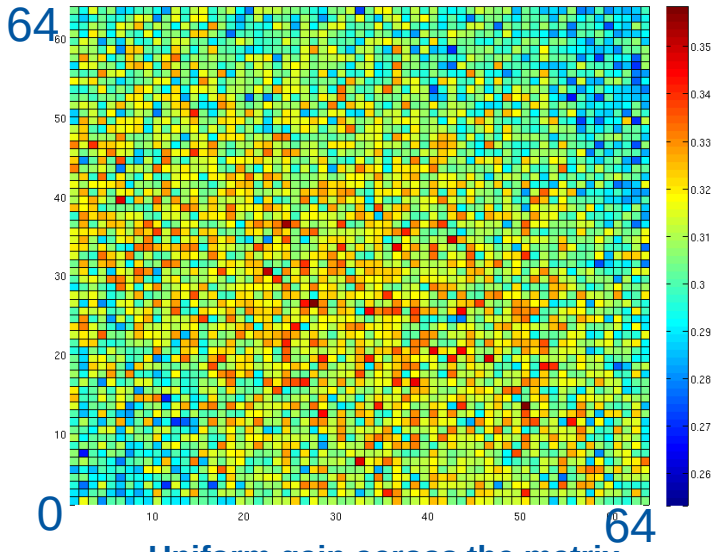
Calibrated spread is 0.89 mV (about 22 e-) across the whole matrix

ASIC Development : CLICPix



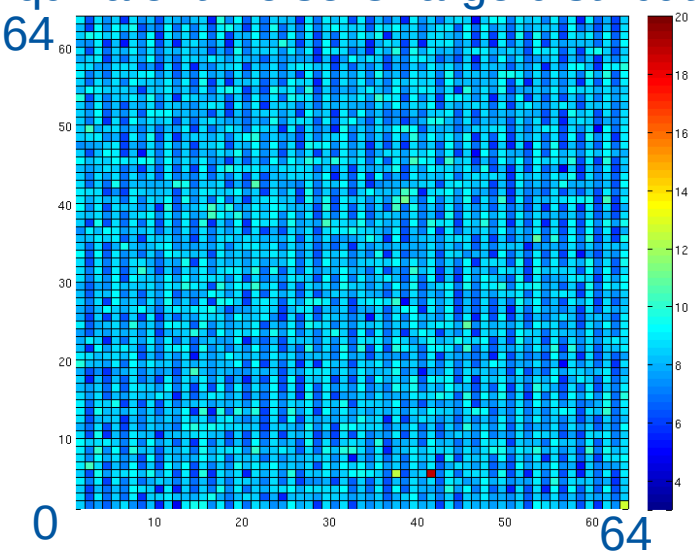


TOT Gain Distribution



- **Uniform gain across the matrix**
- **Gain variation is 4.2% r.m.s. (for nominal feedback current)**

Equivalent Noise Charge distribution

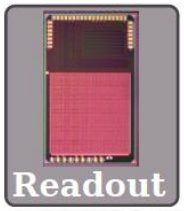


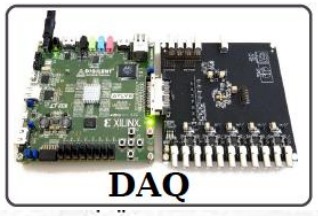
- **Uniform ENC across the whole matrix**
- **Mean ENC is 55 e^- (without sensor)**

- CLICPix prototype behave as expected from simulation and meet CLIC Vertex Detector specifications
- Hybridation to Sensor is an ongoing issue
  - Multi-Project Wafer -> Only single dies available
  - 25 µm pitch challenging for the industry
- There is hope, 25 µm hybridation with single die achieved by PSI

(see X-ray detector developments for synchrotrons, Bernd Schmitt, Vertex2013)

Interconnect R&D : TSV





Through Silicon Via: vertical electrical connection passing through Si wafer.

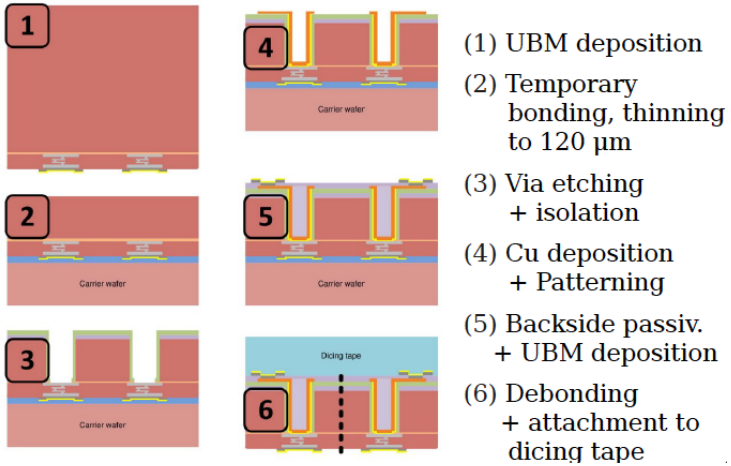
- eliminates need for wirebonds
- 4-side buttable chips
- increased reliability, reduced material budget

First Medipix3 Image through TSV

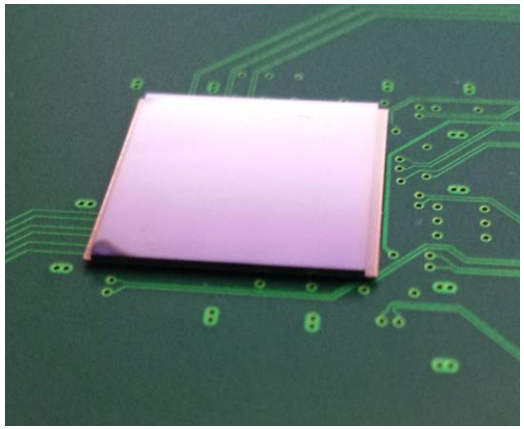
CLIC was a participant in Medipix TSV Project with CEA-LETI

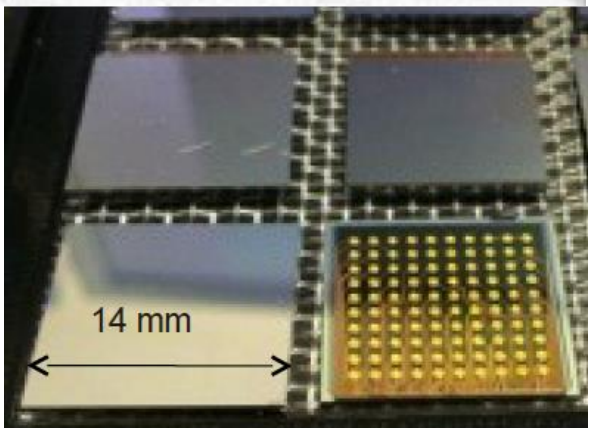
- Successful first run aimed at demonstrating feasability
- Second run ongoing to demonstrate good yield

CEA-Leti via-last process flow

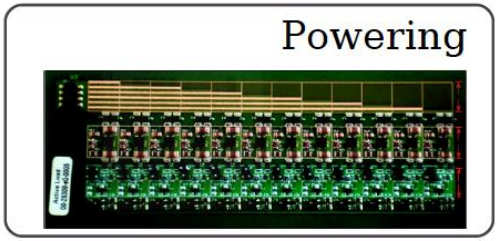


(1) UBM deposition
(2) Temporary bonding, thinning to 120 µm
(3) Via etching + isolation
(4) Cu deposition + Patterning
(5) Backside passiv. + UBM deposition
(6) Debonding + attachment to dicing tape





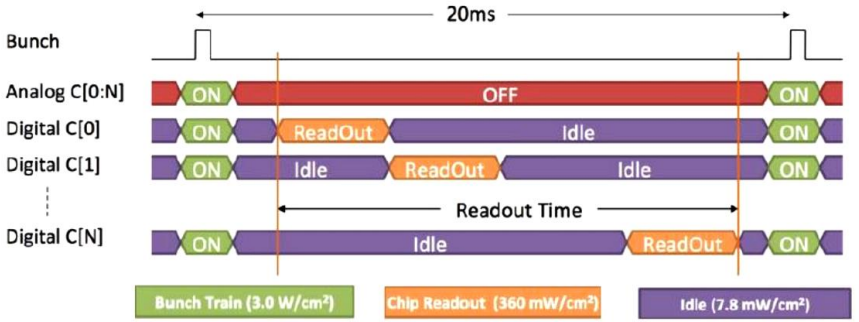
Powering for CLIC Vertex detector

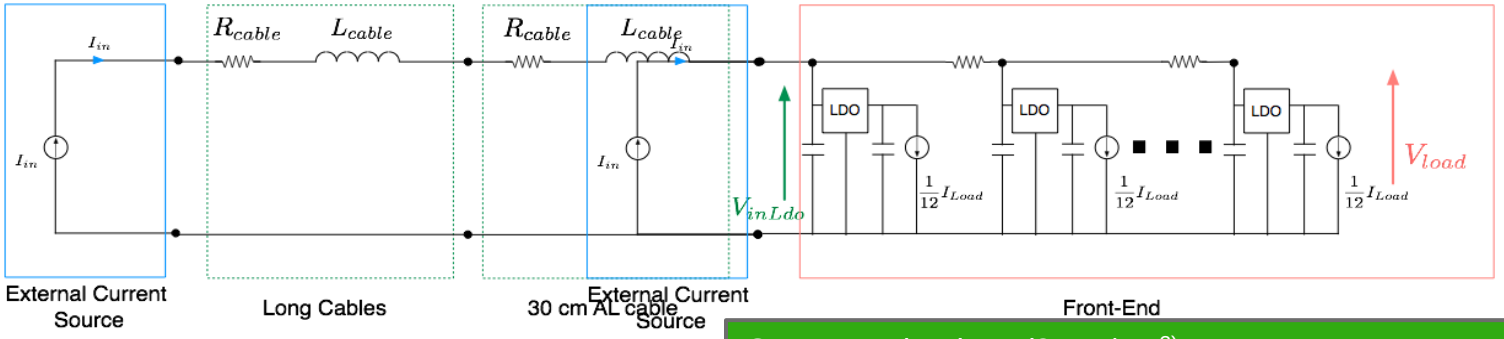


Power pulsing (of unused blocks) to reduce average power consumption!

Challenges:

- High peak current **> 40A/ladder**
- High magnetic field **4-5T**
- Material budget **< 0.1% X_0**
- Regulation **< 5% (60 mV)**





Implementation:

- **aluminum cables** on kapton tape
- **silicon capacitors** (80 µm thick, low mass)
- **LDO voltage regulators** (good regulation)

Currently Achieved material budget : 0.1 %X_0

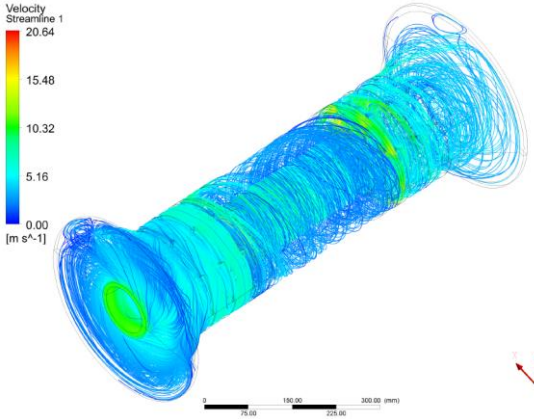
Current technology (25uF/cm^2)

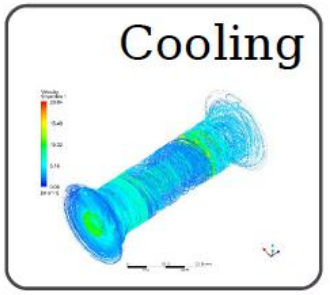
- Analog : 10% Flex,15%LDO, 75% Si Cap. ->0.064 % X_0
- Digital : 15% Flex, 1% LDO, 84% Si Cap. -> 0.04% X_0

Future Technology (100uF/cm^2)

- Analog : 22% Flex, 35% LDO, 43% Si Cap. -> 0.028 % X_0
- Digital : 42% Flex, 1% LDO, 57% Si Cap. -> 0.015% X_0

Air cooling studies





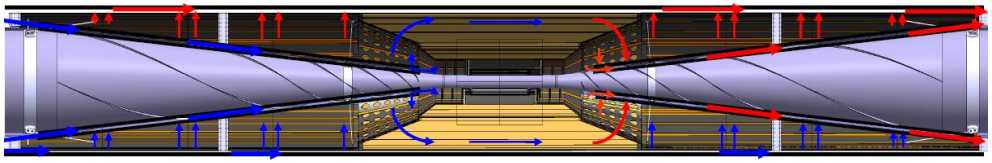
Challenges:

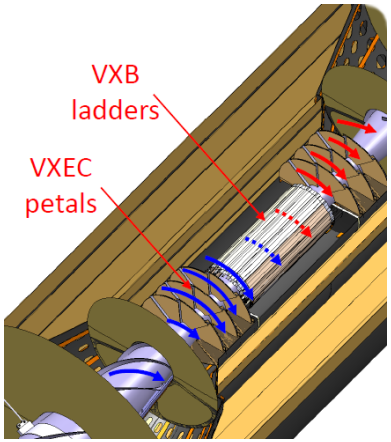
- Low material budget
- ~470 W heat load to extract (50mW/cm^2)
- High dimensional stability
- Assembly and cabling integration

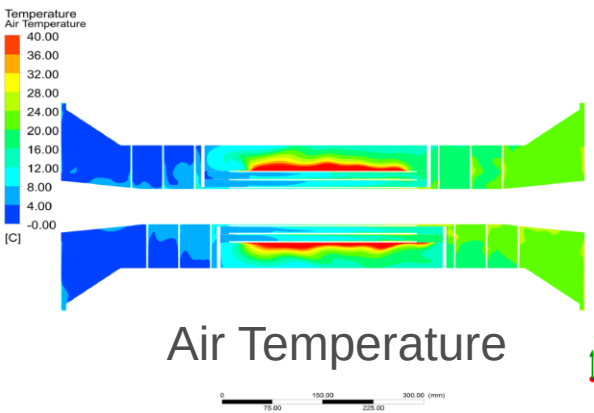
Solution:

- Forced air-flow cooling, spiral endcap geometry

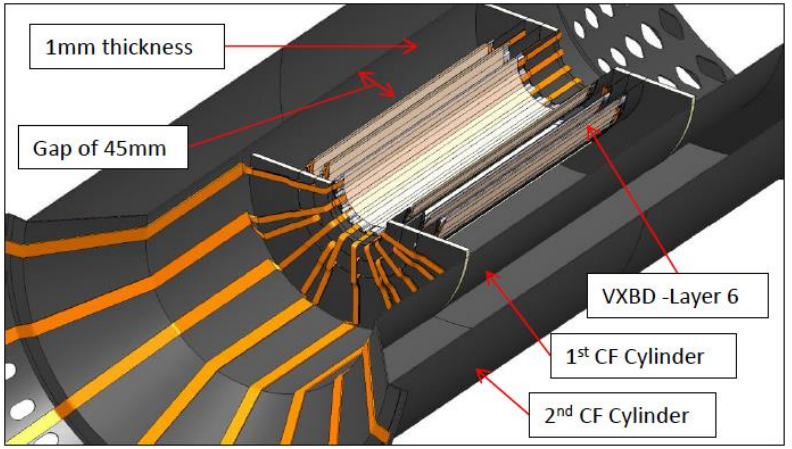
- Mass flow: **19.9 g/s**
- Avg. velocity in barrel: **6.3 m/s**





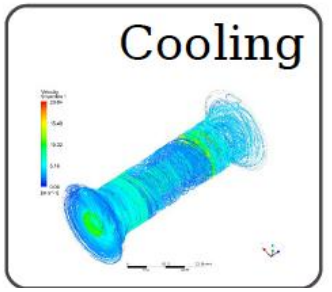


Air Temperature



- Silicon temperature below **30ºC**
- Conduction not taken into account

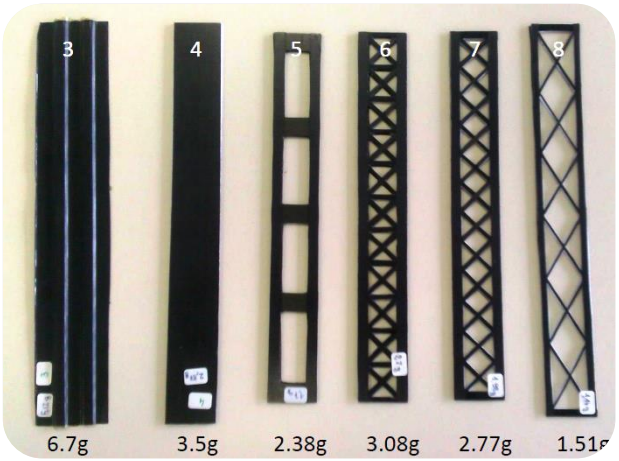
Air cooling studies

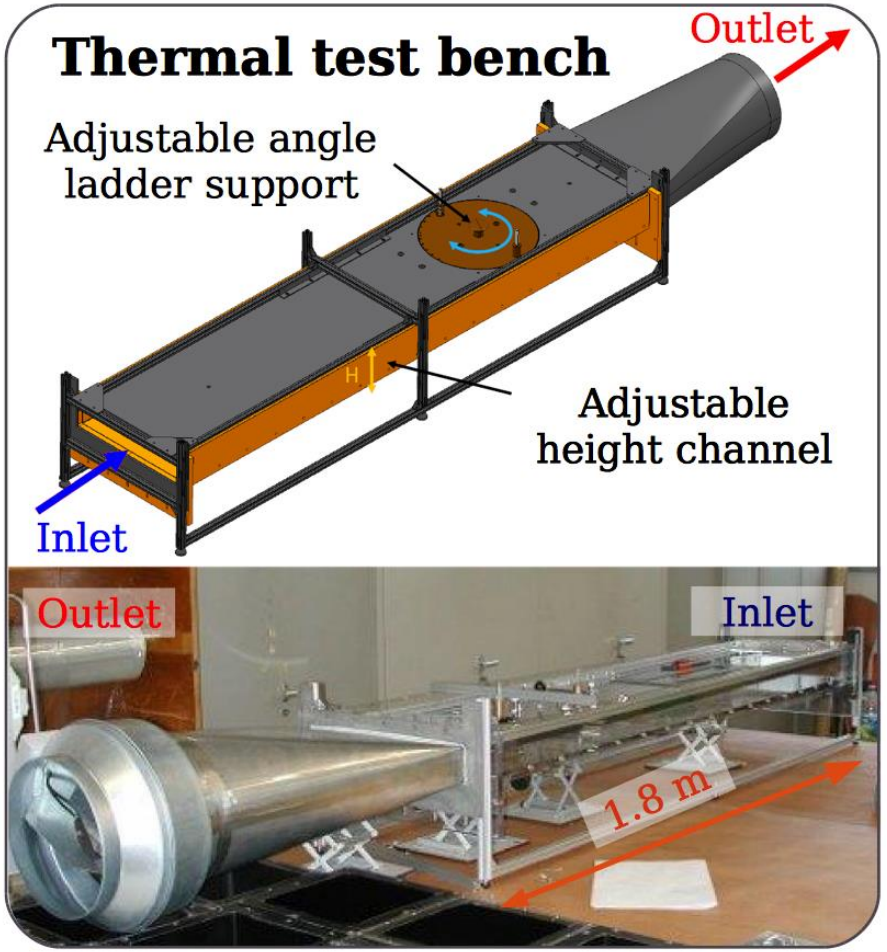


Test program:

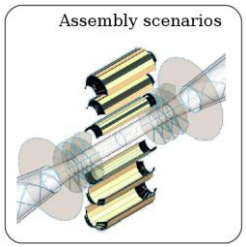
- Evaluate forced convection air cooling
- Measure & characterize air-flow induced vibrations
- Validate the dedicated finite element simulations
- Develop and characterize low-mass ladder support *(~0.05% X_0)*

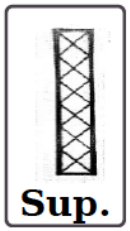
Ladder support structure prototypes

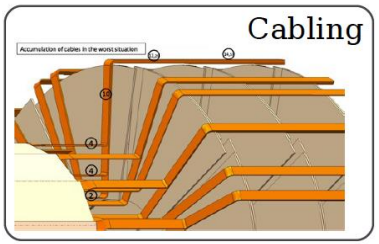




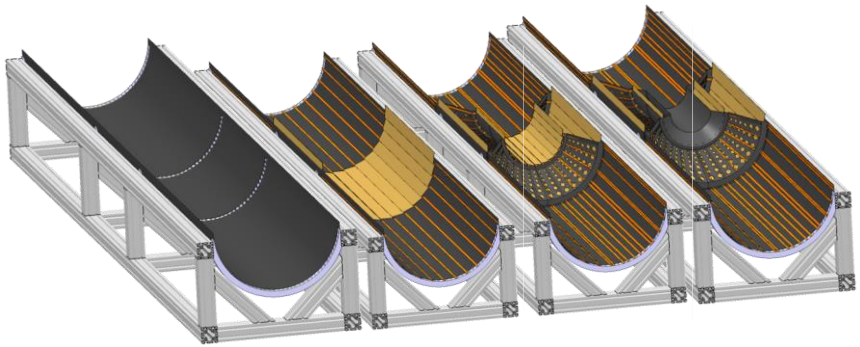
Mechanical assembly and cabling

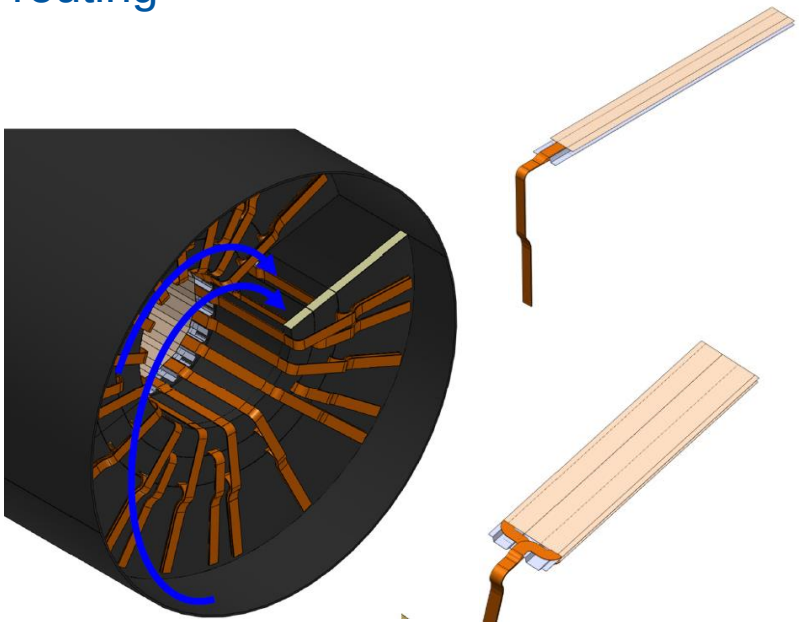


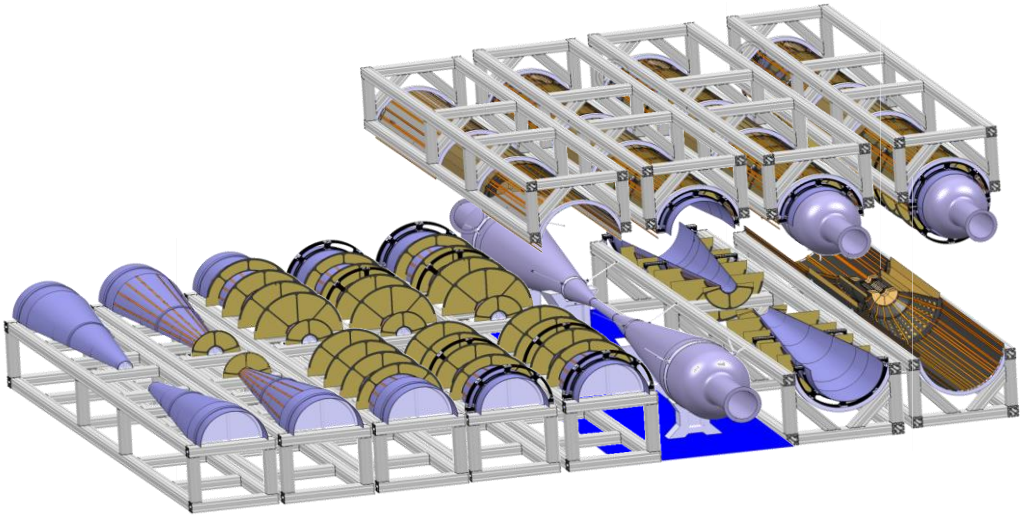




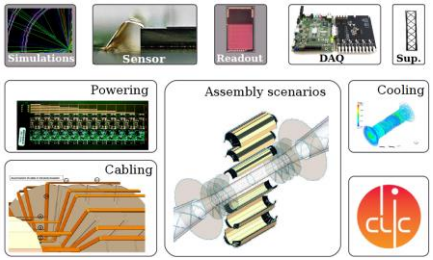
Modular assembly Scenario for the Vertex detector has been studied, including the integration of spiral endcaps for air cooling, taking into account stave design and cabling routing



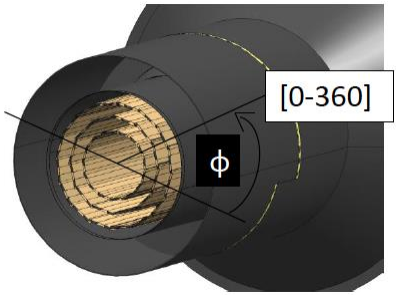


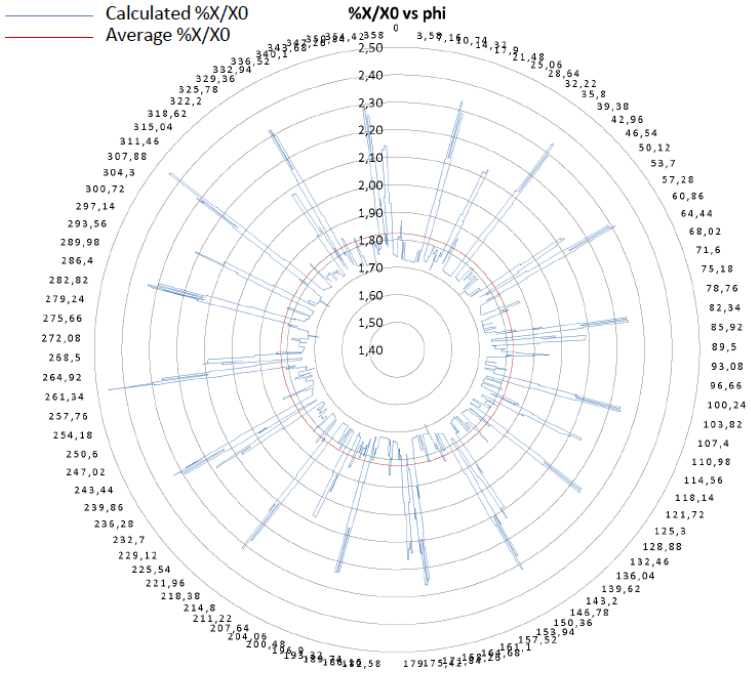


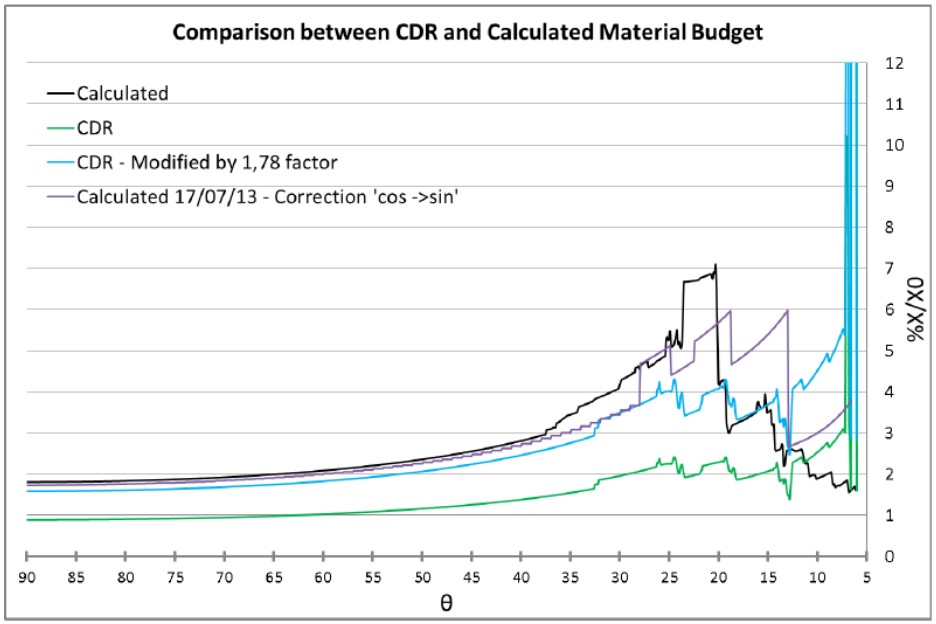
Material Budget estimation



Using an automated tools developped by LPNHE Paris, we are now able to extract realistic material budget estimation from the CAD model of the vertex detector and compare with results in GEANT4. Key design flaw and weak point can better be identified and redesigned.







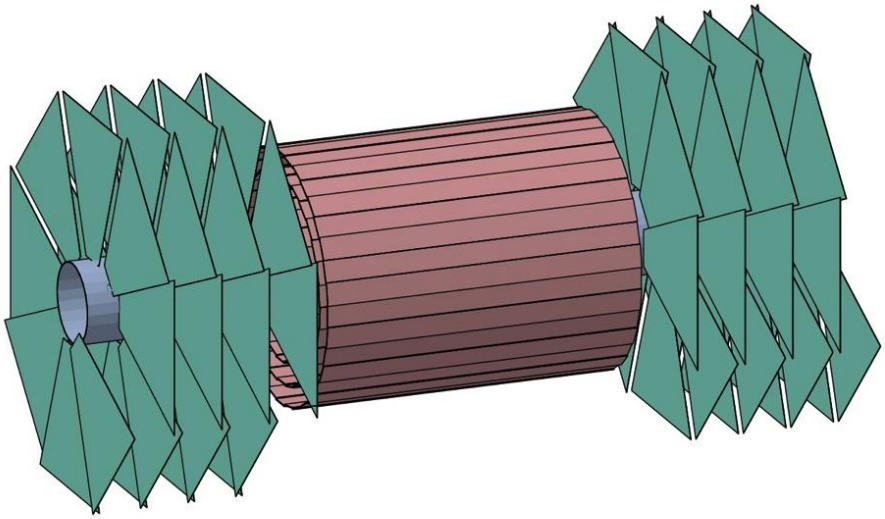
Simulation

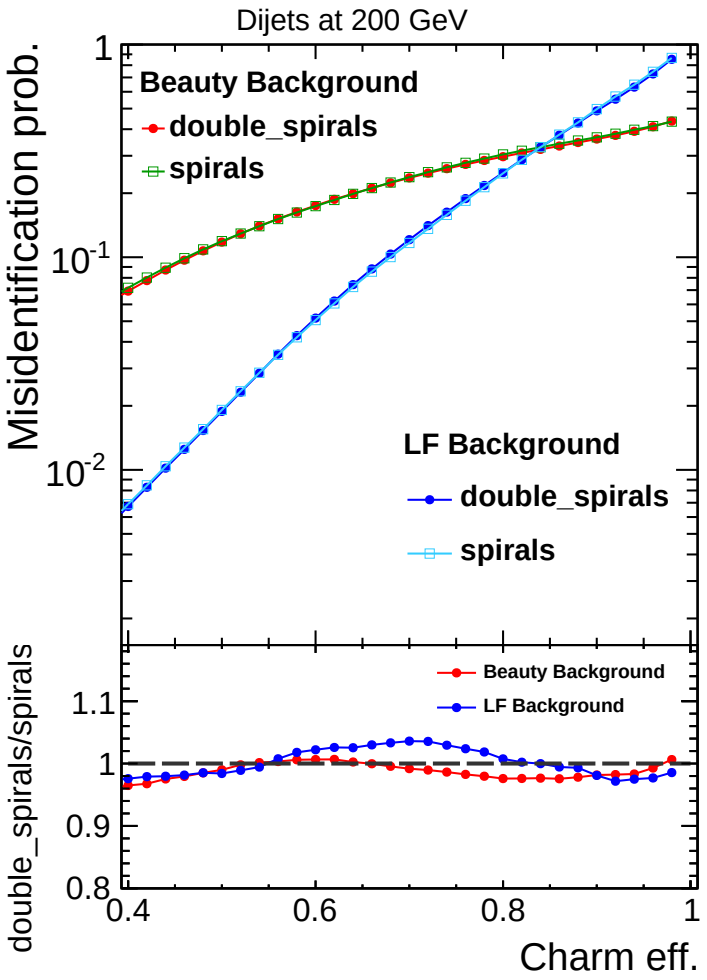
CLICdp has an ongoing campaign of simulation of more realistic models of the vertex detector aiming to optimize the layout, taking into account engineering constraints

- Double vs Single layers
- Spiral vs Standard Disks
- « Heavy » vs Standard Material Budgets

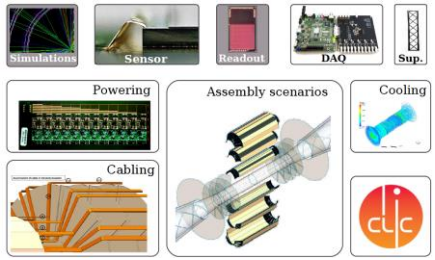
For details, please see :

Physics performance studies for different CLIC vertex detector geometries, Niloufar Alipour Tehrani



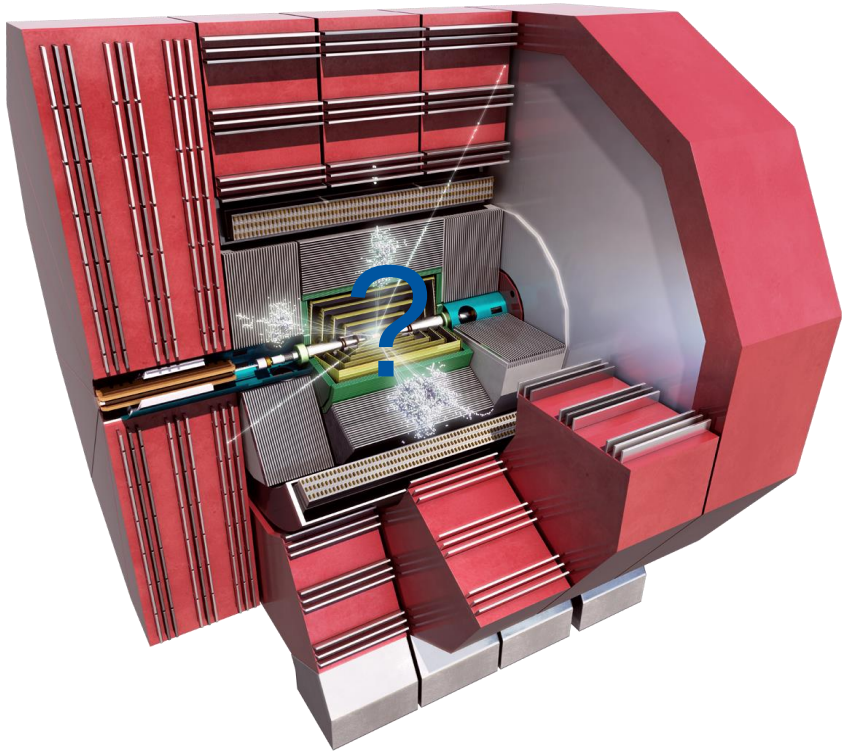


Towards a CLIC Vertex detector model



CLIC Detector and Physics Study has for goal to produce a new, unified detector model for 2015. Concerning the Vertex Detector, several studies presented here aims at addressing current issues :

- Magnetic field magnitude (4 or 5 T ?)
- Realistic expected Material budget
- Ladders and disks layout and radius taking into account volume of modules and assembly procedures
- Power distribution, heat generation and cooling integration to the design



Collaborators are welcome to join our efforts !

ご清聴ありがとうございました

Go seichō arigatōgozaimashita

Thank you very much for you attention !