Technical R&D towards a Silicon-Tungsten EM calorimeter for ILD

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On behalf of the CALICE collaboration

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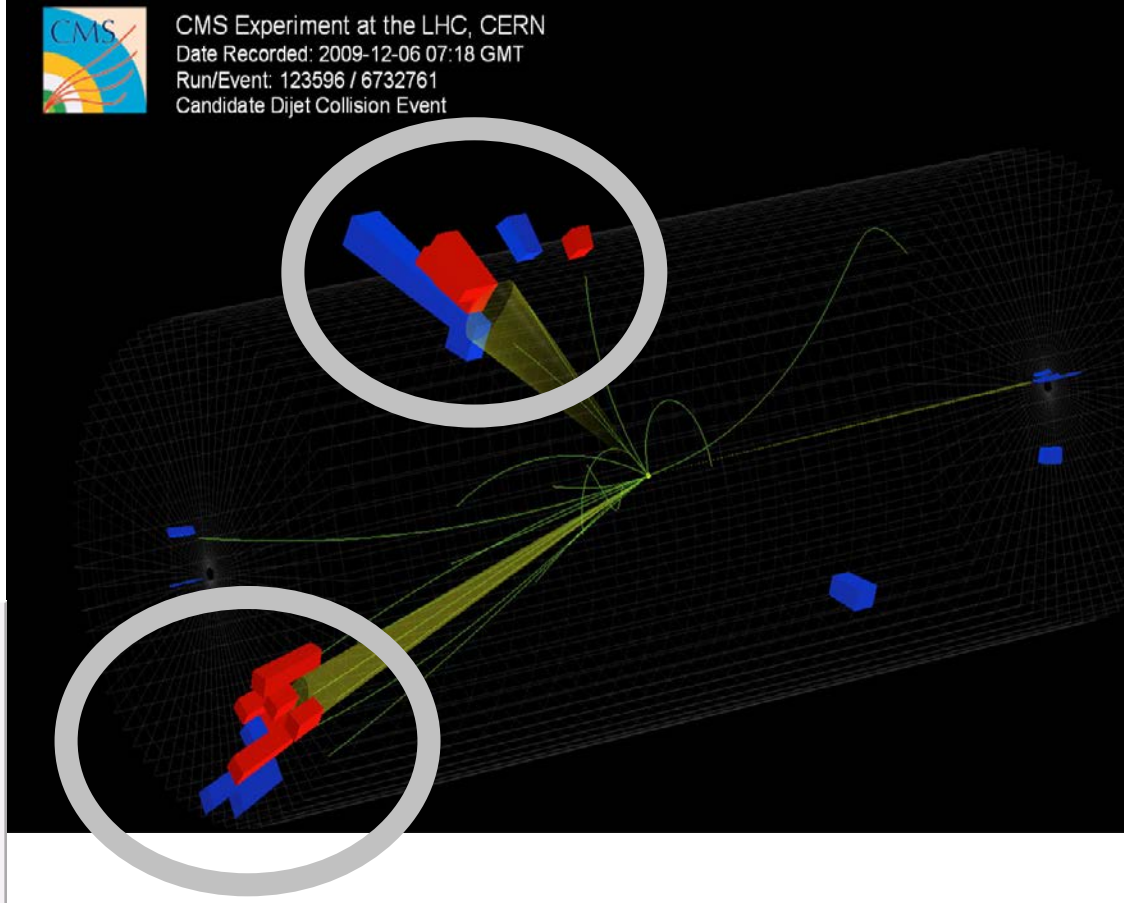

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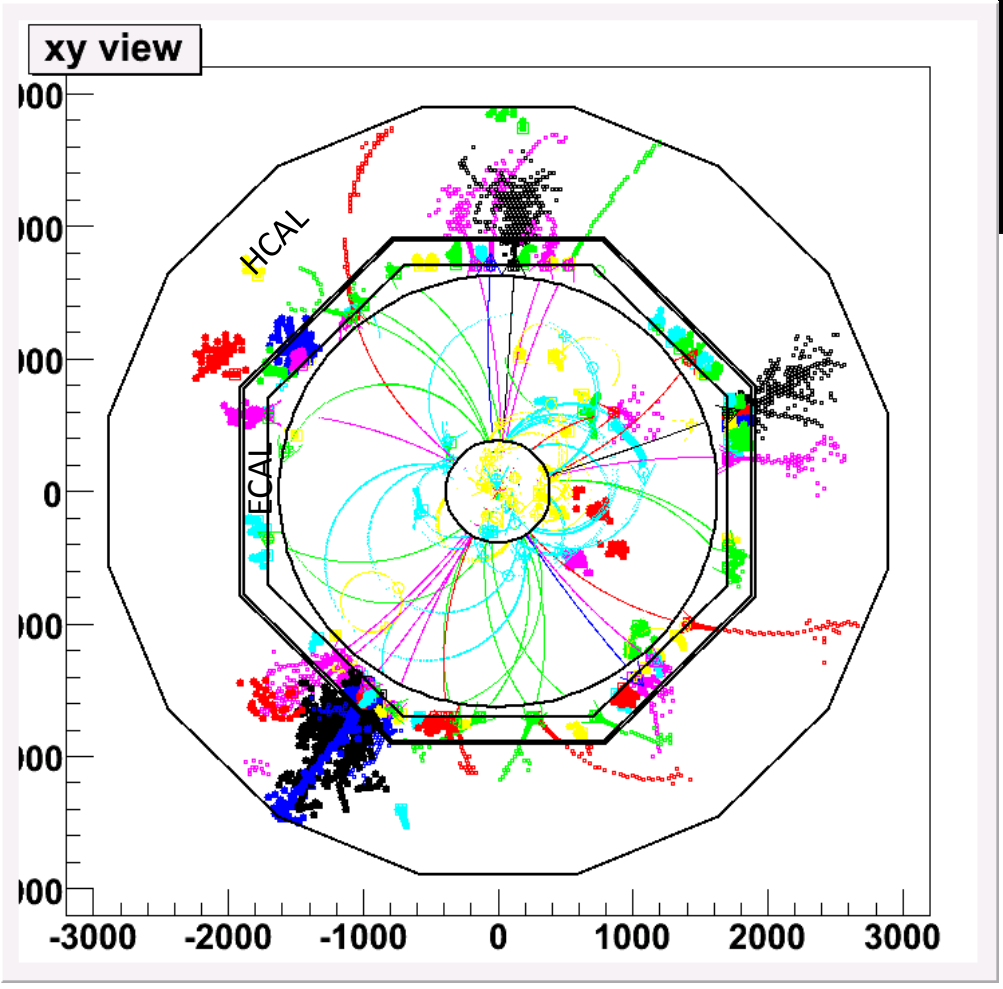


A mix of technologies qualified with prototypes

Time line

Physics prototype

Technological prototype

ILD ?

Proof of concept

- Linearity
- Resolution
- Sensors
- Very front-end

1500 channels/dm^3

Feasibility of design options

- Compactness
- Granularity
- Front-end
- Power pulsing
- Long SLAB

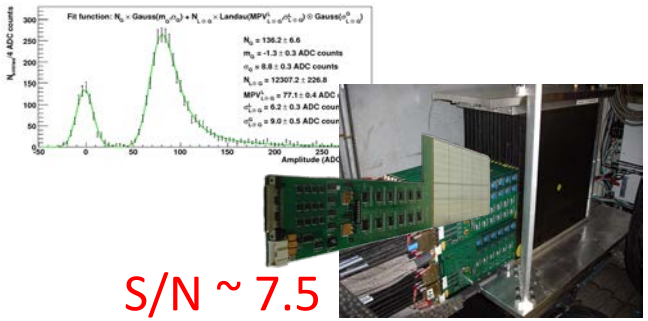
4000 channels/dm^3

Construction

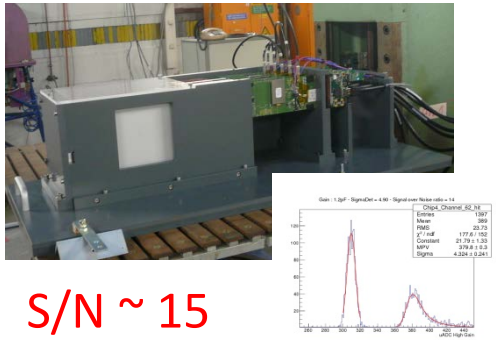
- Integration
- Environement
- Services
- Industrialization
- Tooling
- Project org.

4000..10000 channels/dm^3

2004-2008
30 layers
4000 channels

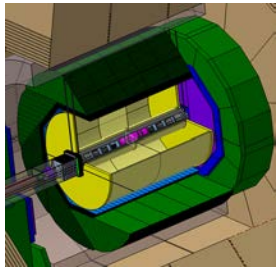


S/N ~ 7.5



S/N ~ 15

~24 X0, 20 cm thick
~2500 m^2 active detectors
~100M readout channels



Technological prototype (2011..) : Proof of feasibility

→ **embedded "system on chip" electronics** with two options:

- **packaged chip + external components (conservative baseline)**
- die bonded into to PCB + NO external components (challenge)

→ **Long detector SLAB** (up to 160 chips, 10k chn.)

- Propagation of critical signals over 2m (high load + interconnects)
- Distribution of power supply (would require external capacitors)

→ **wide sensors** (81 cm², HighRes silicon)

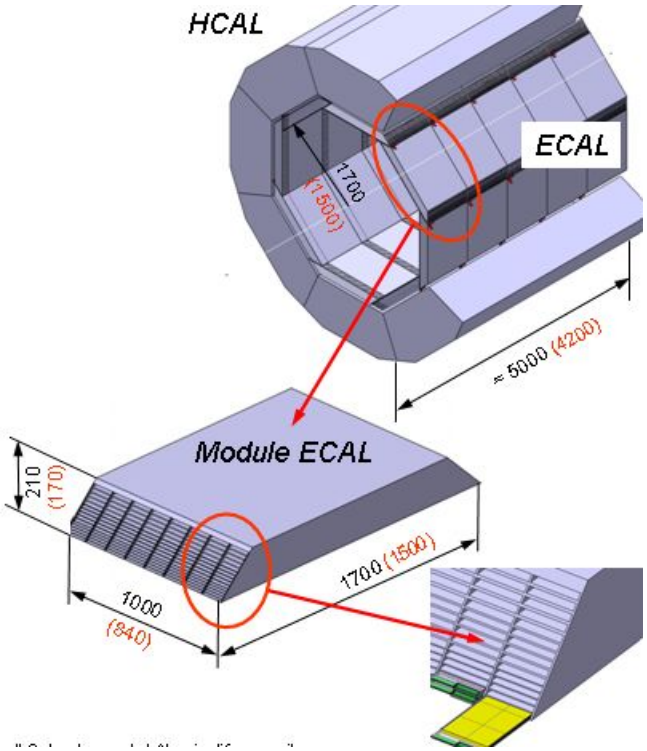
- Non standard guard-rings required to avoid cross-talk

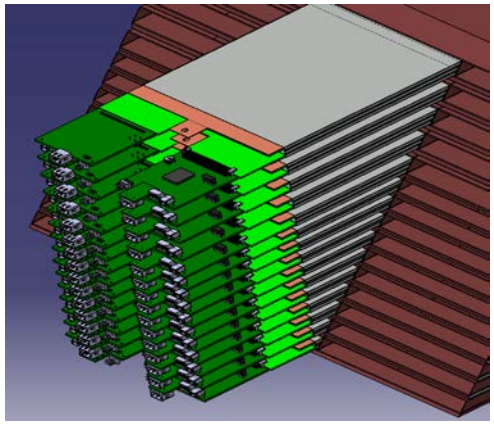
→ **large composite mechanical structure**

→ readout technology insensitive to ~4T field

→ integrated DAQ system & services (LV, HV, ECS…)

→ manufacturing tools: gluing, assembly, qualification





Short term goals (2 yr.):

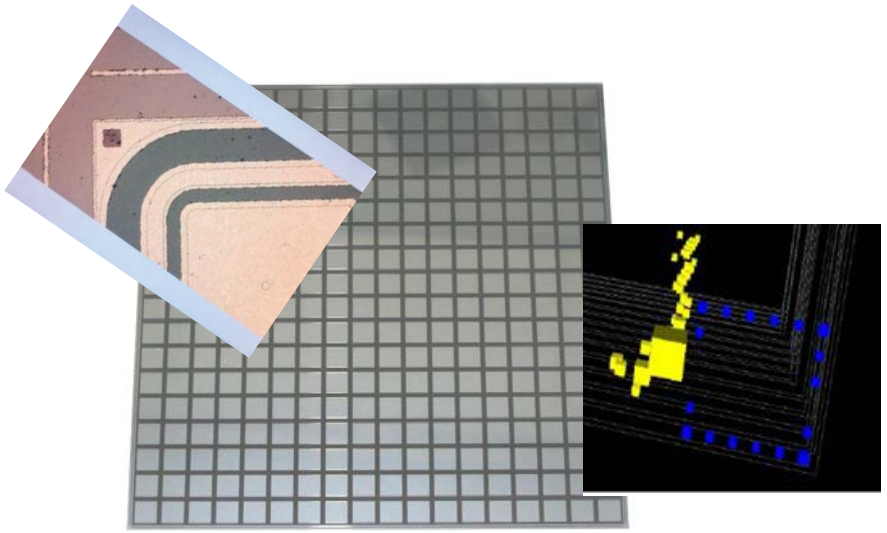
- 1 long slab partly instrumented
- 1 tower made up of short SLAB, 1k chn. each (~20k channels, 18 cm² crosssection)

PIN diode matrices design

The simplest design to control the cost
- Few thousands of m² needed for ILD
- Glued on PCB (cheap & low risk process)
- Square shape (easy dicing & integration)

Drawbacks :
- Floating Guard Rings: Crosstalk with GR

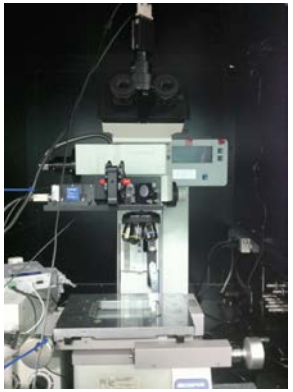
R&D in close collaboration with HPK
- Split GR and/or complete removal of GR
- Laser dicing : gain a factor 2 on dead zone
- Smaller size abutted matrices may improve yield
- Several batches, ~150 sensors tested

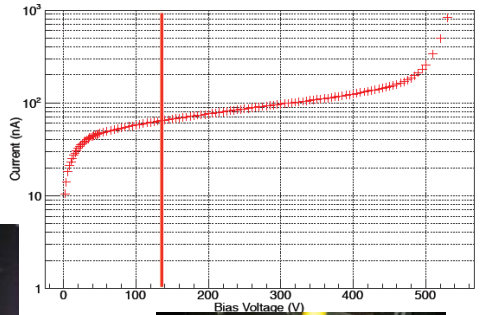


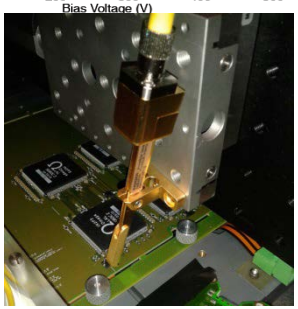
HPK : 9x9 cm², 256 pixels

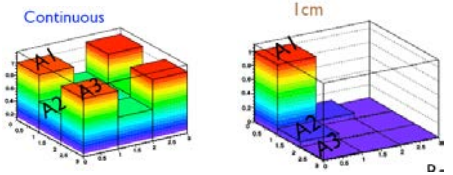
A large set of measurement benches
- DC characteristics wrt. T & RH
- Crosstalk measurement
- Laser setup

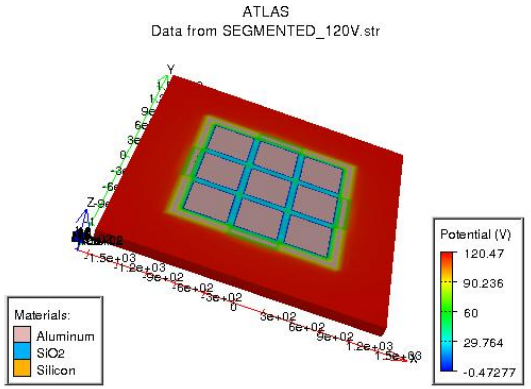
Simulations
- Crosstalk models
- Charge collection







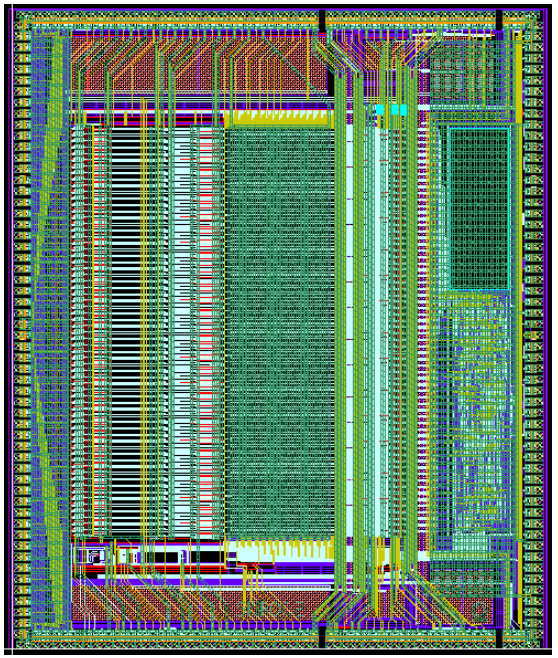




SKIROC2 chip

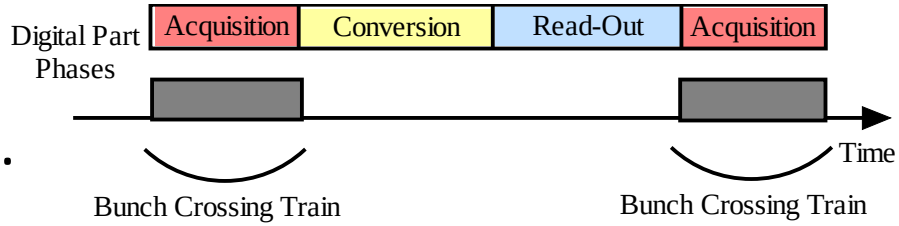
Silicon Kalorimeter Integrated Read Out Chip

- Technology SiGe 0.35µm AMS. Power-pulsing → 25 µW/channel
- 64 channels, variable gain charge amp, 12-bit ADC, digital logic
- In test beams : excellent S/N = [10-20]
- Some digital/analogue couplings



New technology : XFAB 0.18 µm SOI

- Suppresion of the crosstalk via substrat.
- New architectures for the preamplifier (differential architectures) improves PSRR/dynamic range/power consumption.
- Greatest challenge : Power supply of 2 V



Detector slab : “extreme” design

Compact assembly of 2 layers of 1 to 8 Active Sensor Units (ASU)

1 ASU = 1 kapton (HV bias for PIN diodes)

+ 1 layer PIN diodes

+ 1 PCB with microchips embeded (bonded at CERN)

+ 1 thermal drain (copper)

PCB is critical : 1.2 mm tick, 8 layers, chips bounded *into*

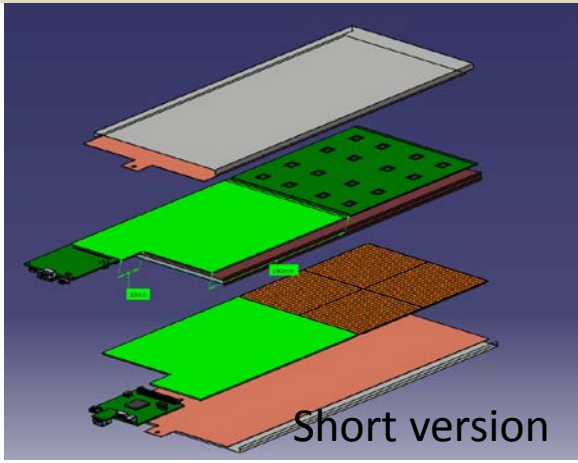
500 µm flatness targeted

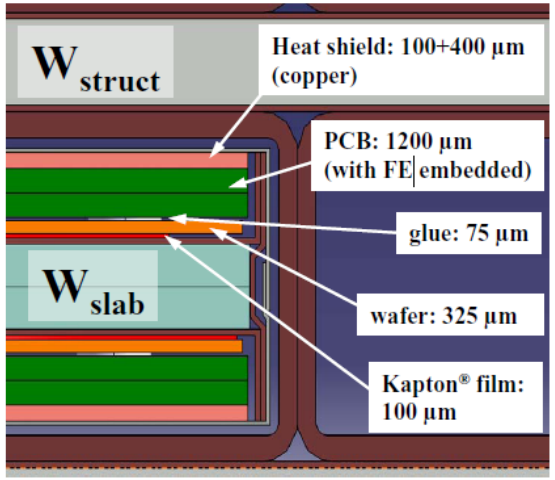
(1200 µ obtained: issue for gluing sensors)

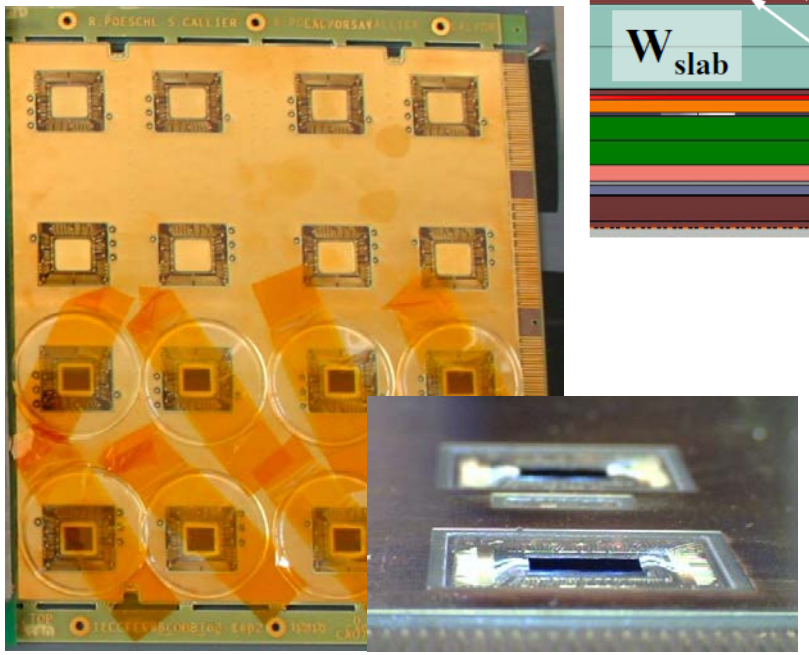
Board exists and partly

tested (pedestals).

R&D task to be continued



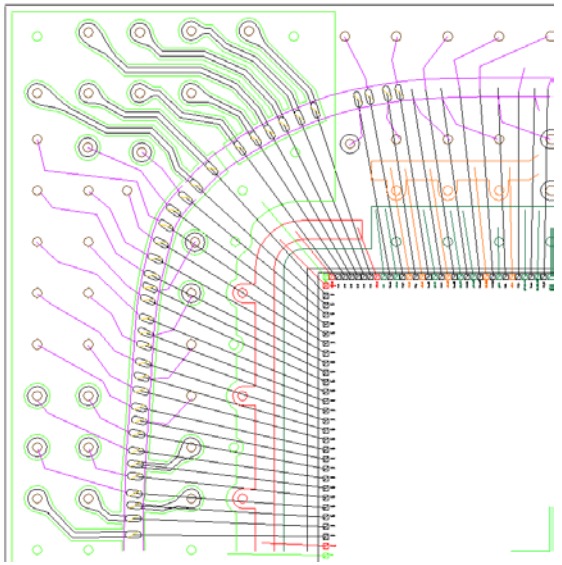


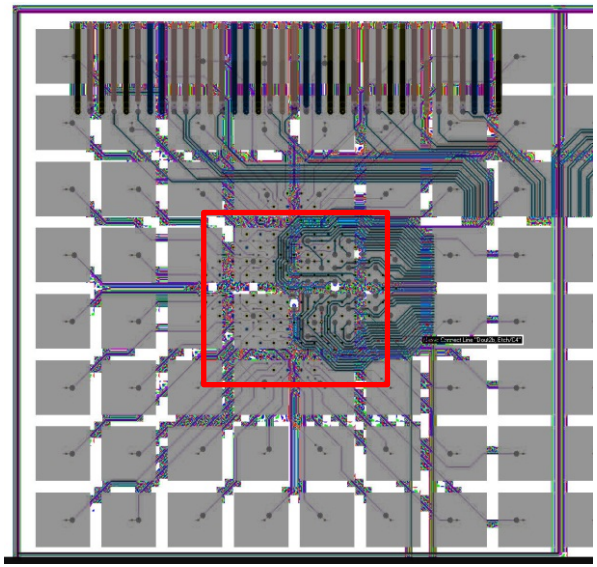


Detector SLAB « Conservative design »

Same concepts but with chips in package

- BGA design requires additional 3 mm in SLAB thickness
- Ultra thin BGA under study : promising
  - Feasibility of lidframe : done
  - Impact on Xtalk, noise : to be studied
  - Length of pixel-chip traces divided by 2-3 w.r.t. PQFP design





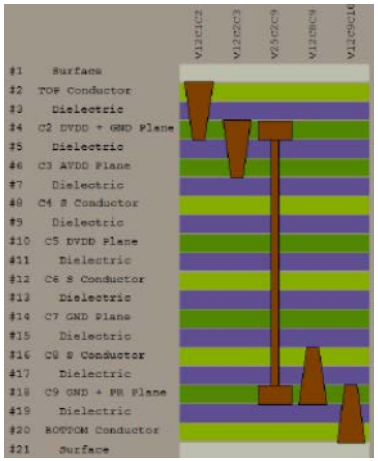
BGA pattern : 1/16th of the PCB

Advanced package technologies

- Thicknesses as low as 0.5mm (1.7 mm now)
- Ball bonded Flip chip
- Allow efficient routing of pcb traces and digital/analog separation : longest analog trace is ~2 cm

(very first tech. prototype build using PQFP to ease debugging)

Very next prototype



Symmetric stacking will improve flatness, good for wafer gluing

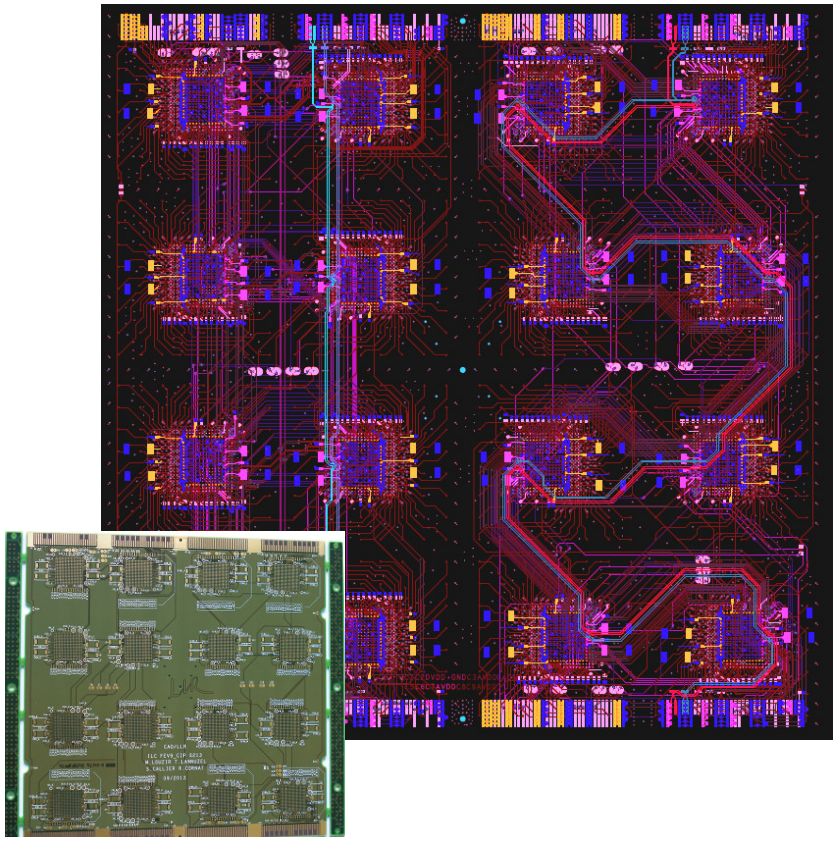
Analogue signals shielded up to the chip

Digital traces shielded and kept away of analogue (as much as possible)

Large number of power planes (EMI & distribution)

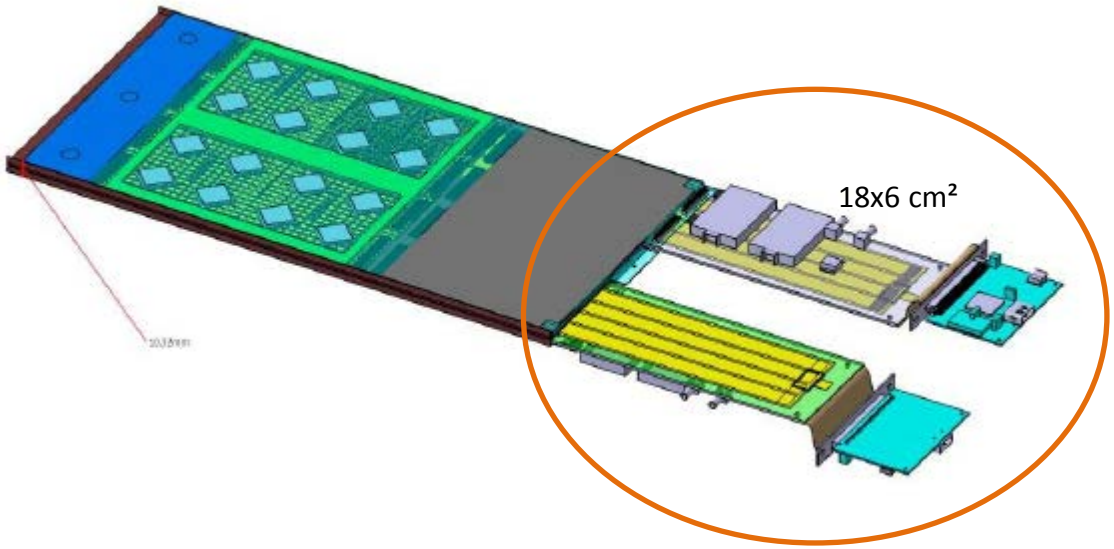
The FE board will implement two versions for the routing of differential signals:

- straight lines (needs 2 times more buffers & connectors)
- or snake line (more risky as it maximizes load but optimize power and connectors)



Boards and packaged chips are received

Next steps for SLAB

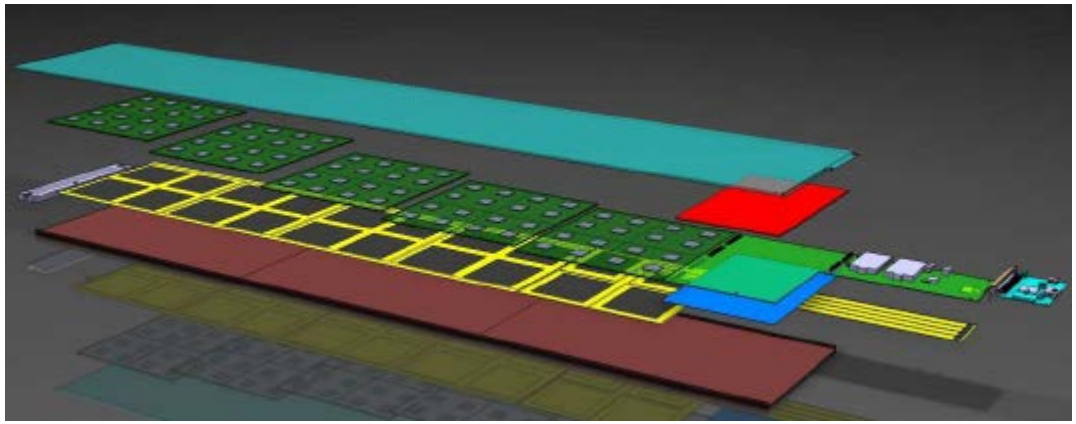


Have to work on front-end board:

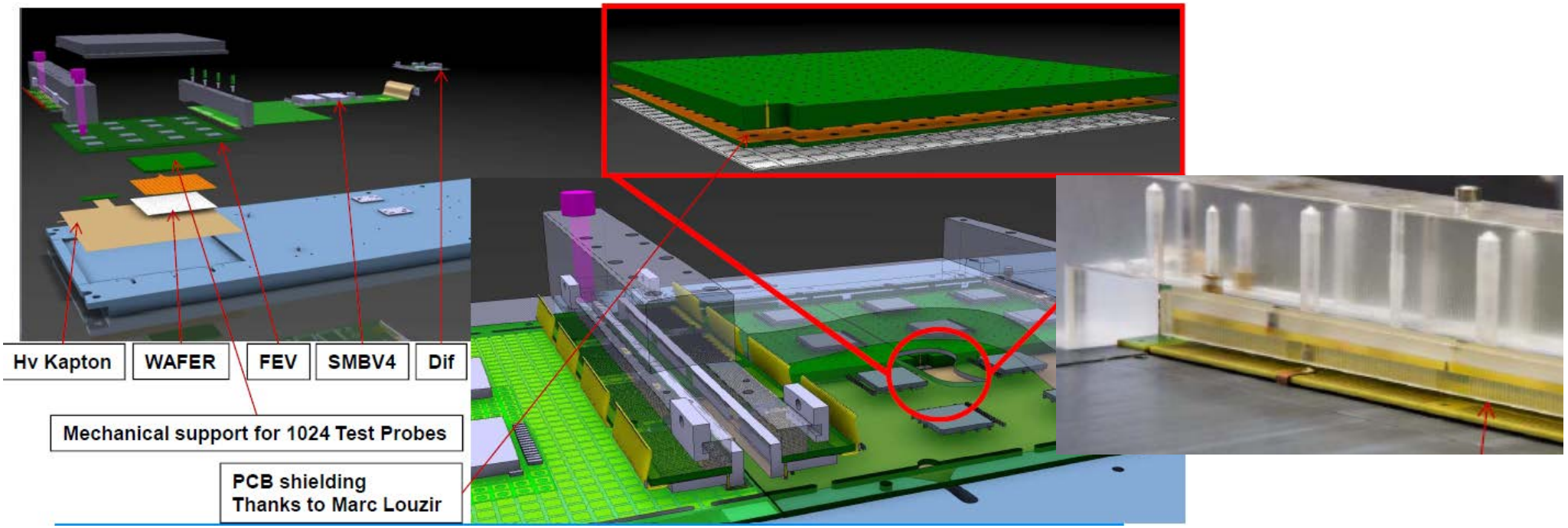
- Power supplies (regulators, sequencing)
- Local power storage
- line drivers

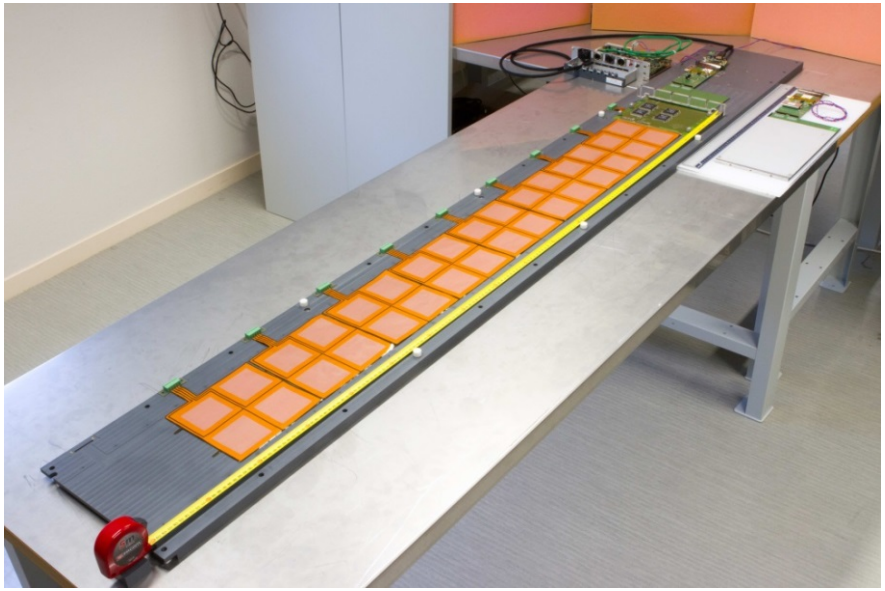
It is urgent for us to test long slabs:

- Up to 10-12 ASUs long
- Complex transmission line
  - Loads, stubs and connectors
  - 160 chips / SLABs !
- Power distribution
  - 12A peak power !
- Maintenance ?
- Test bed ready



Example of tools



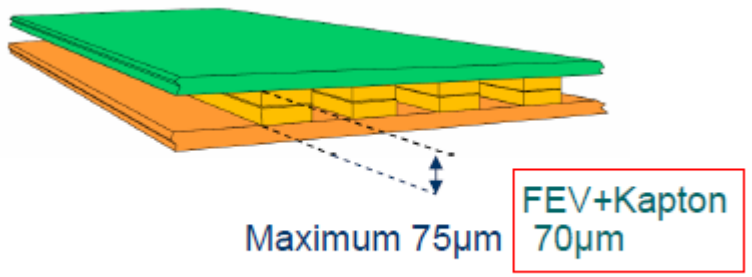


Designing tools is also an R&D task

- Integration of spring-contacts
- Alignment at 10µm precision
- Glue deposition…

Long SLAB assembly

A detector SLAB can be madeup of up to 10 PCBs

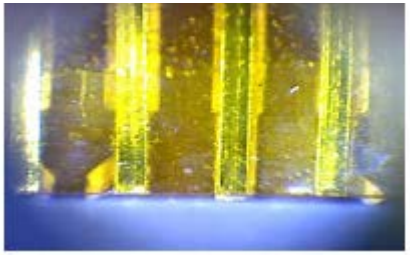


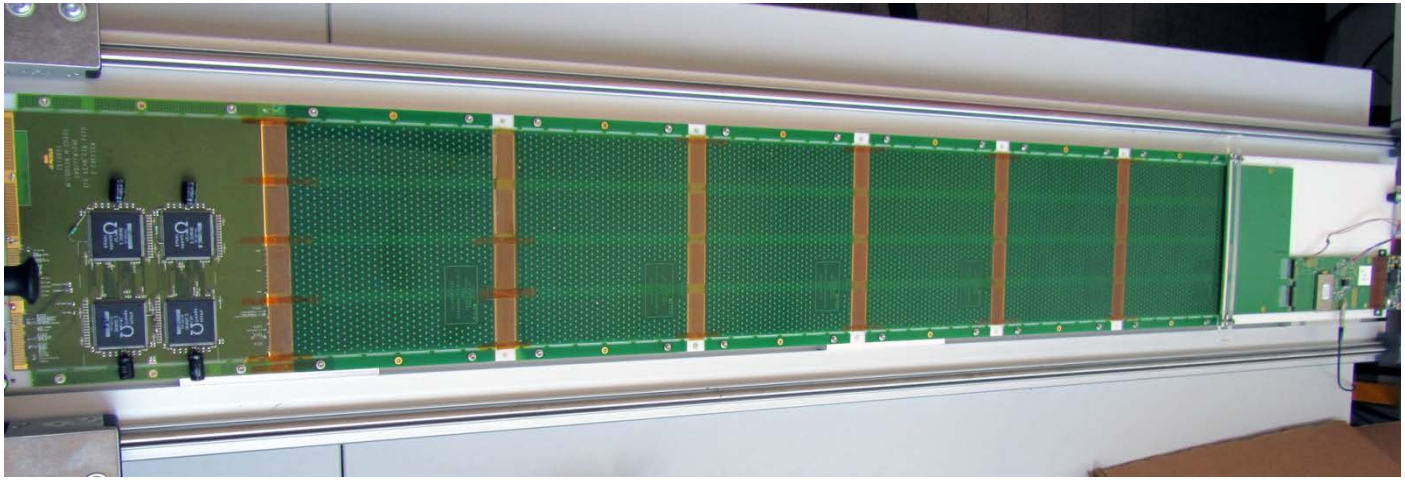
Electrical and mechanical connection made thanks to Kapton flat flexible cable

- Easy for mass production

Challenge:

- Impedence matching for transmission lines
- Power distribution: 12 A peaks along the SLAB





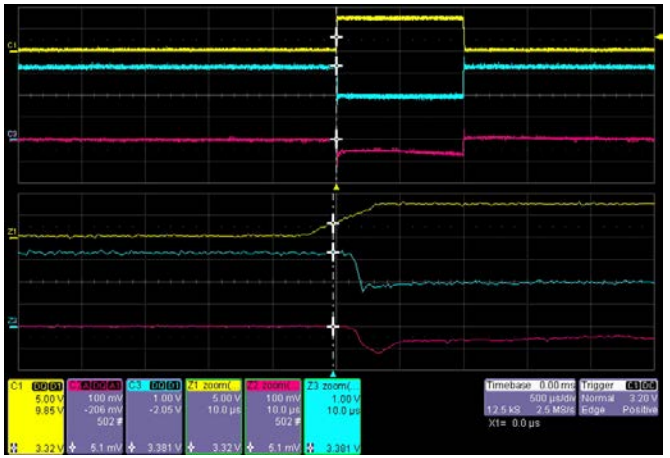
Full size kapton for interconnects

18 cm, 4 slots of 36 pins each

Long Slab : power pulsing

Current pulses from few 100 mA to several A (~10 A), Voltage remains constant (hopefully)

- 1st option : Battery or huge capacitance : few mF to few 100 mF, regulator (actual design) : worked fine in test beams
- 2nd option : current source (charge pump) with regulated voltage output (~mobile phone charger) : ok (test bench)
  - Allow poor power distribution network
  - Power pulsing only



Command : 1% duty cycle
Output : 6 A@3.3V, 1 ms, rise=1 us
Vout undershoot : 100 mV

Tested in 2T B field (pedestal run)

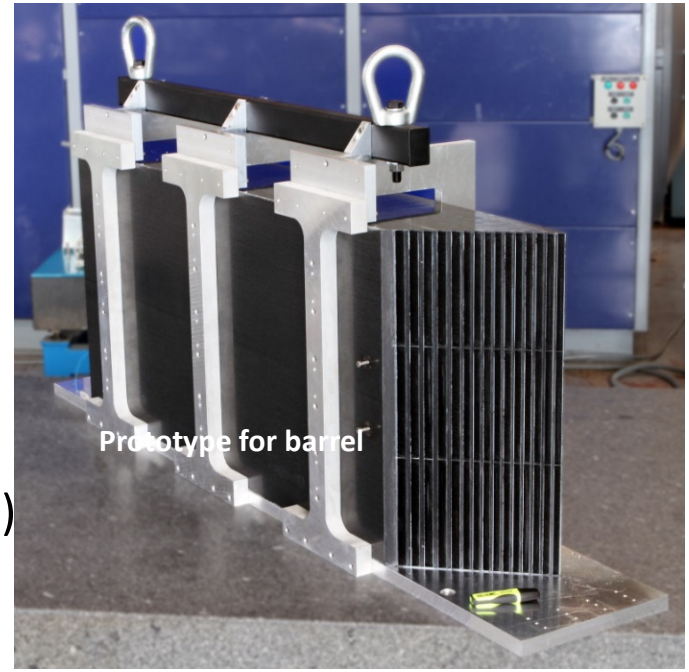
- similar behavior than in constant power mode
- No more decoupling caps on chips references
- Connectors stress test: OK

Large mechanical structure done

Tungsten plates wrapped into carbon fibre: 15 layers, 800 kg

Each layer build separately then “cooked” together.

Deeply simulated : mechanical constraints, thermal behavior

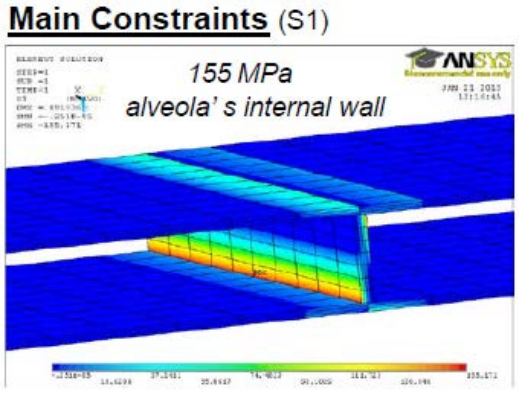


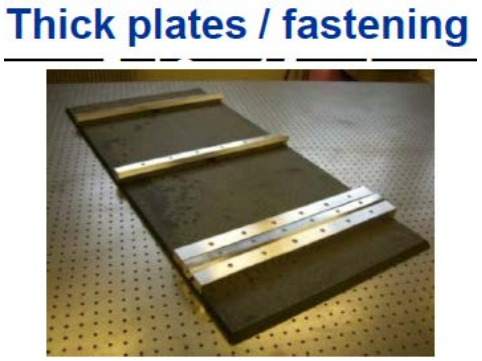
To be continued:

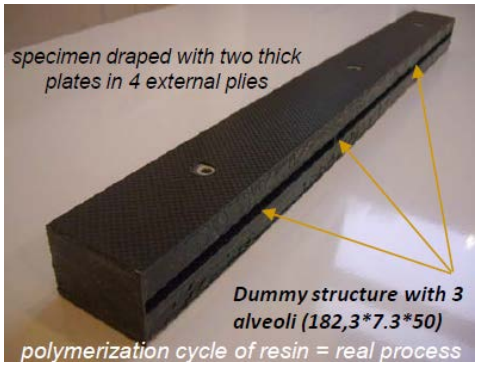
- End-cap design
- Simulations: bending stress, mechanical resistance
- Tools (moulds) & prototyping (samples for destructive tests, …)
- Optimization vs. physics requirements (« fill factor », dimensions…)
- Production of long slabs structures

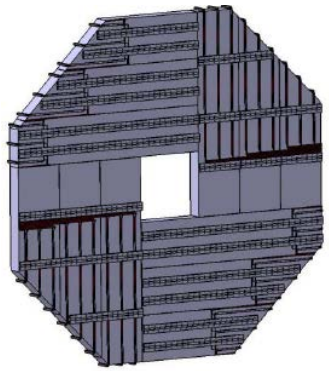
SLABs up to 2.5 m long

To be optimized.







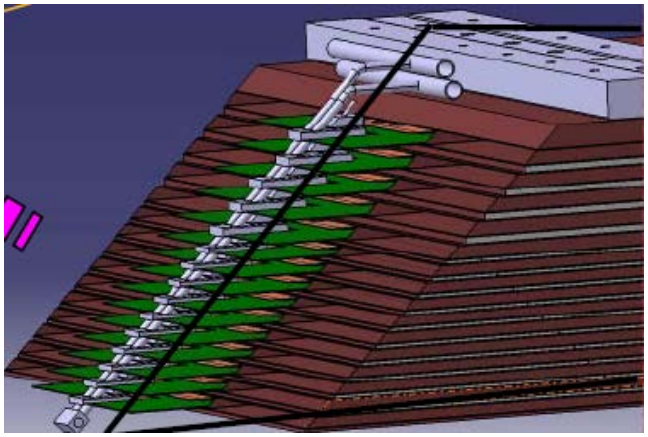


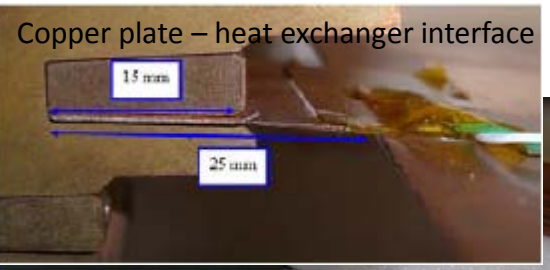
Developing a leak-less water cooling system

Total ECAL power dissipation O(10 kW)

Needs active cooling system (cold water pipe + radiator)

Limits: temperature differences within ECAL
heat transfer to neighboring detectors
integration





Cooling tests in demonstrator module

Results

Barrel : (1.5m)

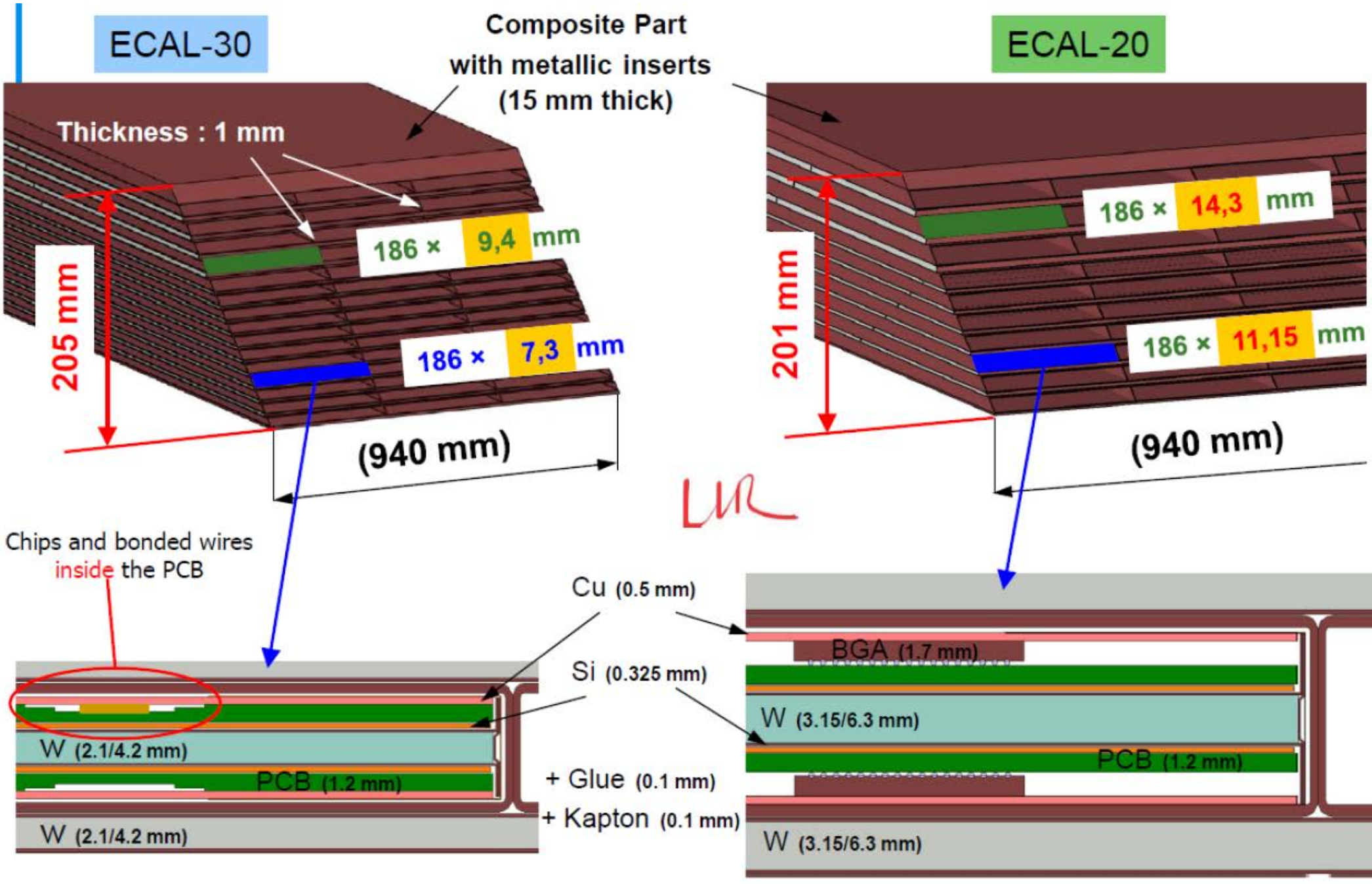
ΔT = 2,2℃

End Cap : (2.5m)

ΔT = 6℃

Thermal simulations of detector

Example of optimization study



DAQ : hardware and software

Scalable : Computing network architecture
Standard : Giga-Ethernet, Serial 8b10B
Backplane-less

Compact

– "one cable for everything"

Data Acquisition, Timing, Slow control

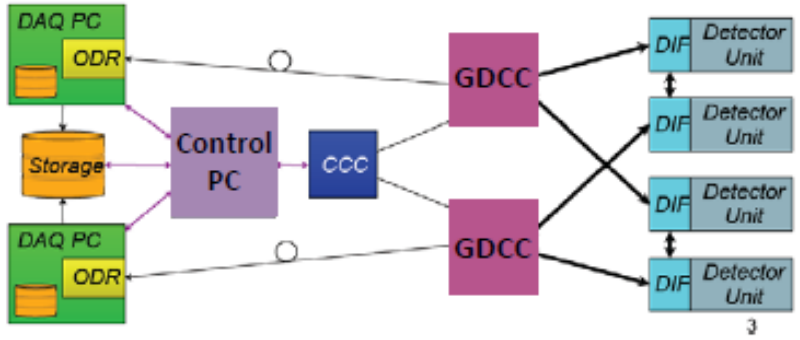
GDCC

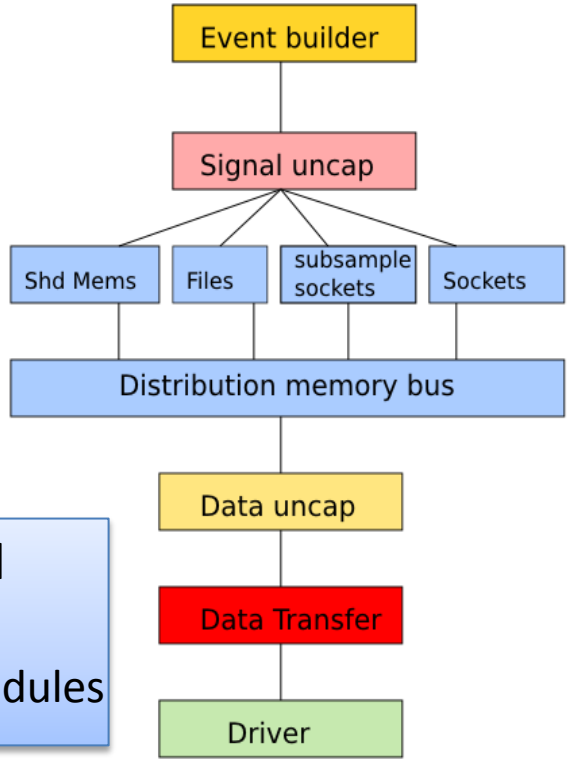
DCC

Flexible and highly modular software
C++ core
Python for scripting
XML for configuration and interoperability
Multiple output formats
- Files (offline)
- Shared memory (online H. Perf)
- TCPSockets (remote online)
- Subsampling (real time processing)

(**Detector Unit** : ASICs)
DIF : Detector InterFace connects generic DAQ and services
GDCC : GigaEthernet Data Concentrator Card

ODR : Off-Detector Receiver is PC interface
CCC : Clock and Control Card fans out to ODRs (or LDAs)

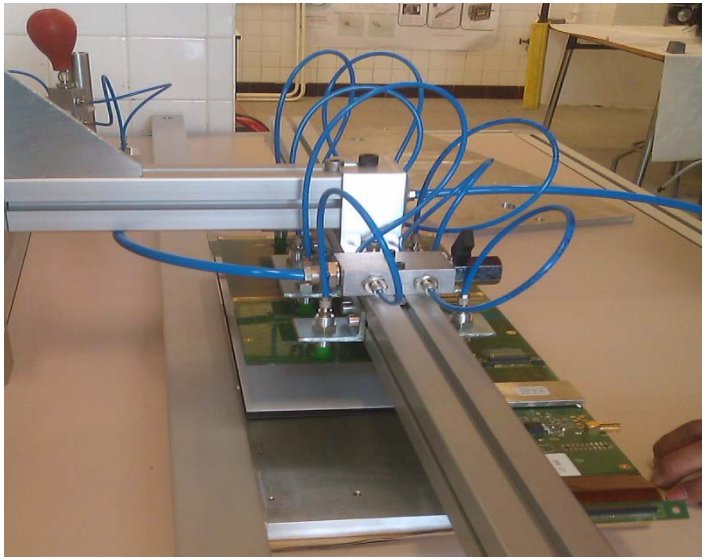


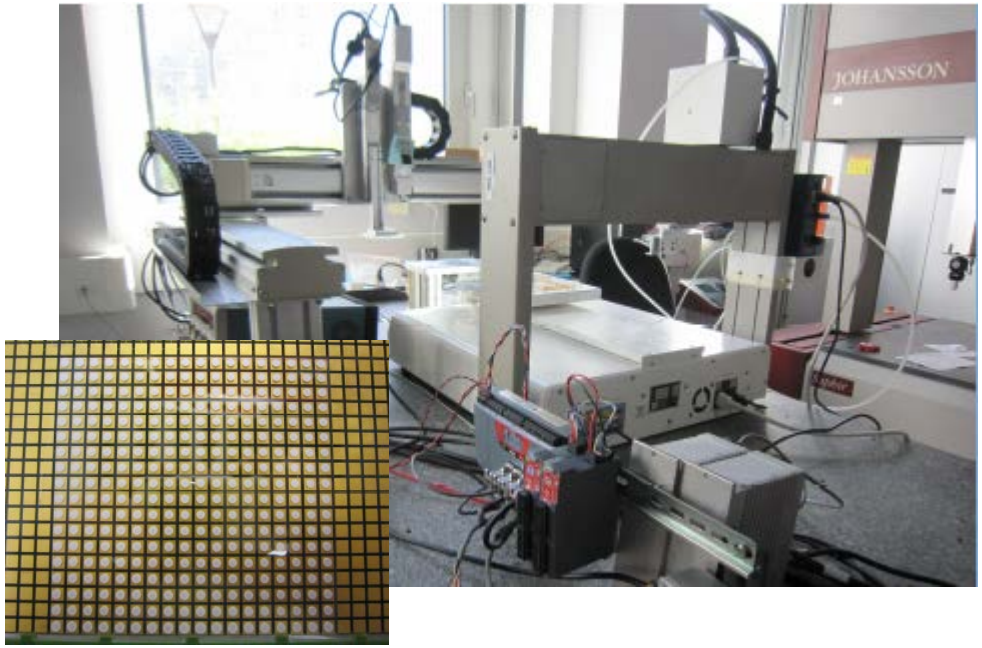


Used for test beams and
Test setups at lab
Scalable to ILC detector modules

Assembly of first SLABs

First approach of an assembly procedure toward automation and industrialization



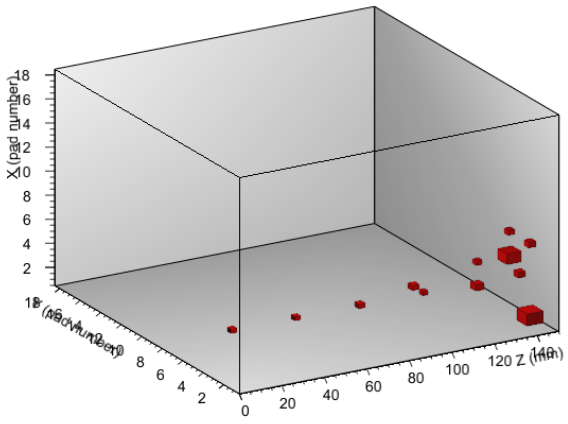


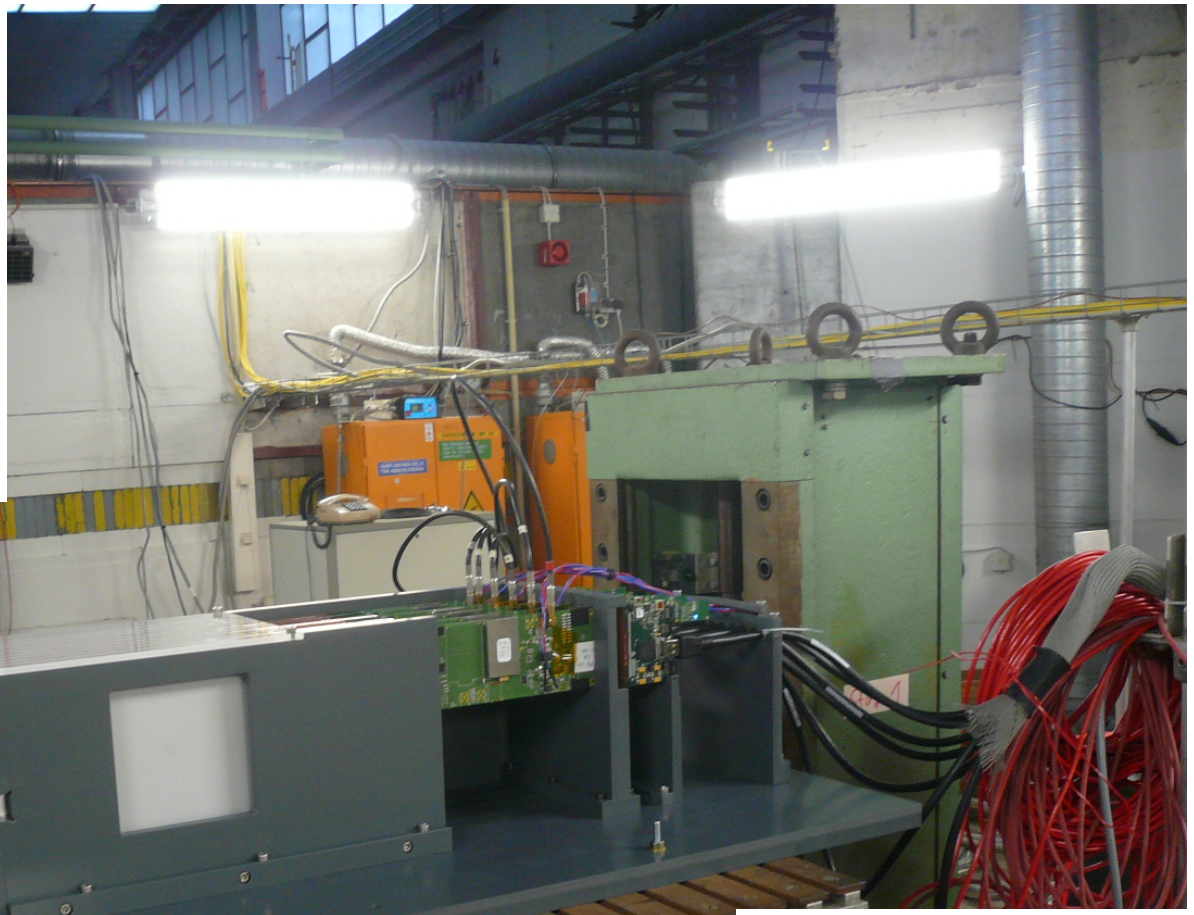
Gluing and positioning robot

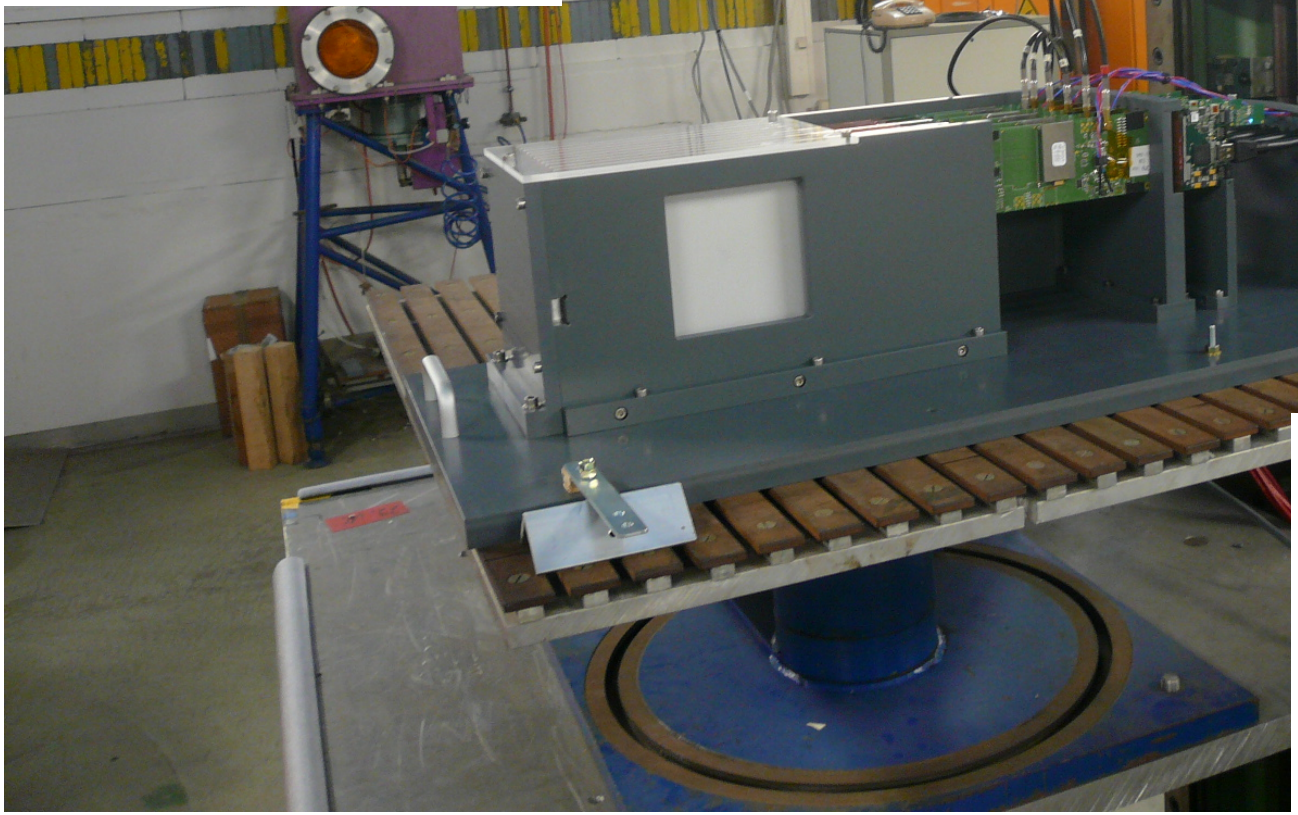
Process is well under control

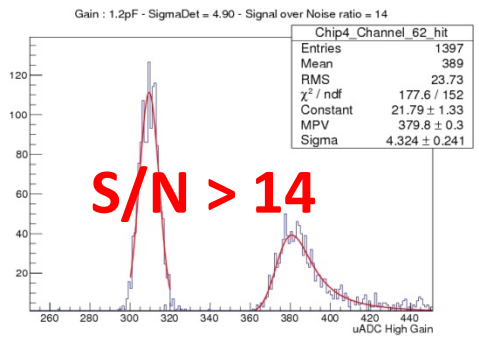
First SLABS tested @DESY (2012-13)

See next talk







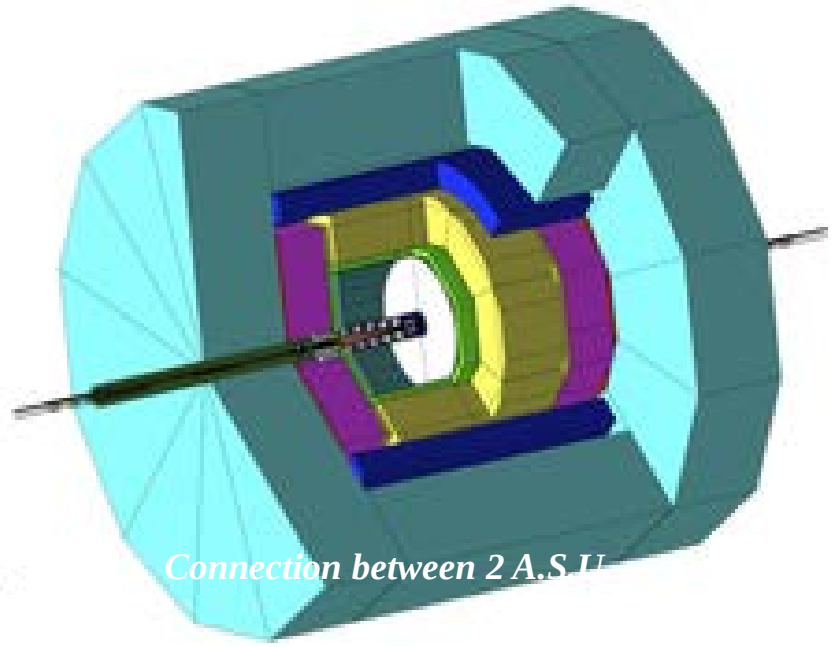


Summary

Step by step prototyping towards the best feasibility/cost compromise

- Low cost (expected) & industry standards
- Feasible (realistic, robust, ~simple)

as soon as **long SLAB** is proven to work (Q4'2014)

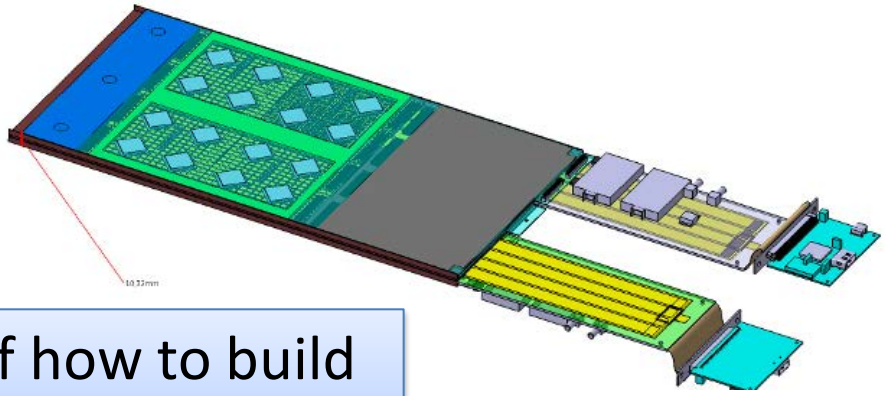


Some effort put on more advanced technologies

- Embedded chips
- SOI chips
- Tooling

Optimization of overall design based on accurate physics simulations

- Number of layers
- Number of pixels
- Dead area
- Allowed material



Now have an acceptable understanding of how to build a complete ECAL with affordable technologies