Beam Test Performance of the SiECAL Technological Prototype

LCWS13 Tokyo

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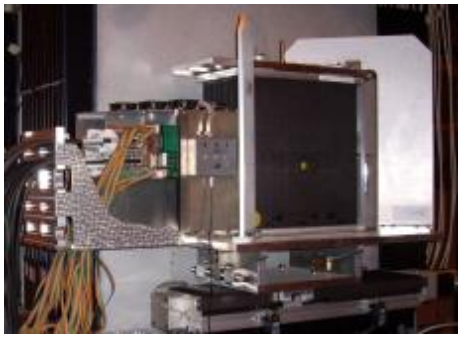
on behalf of the CALICE collaboration

SiW ECAL R&D

Physics Prototype

Proof of principle

2003 - 2011



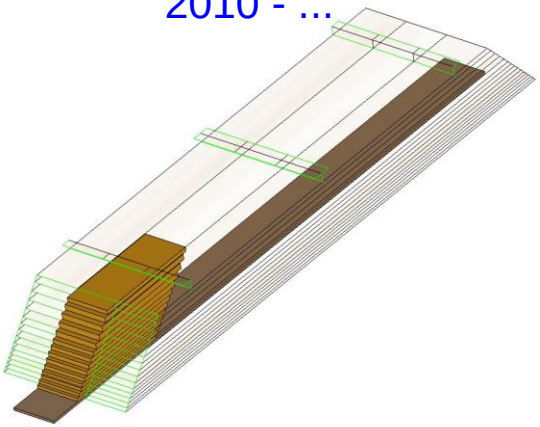
Number of channels : 9720

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

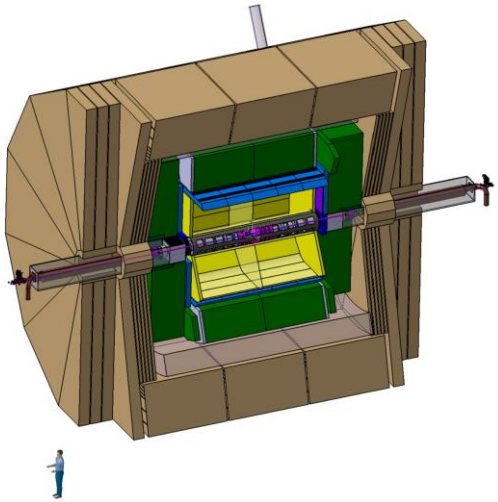
2010 - ...



Number of channels : 45360

Weight : ~ 700 Kg

LC detector



ECAL :

Channels : ~100 10^6

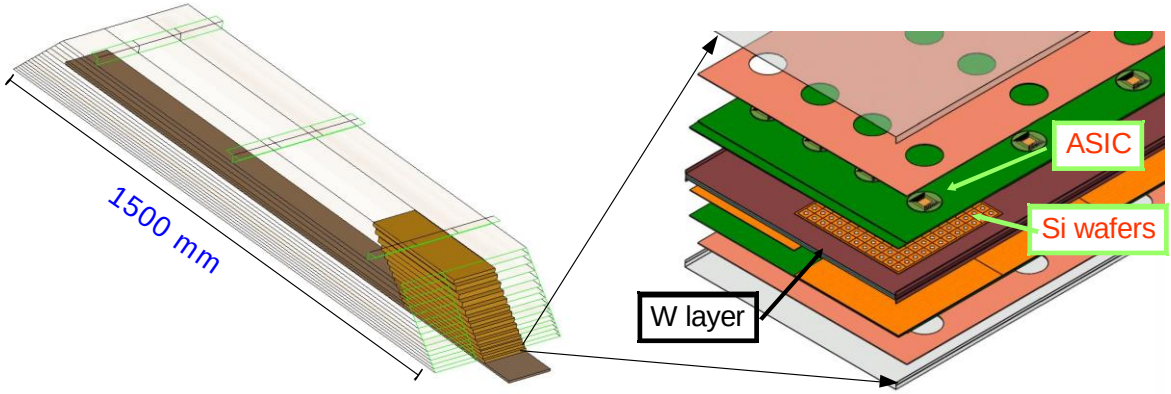
Total Weight : ~130 t

Technological Prototype

Technological solutions for the final detector

Construction start: 2010

Test beam: 2012

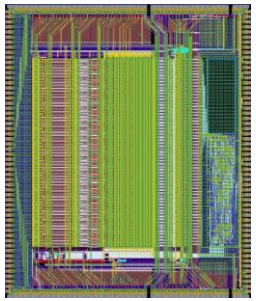


- Realistic dimensions
- Integrated front end electronic
- Small power consumption (Power pulsed electronics)

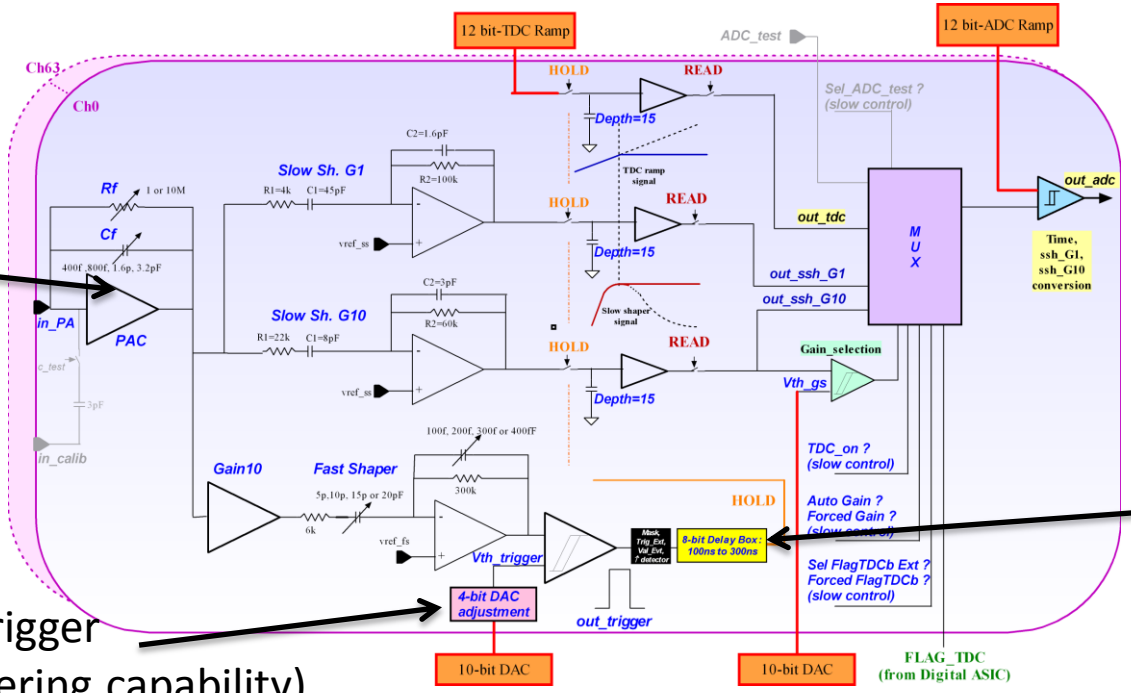
Front end electronics: SKIROC

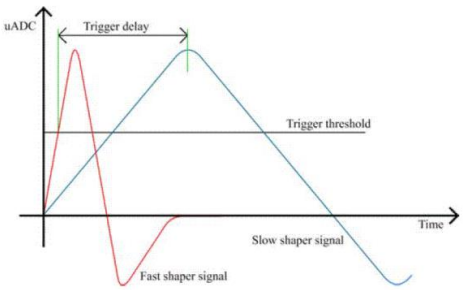
SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- Size 7.5 mm x 8.7 mm, 64 channels
- Variable gain charge amp, 12-bit Wilkinson ADC, digigal logic
- Large dynamic range (~2500 MIPs), low noise (~1/10 of a MIP)
- Auto-trigger
- Low Power: (25 µW/ch) power pulsing



Preamplifier





Trigger delay

Internal trigger
(self-triggering capability)

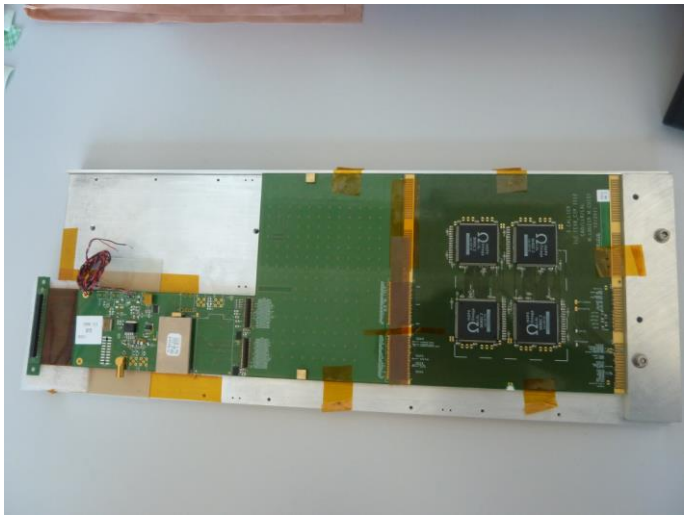
Test beams with fabricated layers

Layer design for beam tests

Integrated FE electronics

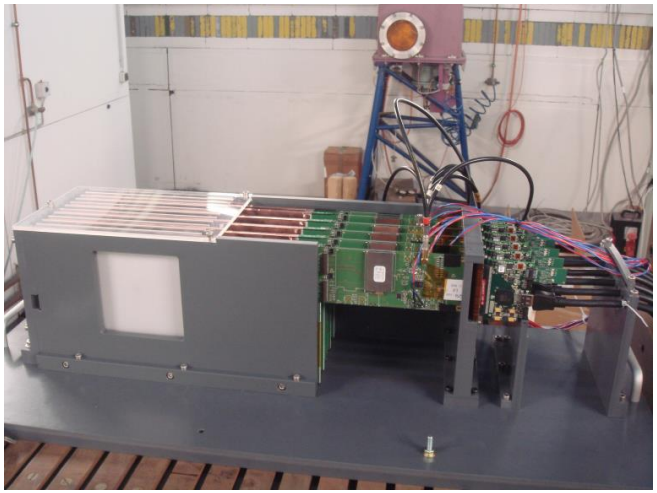
Conservative ASU design for beam test

- 1 Si Wafer with 256 pixels of 5x5 mm2 and thickness of 325 µm
- Wafer glued onto PCB
- 4 ASICs in PQFP package
- Up to 10 layers

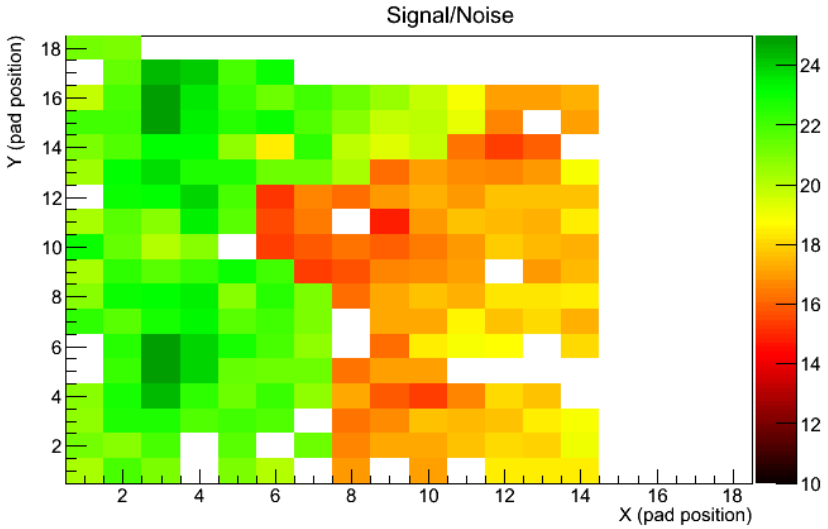


Test program

- 2012: Commissioning
  - Test of highly integrated electronics in continuous power mode
- 2013: Test of power pulsing
  Test in magnetic field

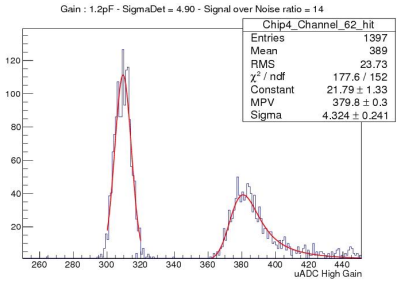


Data Analysis 2012 – Signal over Noise ratio

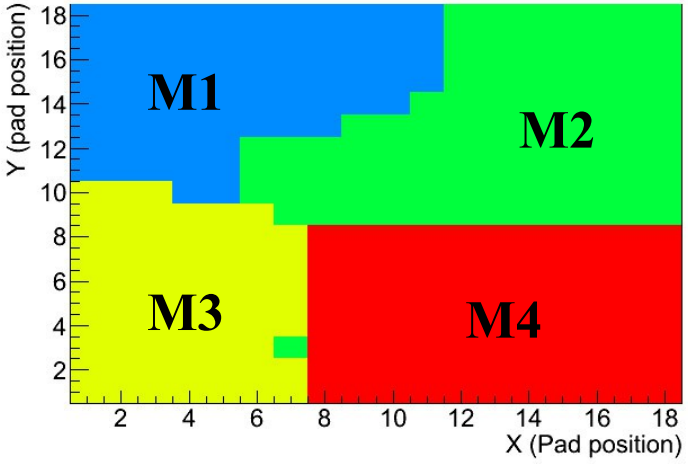


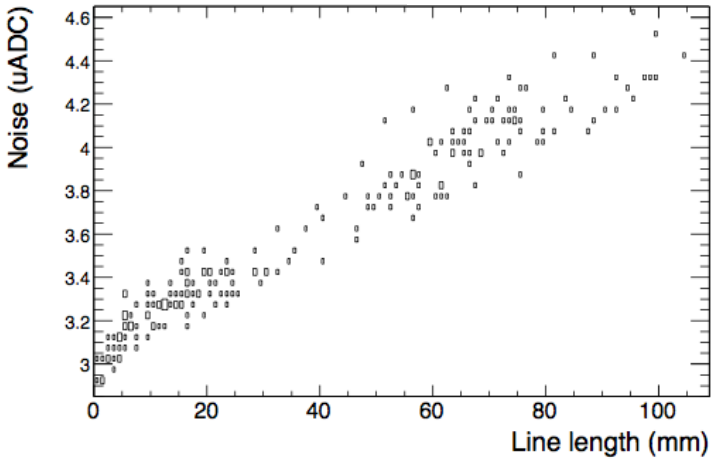
Results after setting of trigger thresholds and event filtering
White cells (noisy channel) : high threshold
Correlation between noise and PCB routing

S/N > 10 (for all gains available with SKIROC2)
R&D target is S:N = 10:1



4 ASICs are mounted on a layer

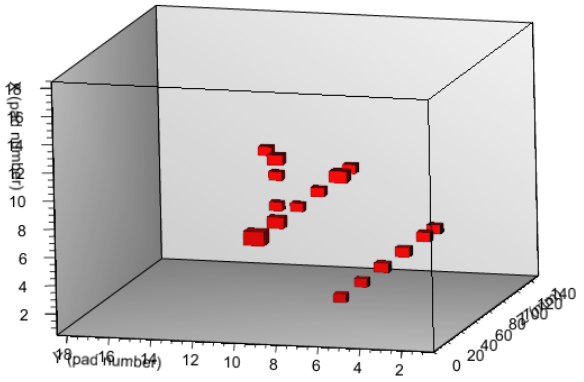




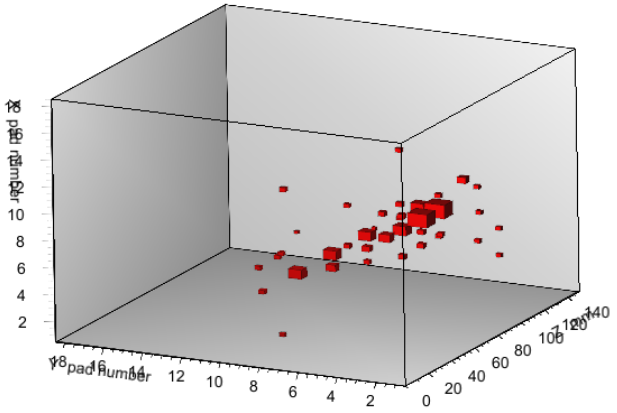
Line length of a channel to a leg of ASIC

Event displays

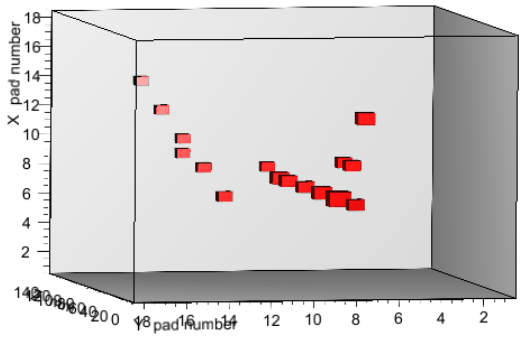
2 e- (3 GeV, no tungsten)



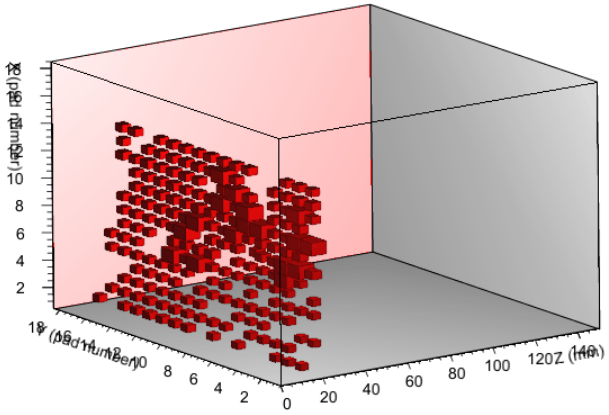
1 e- (5 GeV)
5 W plates between layers



1 cosmic + 1 e-
(3 GeV, no tungsten)

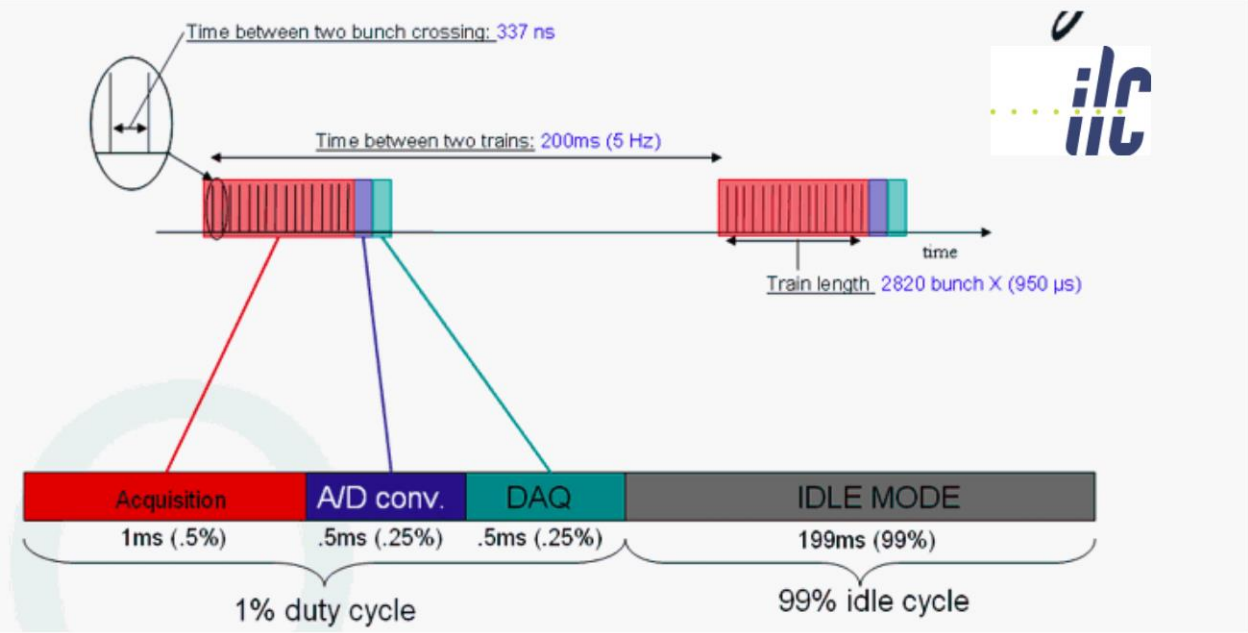


'Plane events???'



Plane events observed in 2012 with significant frequency
It can be remedied by correct PreAmplifier reference

Power pulsing



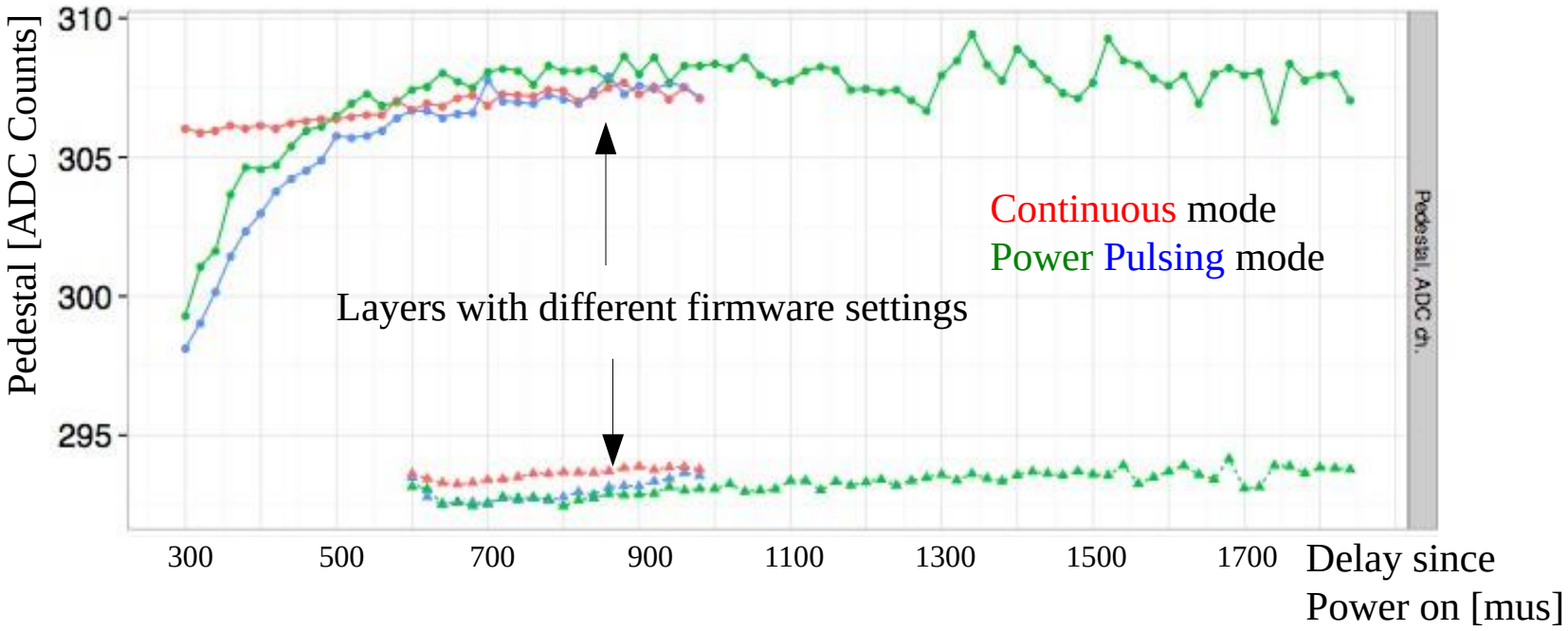
N.B. Final numbers may vary

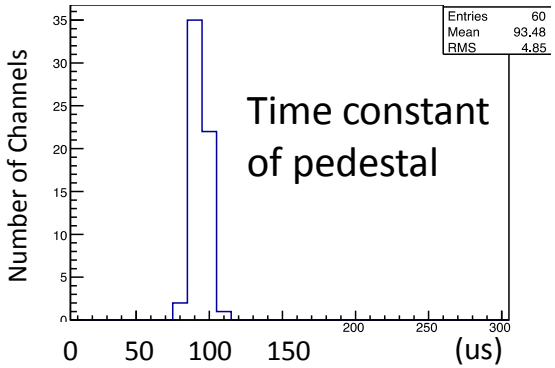
- Electronics switched on during a few ms: ~1 ms of ILC bunch train and data acquisition
- Low voltage of electronics are shut down between bunch trains

Mastering of technology is essential for operation of ILC detectors

Power pulsing – “ramp up” time

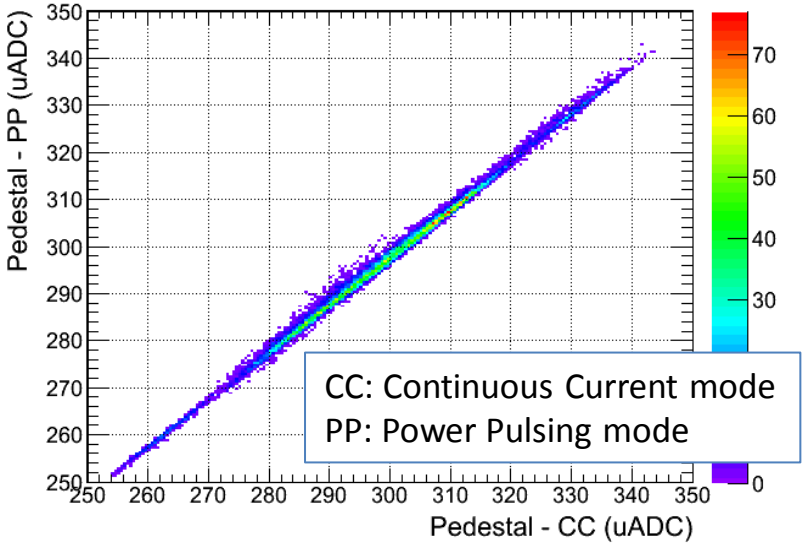
- Analysis of detector response as function of delay between enabling of bias currents and signal arrival

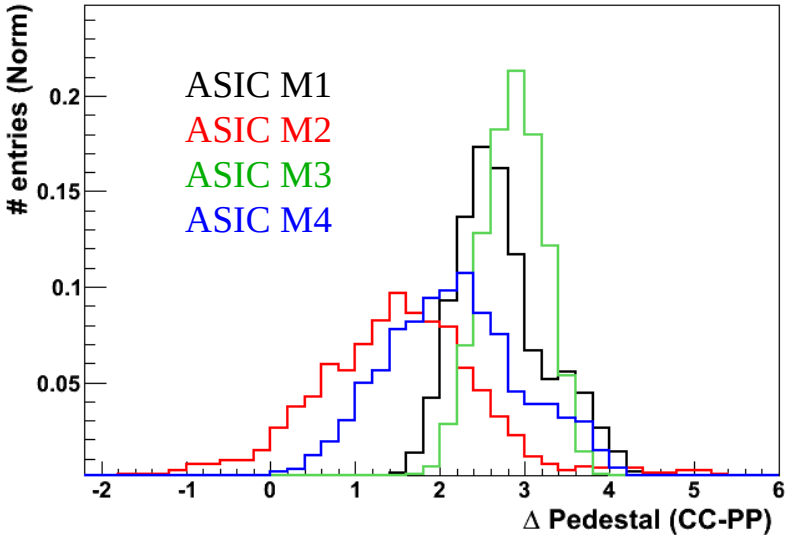


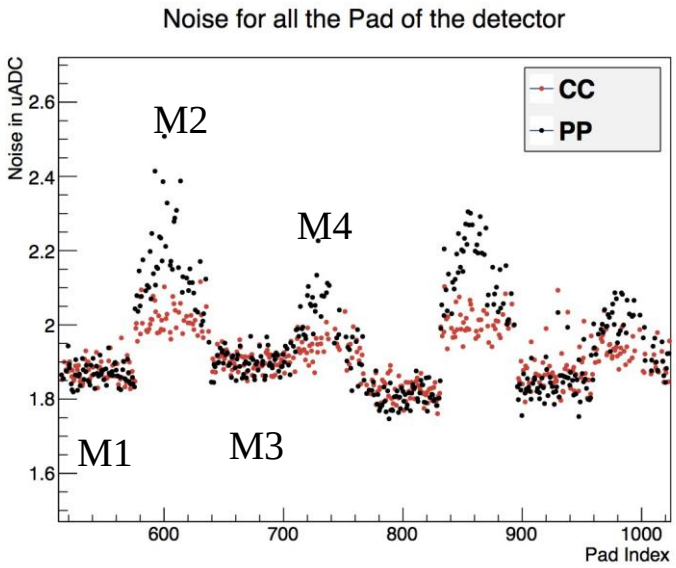


- Stable pedestal after around 600 µs
- Time constant of pedestal ~100 µs
- Time dependence of pedestal width under investigation

Power pulsing – Pedestal analysis







Clear pattern for ASICs M1, M3

Pedestal shift of ~1% in PP mode

Pedestal width constant

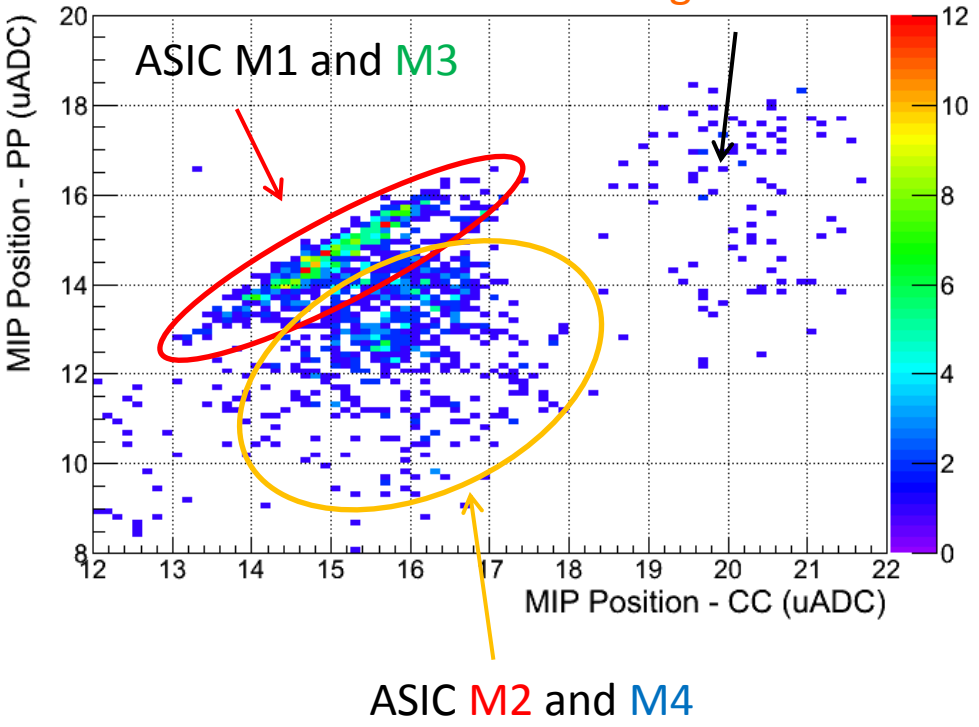
Less clear situation for M2, M4

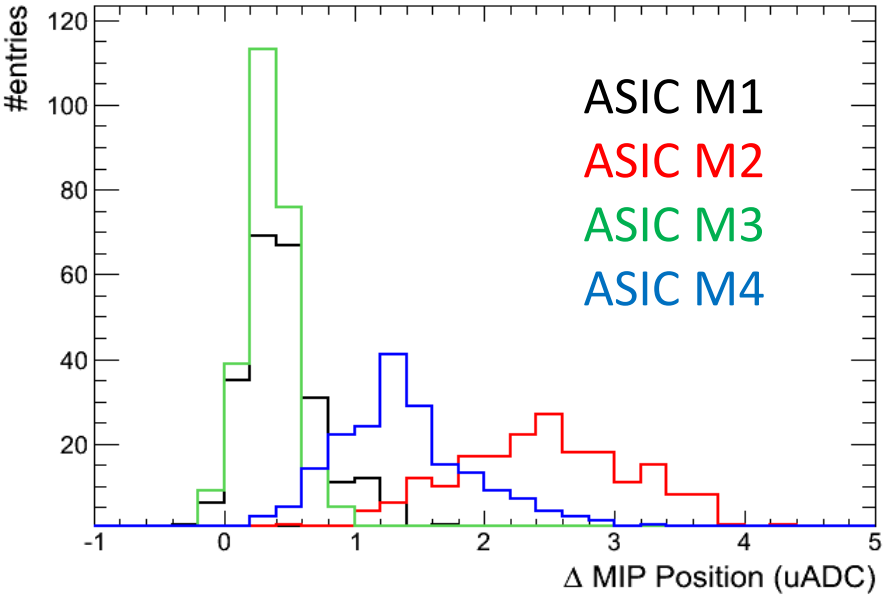
PCB routing seems to distort pedestal spectra

Power pulsing – MIP analysis

- Fit energy distribution: Landau convoluted with a Gaussian
- Sigma of the Gaussian is fixed to the noise

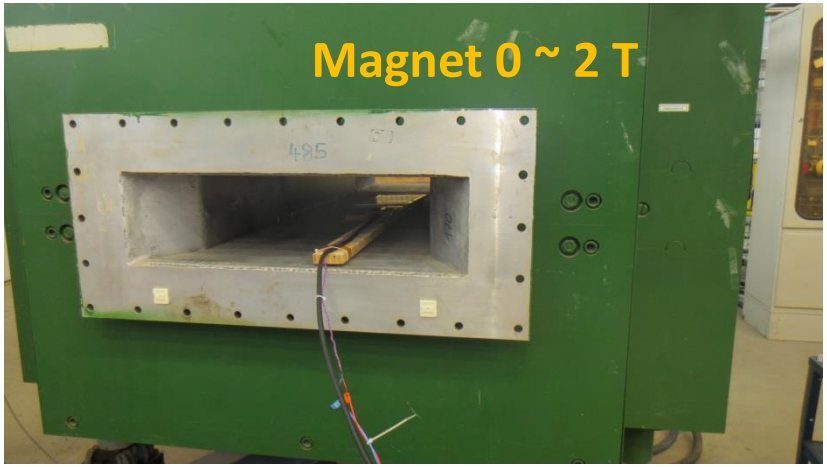
Trigger threshold
Too high

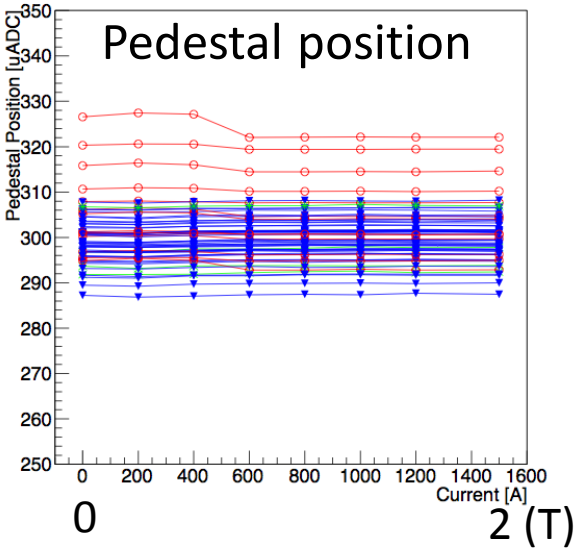


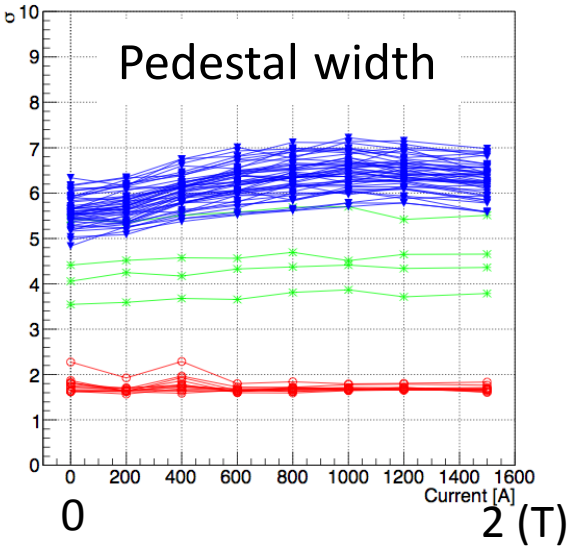


- ASIC M1 and M3 are ok under power pulsing operation.
- The activity of digital lines disrupts ASICs M2 and M4.

Power pulsing tests in magnetic field I

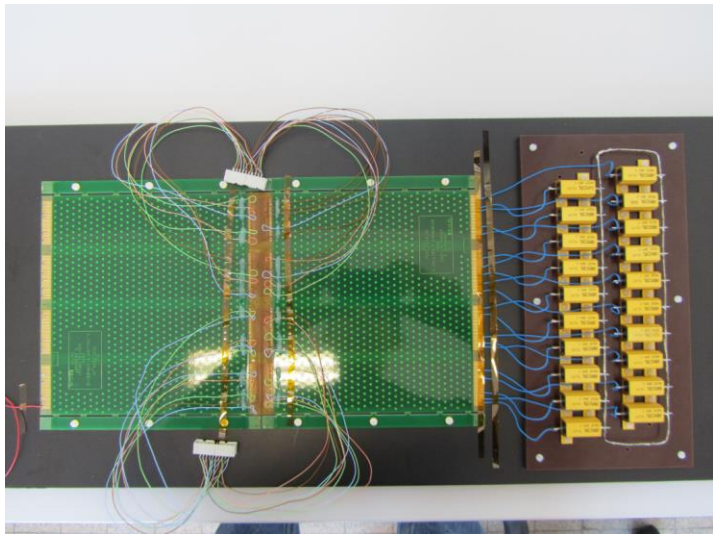




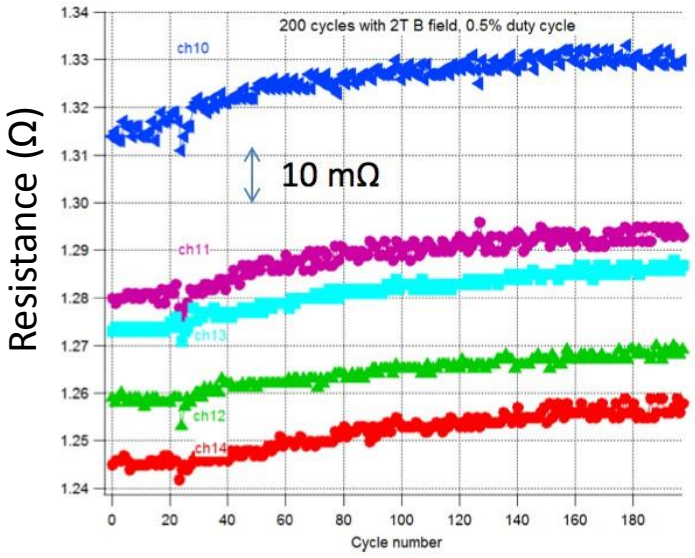


- Active channels are stable up to 2T B field

Test in magnetic field II



Measurement of the ohmic resistance across the interconnection between two ASUs
With and w/o B-Field, various duty cycles and frequencies



- The ohmic resistance varies by about 20 mΩ (thermal effect)

Conclusion and outlook

- Since beginning of 2012 SiEcal R&D is running at full speed

- Four beam tests with conservative but yet progressively complicated setup
  Detailed evaluation of performance of system
  A number of observed odd behaviors were actually related to peripheral devices or non optimal power supply
  Self-triggering ASICs require very careful power management

Power pulsing is full system issue
Satisfactory when ASICs properly connected
Less satisfactory in other case
Active channels are stable up to 2T B field

- Addressing now issues of a real calorimeter system

16 ASICs per ASU, up to 160 ASICs per layer
Next ASIC version
Long layer
Cooling
First ideas on industrialisation
Test in strong B field

Backup

Si-W ECAL DAQ system

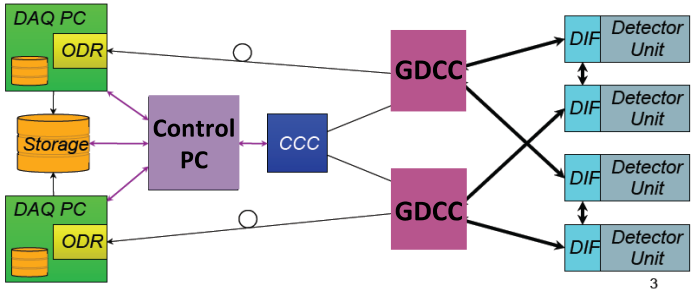
Standard: Giga-ethernet, 8b10b encoded local link, diff. pairs lvds signals over HDMI

Scalable: architecture of a computing network w/o routing, modular software configured using XML, scripted using python.

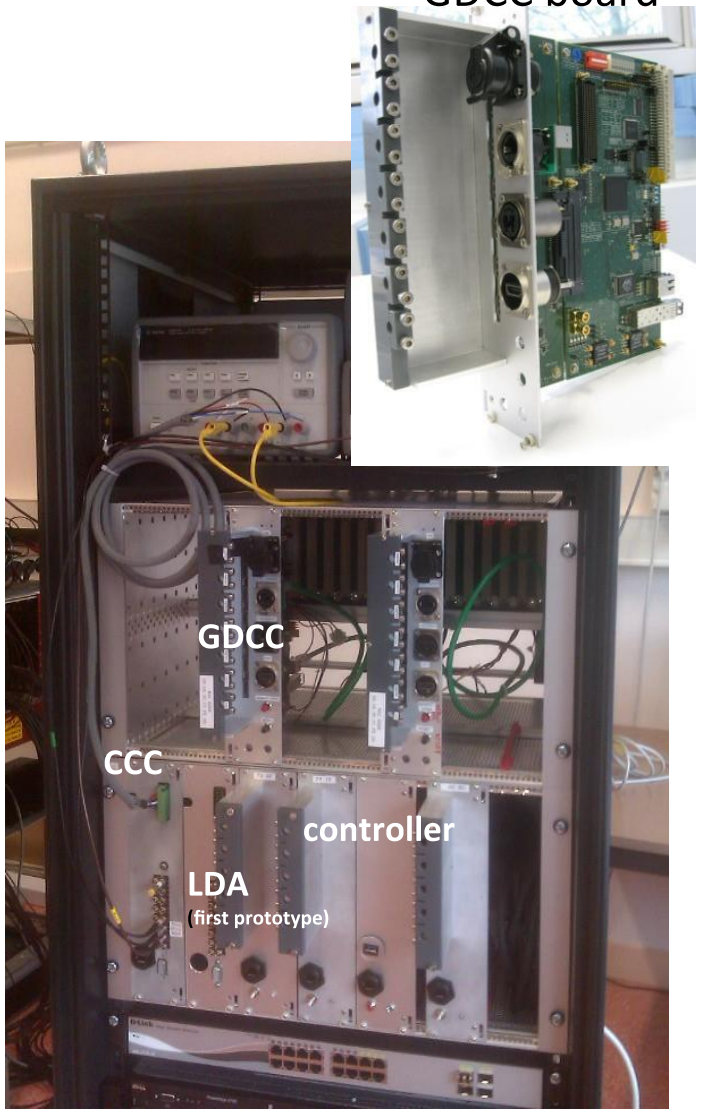
Compact: one cable for slow control, data acquisition, fast signals and possibly power

(**Detector Unit** : ASICs)
DIF : Detector InterFace connects generic DAQ and services
GDCC : GigaEthernet Data Concentrator Card

ODR : Off-Detector Receiver is PC interface
CCC : Clock and Control Card fans out to ODRs (or LDAs)



GDCC board

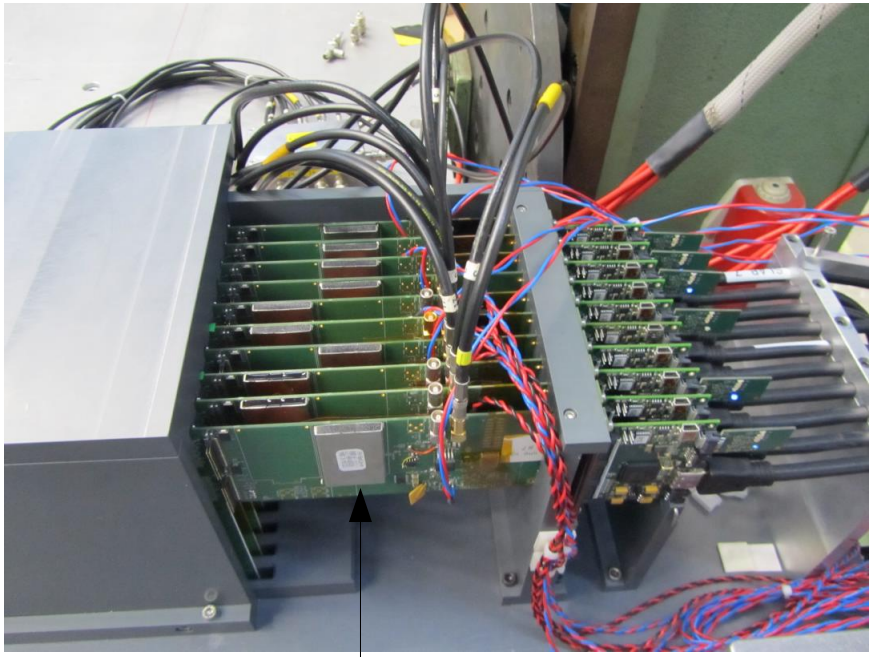


Scaled for low occupancy, low noise detectors featuring **auto-trigger & zero suppression at read-out chip level**. 40 Mbit/s link at detector interface allow to control & read 10k channels.

Central clock and control board (CCC) for overall synchronisation

Modular integration of components into 6U modules for use in test beams.

2013 beam tests



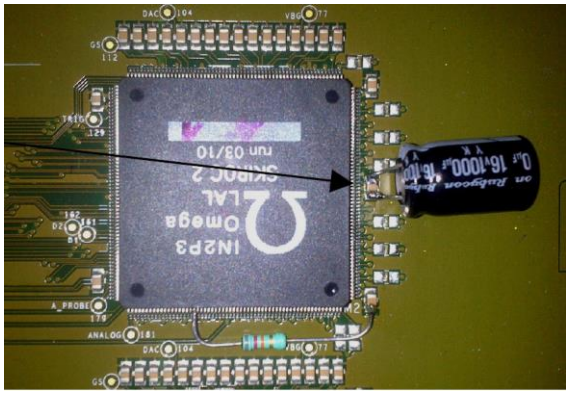
Battery charger application
AVX BestCap BZ01
After regulator

SKIROC integration defaults

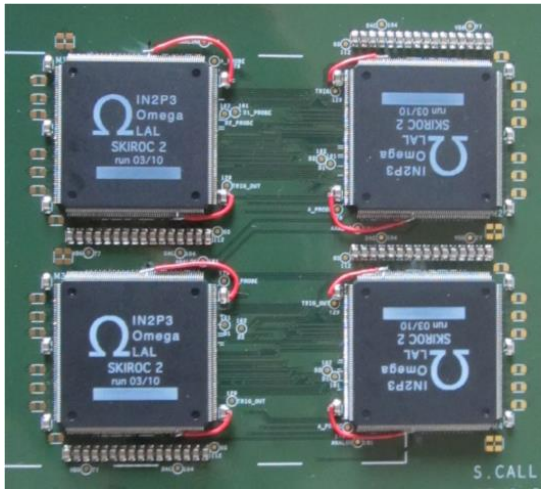
Pre Amplifier is referenced to the analog power supply level
Instabilities of power supply level → fake events

- Some analogue signals plugged on digital power supply → Noise at ASIC inputs
- Analog power supply common to the 4 ASIC
- Self-sustained → sometimes filled all the 15 ASIC memories
- Highly dependant of the number of ASIC with hits, dependant of the number of triggered channels

Patches

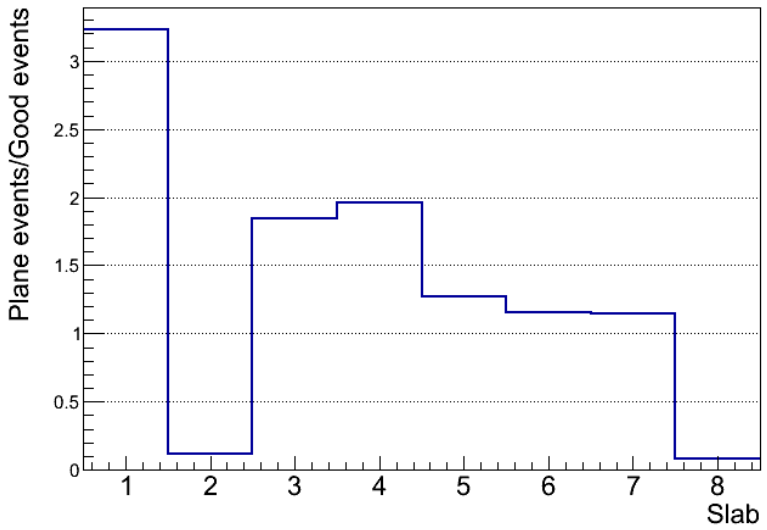


Big capacitance to stabilise power supply



Re-routing of analog and digital power supply

2013 beam tests first results



Frequency of plane events

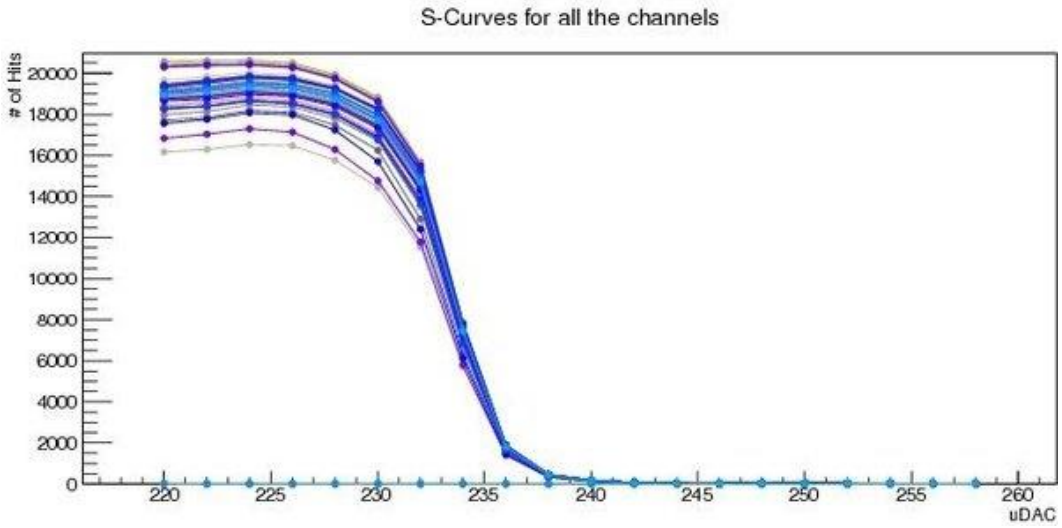
- Slab 2 and 8 were subject to patches
  - Smaller frequency of plane events observed
- However effects of retriggering are still under investigation

Calibration of ASICs

Establishment of calibration procedure for a larger number of cells

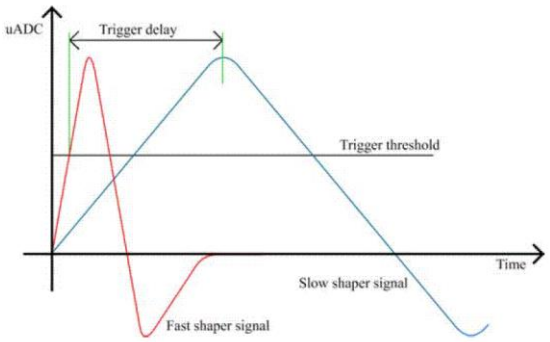
Trigger threshold

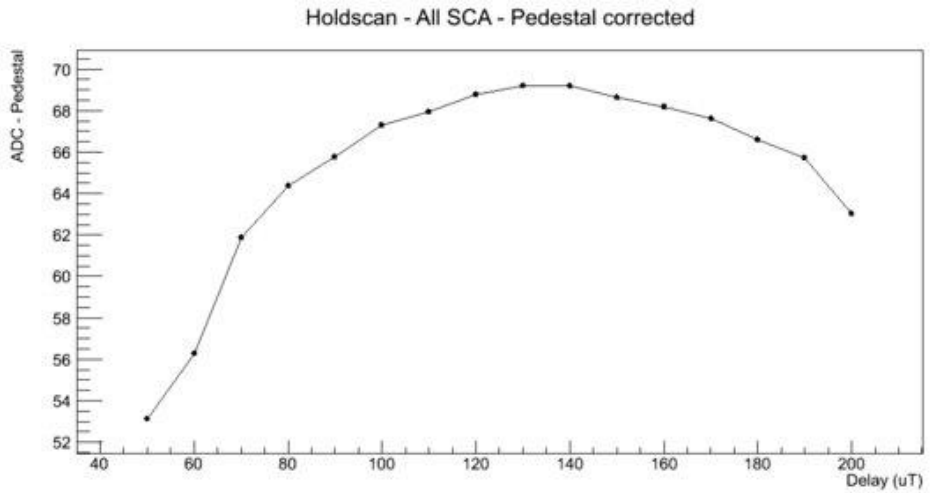
- depends on the gain



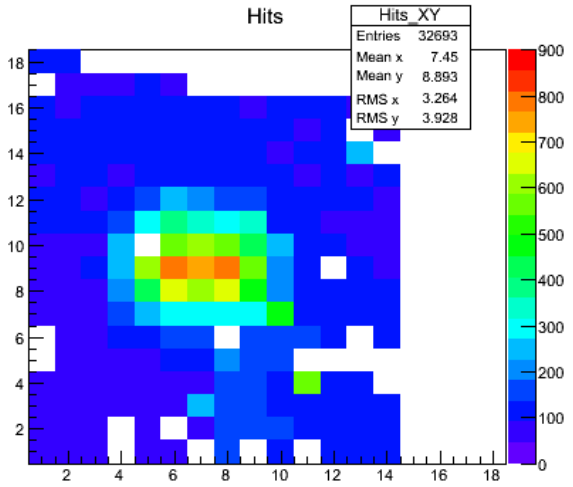
Trigger delay

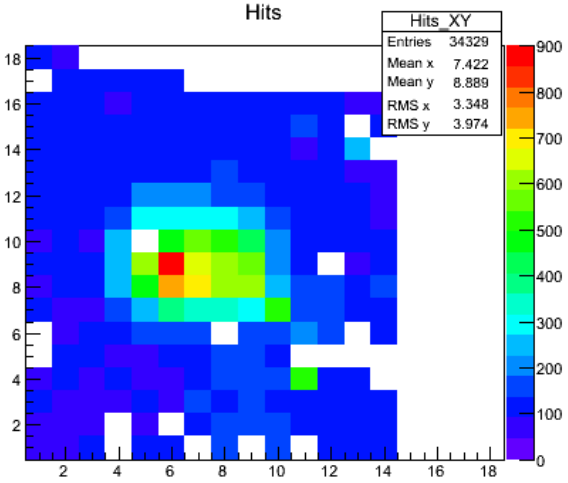
- depends on the trigger threshold

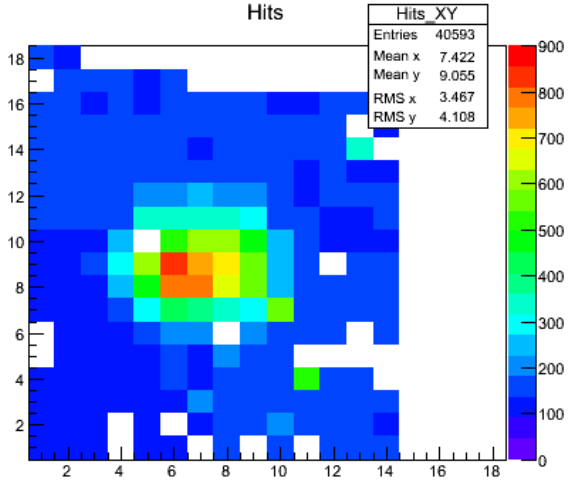


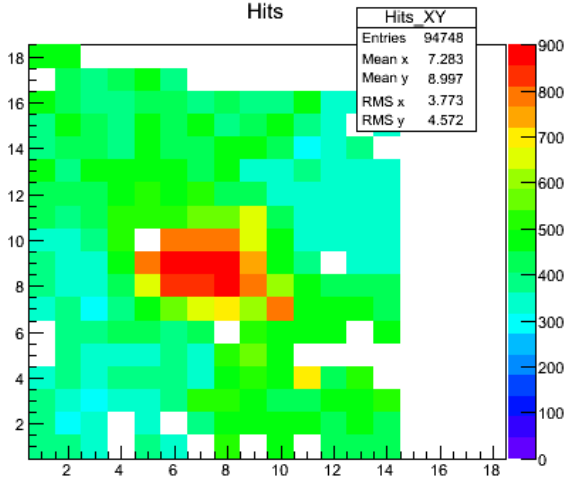


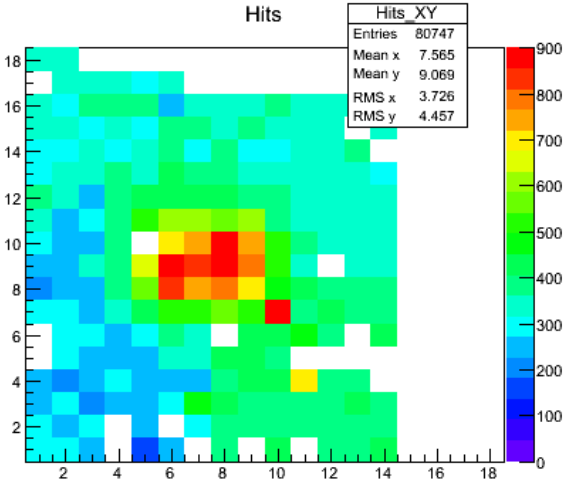
Beam spot

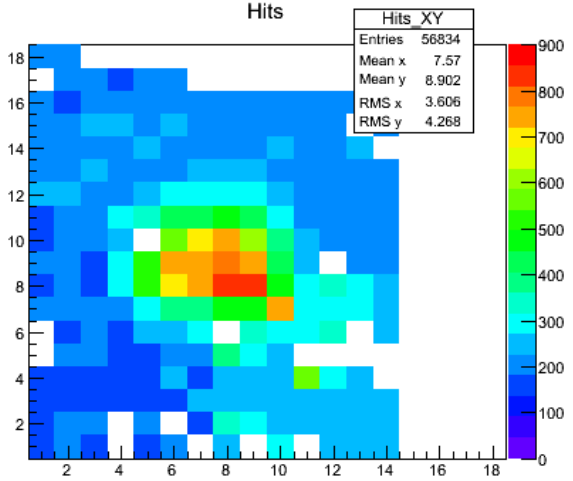

Hits
Hits_XY
Entries 32693
Mean x 7.45
Mean y 8.893
RMS x 3.264
RMS y 3.928


Hits
Hits_XY
Entries 34329
Mean x 7.422
Mean y 8.889
RMS x 3.348
RMS y 3.974


Hits
Hits_XY
Entries 40593
Mean x 7.422
Mean y 9.055
RMS x 3.467
RMS y 4.108


Hits
Hits_XY
Entries 94748
Mean x 7.283
Mean y 8.997
RMS x 3.773
RMS y 4.572


Hits
Hits_XY
Entries 80747
Mean x 7.565
Mean y 9.069
RMS x 3.726
RMS y 4.457

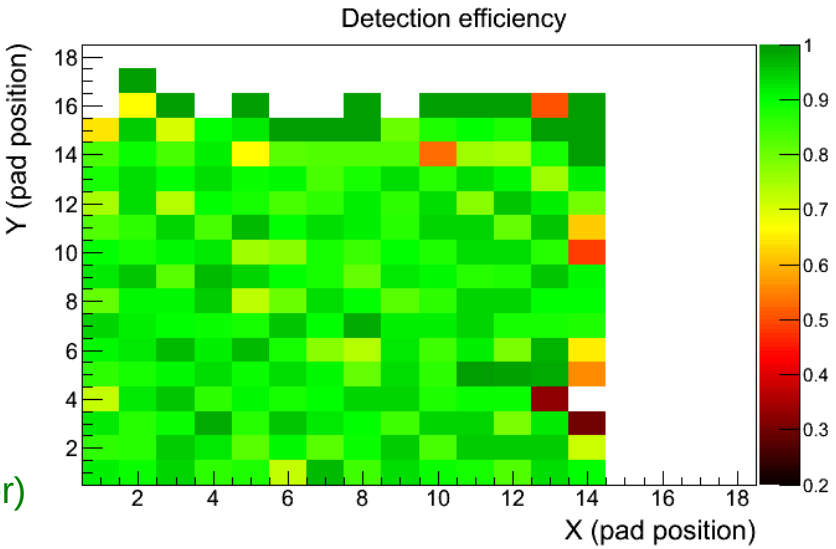

Hits
Hits_XY
Entries 56834
Mean x 7.57
Mean y 8.902
RMS x 3.606
RMS y 4.268

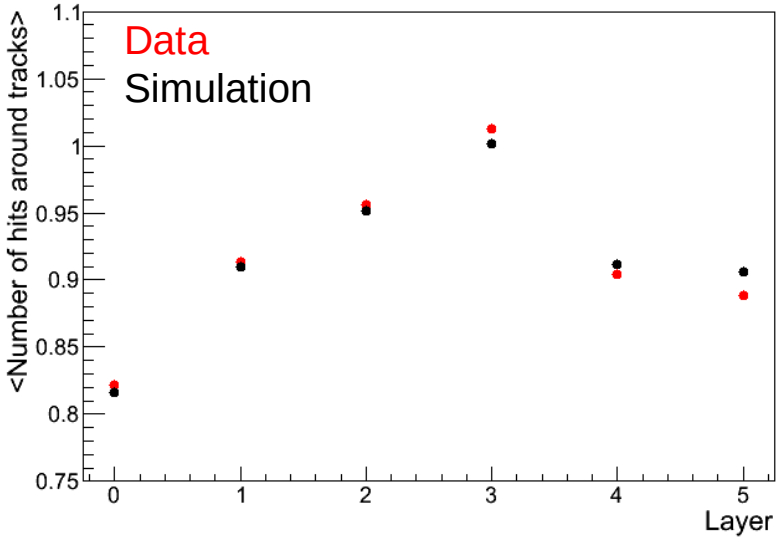
Detection efficiency

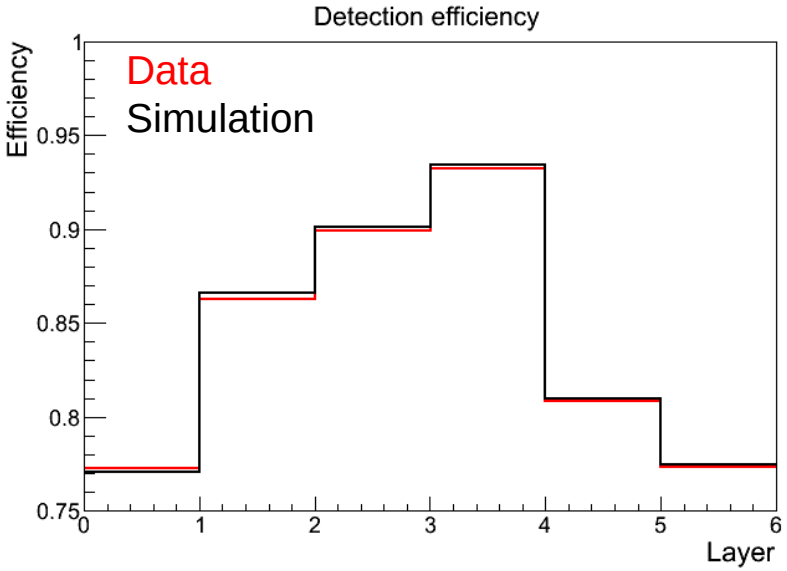
Data: 3GeV – No W – XY scan
Total number of events: 2,3.10^6
Track selection:

At least 3 layers with hits
Linear fit of the e- track
Nhits<10

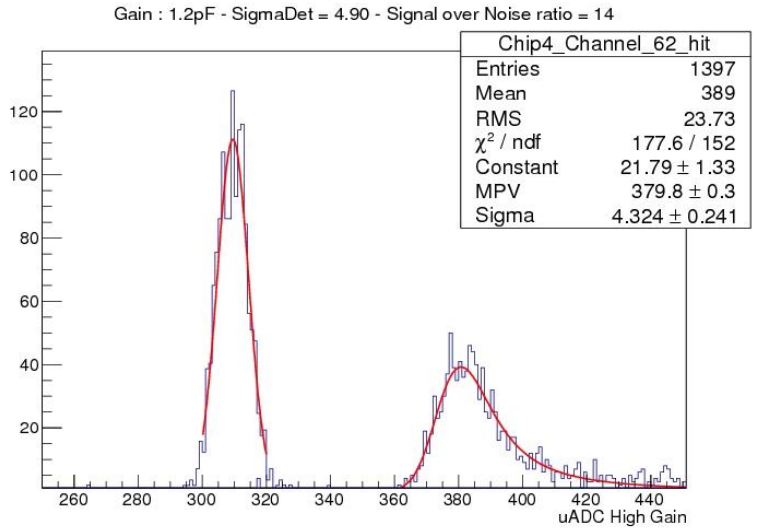
Inefficiencies due to:
Switched off channels
Too high trigger thresholds (80%-95% of the MIP)
➡ Should be improved with the next test beam (December)

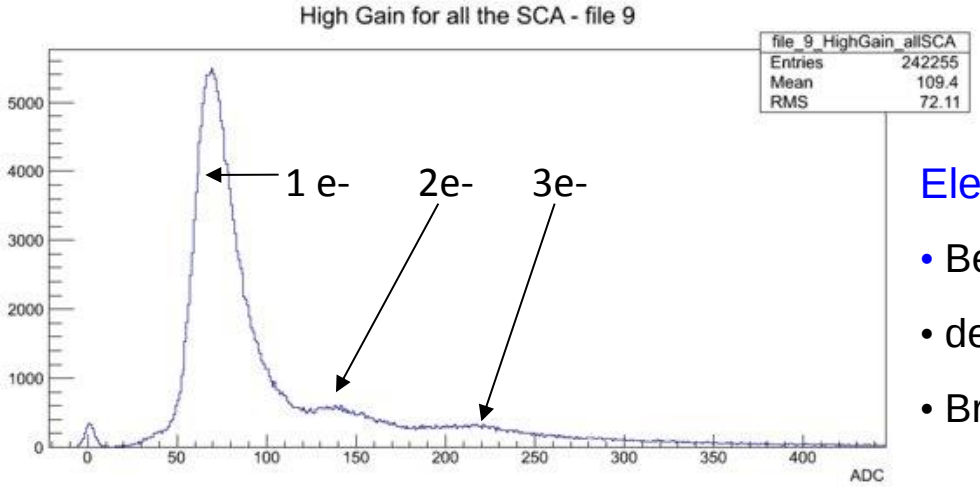






Energy measurement



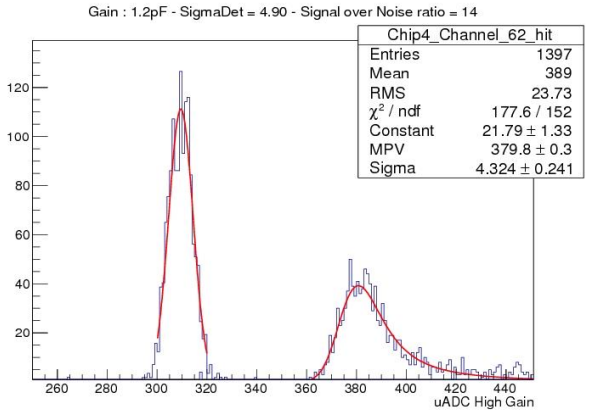


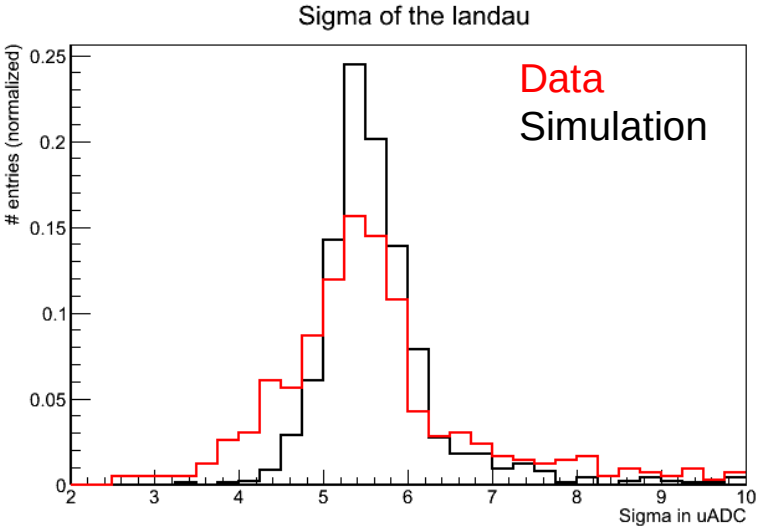
Electron sources:

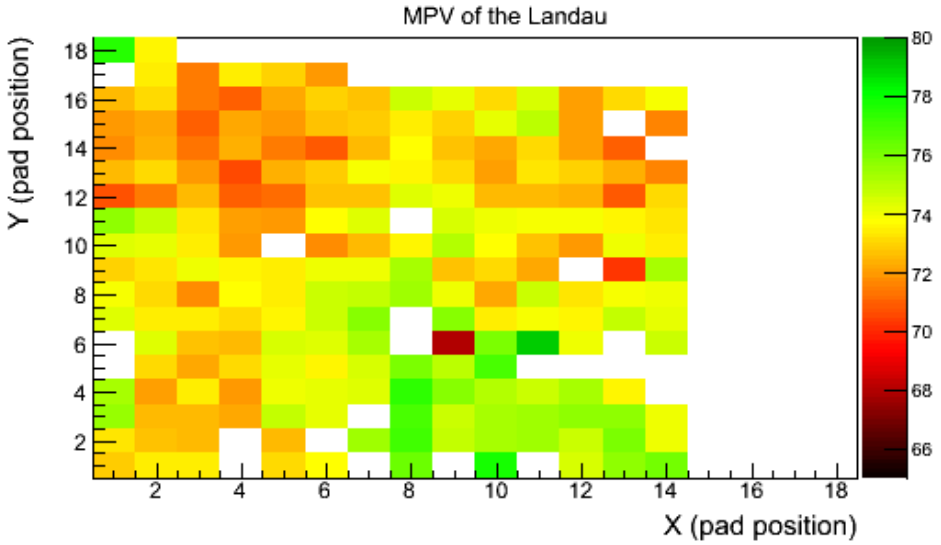
- Beam
- delta rays
- Bremsstrahlung + gamma conversion (2e-)
  + Compton

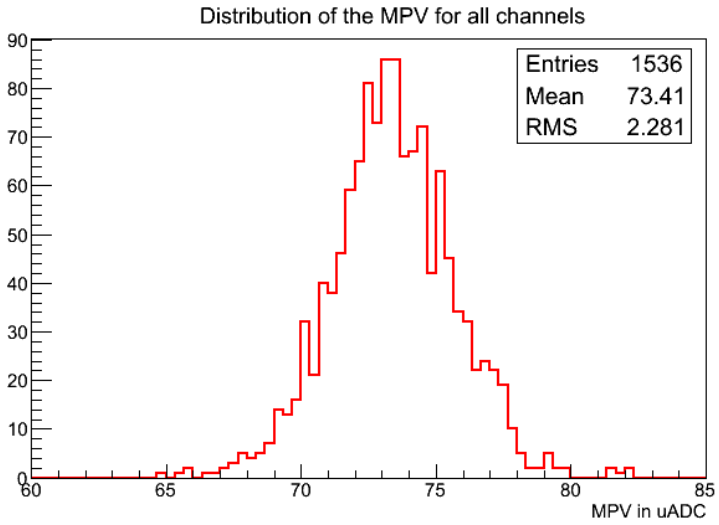
Energy calibration

Establishment of calibration procedure for a larger number of cells
Homogeneity of response (x,y scan of detector)



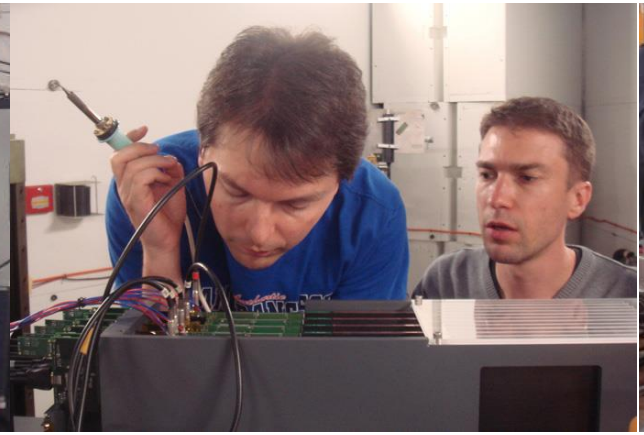
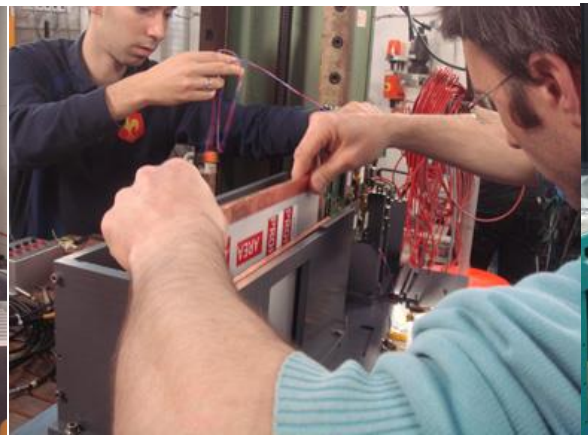






Thanks

Special thanks to our experts:
Frédéric, Mickael, Patrick, Rémi and Stéphane

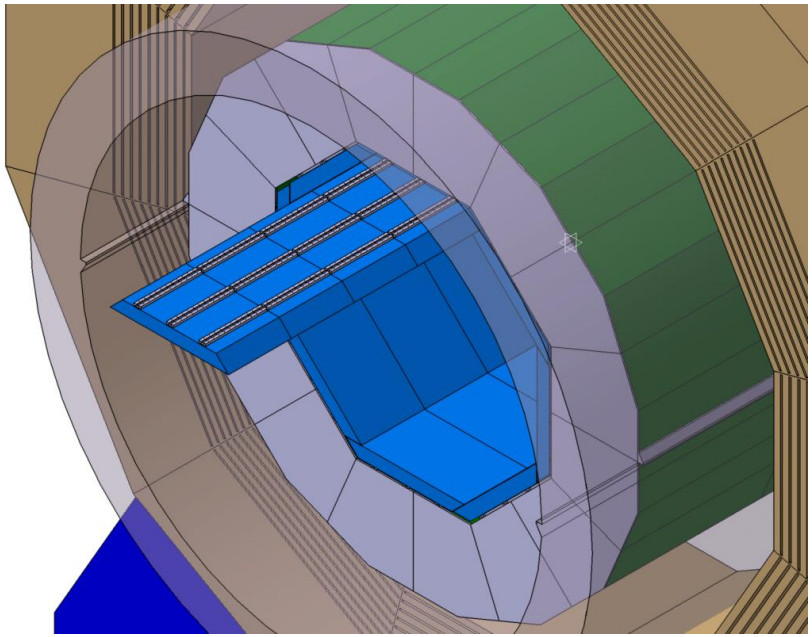





And to everyone who took part in the preparation of the test beam:
- LLR, LAL+OMEGA, LPNHE
- Kyushu University, Tokyo University, Nippon Dental University
- SKKU

SiW ECAL for a future LC

SiW ECAL is one of the prototypes for future LC detectors

➡ Optimized for Particle Flow Algorithm:



The SiW ECAL in the ILD Detector

Basic Requirements:

- Extreme high granularity
- Compact and hermetic

Basic Choices:

- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design

- Silicon as active material
  - Support compact design
  - Allows for pixelisation
  - Large signal/noise ratio