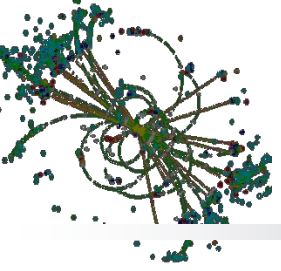


Chronopixel R&D status – November 2013

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Eugene, OR), C.Baltay, W.Emmet, D.Rabinovitz (Yale University,
New Haven, CT)*

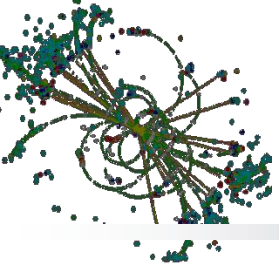
EE work is contracted to Sarnoff Corporation



Outline of the talk



- Very brief reminder of Chronopixel concept:
 - ↳ **Chronopixel** is a **monolithic CMOS** pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and **record the time** (time stamp) **of each hit**.
- Project milestones.
- Prototype 1 design
- Prototype 2 design
- Summary of prototypes 1 and 2 tests.
- Changes suggested for prototype 3
- Conclusions and plans

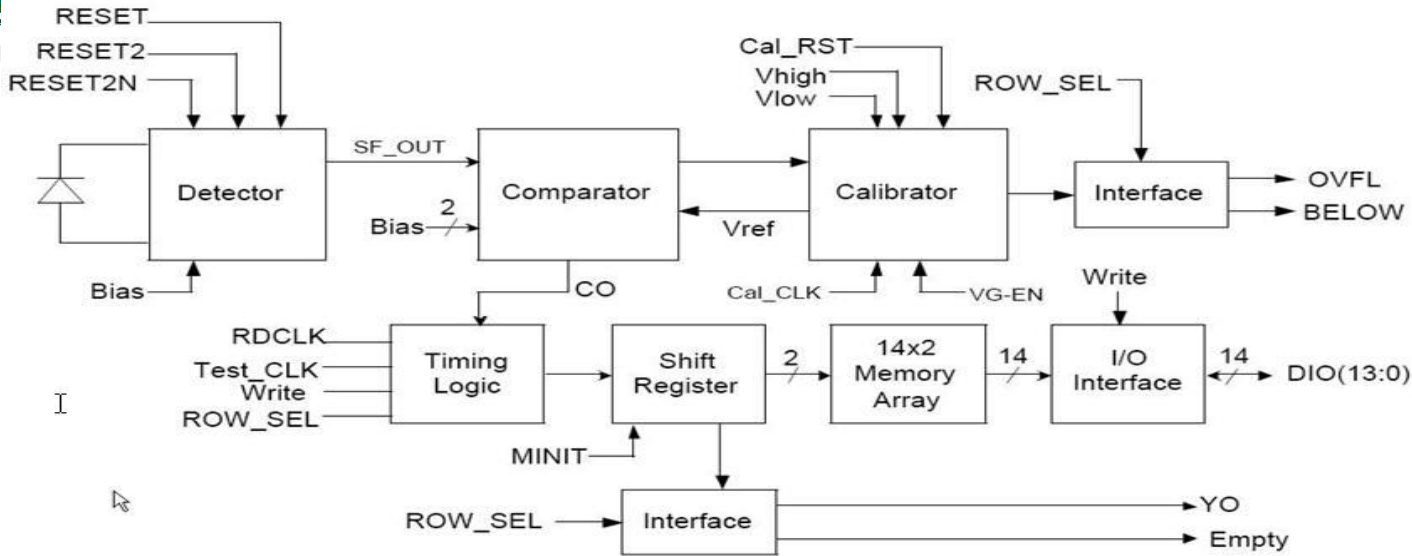


Timeline

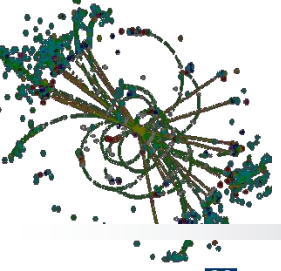


- **2004 – talks with Sarnoff Corporation started.**
 - ✦ Oregon University, Yale University and Sarnoff Corporation **collaboration formed.**
- **January, 2007**
 - ✦ Completed design – Chronopixel
 - ❖ **2 buffers, with calibration**
- **May 2008**
 - ✦ **Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each**
 - ✦ **TSMC 0.18 μm \Rightarrow ~50 μm pixel**
 - ❖ Epi-layer only 7 μm
 - ❖ Low resistivity (~10 ohm*cm) silicon
- **October 2008**
 - ✦ Design of **test boards** started at SLAC
- **September 2009**
 - ✦ Chronopixel chip **tests started**
- **March 2010**
 - ✦ **Tests completed, report written**
- **May 2010**
 - ✦ Second prototype **design started**
- **September 2010**
 - ✦ **contract** with Sarnoff for developing of second prototype **signed.**
- **October 2010**
 - ✦ Sarnoff works **stalled**
- **September 2011**
 - ✦ Sarnoff **resumed** work.
- **February 2012**
 - ✦ **Submitted** to MOSIS for production at **TSMC.** (48x48 array of **25 μm pixel, 90 nm process**)
 - ✦ **Modification** of the **test stand** started as all signal specifications were defined.
- **June 6, 2012**
 - ✦ **11 packaged chips** delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
 - ✦ Tests at SLAC started
- **March 2013**
 - ✦ Test results are discussed with Sarnoff and prototype 3 design features defined
- **July 2013**
 - ✦ **Contract with Sarnoff (SRI International) is signed.** Packaged chip delivery – may be 1st quarter of 2014.

First prototype design



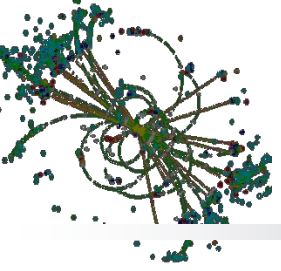
- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with **Sarnoff** company.
- When **signal** generated by particle crossing sensitive layer **exceeds threshold**, snapshot of the **time stamp**, provided by 14 bits bus is **recorded** into pixel memory, and **memory pointer is advanced**.
- If **another particle** hits the same pixel during the same bunch train, **second memory cell** is used for this event time stamp.
- During readout, which happens between bunch trains, **pixels which do not** have any time stamp **records**, generate **EMPTY** signal, which **advances IO-MUX** circuit to next pixel without wasting any time. This **speeds up readout** by factor of about **100**.
- **Comparator offsets** of individual pixels are determined in the **calibration cycle**, stored in digital form, and reference voltage, which sets the comparator threshold, is shifted to **adjust thresholds** in all pixels to the **same signal level**.
- To achieve required noise level (about **25 e r.m.s.**) **special reset** circuit (**soft reset** with feedback) was developed by **Sarnoff designers**. They claim it reduces reset noise by **factor of 2**.



Prototype 1 summary



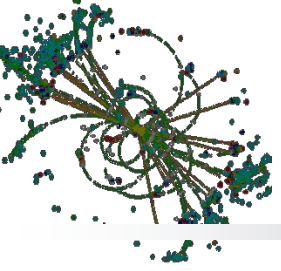
- Tests show that general **concept is working**.
- **Mistake was made in the power distribution** net on the chip, which led to only **small portion of it is operational**.
- Calibration circuit **works as expected in test pixels**, but for unknown reason **does not work in pixels array**.
- Noise figure with “soft reset” is within specifications ($0.86 \text{ mV}/35.7 \mu\text{V}/e = 24 \text{ e}$, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is **2.7 times larger** required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8} \text{ A}/\text{cm}^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz .
- No problems with **pulsing analog power**.
- Pixel size was $50 \times 50 \mu\text{m}^2$ while we want $15 \times 15 \mu\text{m}^2$ or less.
- However, CMOS electronics in prototype 1 could allow high charge collection efficiency only if encapsulated in **deep p-well**. This requires **special process, not available for smaller feature size**.



Prototype 2 features



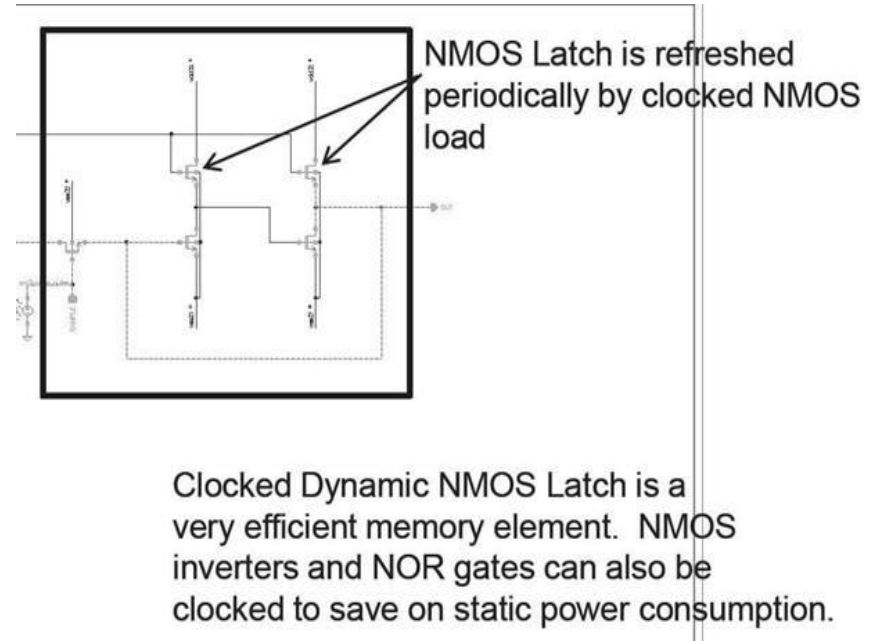
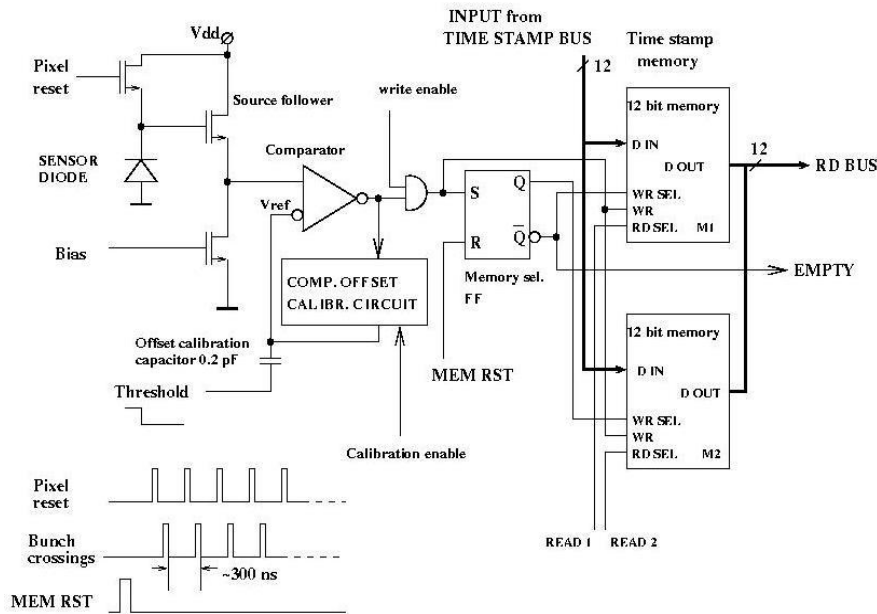
- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge collection without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.
- **New** comparator offset compensation (“**calibration**”) scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.
- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.
- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25 μ x 25 μ**
- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.



Prototype 2 design

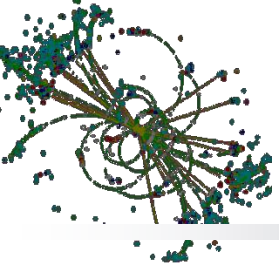


BLOCK DIAGRAM OF ONE PIXEL

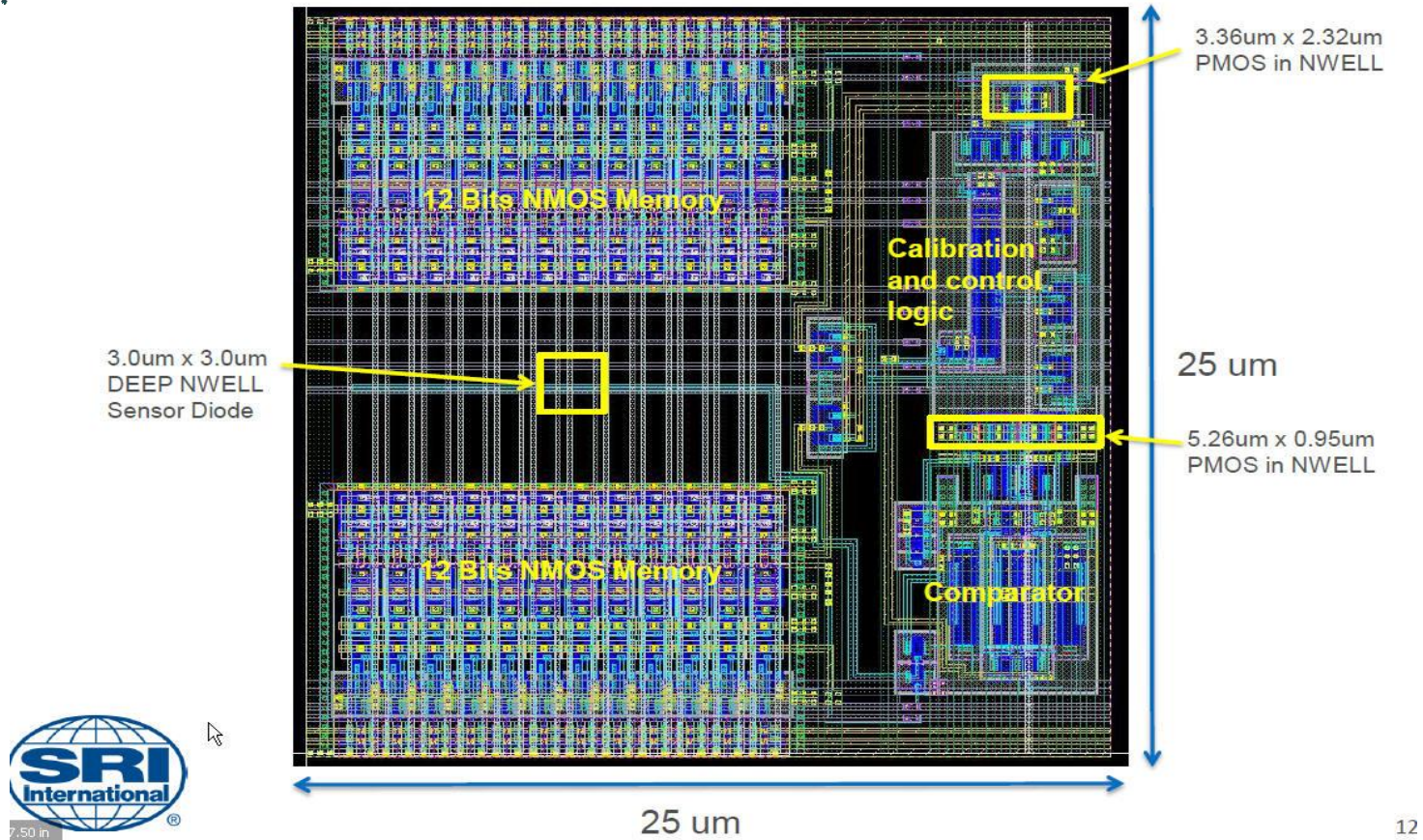


Comparator offset calibration circuit charges calibration capacitor to the value needed to compensate for the spread of transistor parameters in individual pixels. We needed to prove, that the voltage on this capacitor will stay unchanged for the duration of bunch train (1 ms).

Proposed dynamic latch (**memory cell**) has technical **problem** in achieving very **low power** consumption. The problem is in the fact, that NMOS loads **can't** have very **low current** in conducting state – lower practical **limit is 3-5µA**. This necessitate in the use of **very short pulses** for refreshing to **keep power within** specified limit. However, we have **suggested solution** to this problem, which allows to **reduce average current** to required value **without** need for **short pulses**.

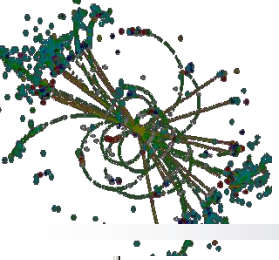


Prototype 2 pixel layout



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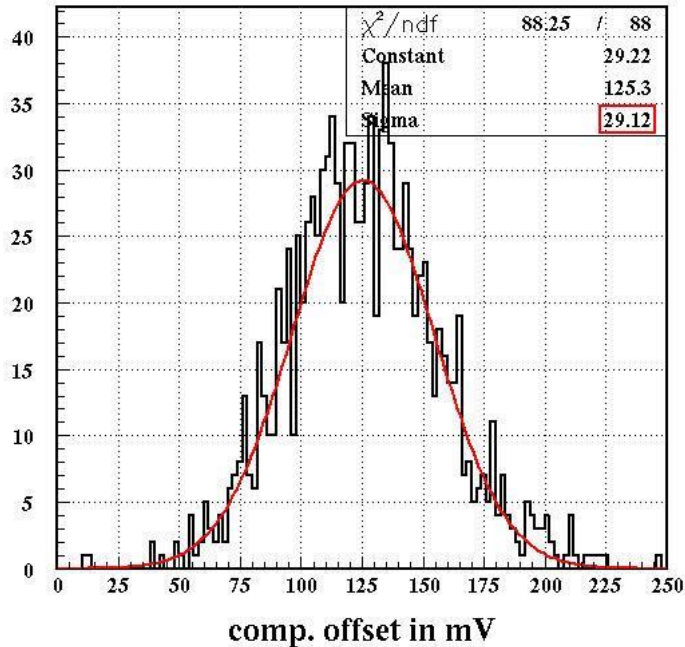
All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP N WELL), half of the pixels have it's size increased to $4 \times 5.5 \mu^2$.



Test results - calibration

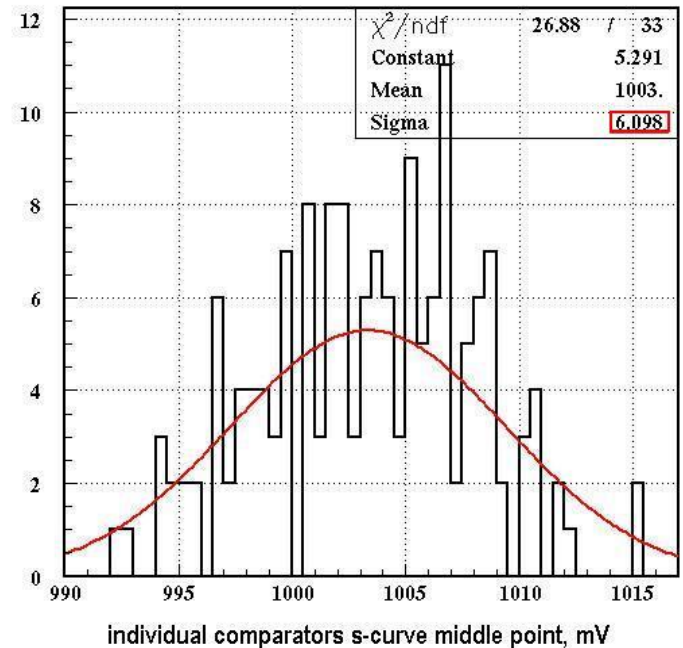


Offsets before calibration



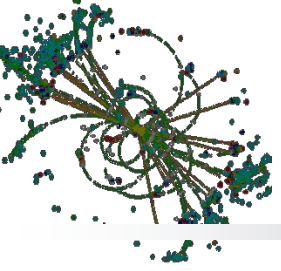
Prototype 2

Prototype 1 comparator offsets measurements

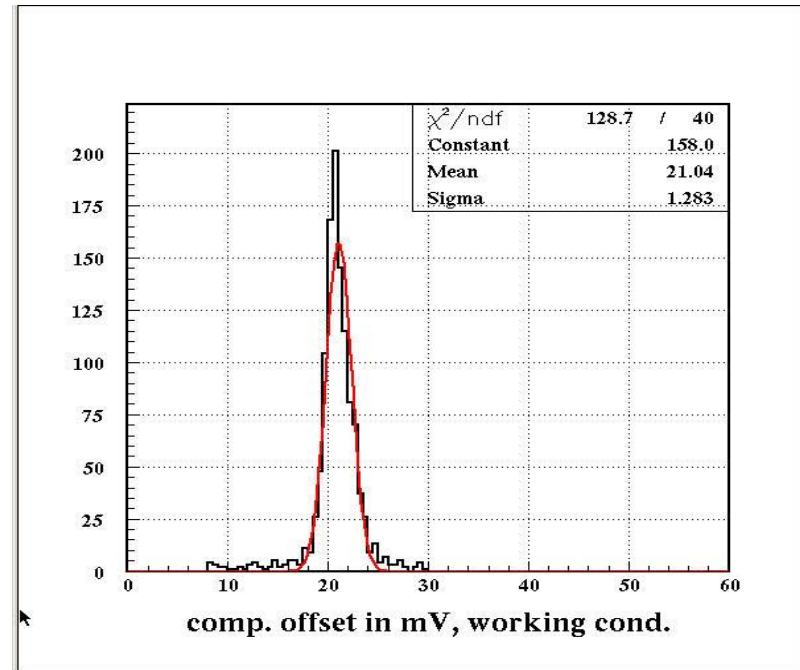
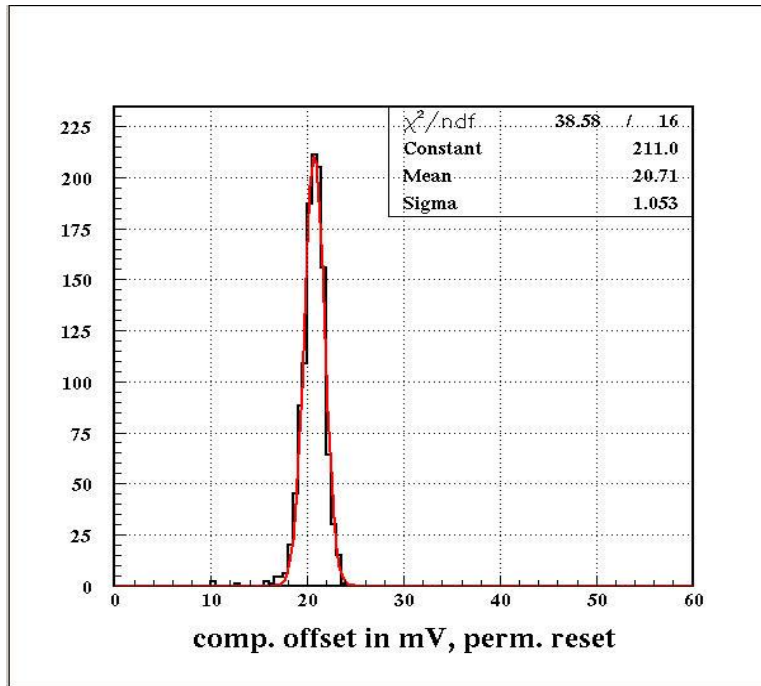


Prototype 1

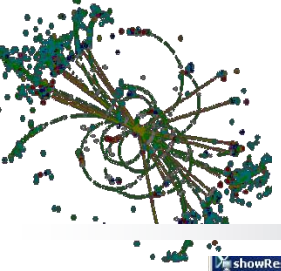
Comparator offsets spread comparison. Because of smaller feature size, it is more difficult to keep transistor parameters close to design values and different transistor with same design parameters in reality behave differently. This leads to the comparator offsets spread in prototype 2 almost 5 times larger than in prototype 1



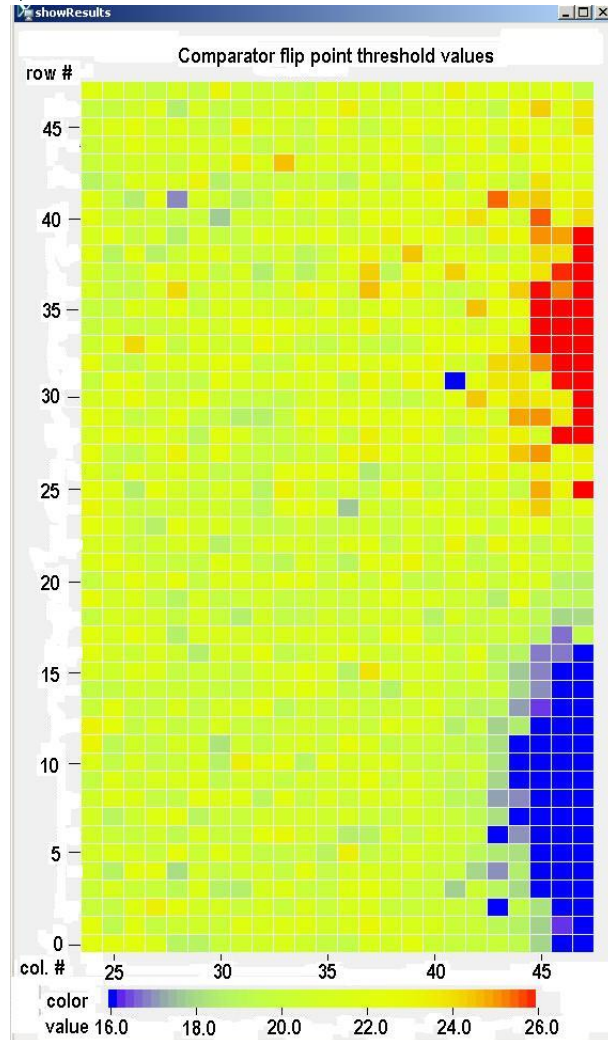
Comparator offsets calibration



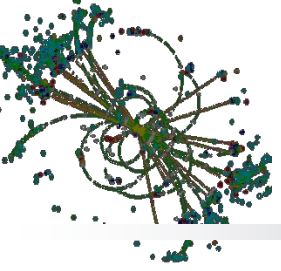
- To test how well comparator offset calibration (compensation) works, we first tried it **with sensor permanently in reset** state (connected to photodiode bias voltage). For convenience of measurements, we used pulse with 25 mV amplitude to simulate signal during offsets measurements. Plot at **right** shows offsets compensation **in working** conditions – sensor photodiode is connected to bias voltage only for short period of time during each measurement period.



Test results – cross talks



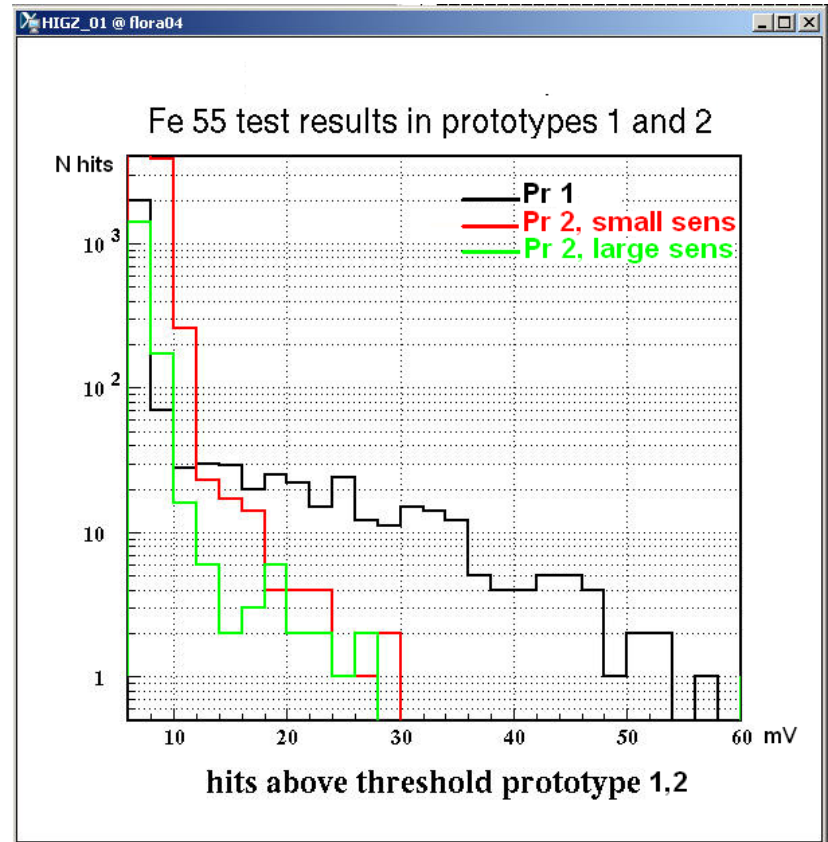
- On the right plot on previous slide we could see long tails of the offsets distribution. If we look at the picture how offsets values vary across chip area we can see two blobs of the pixels with large deviation of offsets from the average value (red and blue areas). These are pixels, **close to clock drivers**. So, there are some cross-talks from drivers.

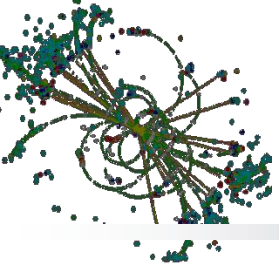


Test results – sensor capacitance

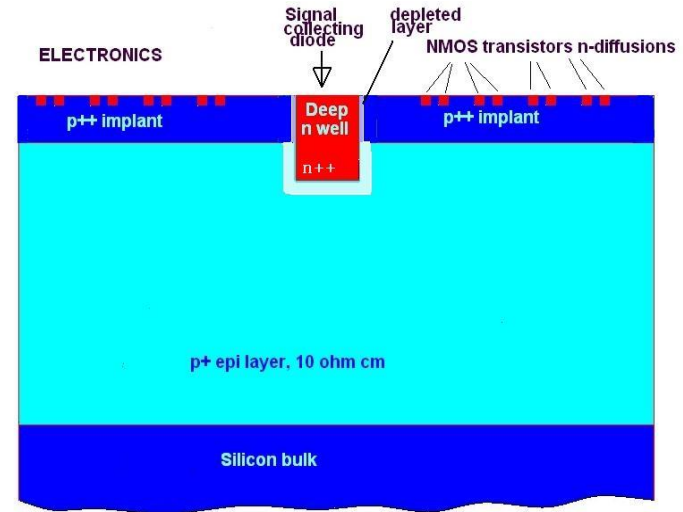
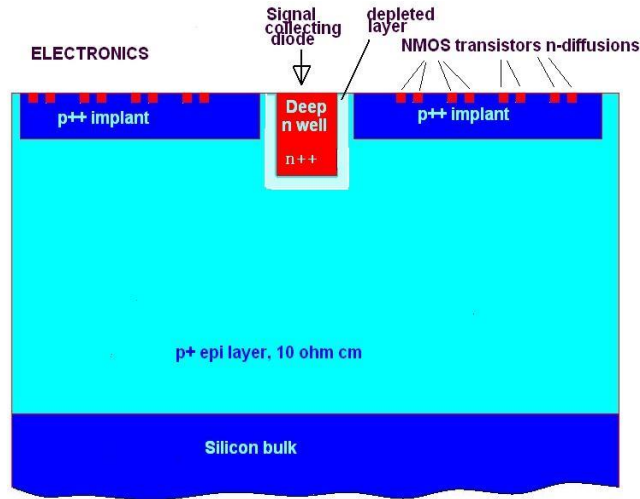


- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – $9 \mu^2$ and $22 \mu^2$ (“small” and “large” on the plot) . The maximum signal value is **roughly in agreement with expected capacitance difference** , though we would expect larger difference in maximum signal values here. But capacitance of the sensor from this measurements (~ 7.5 fF) appeared much larger than our expectation ($\sim 1-2$ fF).

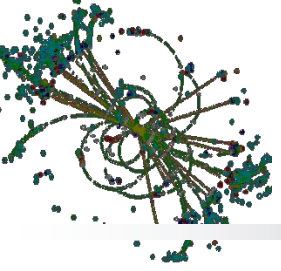




What got wrong?



- We **hoped**, that pixel cross-section will look like what is **shown on left** picture. But it appeared, that in 90 nm design rules it is **not allowed** to have window in the top p++ implant **around deep n-well**, which forms our sensor diode. Resulting pixel cross-section is shown on **right** picture. **Very high** doping concentration of p++ implant leads to **very thin depletion layer** around side walls of deep n-well, which creates additional **large capacitance**.

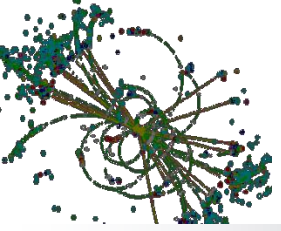


Power dissipation



Circuit	I total (mA)	I/pixel (nA)	P/pixel (nW)	Reduction strategy	Expected P/pix (nW)
1.2 V mem	0.46	200	240	Keep power only when hit	2.4 - 50
0.7 V mem	0.13	56.4	39.5	Keep power only when hit	0.4 - 8
1.2 V comp	0.53	230	276	Power only during BT	2.8
2.5 V SF	0.12	52.1	130.2	Power only during BT	1.3
Total			685.7		6.9 – 62.1
Spec			34.		

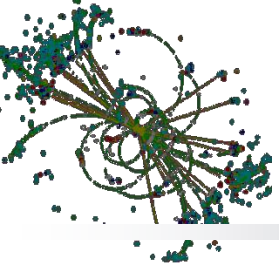
Design specification calls for 0.15 mW/mm² (100W for entire vertex detector), or 34nW/pixel assuming 15x15 μ² pixels.



Summary of prototypes tests



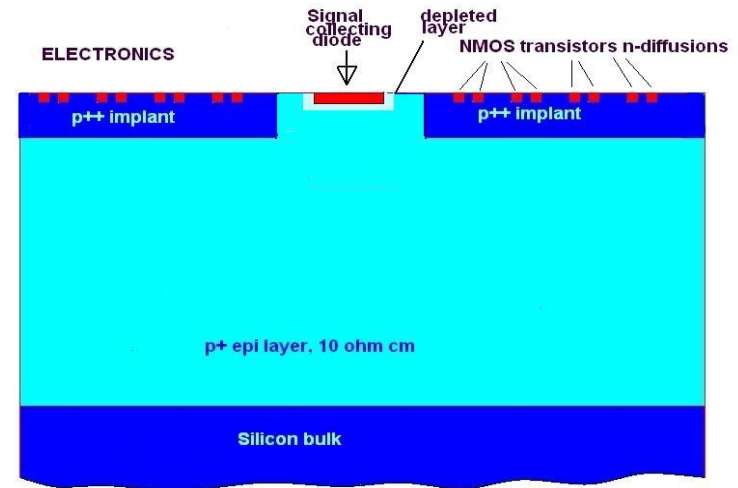
- From both, first and second prototype tests we have learned:
 - ↵ 1. We **can** build pixels which can record **time stamps with 300 ns period** (1 BC interval) - prototype 1
 - ↵ 2. We **can** build readout system, allowing **to read all hit pixels** during interval between bunch trains (by implementing **sparse readout**) - prototype 1
 - ↵ 3. We **can** implement **pulsed power** with 2 ms ON and 200 ms OFF, and this **will not ruin** comparator performance - both prototype 1 and 2
 - ↵ 4. We **can** implement **all NMOS** electronics **without** unacceptable **power consumption** - prototype 2. We **don't know yet** if **all NMOS** electronics is **a good alternative solution** to deep P-well option.
 - ↵ 5. We **can** achieve comparators **offset calibration** with virtually **any required precision** using **analog calibration** circuit.
 - ↵ 6. Going down to **smaller feature size is not as strait forward** process as we thought.

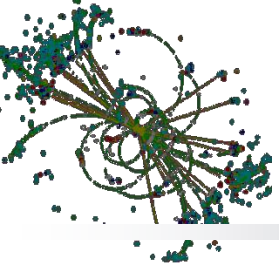


Suggestions for prototype 3



- It appeared, that **prohibition** of creating windows in top implant **does not apply** if we want make not deep n++ well for sensor diode, but create so-called **native diode** on the epitaxial layer : n+ implant in p+ epi layer, as shown on the picture. Simulation, made by Sarnoff people, claims **10-fold decrease** in the sensor **capacitance** in that case.
- Fighting cross-talks is always a challenge. But what was done wrong in prototype 2 – **common power supply** for analog and digital part of electronics. It **need to be fixed**.

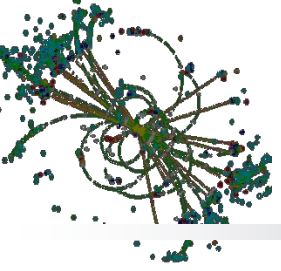




Prototype 3 wish list



- **Wish list, accepted by Sarnoff for the next prototype:**
 - ↵ **1. Find a way to decrease sensor capacitance** (they think they know how – see previous slide, and their calculations show decrease by factor 10).
 - ↵ **2. Take care about crosstalk** : separate analog and digital power and ground, shield trace, connecting sensor to source follower input from busses, caring strobes and clocks (by changing metal layers designations)
 - ↵ **3. Implement 2-way calibration** process
 - ↵ **4. Remove buffering of sensor reset** pulse inside the chip. It will allow us to **control the amplitude** of this pulse, which is especially important with decreased sensor capacitance.
 - ↵ **5. Remove unnecessary multiplexing of time stamp** (pure technical shortfall of prototype 2 design, which may limit speed and increase feed through noise).
 - ↵ **6. Improve timestamp memory robustness** (right now about 1% of memory cells fail to record time stamps correctly).



Summary and plans



- Chronopixel R&D are moving forward, **we have solved many** problems and proved that concept is valid.
- If suggested **solution** of the major problem of 90 nm technology for our application **will work**, we may have sensor design **implementable on a standard** foundry process.
- We **have signed** contract with Sarnoff for prototype 3 design in July of 2013 and they hope to complete it in the 1st quarter of 2014.
- From our side – we **need to modify** test stand to fit new design, and perform all test as soon as we receive sensors. There should be **no problems** with it.