DEPFET APS for future collider applications - a status report

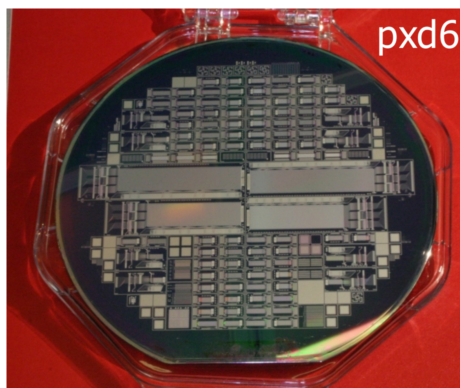
:- Sensors and modules at the Belle II vertex detector

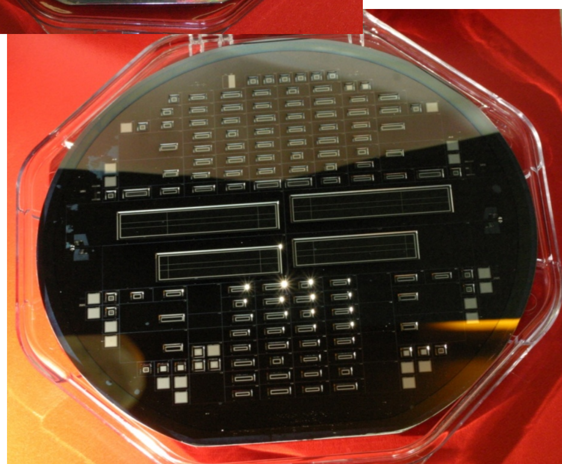
:- new ILC specific activities

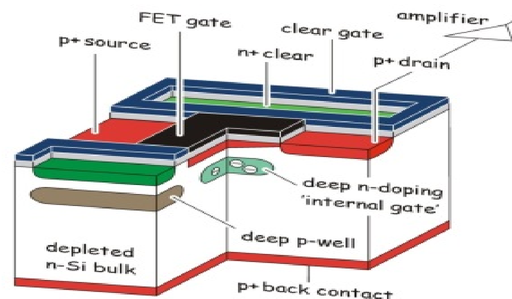
Ladislav Andricek, MPG Halbleiterlabor, München

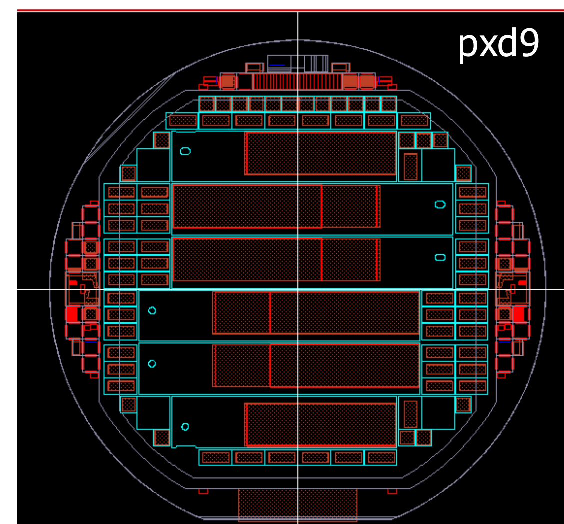
For the DEPFET Collaboration

Thin DEPFETs for vertexing – production status

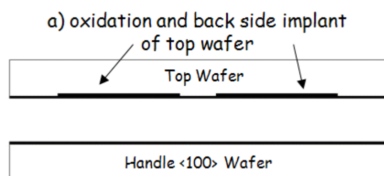


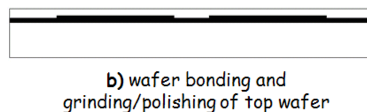


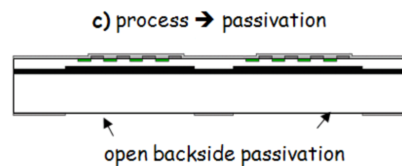


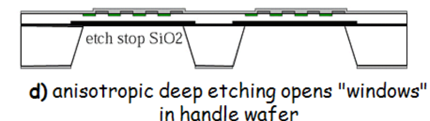


- **pxd6 finished and extensively tested : 50 µm DEPFETs**
- **pxd9 (75 µm DEPFETs) for Belle II**
  - **Three batches in production (10 wafers each)**
  - **FEOL of first batch done (next: metal system)**
  - **2nd and 3rd batch following**



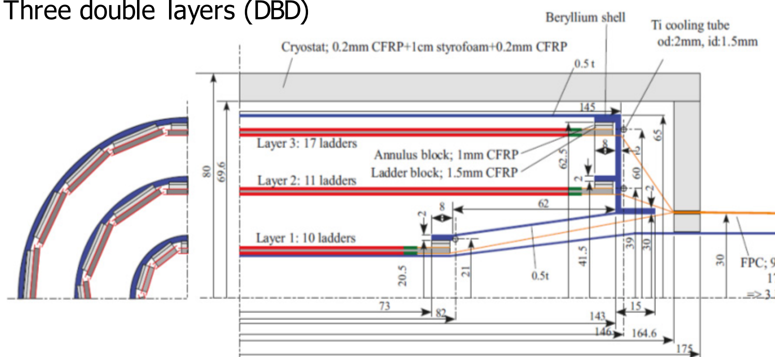




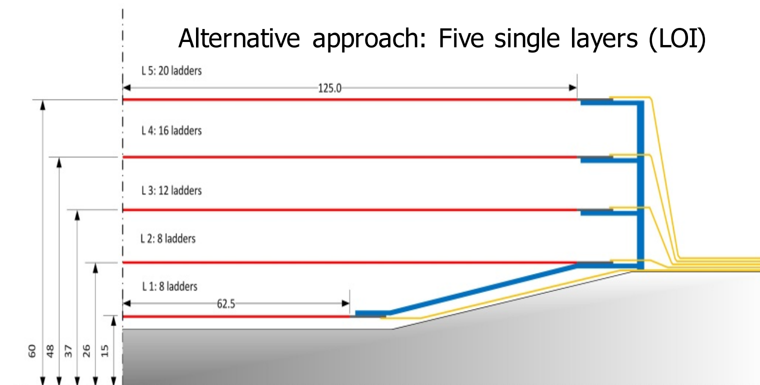


The ILD VXD ←→ Belle II PXD

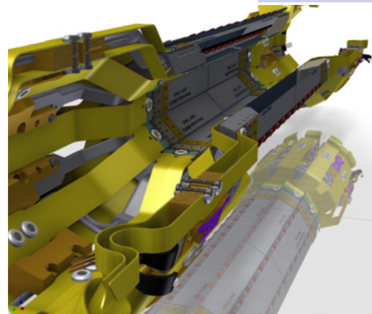
Three double layers (DBD)

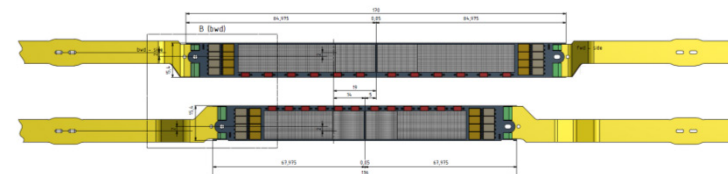


Alternative approach: Five single layers (LOI)



	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Sensitive length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	55x50 & 60X50 (L1) 70x50 & 85x50 (L2)	25x25 (L1-L5)	μm^2
frame rate	50	20 (L1), 4 (L2-L5)	kHz
Number of pixels	8	800	Mpix

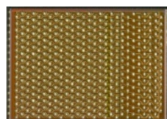




Belle II PXD ladder:
(almost) prototypes for L1 and L2 of ILD LOI layout!!

DEPFET all-silicon module

DCDB (Drain Current Digitizer)
Analog front-end

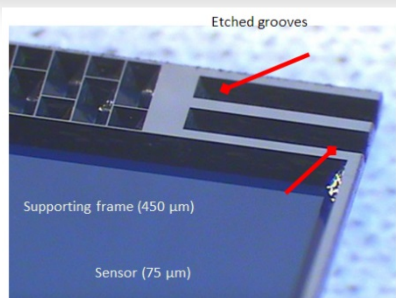


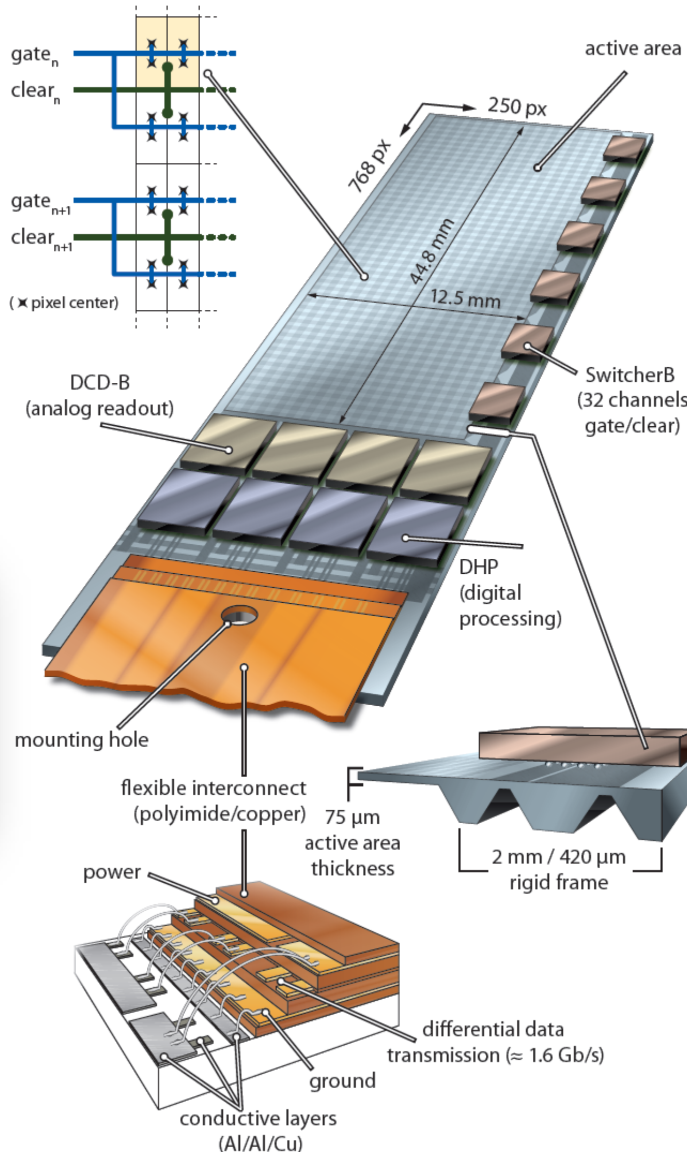
Amplification and digitization of DEPFET signals.

256 input channels
8-bit ADC per channel
92 ns sampling time
UMC 180 nm
Rad hard design

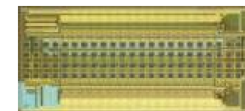
Low mass modules

→ MCMs w/ highest possible integration!
- ↳ Thin sensor area
- ↳ r/o ASICs outside acceptance
- ↳ Thin (perforated) frame w/ steering ASICs



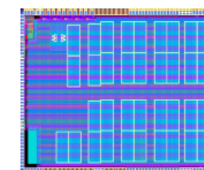


SwitcherB - Row Control



AMS/IBM HVCMOS 180 nm
Size 3.6 × 1.5 mm^2
Gate and Clear signal
32x2 channels
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)
First data compression



IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing and trigger control
Rad. Hard proved (100 Mrad)

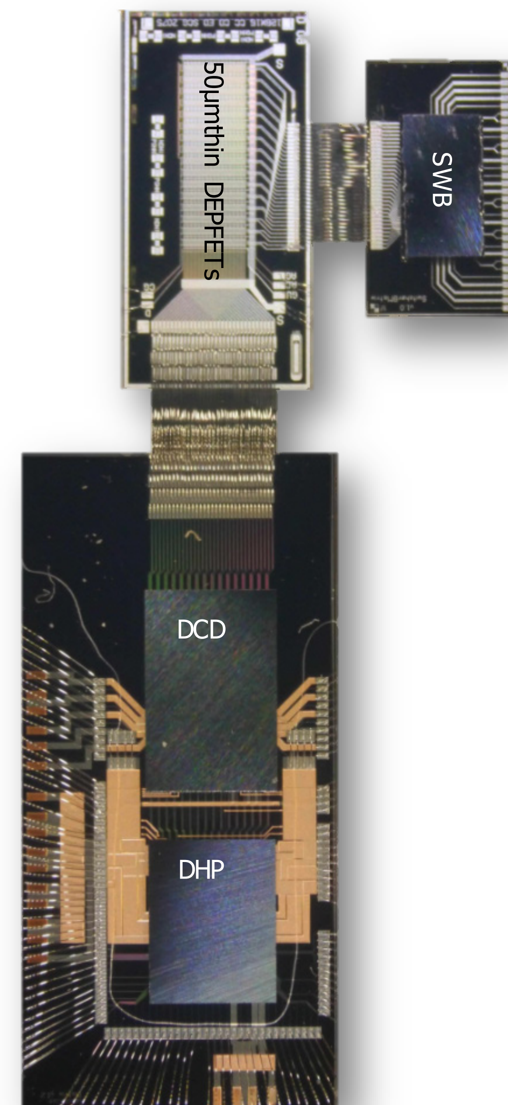
Sensor and r/o electronics: Beam test with the full system

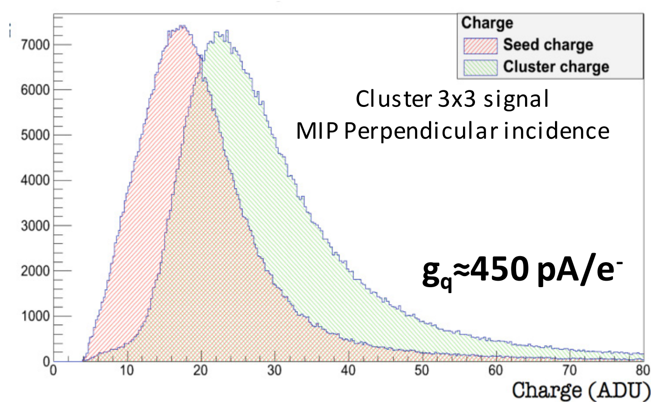
PXD6 Belle II design

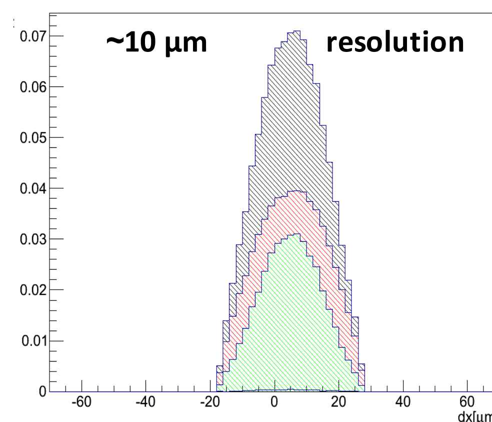
- ▷ Thin (**50 µm**) sensor 32x64 pixels
- ▷ Pitch 50x75 µm^2

- ▷ SwitcherB and DCDB at full speed
- ▷ Belle II prototype power supply
- ▷ DCDB readout at 320 MHz → **100 ns row time**
  - ↳ 20 µs frame time for Belle II full ladder

- ▷ 99% Efficiency
- ▷ S/N for MIPs: 20-40 depending on gate length







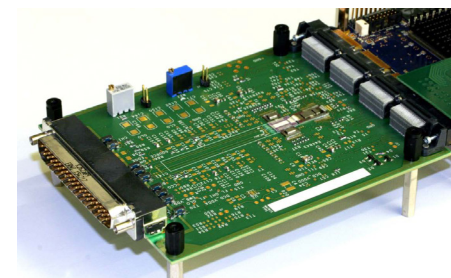
Towards a real ladder

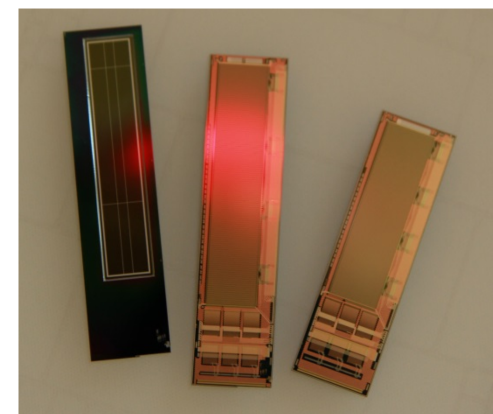
Transition from test systems to integrated modules

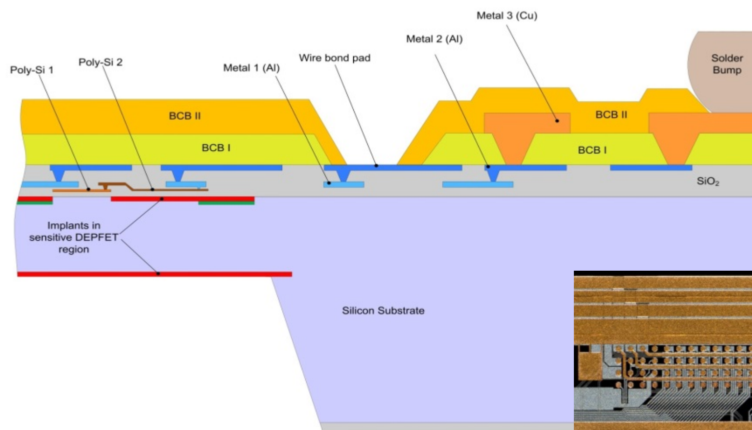
» PCB for the various matrices ….. "hybrids"

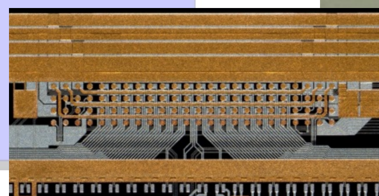
» first bump bonded chip on PXD6 prototype matrices
- ↳ 2 metal layers, not the final geometry, simple 3rd metal
- ↳ need still support PCB for I/O
- ↳ not perforated balcony

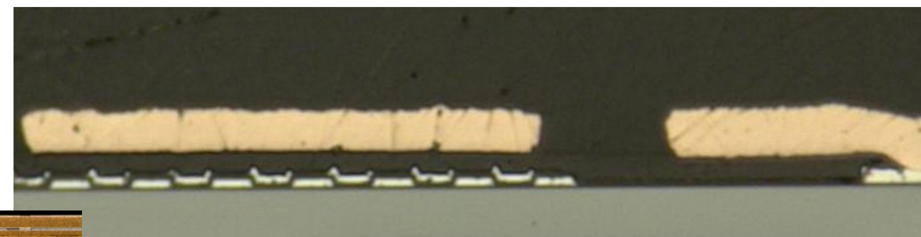
» Belle-II PXD Module (two modules form a ladder)
- ↳ **three metal layers, Cu as LM only on periphery**
- ↳ MCM: 4 DCD, 4 DHP, 6 Switchers → ~3000 bonds/module
- ↳ **Cu as UBM, bumps partly on thinned perforated frame**
- ↳ passive components soldered to substrate
- ↳ I/O and power over Kapton cable







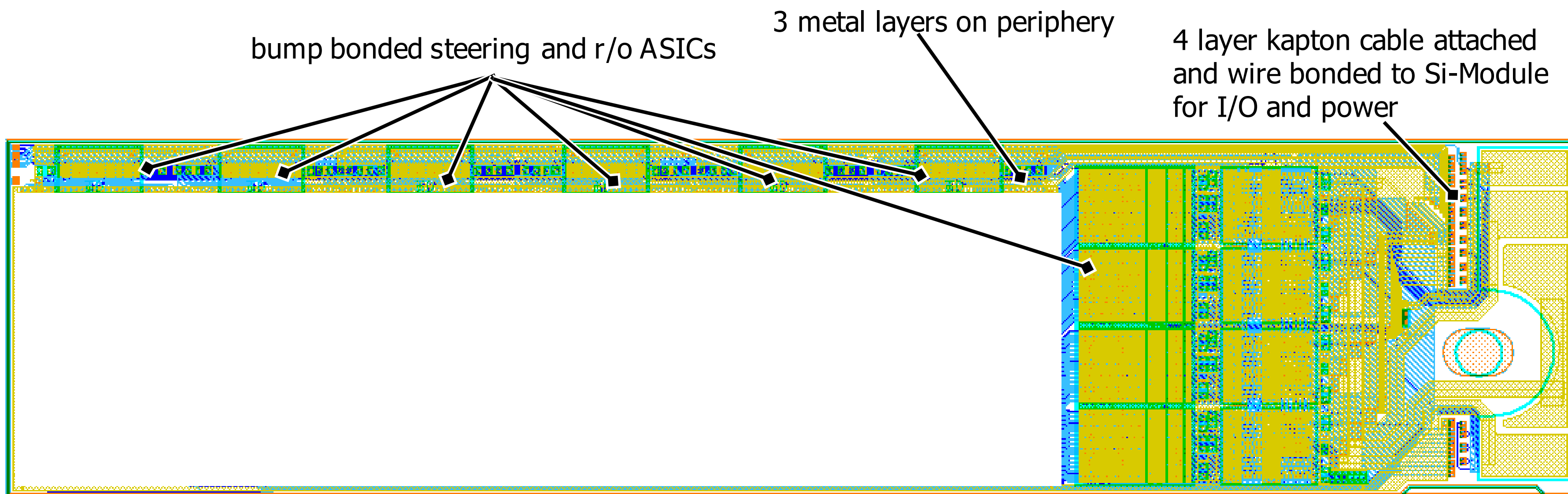




→ Test the full metal system
- ↳ technology
- ↳ electrical performance

E-MCM – everything but the DEPFET

Electronic Multi-Chip Module



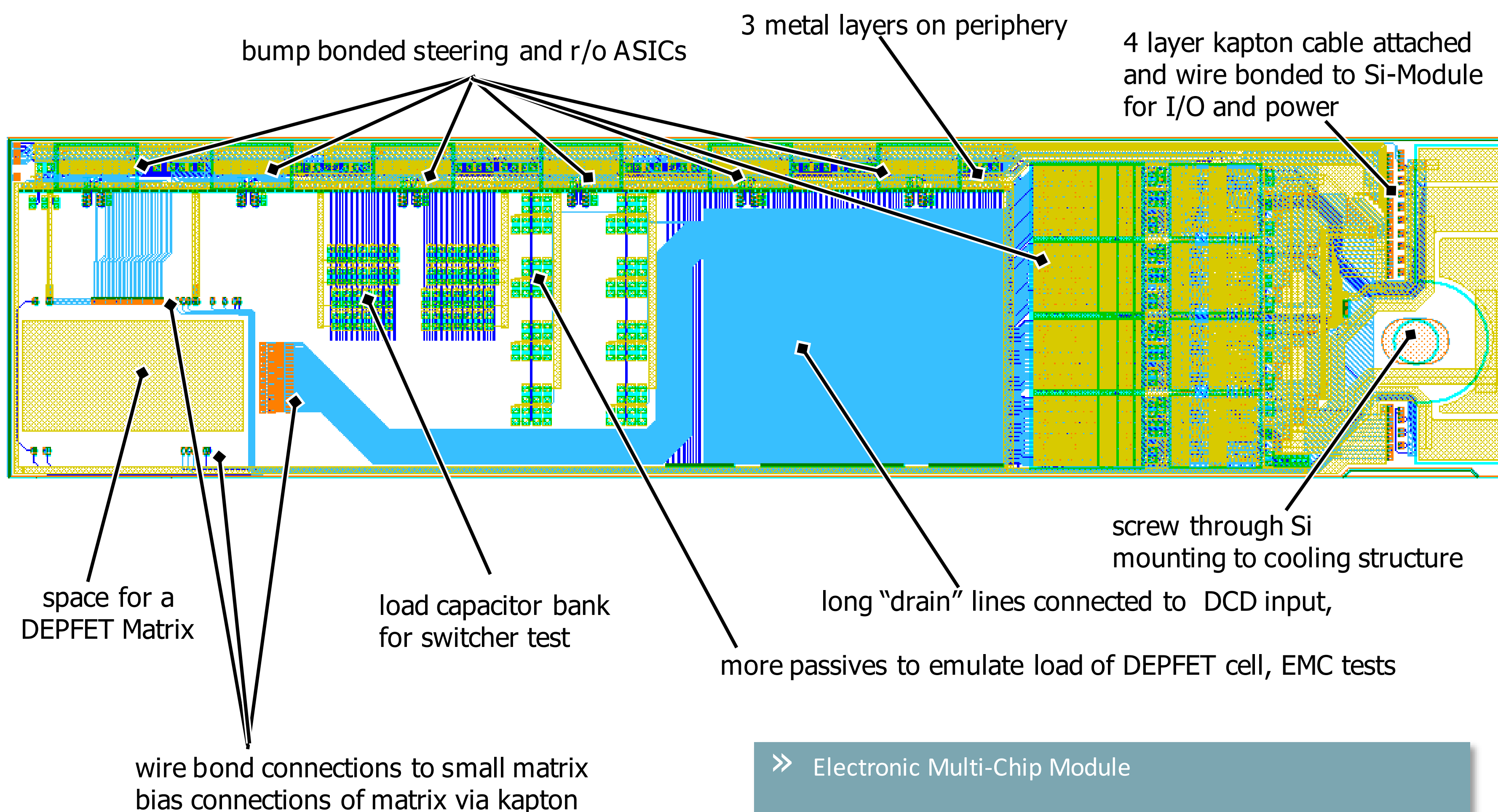
» metal system as close as possible to final, best guess for the layout → same as for final production

- ↳ full schematic at the periphery for 6 Switcher, 4 DCD, 4 DHP
- ↳ landing pads for solder bumps on ASICs
- ↳ space for passives (caps and termination resistors)

- ↳ I/O and power over 4-layer kapton cable at EOS

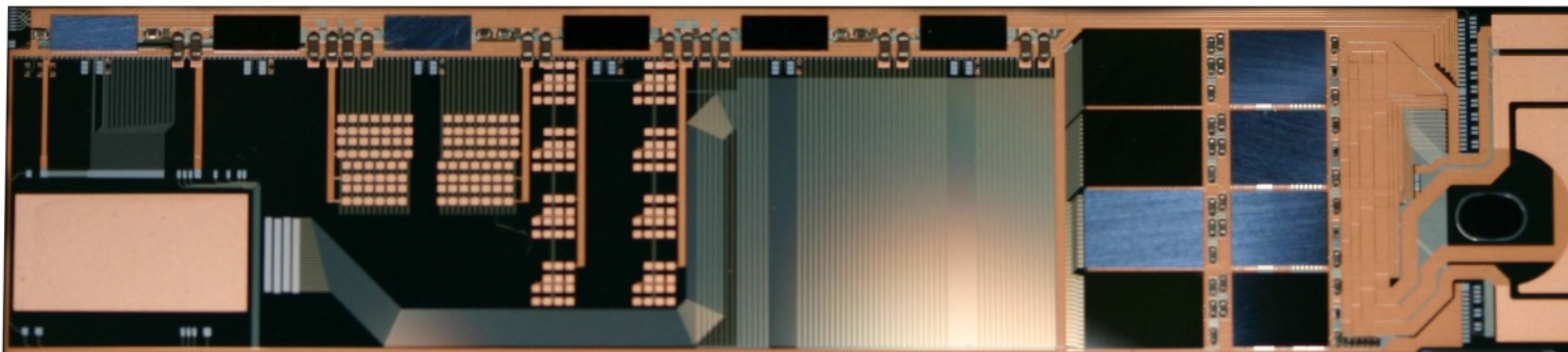
- ↳ mechanically attached to cooling end-flange

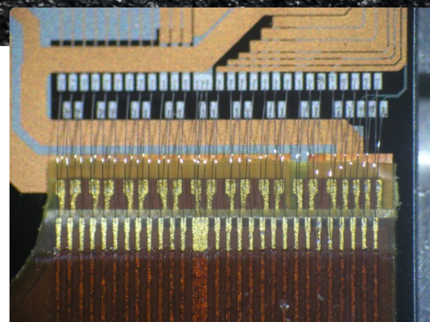
E-MCM – everything but the DEPFET

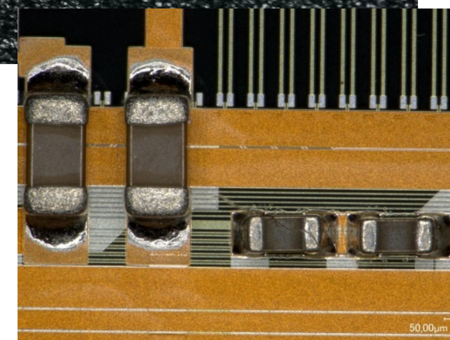


- Electronic Multi-Chip Module
- basically an electrically active prototype of half-ladder
- even beam tests are possible with small piggy-back matrix

E-MCM as of today ….



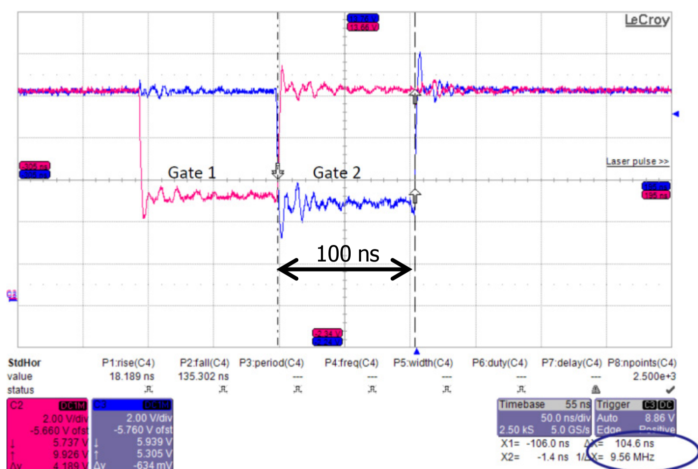


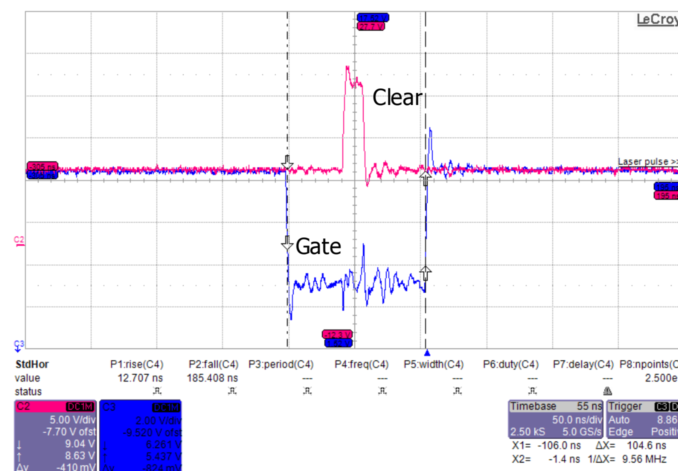


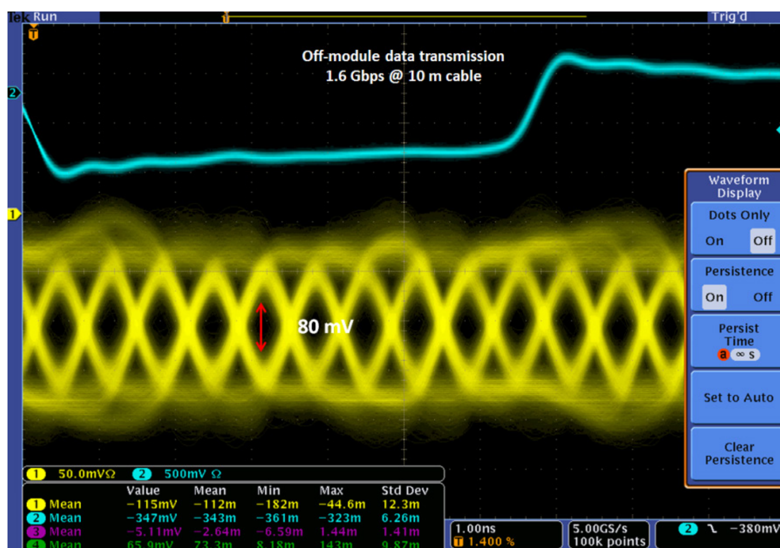
First samples fully populated

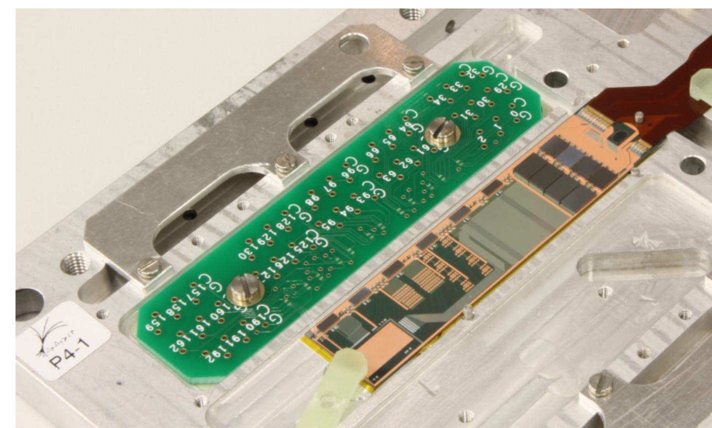
Tests and evaluation ongoing

First test results – Gate, Clear and signal transmission









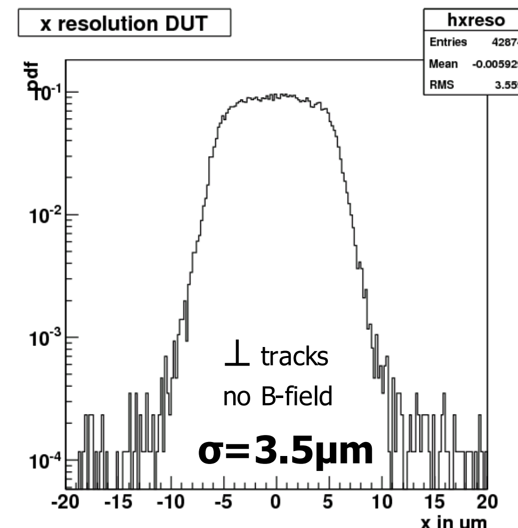
Next step is to mount a small DEPFET Matrix and test performance on the Bench and in a test beam

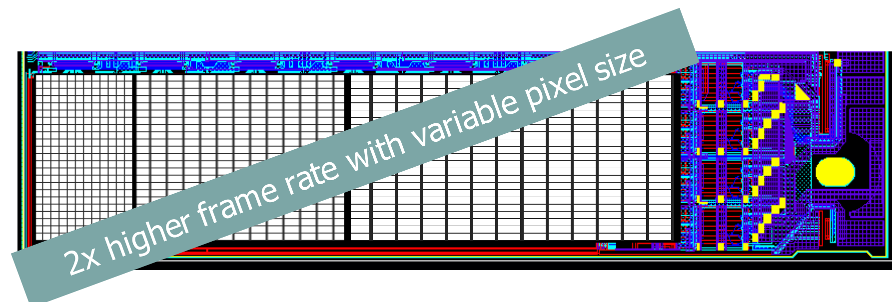
DEPFET at the ILC: the challenges

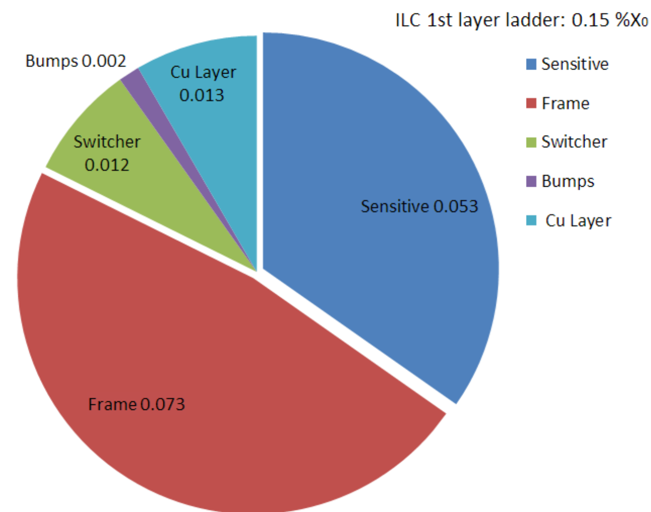
:- small pixels (~20µm) for excellent single point resolution (~3µm)

:- the DEPFET runs in a rolling shutter mode (read-out during the bunch train)
- → 100ns per r/o @ Belle II
- → 2048 rows per half-ladder, 2-fold r/o
- → **~1/100µs frame rate state of the art**
- → our **goal is ~1/50µs** frame rate (innermost layer)

:- minimal material down to very small angles
- → thinner sensors with large S/N
- → minimize support, services, and cooling material
- → **pixelated forward discs**
- → **power pulsing, low mass cooling**





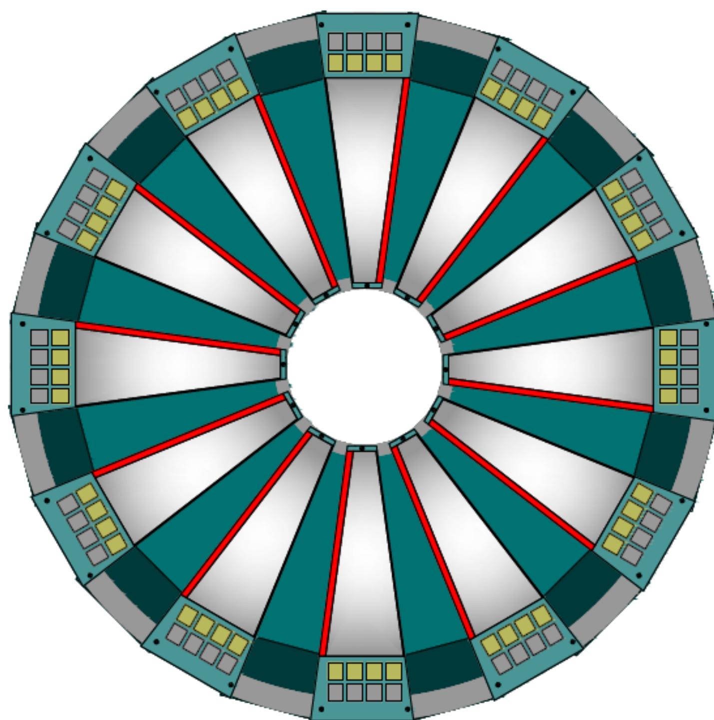


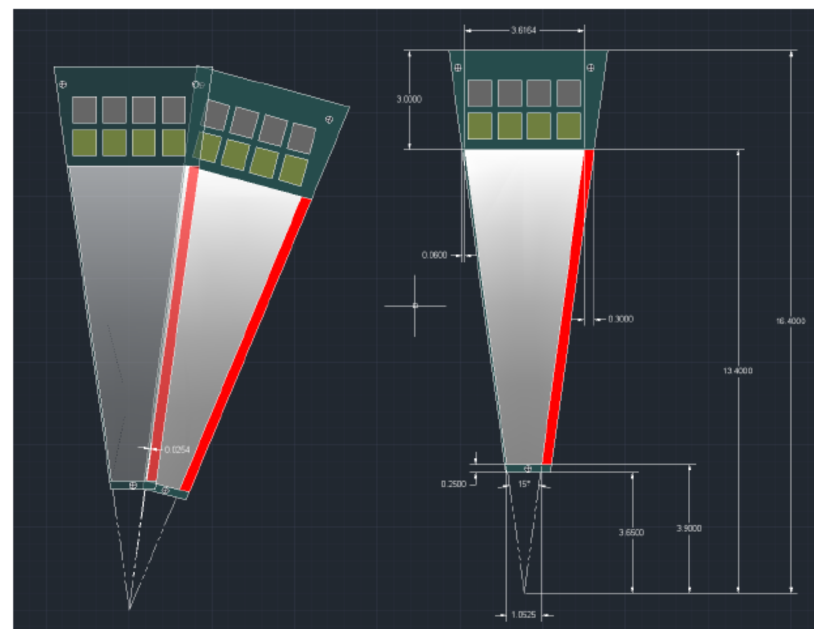
Stepping forward

LC Detector concepts require pixelated forward discs

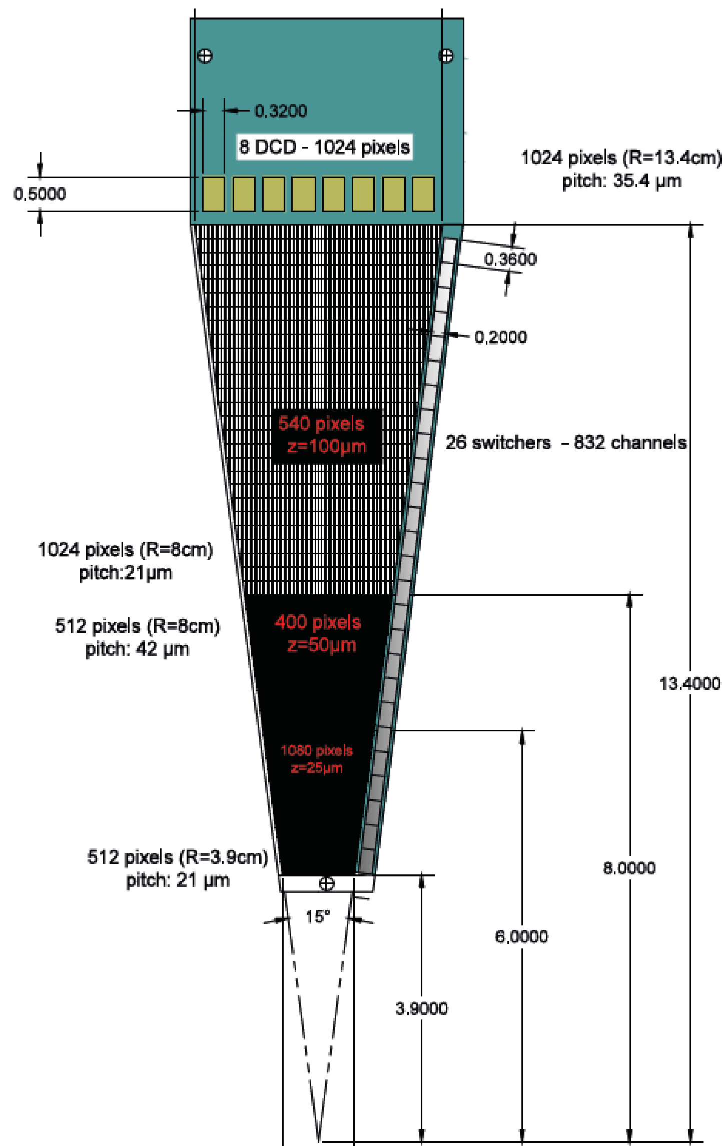
» SiD : vertex detector end-cap
» ILD : forward tracking discs

→ Adapt all-silicon ladder to the forward region: “all-silicon” DEPFET pixel petal





all-silicon petal



Concept

» Thin sensitive region: R= 3.9 to 13.4 cm
» Radially varying pixel size
» r/o at the outer edge with bump bonded ASICs
» Steering ASICs on frame

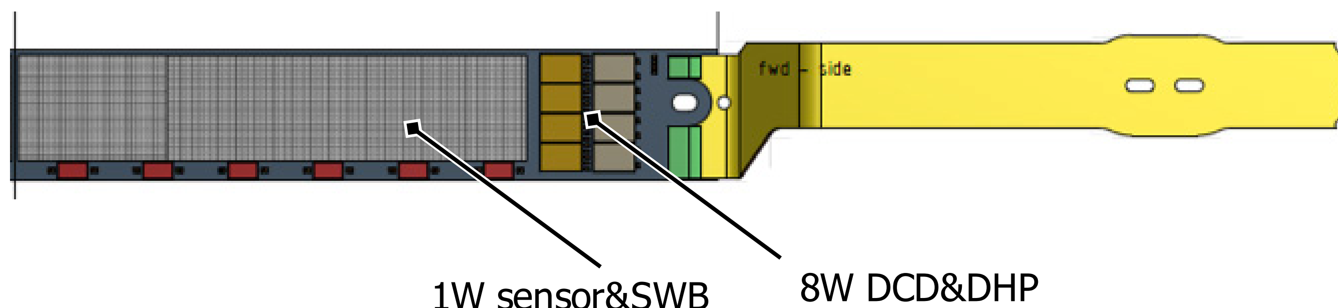
» Technology as for the barrel all-silicon ladder
  ↳ SOI wafer, etched back to SiO2
  ↳ if needed add narrow radial support bars

Status

» Mechanical feasibility study started
» SOI wafers for thermo-mechanical dummies

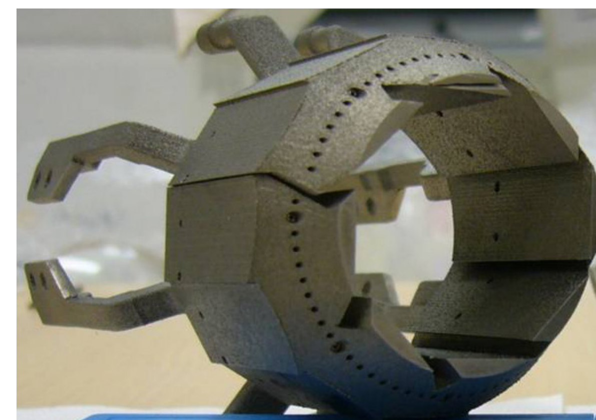
» Setups for thermal tests in preparation

Thermal management



- Belle II
  - 9W/half ladder, 8W at EOS
  - Active (CO_2) cooling at EOS, cooling block
- Power distribution at ILC very similar
- Power pulsing → 1/200??, 1/100??, 1/50??
- Air cooling mandatory (and most likely possible)
- at EOS still high power density, active cooling might be needed

→ How about micro cooling channels there ????

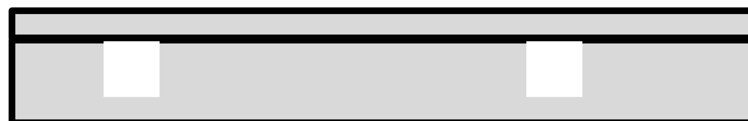


The idea

Start with oxidized handle wafer

Define lithographically micro-channels, etch oxide

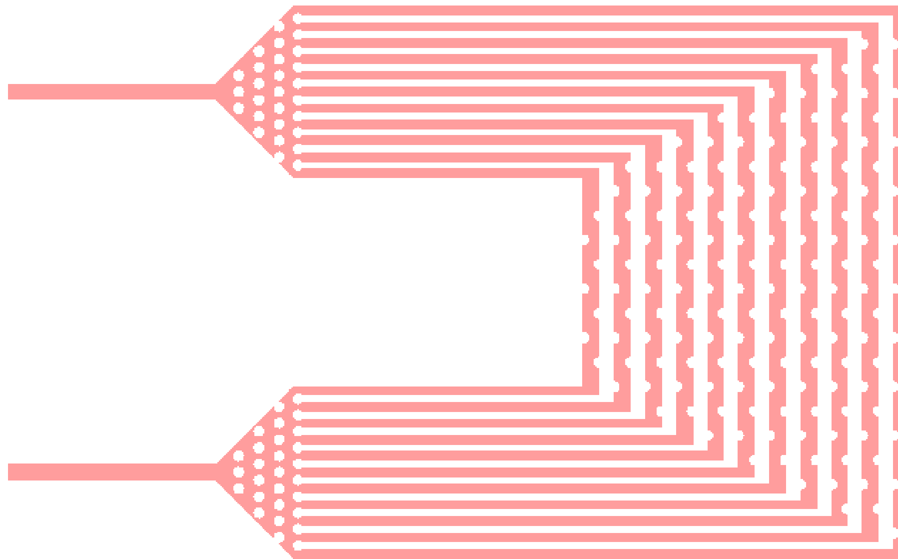
Etch micro-channels, blind via



» Bond prepared top wafer as usual
» Finish SOI wafer ("Cavity SOI")
» top wafer for DEPFETs
» Handle wafer with micro-channels under ASICs

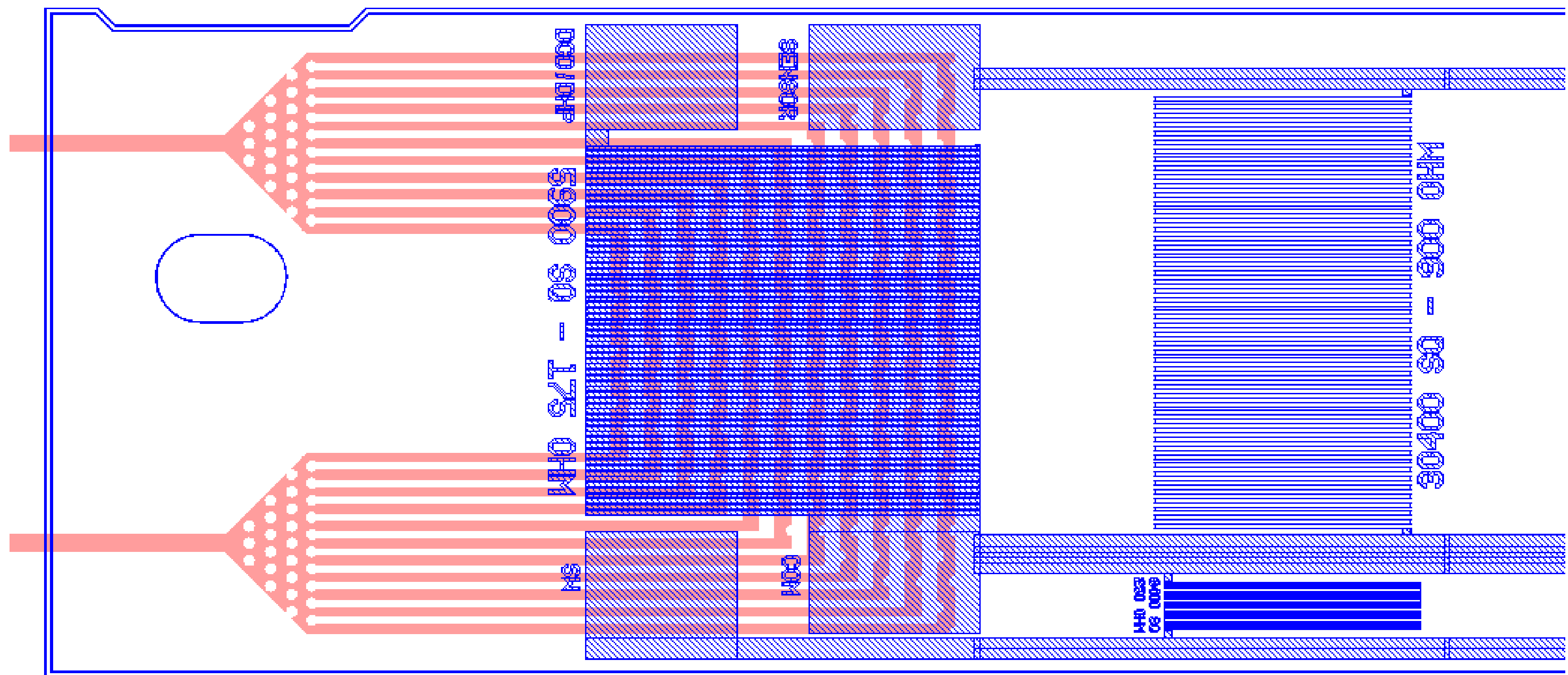
» Handle removed in sensitive area
» Channels exposed after cutting

Feasibility study



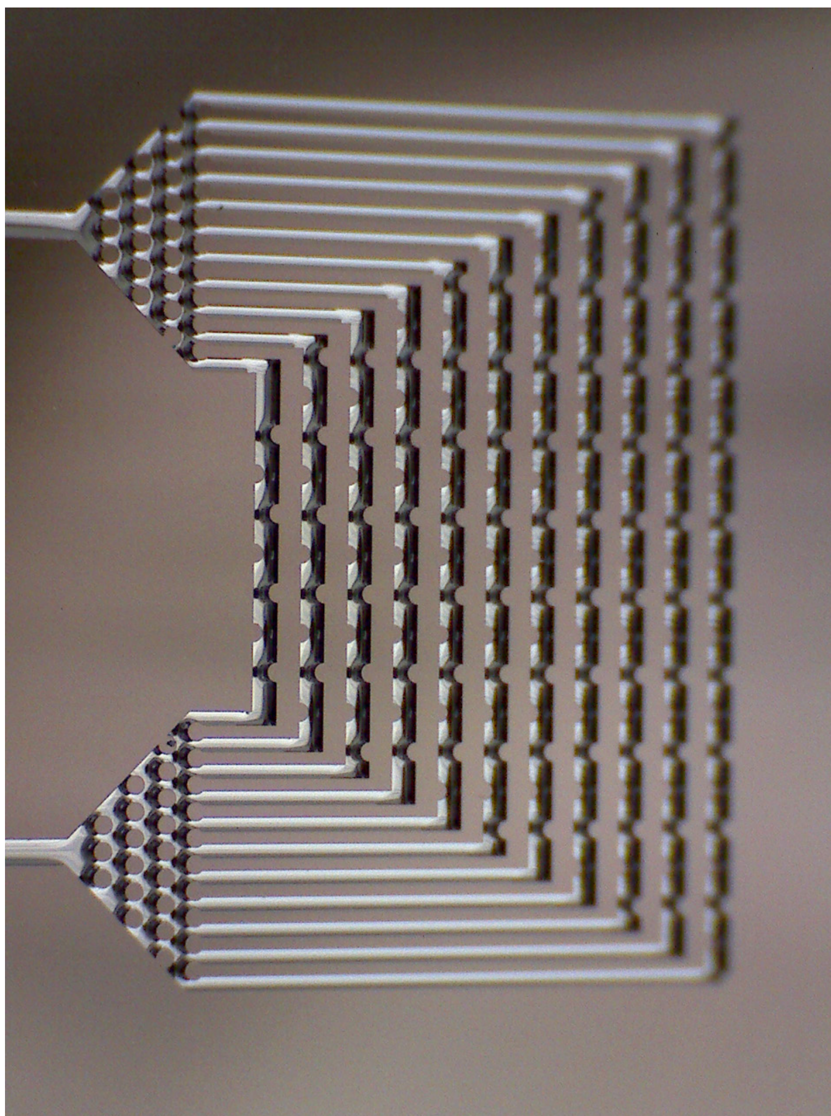
Micro-channel pattern in handle Wafer

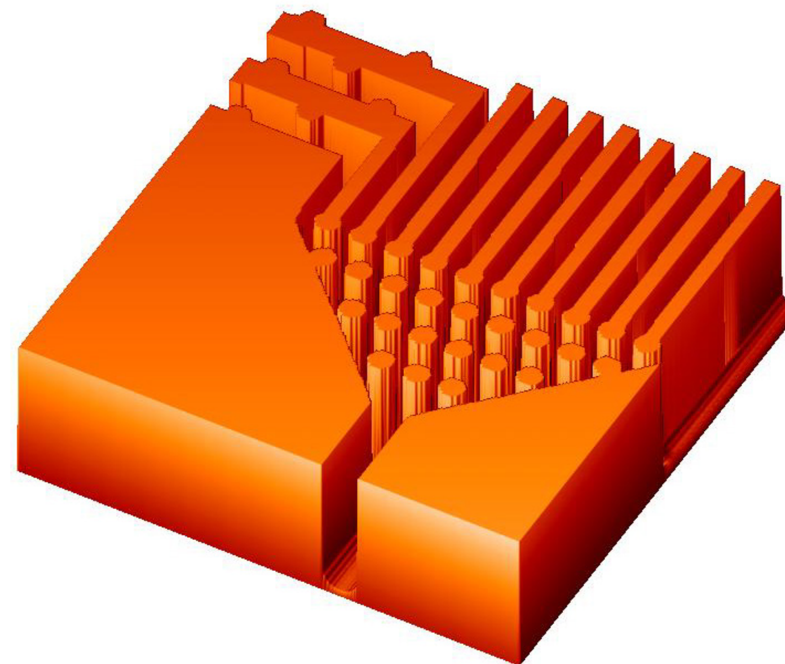
Feasibility study



Alu layer with resistor meanders on 75 µm thin top wafer

Handle wafer before bonding





Inlet and outlet is ~350 µm deep, 400µm wide
Cavity etch and SOI done at Icemos, Belfast

Status:

- ✓ CSOI finished
- ✓ first oxidation done ….

Summary

- **While the production of the Belle II DEPFET sensors is in full swing, we are qualifying the on- and off-module interconnect of the all-silicon ladder**
- **All findings and developments are relevant to the construction of an ILD DEPFET ladder**
  - ↳ **The Belle II ladder is a "prototype" for ILD VXD**
- **New exclusively ILC related activities are:**
  - ↳ **feasibility study for all-silicon DEPFET forward discs**
  - ↳ **Micro-channel cooling at the end-of-stave**

ILC and Belle II

» Both detectors have very similar requirements

	Belle II	**ILC**
Occupancy	0.1 hits/μm^2/s	0.13 hits/μm^2/s
Radiation damage	2 Mrad/year	< 100 krad/year
Duty cycle	1	1/200
Frame time	20 µs	25-100 µs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17°-155°	6°-174°

» ILC

↳ Excellent single point resolution (3-5 µm) → Small pixel size 25 μm^2

↳ Low material budget (0.1%X_0/layer)

» Belle II

↳ Modest spatial resolution (10 µm) → Moderate pixel size (50 x 75 μm^2)

↳ Few 100 MeV momenta → Lowest possible material budget (0.2% X_0/layer*)

* Including support Si, bumps and metal layers

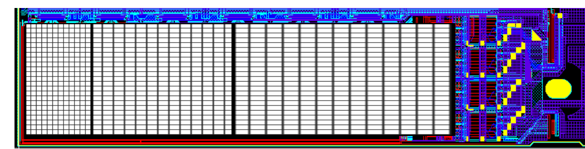
Requirement II: higher read-out speed

» 100ns per r/o → 2048 rows per half-ladder, 2-fold r/o → **~1/100µs frame rate state of the art**

» possible improvements (with current f/e electronics and ADC)

↳ **Sensor technology**: a third metal layer in the sensitive area is within reach

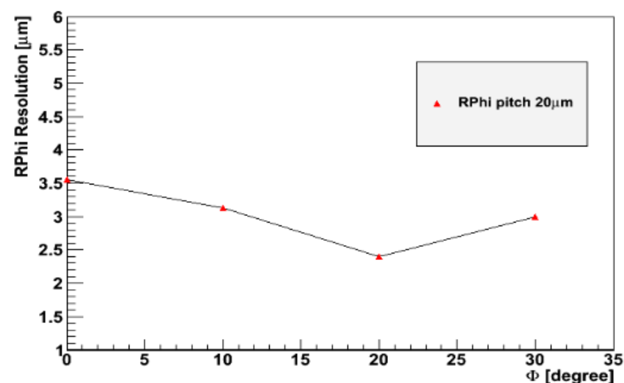
→ 4-fold read-out with small pixels → **1/50µs frame rate**



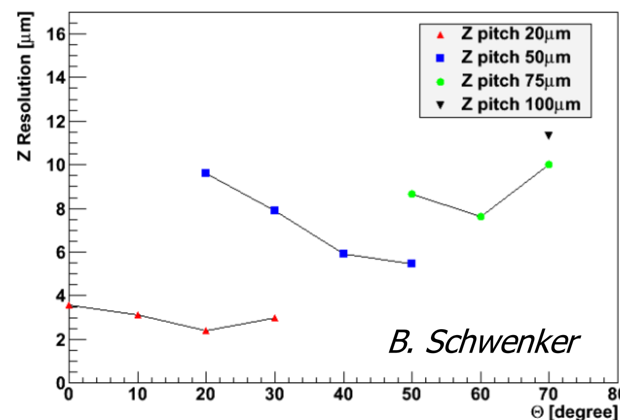
↳ **optimization** of cluster size for shallow(er) tracks

→ Introduce three regions in z with ~25µm/50µm/100µm pixel pitch in z (similar to Belle II)

→ #rows reduced by factor ~2 → **1/25 µs frame rate possible**



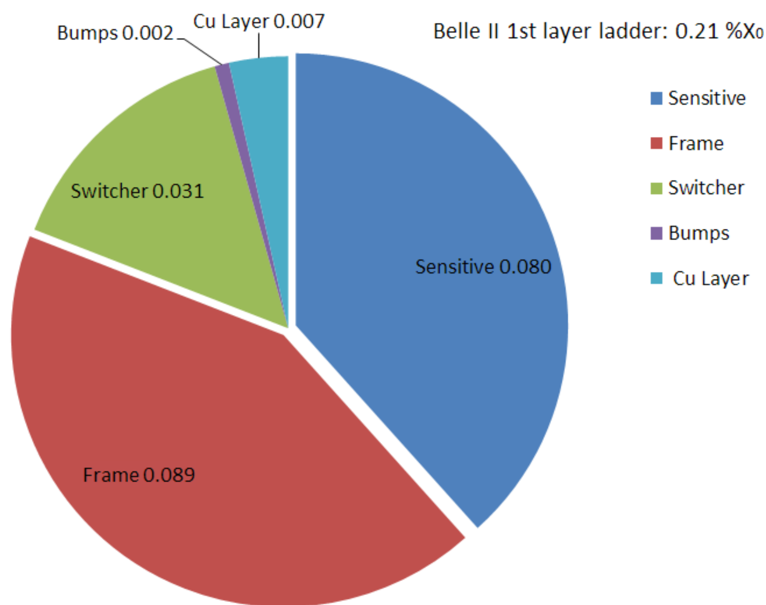
rφ-resolution varies between 2.3 - 3.5 µm

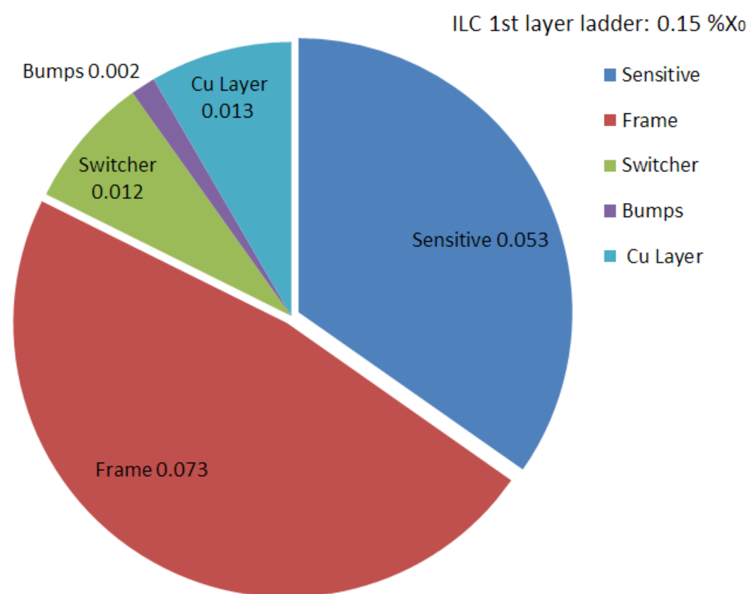


z-resolution is similar for Θ < 45°, degradation for shallower tracks

→ state of the art is factor 2 too low for ILC vertexing
↳ improve technology
↳ optimize pixel size, improve technology

Requirement III: even less material





	Belle II	ILC
Frame thickness	525 µm	450µm
Sensitive layer	75 µm	50µm
Switcher thickness	500µm	100µm
Cu layer	only on periphery	50% cover over all
Total	0.21 %X0	0.15 %X0

→ less material with small modifications/improvements of module technology within reach