CMOS Pixel Sensors for High Precision Vertexing : Recent Progress and Emerging Perspectives

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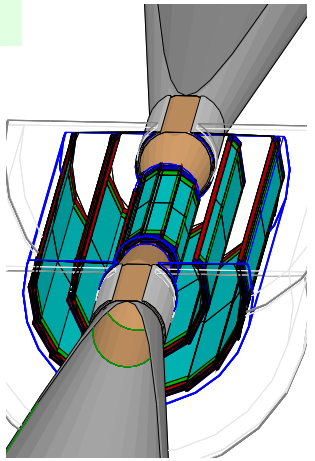
- Sensor design : contrib. from Y.Degerli (AIDA/Saclay) -

LCWS-13, Tokyo Univ., 12th Nov. 2013

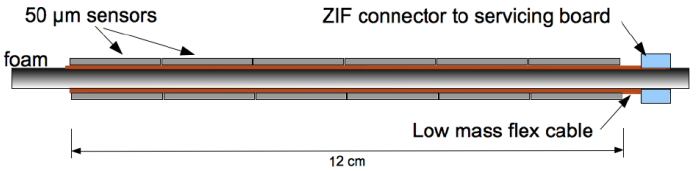
Outline

- *VXD concept based on CMOS Pixel Sensors (CPS)*
- *Status of CPS development for running at* $\sqrt{s} \lesssim$ *500 GeV* (0.35 μm process)
- *Improvements coming from 0.18* μm *CMOS process*
  - ↪ *fast CMOS sensor (AROM) with* μs *level timestamping*
- *First test results of 0.18* μm *CPS*
  - ↪ *perspectives of single bunch tagging possibility*
- *Summary*

CMOS Pixel Sensors for the ILD-VXD

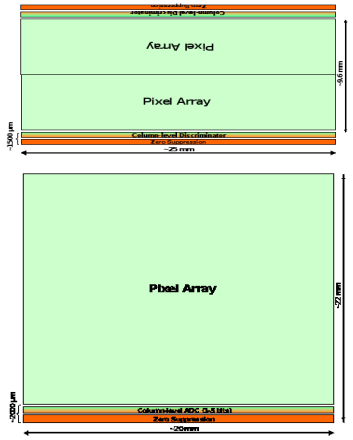


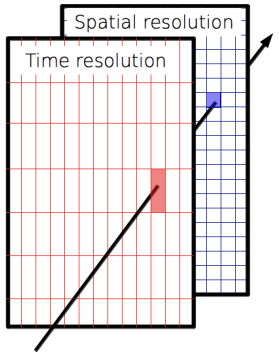
- **Two types of CMOS Pixel Sensors :**
  - ⁂ **Inner layers** ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small/stretched pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm
  - ⁂ **Outer layers** ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⁂ Total VXD instantaneous/average power $<$ 600/12 W (0.18 μm process)



- **2-sided ladder concept for inner layer :** PLUME coll.
  - ⁂ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)

    & *E*longated pixels (16×64/80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



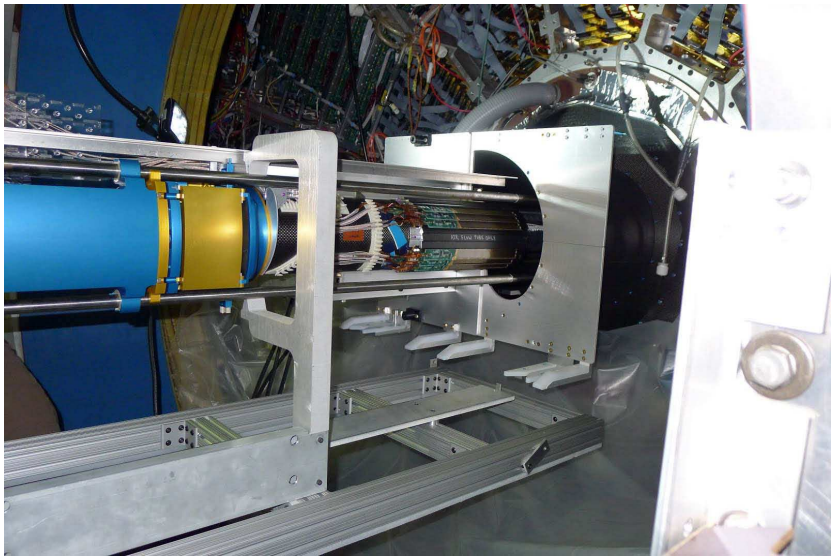


- **Final "500 GeV" CPS prototypes :** fab. in Winter 2011/12
  - ⁂ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷
    - ↪ one side : 256 pixels (16×16 μm^2)

      other side : 64 pixels (16×64 μm^2)
  - ⁂ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC
  - ⁂ prototypes were still fabricated in 0.35 μm CMOS process (cost saving)

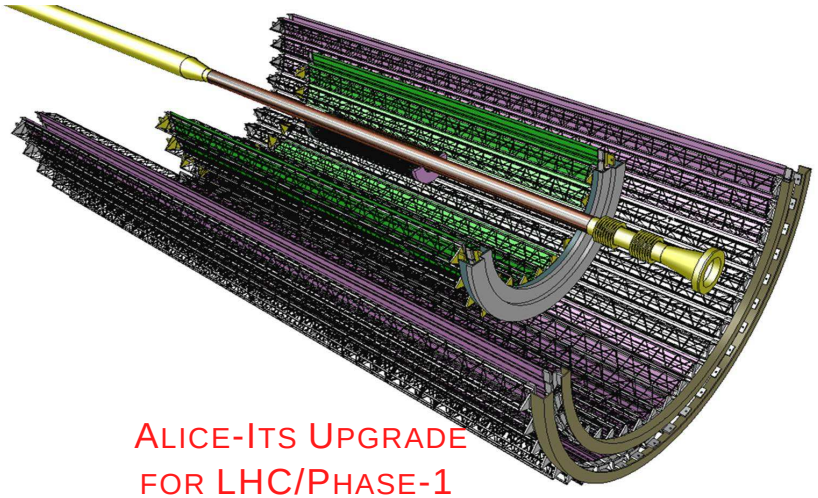
CMOS Pixel Sensors: Present Status

- ESTABLISHED ARCHITECTURE :
  - CMOS process : 0.35 μm, 2-well, 4 ML, 15/20 μm & $\sim$ 1 k$\Omega \cdot cm$ EPI
  - in-pixel CDS
  - end-of column discri. (binary encoding)
  - single-row rolling shutter read-out
  - sparse data scan on chip periphery
  - 18.4/20.7 μm pitch $\Rrightarrow$ $\gtrsim$ 3.3.5 μm resolution
  - used in EUDET BT (115 μs) & STAR-PXL (190 μs)
    - ▷ **recent step:** Commissioning of 3/10 STAR-PXL completed at RHIC with pp & ArAr collisions in May-June 2013



STAR-PXL-3SECT INSERTION
PP & ARAR RUN IN MAY-JUNE'13

- NEW PROCESS UNDER STUDY SINCE 2011/12 :
  - CMOS process : 0.18 μm, 4-well, 6 ML, 15/40 μm & $\sim$ 1-6 k$\Omega \cdot cm$ EPI
  - allows in-pixel discrimination $\Rrightarrow$ faster read-out & reduced power, etc.
  - development driven by ALICE-ITS upgrade & CBM-MVD/FAIR ($\sim$ 20 μs)
    - ▷ **recent step:** Assessment of CMOS proces detection performances & validation of rolling-shutter read-out completed in 2013

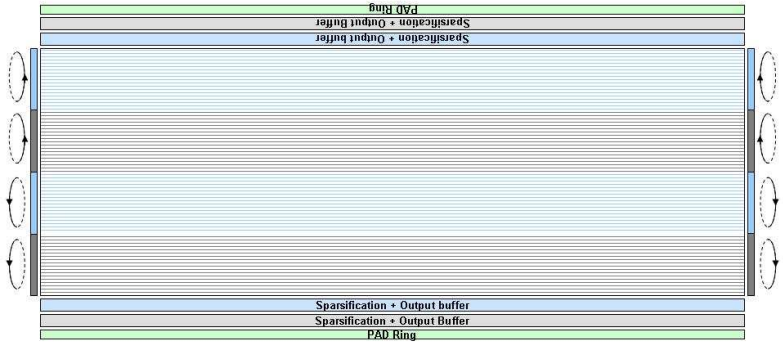


ALICE-ITS UPGRADE
FOR LHC/PHASE-1

Acceleration of Frame Read-Out

- **Motivations for faster read-out:**
  - ⁕ robustness w.r.t. predicted 500 GeV BG rate (keep inner radius small, ...)
  - ⁕ standalone inner tracking capability (e.g. soft tracks)
  - ⁕ compatibility with high-energy running: expected beam BG at $\sqrt{s} \gtrsim 1$ TeV $\simeq$ 3–5$\times$BG (500 GeV)

- **How to accelerate the elongated pixel read-out**
  - ⁕ elongated pixel dimensions allow for in-pixel discri. $\Rrightarrow$ $\geq$ 2 faster r.o.
  - ⁕ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⁕ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm process needed: 6-7 ML, design compactness, in-pixel CMOS T, ...
  - ⁕ conservative step: 2 discri./col. **end** (22 μm wide) $\Rrightarrow$ simult. 2 row r.o.



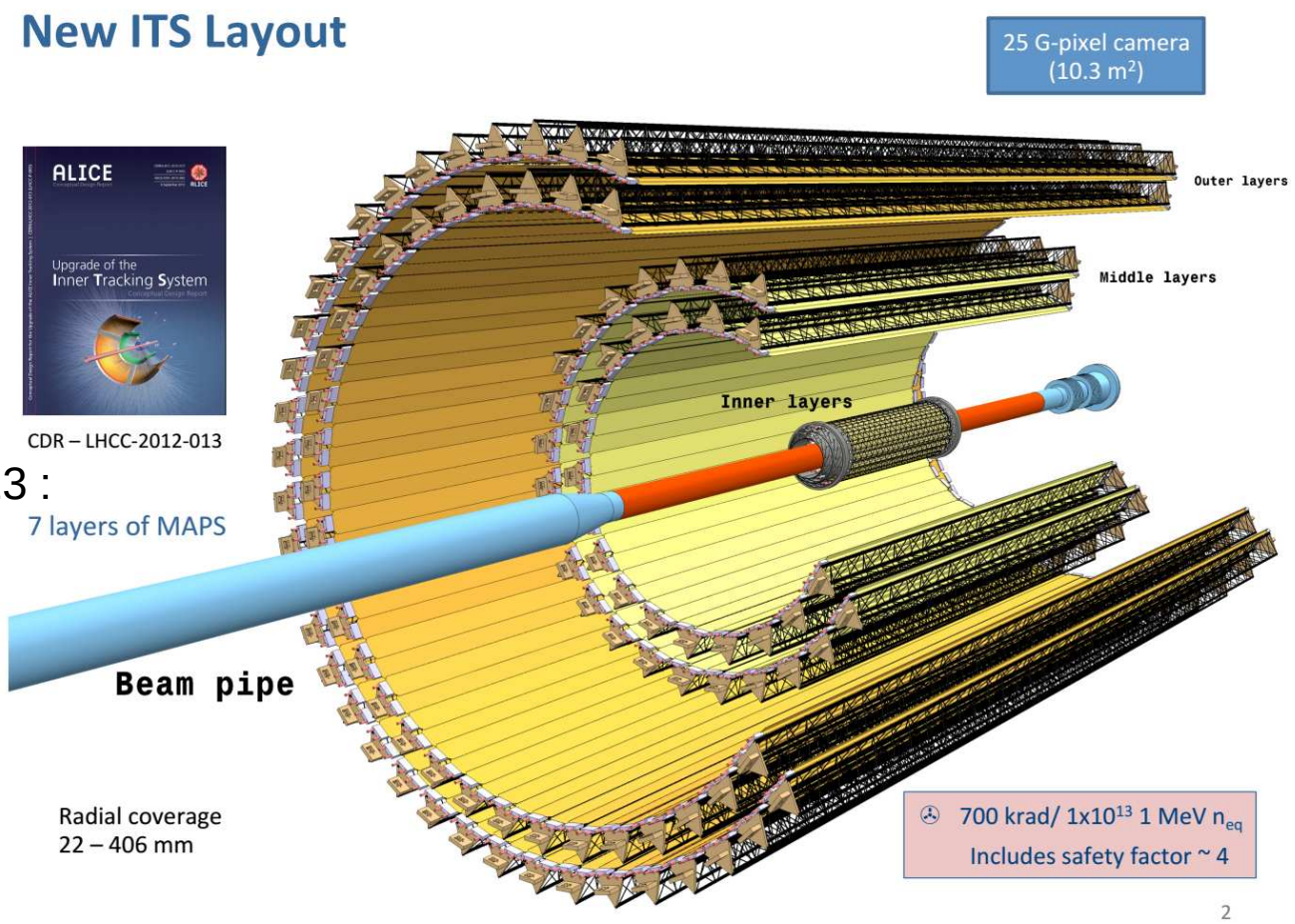
- **Expected VXD performances at 1 TeV (and 0.5 TeV)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** 1 TeV (0.5 TeV)	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (10 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

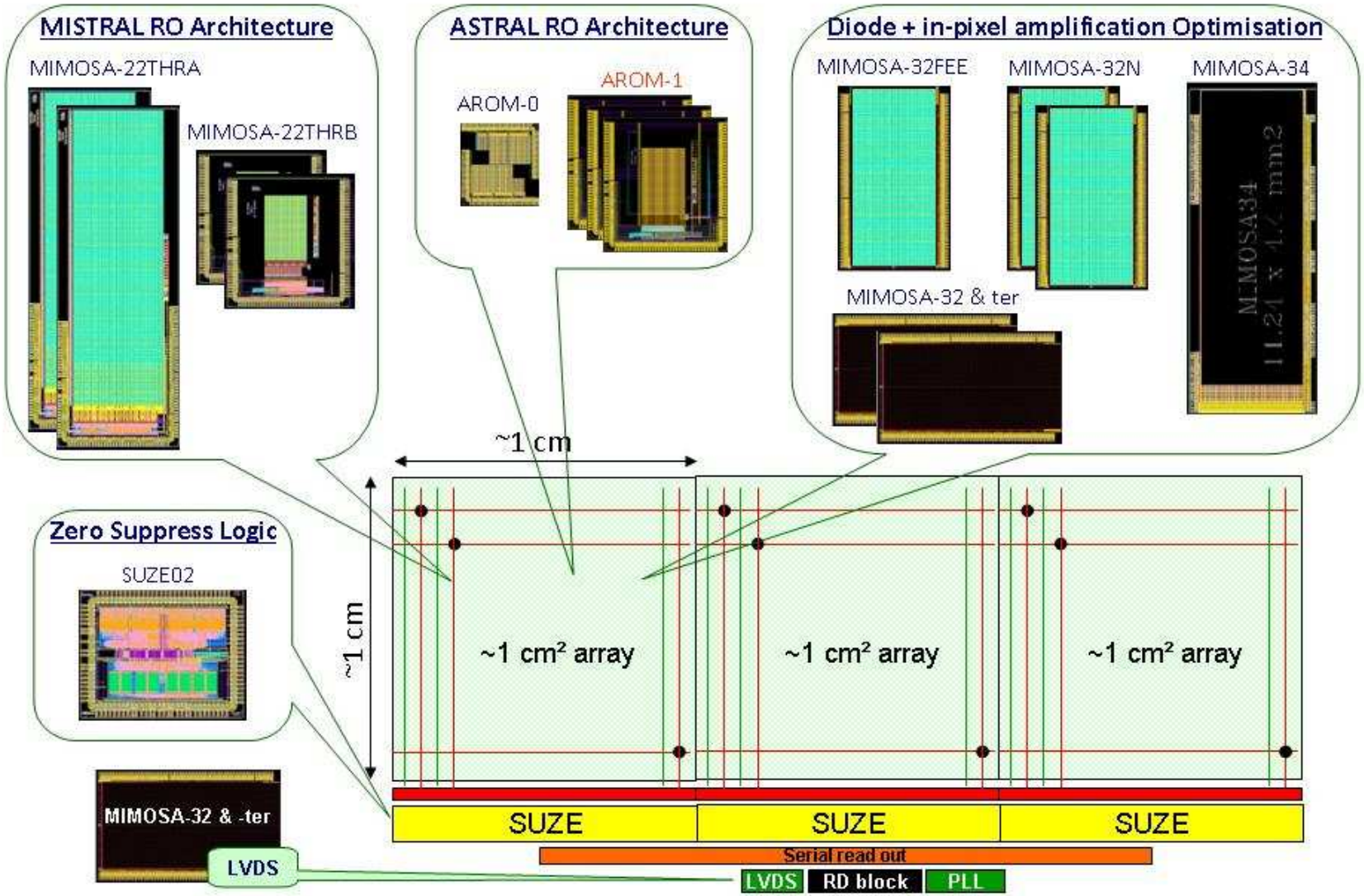
ALICE-ITS Upgrade

- 2 alternative sensors developped :
  - ⁕ Baseline : **ASTRAL** (in-pixel discri.)
    - ↪ $\gtrsim$ 15 μs, 85 mW/cm^2
  - ⁕ Back-up : **MISTRAL** (end-of-col. discri.)
    - ↪ $\gtrsim$ 30 μs, $<$ 200 mW/cm^2

- All main components investigated in 2013 :
  - ⁕ sensing node properties
  - ⁕ in-pixel ampli+CDS
  - ⁕ in-pixel discriminators
  - ⁕ rolling-shutter with end-of-col. discri.
  - ⁕ simultaneous 2-row read-out
  - ⁕ sparse data scan
  - ⁕ programmable chip steering (JTAG)



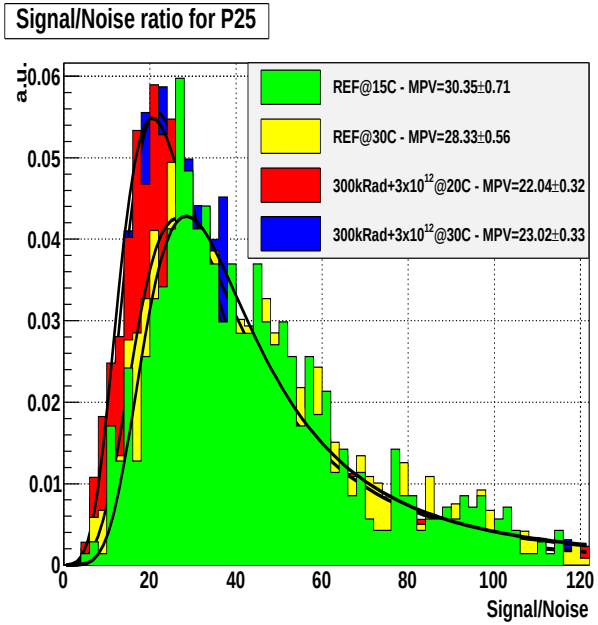
CPS fabricated in 2012/13 in 0.18 μm Process

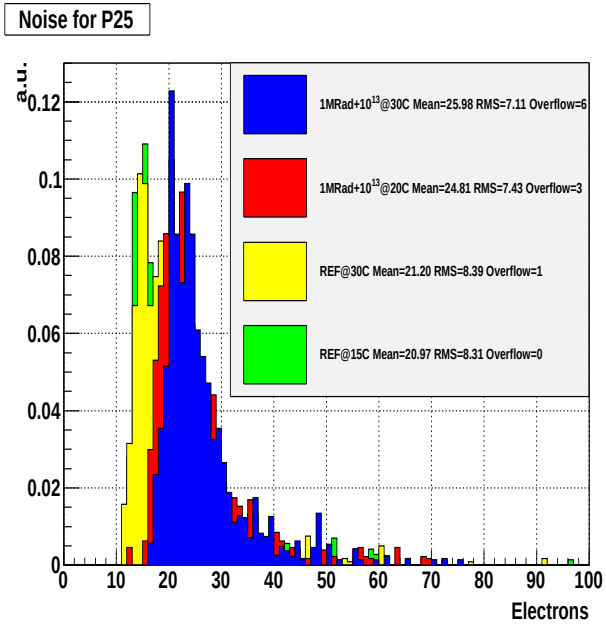


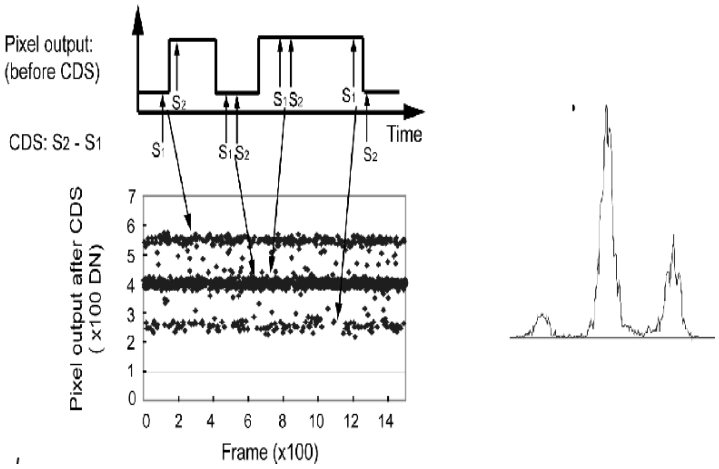
Outcome of 2012 Exploration of the 0.18 μm Process

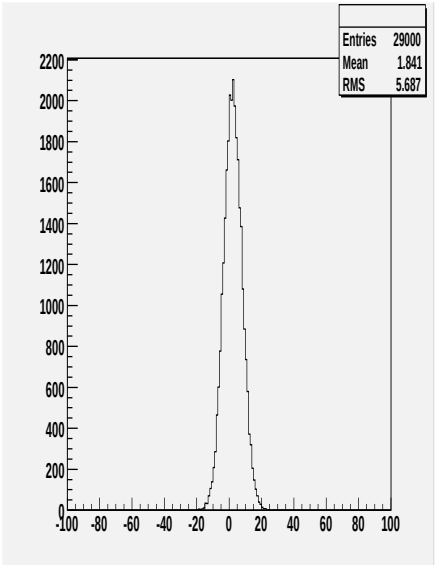
- STEPS VALIDATED IN 2012 :
  - ⁂ Several in-pixel amplifier variants lead to satisfactory SNR & det. eff. ($20 \times 20\ \mu m^2$) incl. after 1 MRad & $10^{13} n_{eq}/cm^2$ at 30°C
  - ⁂ Results pres. at VCI-2013 (J. Baudot)

- CALL FOR IMPROVEMENT :
  - ⁂ **Pixel circuitry noise :**
    tail due few noisy pixels
    ↪ **attributed to RTS noise**
    ⇒ required optimising T geometries



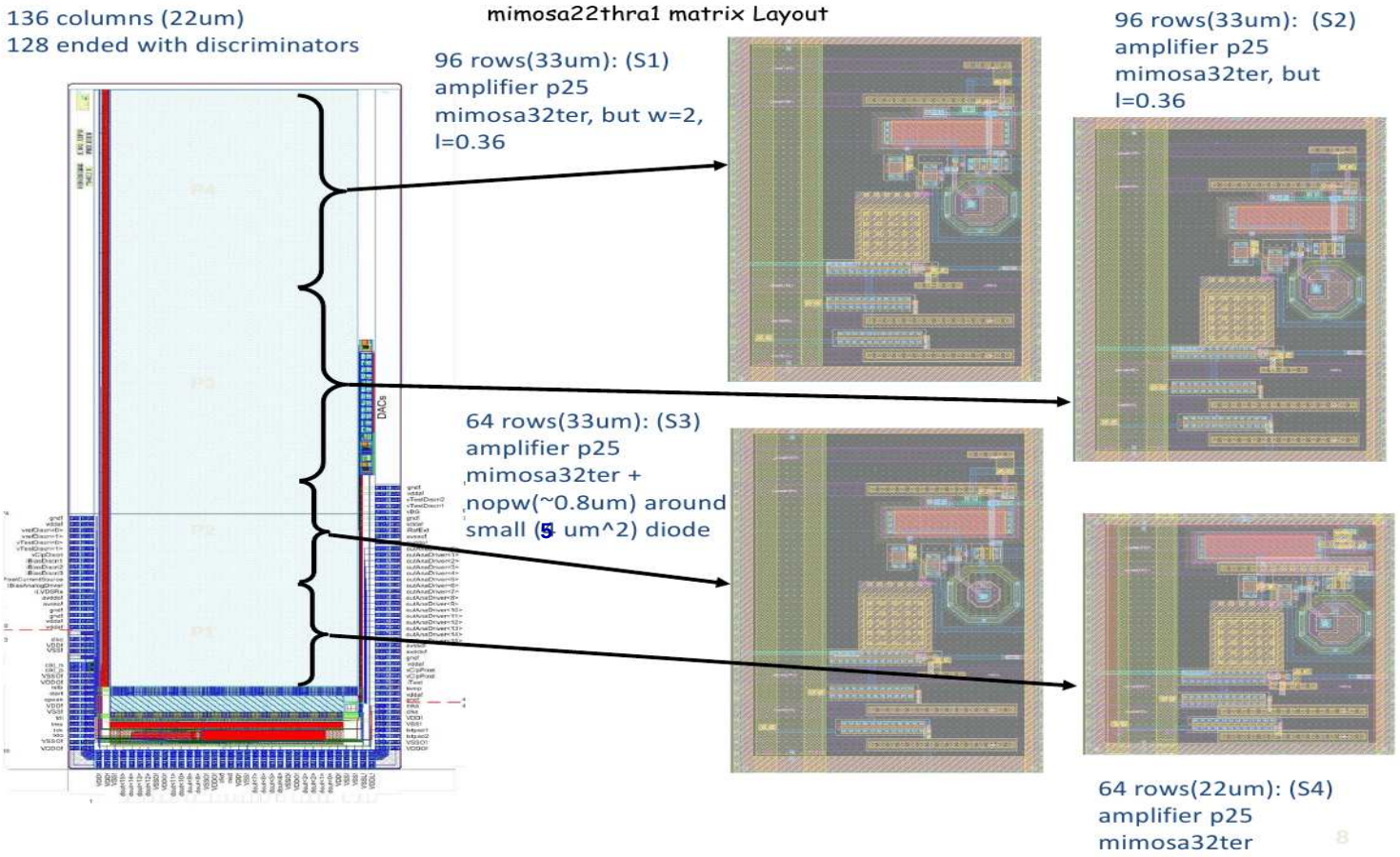






MISTRAL : In-Pixel + Read-Out Circuitry Studies

- **MIMOSA-22THRa1 : single row read-out ($\equiv$ MIMOSA-28/STAR-PXL)**
  - ⁕ 128 col. of 320 pixels (22$\times$22/33 μm^2) ended with a discri. + 8 col. without discri. for tests
  - ⁕ In-pixel CDS in 4 variants (2 with enlarged pre-amp T gate against RTS noise)
  - ⁕ Rolling-shutter (single row) read-out $\longrightarrow$ $t_{int} \simeq 50\ \mu s$



MISTRAL : In-Pixel + Read-Out Circuitry Studies

- **MIMOSA-22THR threshold scans of single- & double-row read-out to derive TN and FPN**

- **TN of single-row array:**

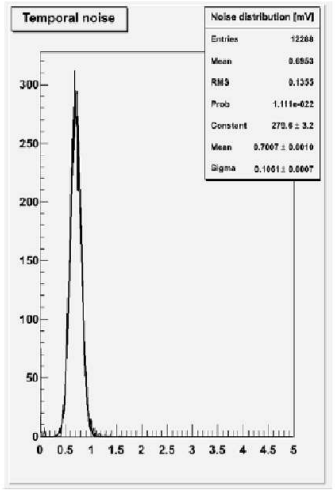
  ⁂ S4 pre-amp T gate : L/W = 0.18/1 μm

  ⟶ TN ∼ 17 e^- ENC **+ tail**

  ⁂ S2 & S1 pre-amp T gate : L/W = 0.36/1 & 2 μm

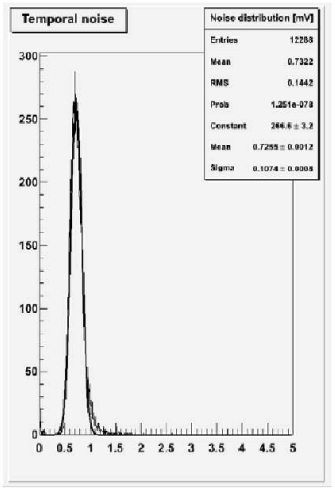
  ⟶ TN ∼ 16–18 e^- ENC **with minor/no tail**

  ⇛ **Effective mitigation of noise tail by doubling input T gate dimensions**



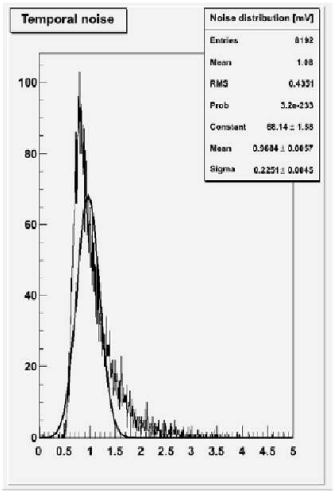
S1 (L & W increase)

Low Res	HR18 >1kO	HR20 >2kO
TN: 695 µV	TN: 670 µV	TN: 682 µV
FPN: 168 µV	FPN:176µV	FPN: 175 µV



S2 (L increase)

Low Res	HR18 >1kO	HR20 >2kO
TN: 732 µV	TN: 692µV	TN: 702 µV
FPN: 178 µV	FPN: 183µV	FPN: 175 µV



S4 (P25 mi32Ter)

Low Res	HR18 >1kO	HR20 >2kO
TN: 1080 µV	TN: 945µV	TN: 980 µV
FPN: 207 µV	FPN: 208µv	FPN: 212 µV

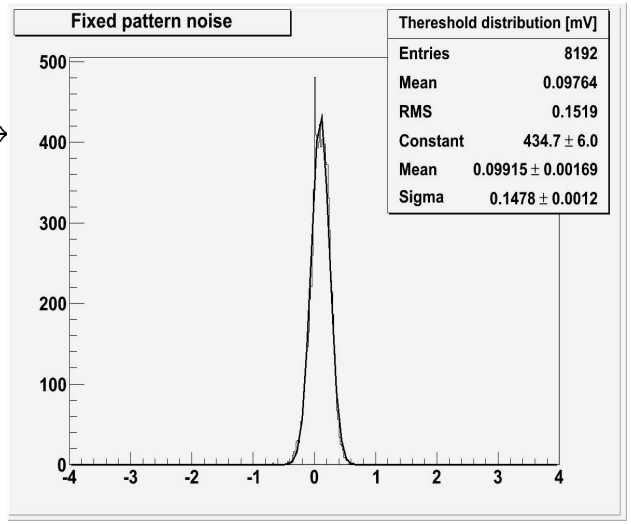
- **FPN of 2-row r.o. (2 discri./col.):**

  ⁂ Concern: analog/digital signals coupling ⇛ FPN ⟶

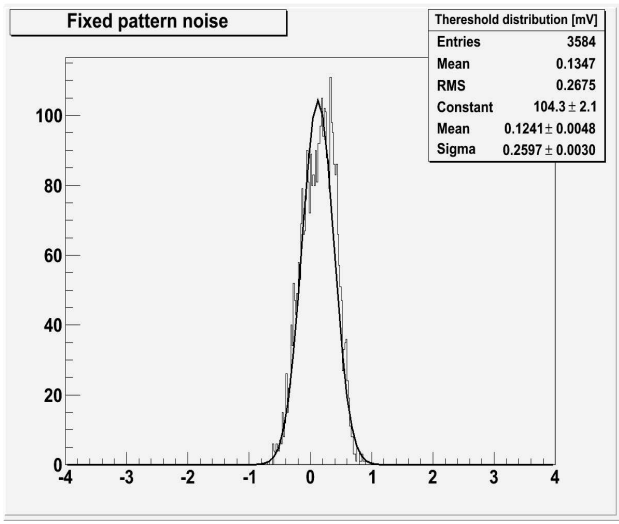
  ⁂ Measured FPN (dble-row) $\lesssim$ 5 e^- ENC

  ⟶ FPN (sgle-row) $\lesssim$ 3 e^- ENC

  ⇛ **Marginal noise increase**



1 discri./col.



2 discri./col.

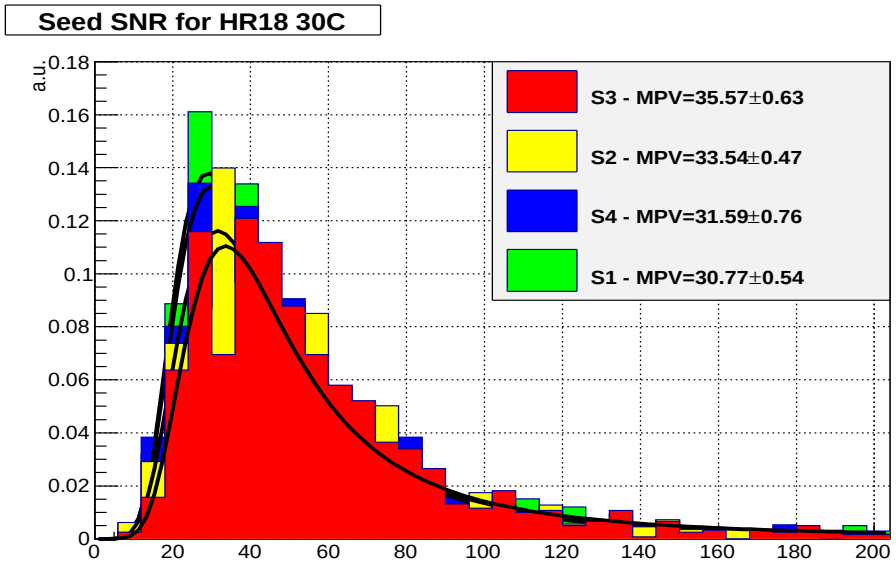
SNR of Pixel Array

- MIMOSA-22THRa1 exposed to $\sim$ 4.4 GeV electrons (DESY) in August 2013
- Analog outputs of 8 test columns (no discri.)

  $\hookrightarrow$ SNR with HR-18 epitaxy, at T=30°C

  ✳ Noise determination with beamless data taking

  ✳ Ex: S2 (T gate L/W=0.36/1 μm against RTS noise)
  S1 (T gate L/W=0.36/2 μm against RTS noise)

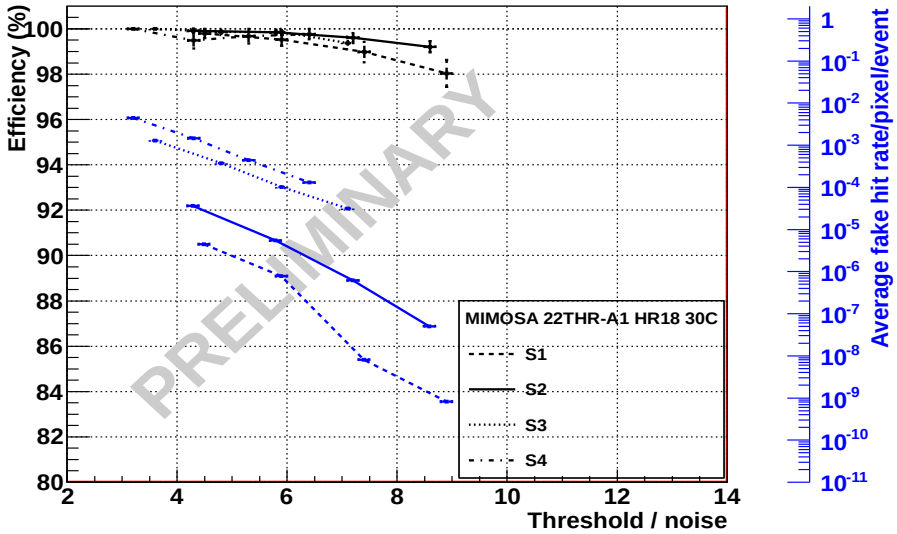


- Results :

  ✳ Charge collected in seed pixel $\simeq$ 550 e^-

  ✳ Binary read-out : detection efficiency of S1 & S2
  $\gtrsim$ 99.5% while Fake rate $\lesssim$ O(10^{-5}) for
  Discriminator Thresholds in range $\sim$ 5N – 8N

  ✳ Mitigation of Fake Hits due to RTS
  noise fluctuations confirmed



  ✳ A few 10^{-3} residual inefficiency calls
  for in-pixel circuitry optimisation

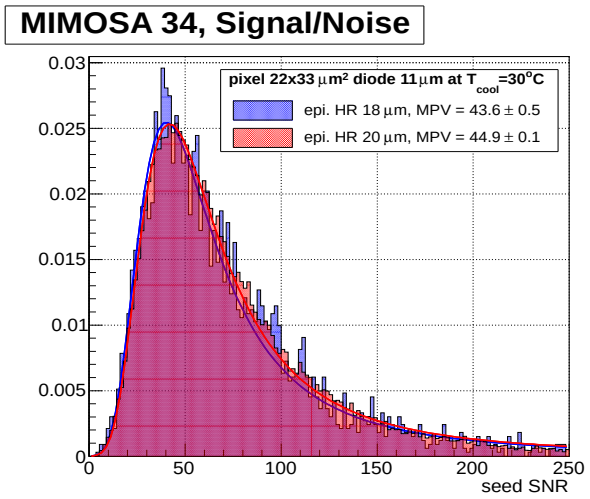
  $\Rightarrow$ new design in perspective of next submissions

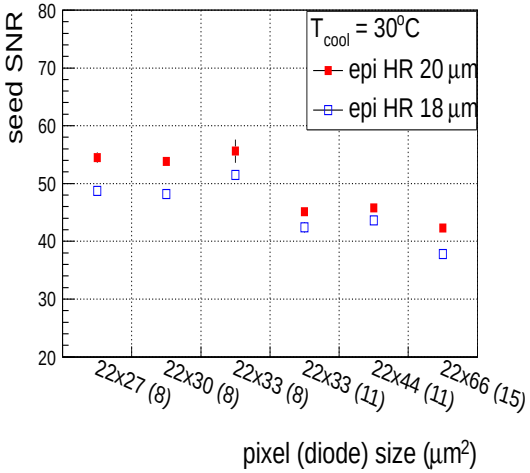
Pixel Optimisation : Epitaxial Layer and Sensing Node

- **Pixel charge coll. perfo. for HR-18 & VHR-20 (no in-pixel CDS) :**
  - ⁂ SNR distributions ⟼ MPV & low values tail
  - ⁂ $22 \times 33\ \mu m^2$ (2T) pixels at 30°C

⇛ **Results :**

- ◇ only ∼ 0.1 % of cluster seeds exhibit SNR $\lesssim$ 7–8
- ◇ SNR(VHR-20) ∼ 5-10% higher than SNR(HR-18)

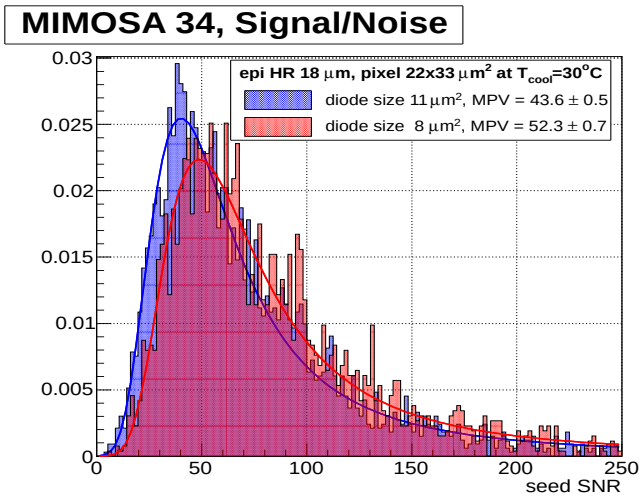


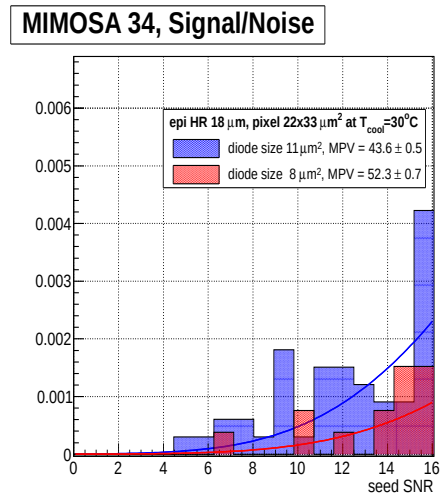


- **Pixel charge coll. perfo. for 2 diff. sensing nodes:**
  - ⁂ 10.9 μm^2 large sensing diode
  - ⁂ 8 μm^2 cross-section sensing diode underneath 10.9 μm^2 large footprint

⇛ **Results :**

- ◇ 8 μm^2 diode features nearly 20% higher SNR(MPV) & much less pixels at small SNR (e.g. SNR <10)
  - ⟼ $Q_{clus} \simeq$ 1350/1500 e^- for 8/10.9 μm^2
  - ⇛ marginal charge loss with 8 μm^2 diode





ASTRAL : AROM-0 Pixel Design

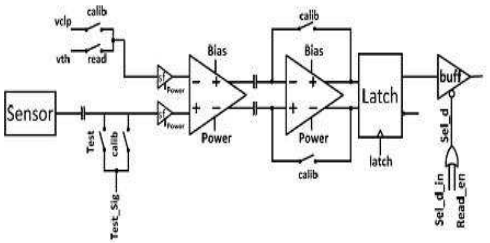
- **Chip contents :**
  - ⁂ 2 different sub-arrays of 32×32 pixels with single row read-out
    ⇛ t_{Int} = 3.2 μs
  - ⁂ 1 sub-array of 16×16 pixels with double-row read-out
  - ⁂ pixel dimensions : 22×33 μm^2

- **3 alternative pixel schematics :**
  - ⁂ sensing node & pre-amp as in MIMOSA-22THRa1 pixel (P25)
  - ⁂ various amplification schemes (offset compensation alternatives)
  - ⁂ various clamping circuitry implementations and designs

- **Design (layout) constraints wrt end-of-column discriminators :**
  - ⁂ originate from limited space & power saving
  - ⁂ matching more delicate ⇛ FPN
  - ⁂ less offset compensation capacitors ⇛ FPN
  - ⁂ discriminator alternatively switched on & off ⇛ TN, FPN

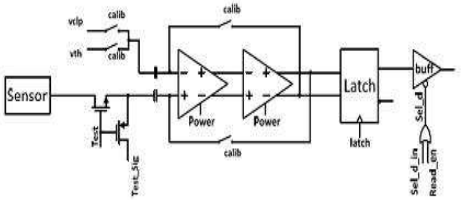
Different versions of pixel:

Version 1

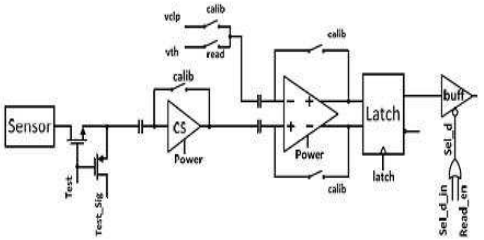


Version 2

V2



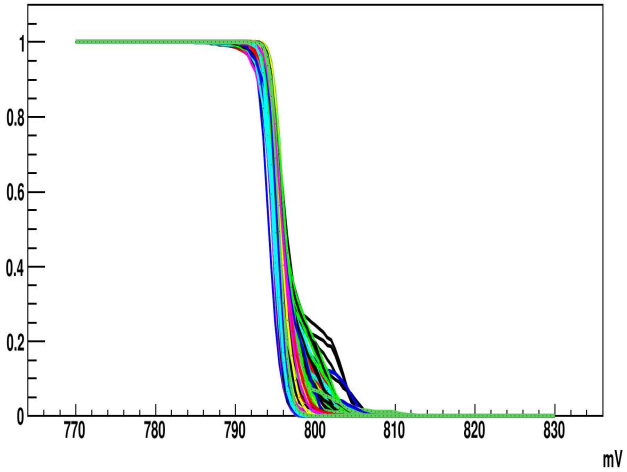
Version 3



ASTRAL : AROM-0 Test Results

- **Tests realised in lab :**
  - ⁕ Characterise analog output (after pre-amp)
  - ⁕ Characterise digital output (after discri)
  - ⁕ Assess TN and FPN at room temperature
    and nominal frequency ($\Rightarrow$ t_{Int} = 3.2 μs)

- **Preliminary results** *(compared to MIMOSA-22THRa1/S4)* **:**



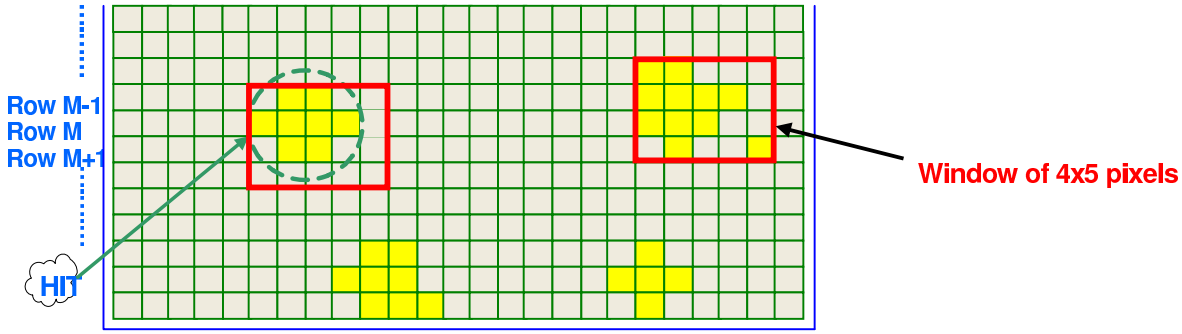
$\Rightarrow$

Chip	TN(pix)	TN(discri)	FPN(discri)	Total N
AROM-0	$\lesssim$ 1 mV	$\sim$ 1 mV	$\lesssim$ 0.5 mV	$\gtrsim$ 1.5 mV
MIMOSA-22THRa1	$\lesssim$ 1 mV	$\ll$ 1 mV	$\lesssim$ 0.2 mV	$\lesssim$ 1.mV

- **Comments on results :**
  - ⁕ TN (discri) is too high by factor of $\sim$ 2 (only)
  - ⁕ FPN (discri) is almost acceptable but it may increase when moving to large area
  - ⁕ Total noise is $\sim$ 1.5-2 times too high $\Rightarrow$ AROM-1 in fabrication to validate noise reduction approach

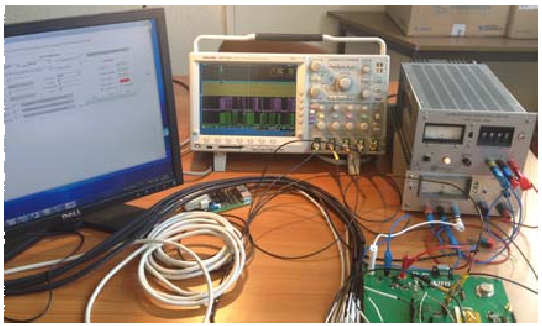
Zero Suppression Logic (SUZE02)

- *AD conversion (pixel-level or column-level) outputs are connected to inputs of SUZE*



- *More efficient encoding then the previous one (SUZE01) implemented in ULTIMATE sensor*
  - *It is sizable and suitable to process the binary information coming from a 1 cm large pixel array*
    - *Hit density of ~100 hits/cm² + safety factor of 3-4*
    - *Compression factor: 1 to 4 order of magnitudes*
  - *It searches windows of 4x5 pixels which contain hit cluster information*
  - *Results are stored in 4 SRAM blocks allowing either continuous or triggered readout*
  - *Sparsified data are multiplexed onto a serial LVDS output*
    - *Prototype data rate: 320 Mbit/s per channel (1 or 2 channels in SUZE02)*

- *Preliminary test results: SUZE02 is functional for main configurations @ full speed*
  - *Full sequence of signal processing steps were validated using various types of patterns*
  - *SEU has to be evaluated*



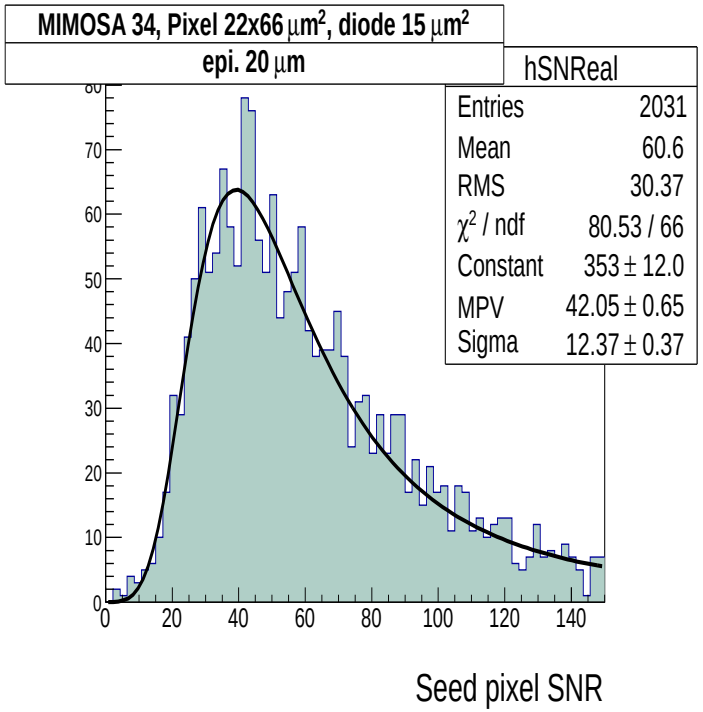
- *For MISTRAL / ASTRAL, a data rate of 0.5-1 Gbit/s is required*
  - *One channel output per sensor*
    - *INFN Torino is working on data transmission up to 2 Gbit/s*

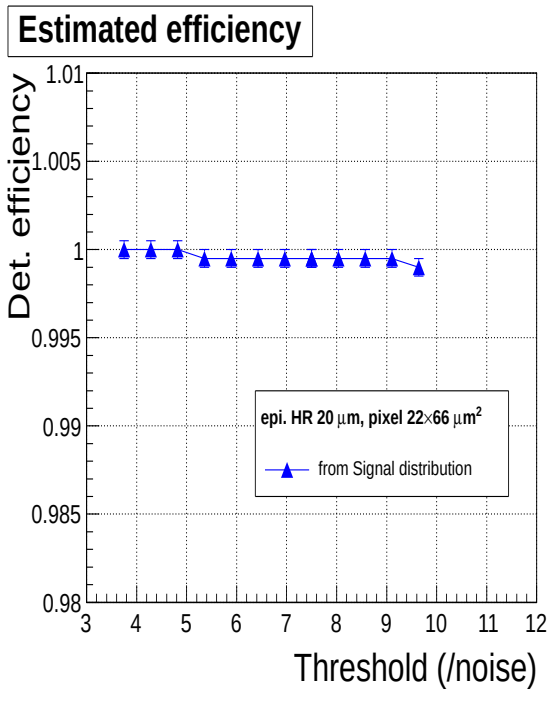
- *Next development step needs trigger's specifications*

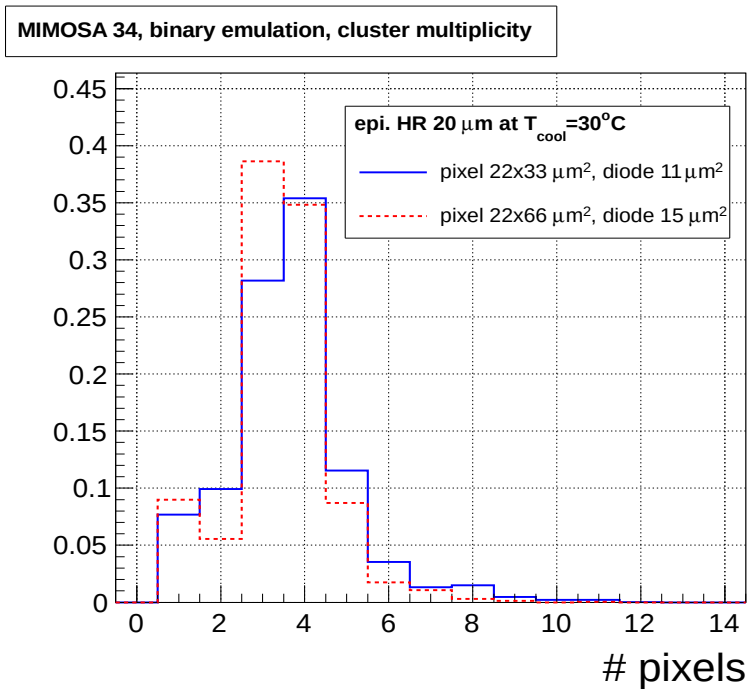
Stretched Pixels for Time Stamping

- **Motivation for LARGE pixels :** reduced number of pixels per column

  ⇛ shorter read-out time & coarser spatial resolution







- **Difficulty :** keep high CCE (all over the pixel) without substantial (capacitive) noise increase and gain loss

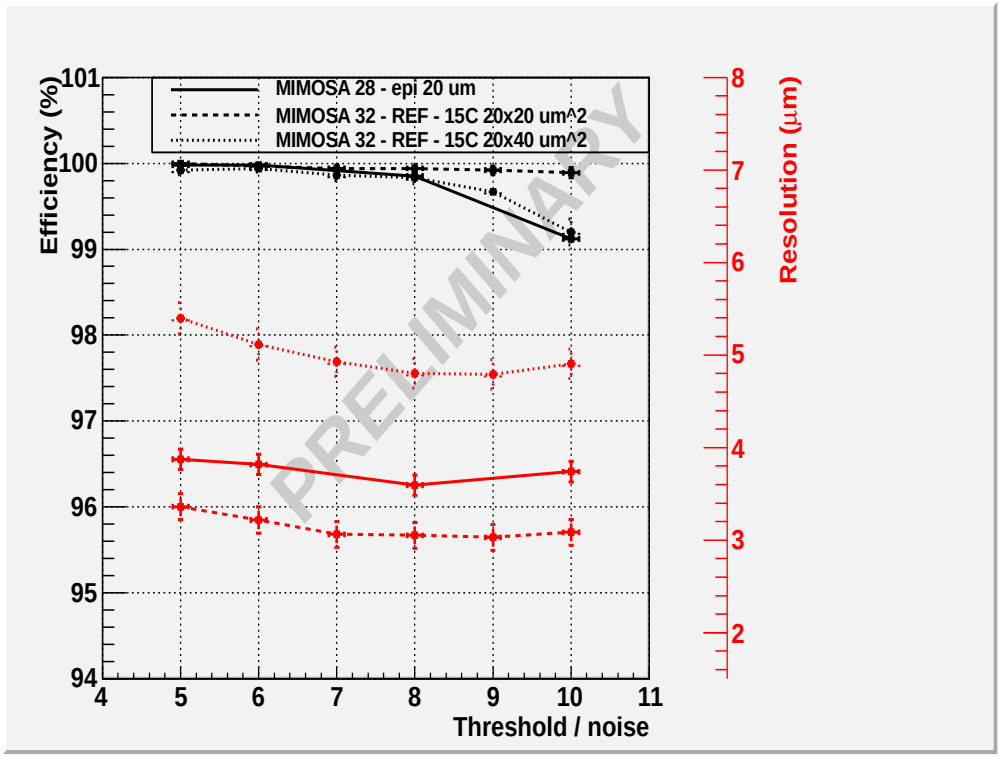
- **Results :** tests with 4.4 GeV electrons, no in-pixel CDS

  ⁕ SNR(MPV) ≃ 42.1 ± 0.7 ⇛ $\epsilon_{det} \simeq 100$ %

  ⁕ cluster multiplicity (22×66) ≃ cluster multiplicity (22×33) ≃ 3 (mean)

Spatial Resolution

- **Beam test (analog) data used to simulate binary charge encoding :**
  - ✳ Apply common SNR cut on all pixels using $<N>$
    ↪ simulate effect of final sensor discriminators
  - ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33, 20x40, 22x66 μm^2 pixels

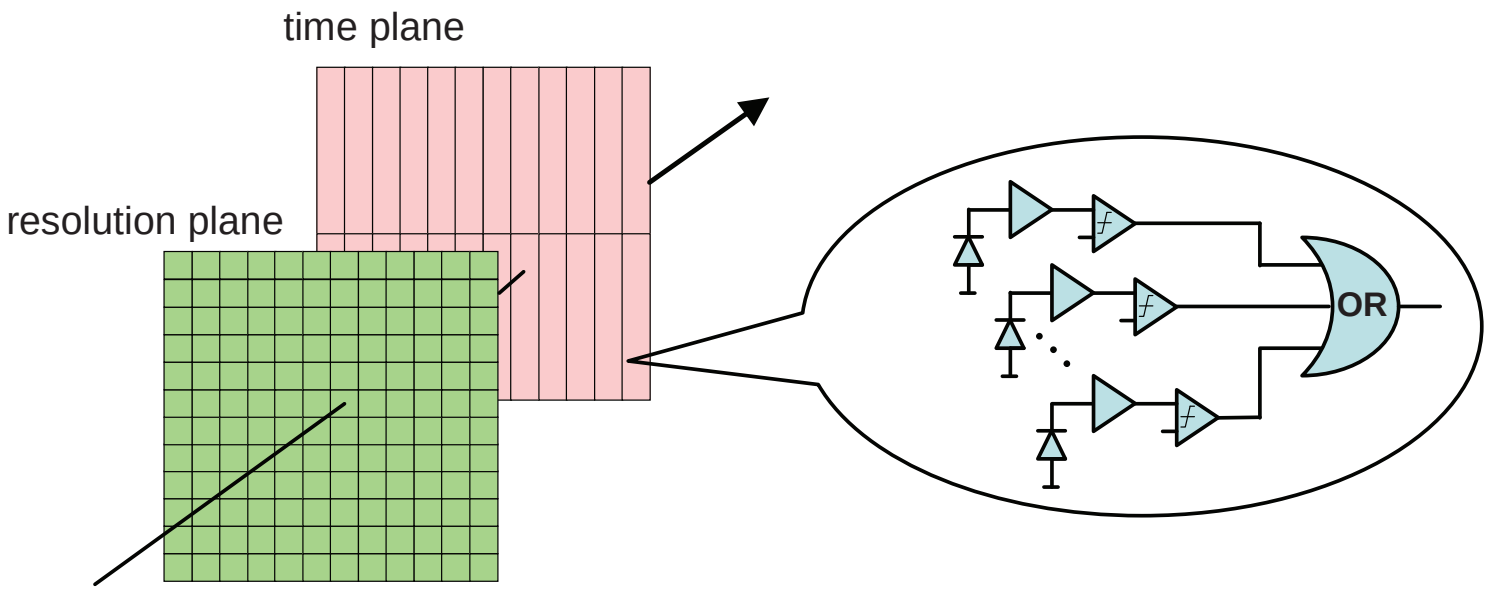


- **Comparison of 0.18 μm technology ($> 1\ k\Omega \cdot cm$) with 0.35 μm technology ($\lesssim 1\ k\Omega \cdot cm$)**

Process ▷	0.35 μm	0.18 μm			
Pixel Dim. [μm^2]	20.7×20.7	20×20	22×33	20×40	22×66
$\sigma_{sp}^{bin}[\mu m]$	3.7 ± 0.1	3.2 ± 0.1	∼ 5	5.4 ± 0.1	∼ 7

Long Range Plan Addressing Stretched Pixel

- Resolution plane:
  - Pixel pitches: ex. 17x17 μm²
  - 640 rows
  - Readout time ~50 ns/row ➔ 32 μs
- Time plane
  - Pixel pitches: ex. 17x1024 μm²
  - 10 rows
  - Readout time ~50 ns/row, ➔ 500 ns



SUMMARY

- **CPS are getting validated in subatomic physics experiments**

  ↪ *STAR-PXL: 400 sensors in 0.35 μm process, 350 Mpixels, 0.37 % X_0, 190 μs, 3.7 μm, 160 mW/cm^2*

- **Recently addressed 0.18 μm CMOS process offers perspective of faster read-out suited to :**
  - 1 TeV ILC running conditions
  - standalone Si tracking based on track seeds in VXD
  - Added value : substantial improvement of radiation tolerance

- **Preliminary test results of 0.18 μm CMOS technology indicate that it is the 1st CMOS process allowing to come close to the real CPS potential :**
  - innermost layer : $<$ 3 μm and $\lesssim$ 2 μs
  - outer layers : $<$ 4 μm and $\lesssim$ 10 μs
  - VXD power consumption : $<$ 600 W (inst.) / $<$ 12 W (average)

- **0.18 μm CPS development sustained by ALICE-ITS, CBM-MVD, AIDA-BT :**
  - 2012: validation of charge sensing properties ✓
    - 2013: validation of upstream and downstream sensor elements ✓
      - 2014/15: validation of complete sensor architecture with "1 cm^2" MISTRAL/ASTRAL prototype
        - 2015/16: pre-production of MISTRAL/ASTRAL sensor for ALICE and CBM

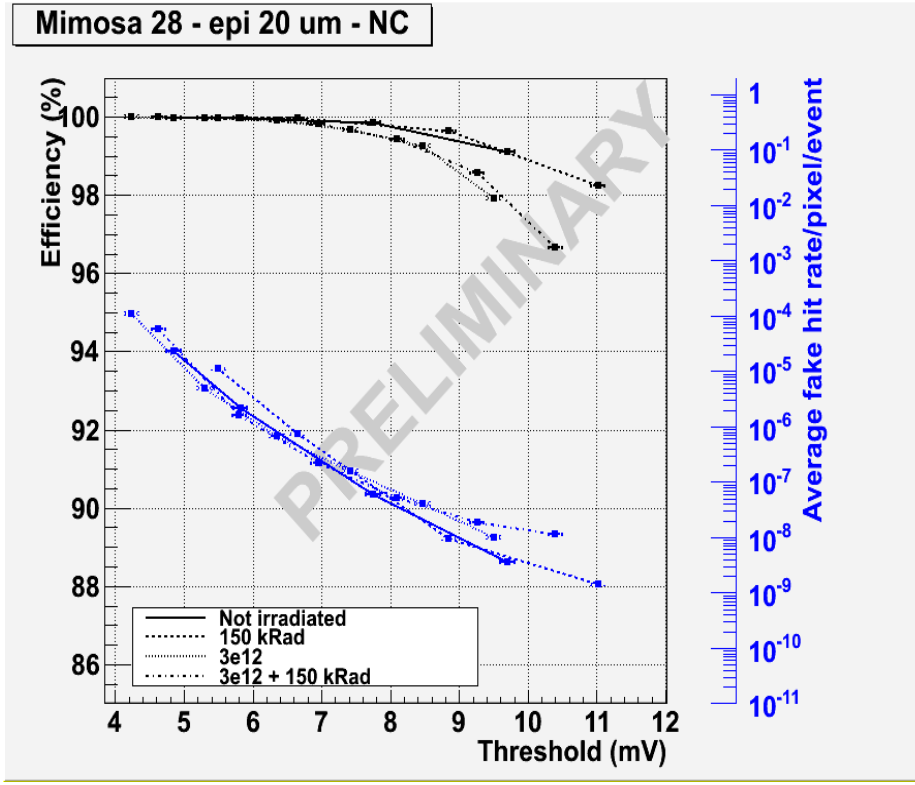
          ↪ **2017-19: adapt MISTRAL/ASTRAL to ILC vertex detector** ⟼ BUNCH TAGGING ?

- **Experience getting accumulated on system integration aspects within STAR & ALICE environments**

State-of-the-Art: MIMOSA-28 for the STAR-PXL

- Details on STAR-PXL in talk of G. Contin
- Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):
  - ⁕ rolling shutter read-out derived from EUDET BT chip: MIMOSA-26
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer
  - ⁕ column // architecture with in-pixel cDS & amplification
  - ⁕ end-of-column discrimination & binary charge encoding
  - ⁕ on-chip zero-suppression
  - ⁕ active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)
  - ⁕ pitch: 20.7 $\mu m \longmapsto \sim$ 0.9 million pixels
    $\hookrightarrow$ charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm
  - ⁕ JTAG programmable
  - ⁕ $t_{r.o.} \lesssim$ 200 μs ($\sim 5\times10^3$ frames/s) $\Rrightarrow$ suited to $>10^6$ part./cm^2/s
  - ⁕ 2 outputs at 160 MHz
  - ⁕ $\sim$ 150 mW/cm^2 power consumption
  - ⁕ N $\lesssim$ 15 e$^-$ ENC at 30-35°C
  - ⁕ ϵ_{det} versus fake hit rate $\longmapsto$ $\longmapsto$ $\longmapsto$ $\longmapsto$
  - ⁕ Radiation tolerance : 3·10^{12} n_{eq}/cm^2 & 150 kRad at 30-35°C
  - ⁕ Detector construction under way (40 ladders made of 10 sensors)

8 May 2013



▷▷▷ 1st step: Commissioning of 3/10 of detector completed at RHIC with pp collisions in May-June 2013

Evolving towards an Optimal CMOS Process

- **Motivation: 0.35 μm process used up to now does not allow to fully exploit the potential of CPS**

- **Main limitations of presently used 0.35 μm CMOS fabrication process:** (not restricted to ILC specs)

CMOS process fab. parametres	In-pixel circuitry	Read-out speed	Power consum.	Insensitive areas	TID ($>$ ILC)	Data throughput
Feature size	X	X	X	X	X	
Planar techno.	X	X	X		x	
Nb (metal layers)	X	X		X		
Clock frequency				X		X

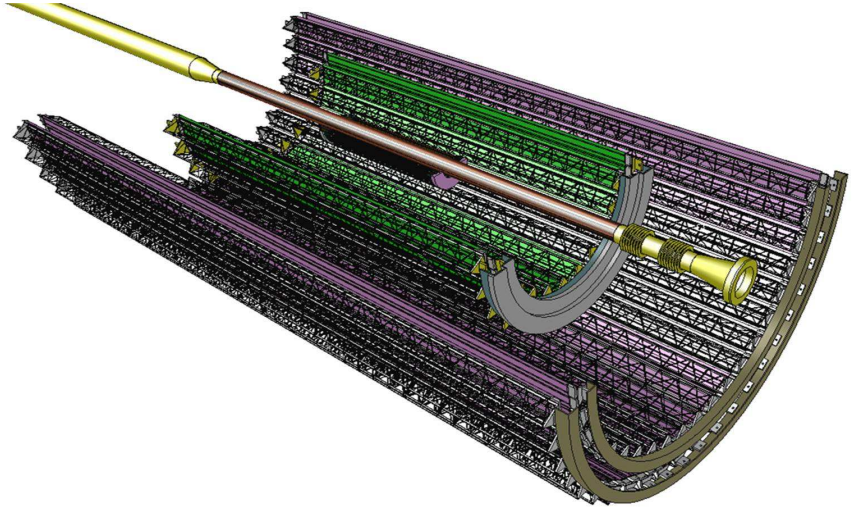
- **Moving to a 0.18 μm imaging CMOS process (Tower/Jazz SC):**
  - ⁂ Deep P-well (quadruple well techno.) $\Rrightarrow$ small-pitch in-pixel discriminators
  - ⁂ 6 metal layers (instead of 4) $\Rrightarrow$ in-pixel discriminators, avoids insensitive zones
  - ⁂ Epitaxial layer : thickness $\sim$ 18–40 μm and resistivity $\sim$ 1–6 k$\Omega \cdot cm$
  - ⁂ Stiching $\Rrightarrow$ multi-chip slabs (yield ?)

  $\Rrightarrow$ process very well suited to the VXD specifications

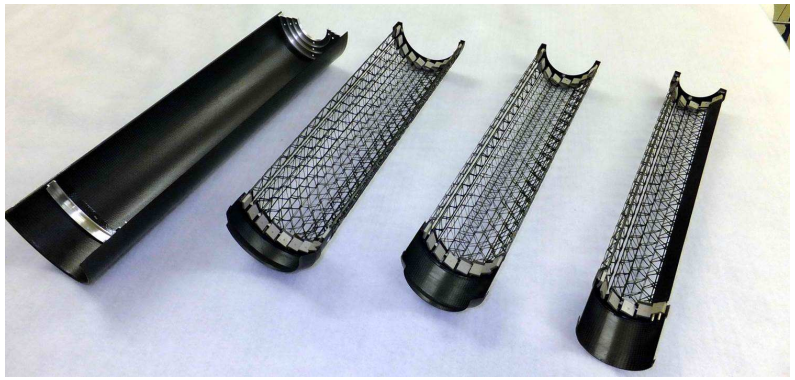
- **Prototyping started in Summer 2011, driven by ILD-VXD, CBM-MVD, ALICE-ITS, etc.**

Applications of CPS : ALICE-ITS Upgrade

- **ITS upgrade :** scheduled for ”2017-18” LHC long shutdown
  - ⁕ see talk of M. Sitta
  - ⁕ exploits space left by replacement of beam pipe with small radius (19 mm) section
  - ⁕ addition of L0 at $\sim$ 22 mm radius to present ITS & replacement of (at least) inner part of present ITS
  - ⁕ 1st tracker entirely omposed of pixel sensors :
    - ◇ 7 layers with pixels : $\gtrsim$ 9 m^2, O(10^{10}) pixels !
    - ◇ material budget of inner layers $\sim$ 0.3 % X_0



- **Differences w.r.t. ULTIMATE/MIMOSA-28 :**
  - ⁕ $\sim$ 0.25/1 MRad & 0.3/1$\cdot 10^{13}$ n_{eq}/cm^2 at T = 30°C (target values)
  - ↪ **0.18 μm 4-well HR-epi techno. (instead of 0.35 μm 2-well hR-epi)**
  - ⁕ $\sim$ 1$\times$3 cm^2 large sensitive area (instead of 2$\times$2 cm^2)
  - ⁕ parallelised rolling-shutter (pot. in-pixel discri.) $\rightarrowtail$ $\sim$ 10–30 μs
  - ⁕ 1 or 2 output pairs at $\gtrsim$ 300 MHz (instead of 1 output pair at 160 MHz)
  - ⁕ $\sigma_{sp} \sim 4\ \mu m$; ladders $\sim$ 0.3 % X_0



  - ▷▷▷ **CDR approved by LHCC in Sept. 2012 $\rightarrowtail$ TDR Draft-1 close to release**
  - ▷▷▷ **2 alternative sensors developed at IPHC : MISTRAL (end-of-col discri) & ASTRAL (in-pixel discri)**

- **Extension to CBM-MVD** $\rightarrowtail$ see talk of M. Deveaux at VERTEX-13