Status of the Forward Tracker Detector





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A.Ruiz-Jimeno, on behalf of FTD team

Outline

- Motivation
- Critical and beyond-the-baseline R&D.
- Brief status report and long term R&D plans.
 - _ Module design: sensors and hybrids.
 - _ Mechanics, integration & services
 - _ Front-end electronics.
 - _ Power distribution & EMC.
 - _ Alignment and monitoring.
- Summary & conclusions

Motivation



Full angular acceptance



Forward tracking increasingly important with higher c.m.s. energy





Figure 11. MadGraph [13] prediction for the fraction of charged leptons emitted in the forward direction $l^+l^- v\bar{v}$ and $l^+l^-l^+l^-$ events. The round markers represent $P_{30}^{l\pm}$, while the squared markers correspond the total fraction of forward charged leptons ($\theta < 30^\circ$).

center-of-mass energy (GeV)

2009 JINST4 P08002

center-of-mass energy (GeV)

(a) $l^+l^-\nu\bar{\nu}$

Good momentum resolution Real layout ILD inner part



Complex tracking system:

 $-\sigma_{r\phi}$ not uniform

- at angles<40^o, N decreases, added to shorter L
- forward tracking, N<10, $\sigma_{r\phi}$ ~7 μm

Multiple scattering contribution depends on the material budget. Equals the other term at p~50GeV, at large angle



Good impact parameter precision



Good pattern recognition OCCUPANCY AT ILD/ILC



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OCCUPANCY AT ILD-ILC (500 GeV operation, LoI results)

Technology	Cell area (µm x µm)	Integration time	Peak occupancy
VXD	25 x 25	50 µs	6 x 10 ⁻⁶ + 1 x 10 ⁻⁶ /BX
Hybrid pixel	50 x 500	10 - 100 ns	2 x 10 ⁻⁴ + 4 x 10 ⁻⁵ /BX
µ–strip	50 x 10⁵	10 – 100 ns	5 % + 1 %/BX

10 cm long, 50 μ m wide strips \rightarrow peak occupancy of 6%/BX, too high

Pixels of 25*25 μm^2 in the most inner region allows robust pattern recognition for a readout time of 50 μ sec (about 100 BX) \rightarrow occupancy at peak about 10⁻⁴, comfortable

Also acceptable pixel CCD detectors 10*10 μm^2 integrating 1312 BX



BX separated 0.5 nsec, tracking and vertex detector integrating over the train duration of 156 nsec.

To maintain comfortable level of occupancy, time stamping with 10 nsec. precision is sufficient

Low-mass and low-power hybrid pixel detectors with a pitch of aprox.25*25 μ m² and readout architecture based on TimePix are foreseen

Ultra-fast detectors with Time stamping at the level of 1 BX in study A. Ruiz-Jimeno, LCWS13-Tokyo

Good pattern recognition

Microstrip detectors in the forward tracker have radially oriented strips. To constraint the second coordinate with a low proportion of ghost hits, an stereo angle α of about 100 mrad will be used

$$\sigma(r\phi) = \frac{\sigma}{\sqrt{2}\cos\left(\alpha/2\right)},$$
$$\sigma(r) = \frac{\sigma}{\sqrt{2}\sin\left(\alpha/2\right)}$$



 α = 100 mrad $\rightarrow \sigma(r) = 20 \sigma(r\phi)$

Moderately precise r-measurements should be needed in all the forward tracking layers to have a robust pattern recognition

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Baseline sensor: conventional microstrip sensor with integrated signal routing in a second metal layer.

Baseline operational unit: petal (sensor+standard hybrid board(s) with readout, powering and data link circuitry.



MECHANIC, CABLES





STUDY, PROGRESSING

ASSEMBLING



Critical & Beyond the baseline R&D

- What are the Critical R&D activities mandatory to fulfill the base line design ?
- What are the R&D beyond-the-baseline RD lines that will enhance the detector performance ?

R&D	Critical	Beyond Baseline
Granularity: Short strips / Resistive electrodes		X
Thermal management: air(gas) cooling, thermal disipation	X	
Front-end: R/O chip, data link.	X	
Powering: Power pulsing, Long term Reliability	X	
Mechanics and integration: Structural Self-monitoring, alignment	14	X



Coordinate (three year scale) R&D project in preparation + Ciemat (Calorimetry)



Critical R&D: Thermal Management



- Goal: gas(air) cooling (avoid active cooling burden)
- Challenging task for inner tracking system.
- Partial synergy with Belle-II PXD cooling system.
 - Air cooling system
 - _ Small footprint fast optical FBGs sensors for thermal mockup diagnostic.







Thermal Management

Valencia PXD Mockup

Stainless Steel Cooling Blocks, enclosed with copper foil ladders equipped with resistive heaters in the end flanges for both layers.

A single Si thinned detector with printed Al resistors

Liquid CO₂ circulating in the cooling blocks at -35 ° C. Injection of N₂ gas cooled at 0°C towards the sensor region at 3 bar and 15L/min flow rate. The beam pipe is kept at 15°C with a composite liquid coolant

The measurement equipment inside a sealed methacrylate box consist of

- Infrared thermal imaging camera
- Fibber Bragg Grating (FBG) temperature and humidity sensors
- Pt110 probes







Sensor T		Ambient $T = 25^{\circ}C$
Without convective cooling	T _{MAX} =~40°C	Δ T =~15°C
With convective cooling	T _{MAX} =~25°C	ΔT=~5°C

No vibrations were observed below 2kHz (sensor cutoff) with the cooling requirements (3 bar in the entrance pipes).





THERMAL MANAGEMENT:

- Needed more effort to characterize innermost disks
- Fabrication mock-ups, measurements and simulation
- We have instalations

FRONT END ELECTRONICS



In an initial phase. Much work to be done There are possible fall-back solutions

Critical R&D: R/O ASIC



- In AIDA-WP9 a readout chip for Si-microstrips for ILD is being developed by UB with 65nm process
 - ✓ Designed:

T indep current source Amplifier in the preamplifier Preamplifier, shaper

To be designed

Analog pipeline, Ramp or SAR ADC,

Discriminator, sparsifier, digital logic, I2C/SPI, LVDS, ...

Concurrent designs with 65nm process:

 65nm process is used in the development of the DHP together with Bonn Univ. in the framework of DEPFET collaboration for Belle II

Designed, fabricated and tested:

T indep current sources, current-mode DAC

Designed

T sensor





Critical R&D: R/O ASIC (2)



Medium term plans

	Pernonsible	Pernonsihle		First	Year		S	econ	d Yea	ar	1	Third	Yea	r
TASKS	Centre	Person	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th
	Centre	FEISOII	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT
5.1 Module design	UB	Coord: AD UB: AD, RC, OA, JC, EV, LUB												
- Front-end, biasing circuits, config. DACs														
- ADC														
- Digital modules														
2.2 Channel integration	UB	Coord: AD UB: AD, RC, OA, JC, EV, LUB												
- Single channel														
- 16/32 channels														
2.3 Customized DAQ and Test ,	UB, USE	Coord: RP, ML UB: AD, ML, OA, JC USE: RP, RF												
- Software and configware development														
- ASIC validation tests														
- Hybrid prototype development														
- DAQ for channel/multi-channel ASICs														

Critical R&D: Pulsed powering . Medium term plans



Critical R&D: Pulsed powering.



	DC-DC	Super-caps
Power dissipation	228 W	395 W
EMI phenomena	Yes	No*
RAD tolerant	Yes	? (First test OK)
Material budget	(240 DC-DC) ?	(80 SC) ?
Reliability	?	?
Power pulse applications	Not frequent	Yes
Installed power	1.4 kW	0.48 kW
Primary PS	≈ 36 W	≈ 15 W
Mains protection (UPS effect)	No	Yes
	WORK ONGOING SATISFACTORILY	

Critical R&D: Pulsed powering (2) Medium term plans

TACKS	Pernonrihle	sible Responsible		First Year			S	Secon	d Yea	r	Third Year			
TASKS	Centre	Person	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th
	Centre	reison	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT
Super-capacitor Hardness Assessment.	ITA	A.Pradas												
EMC issues in power pulsing systems for HEP.	ITA	M.Iglesias												
Reliability studies of Super-capacitors and DC-DC co	ITA	EL Diadvafita												
for power pulsing applications in <u>HEP</u> .	ПА	ra. <u>rieuranta</u>												

			First Year			5	Secon	d Yea	r	Third Year			
DELIVERABLES	Туре	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th	1 st	2 nd	3th	4 th
		QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT	QT
D4.1 Supercapacitor characterization unit for Radiation													
Environments (Prototype)													
D4.2 Specification of radiation hardness of super													
capacitor for physics experiments. (Paper)													
D4.3 EMC (conducted and radiated emissions) mapping													
of a power pulsing system (Paper)													
D4.4 Design criteria to be followed for a FEE – hybrid –													
sensor design to operate in power pulsing system.													
D4.5 Overall reliability of a power pulsing system (Paper)													

ALIGNMENT

· Laser tracks can be used by a hardware system to align the tracker





· First implemented by AMS I, then AMS II and CMS

WELL ADVANCED







Beyond-the-base line R&D:

Sensors: Two R&D lines

- Low gain p-type segmented pixels or strips >thinner sensor with same S/N



- Charge division in microstrips to reduce the complexity of doublesided sensors







Polysilicon resistive detectors







** V. Radeka, IEEE Transaction on Nuclear Science NS-21 (1974) 51



A. RUIZ-JIIIIEIIU, LCVV 313-IUKYU

Polysilicon resistive detectors, integrate routing





Microstrips: Length: 14mm Width: 20um Pitch: 160um R/um=20Ω/um





Beyond the baseline: Smart Mechanics





Beyond the baseline: Smart Mechanics (2) 🛣 🕮

Smart plate able to self monitor its own temperature, torsion and flexion deformations & vibrations







Beyond the baseline: Smart mechanics (3)

 Component-wise characterizations: FBGs calibrations and sensibility to nitrogen, humidity atmosphere.







Summary

– Critical R&D lines with different degree of coverage:

- _ Thermal management & cooling
- _ Pulse powering.
- _ Readout ASIC
- Enhanced performance via additional R&D: Sensor granularity, smart mechanics:
- Moving from generic or Belle-II oriented R&D towards a coordinated and ILD oriented R&D project.

BACKUP

Zgap between the FTD1 and VTX

Comparison z_{gap}

Minimize the gap!

But: if we route the services along the beam pipe, the forward vertexing performance is terrible and essentially insensitive to z_{qap}

* In ILD the distance between VXD and innermost FTD is close to 10 cm. This clearance is motivated by the possibility to fit in a VXD cryostat. If a "cold" VXD technology is chosen, a short gap implies one has to install the innermost disks inside the cryostat.







A. KUIZ-JIIIIEIIU, LCVV315-IUKYU

DC-DC-based Power System



- It absorb transients related to power pulsing system.

Low currents before DC-DC due to converter ratio.



	POWER (W)
HALF SIDE	114 W
TOTAL FTD	228 W

Group	FTD 3+	FTD4+	FTD5+	FTD6+	FTD7+
FEE	4.6	5	5.4	5.6	3
CABLE	0.02	0.033	0.039	0.041	0.012
DCDC*	0.92	1	1.07	1.11	0.61
TOTAL (1/4)	5.55	6.04	6.48	6.74	3.69
TOTAL DISK	22	24.1	26	27	14.7
External cable (20m)	0.23	0.27	0.31	0.34	0.1

Super-capacitor based PS





		Group	FTD 3+	FTD4+	FTD5+	FTD6+	FTD7+
		FEE	4.6	5	5.4	5.6	3
	POWER (W)	CABLE AWG 27	0.04	0.04	0.05	0.06	0.02
		LV REG	4.9	5.41	5.74	5.96	3.24
HALF SIDE	197 W	SUPERCAPS	0.06	0.072	0.083	0.089	0.027
	205 14/	TOTAL (1/4)	9.63	10.6	11.3	11.7	6.4
TOTALFID	395 VV	TOTAL DISK	38.5	42.1	45	46.5	25.5
		External cable (20m) – AWG 16	2.92	3.515	4	4.4	1.26

Radiation test for Super-capacitors

Radiation test has been performed at Electron Stretcher Accelerator (ELSA, Bonn)

- Electrons at 20 MEV
- Beam spot 3x3 cm2
- 4 hours of irradiation.
- Total dose :
 - _ 0.6 Mrad -2.3 Mrad (3%)
- C and ESR were measured



28 [Cu] 27.5 27.5 E 12.5 X C5 - A - 0 27 X C5 - B - 0 11.5 26.5 X C5 - A - 0.6 MRad 26 X C5 - B -0.6 MRad 10.5 25.5 25 L 24 24.5 25 25.5 26.5 27 27.5 28 26 24.5 25 25.5 26.5 27 27.5 28 26 Temeprature [°C] Temperature [°C]

5 canacitors

4.1 Radiation test for Super-capacitors



19 de 21

ILD meeting Cracow, September 2013

4. Conclusions

- A first radiation test campaign has been carried out to validate super-capacitors for HEP applications.
- 5 Super-capacitors
 - Maxwell, Nesscap and Panasonic (10F & 25F)
- Tests have been performed based on constant current
 - Normal operation (2.7A, 5A)
 - Stress operation (10 A and 16 A)
 - ERS,C and T have been measured
- There was not found big difference on the main characteristics and SC performance
 - No stoppers have been found
- More tests and analysis are planned
 - Temperature & Higher dose.

22 de 22 – Annealing effects European Linear Collider Workshop (ECFA 13) Desy - Hamburg, Germany , May 2013



_Bragg grating Multiplexing



D.Moya, CLIC detector and physics collaboration meeting, CERN Oct. 1st 2013