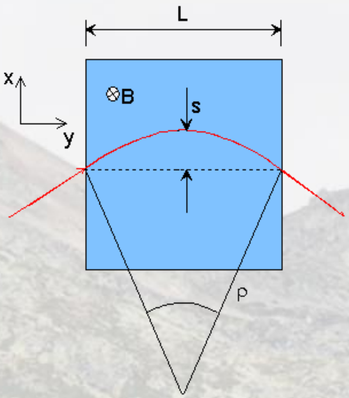
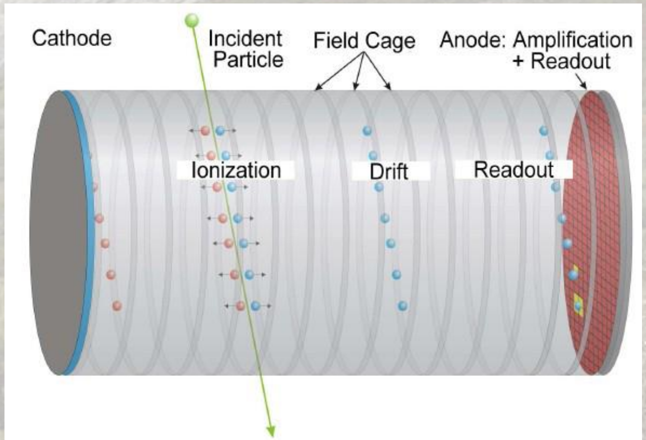
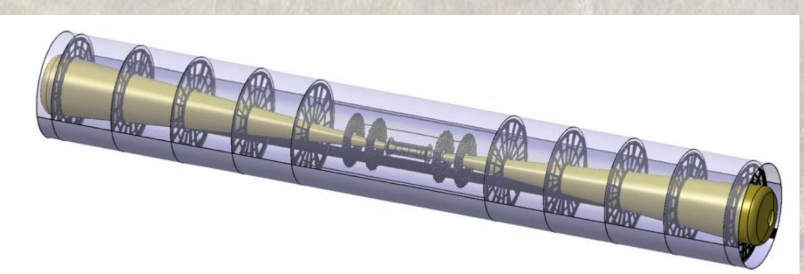
TRACKING IN ILD: A REVIEW







A. Ruiz-Jimeno,ILD-Krakow-Sept2013

Outline

- REQUIREMENTS
- CURRENT SITUATION
- HOW TO PROCEED

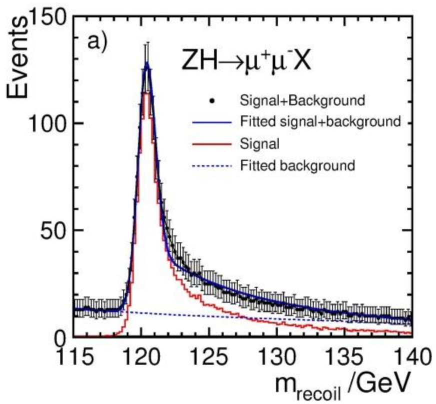
(mainly silicon tracking)

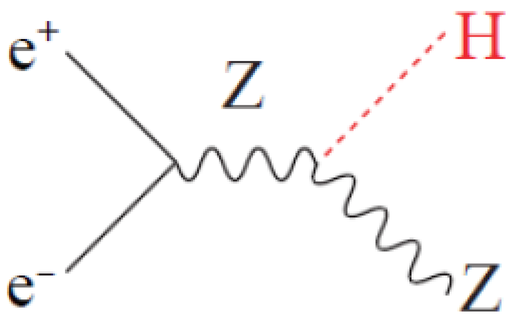
Thanks for their inputs to D.Moya, R. D. Settles, Y. Sugimoto, I. Vila and M. Vos

Requirements

Good momentum resolution

$$\sigma_{p_T}/p_T^2 \sim 2\times 10^{-5}\ \mathrm{GeV}^{-1}$$





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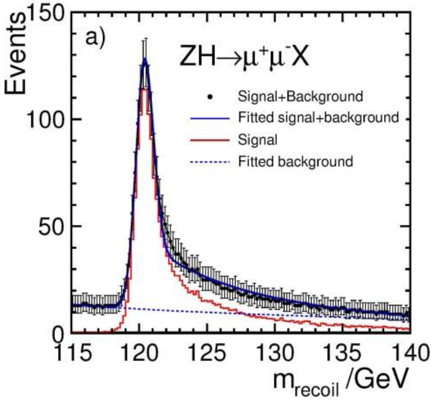

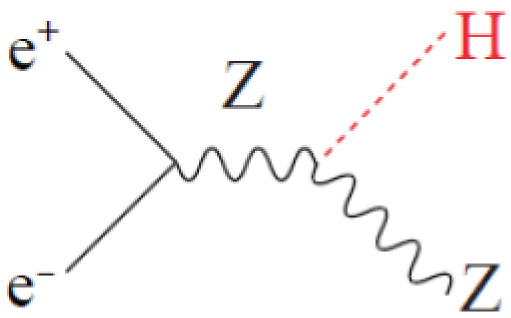

Good impact parameter precision

b,c,τ tagging

$$\sigma_{r\phi} = 5 \oplus 10/(p[\mathrm{GeV}]\sin^{\frac{3}{2}}\theta)\,\mu\mathrm{m}$$

barrel

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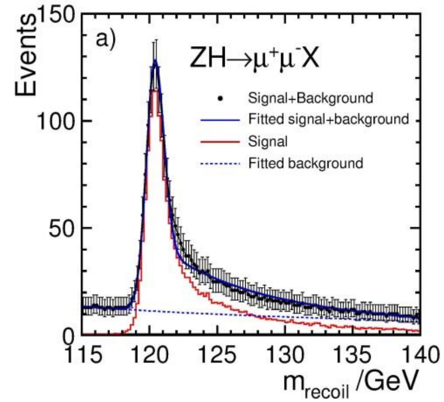

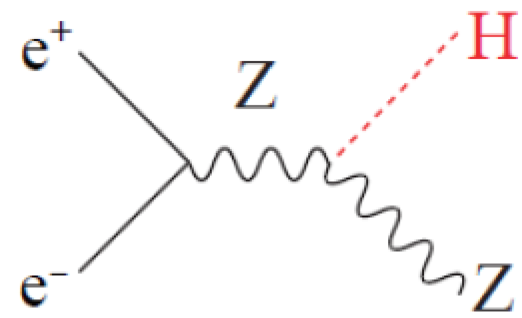

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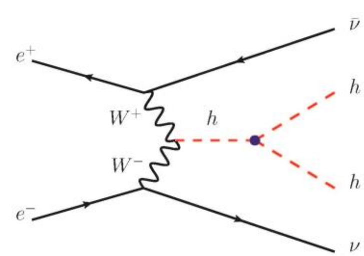
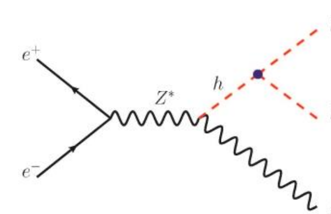
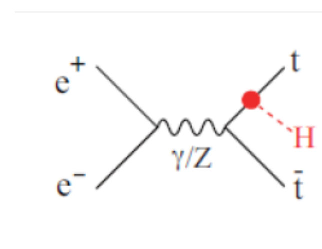
Good pattern recognition





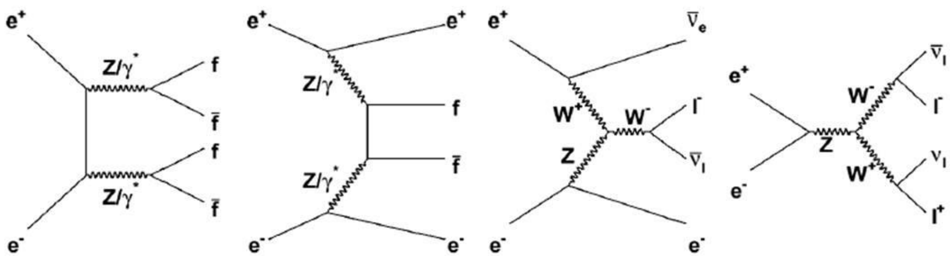
Full angular acceptance

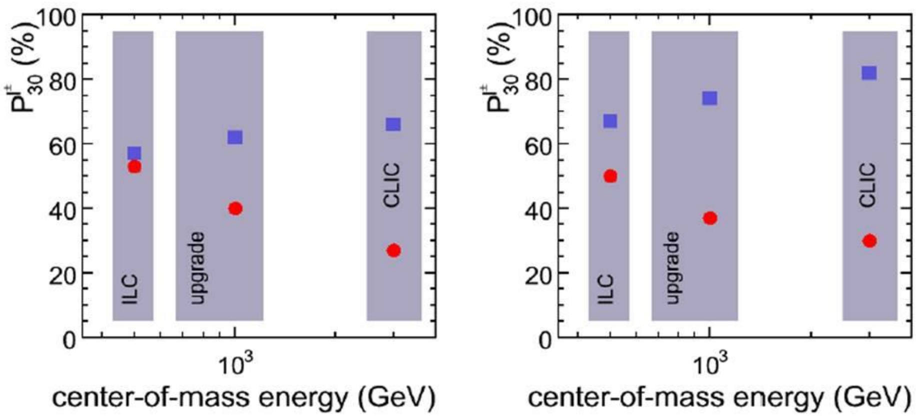
High jet multiplicity



Full angular acceptance

Forward tracking increasingly important with higher c.m.s. energy





(a) $l^+l^-\nu\bar{\nu}$ (b) $l^+l^-l^+l^-$

Figure 11. MadGraph [13] prediction for the fraction of charged leptons emitted in the forward direction in $l^+l^-\nu\bar{\nu}$ and $l^+l^-l^+l^-$ events. The round markers represent $P_{30}^{l\pm}$, while the squared markers correspond to the total fraction of forward charged leptons ($\theta < 30°$).

2009 JINST4 P08002

Full angular acceptance

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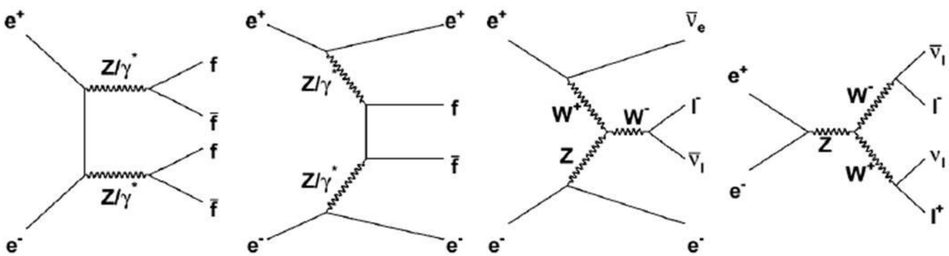

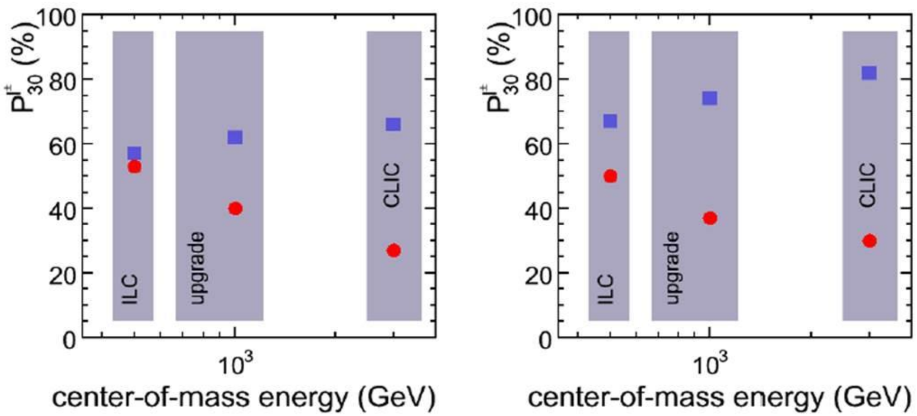

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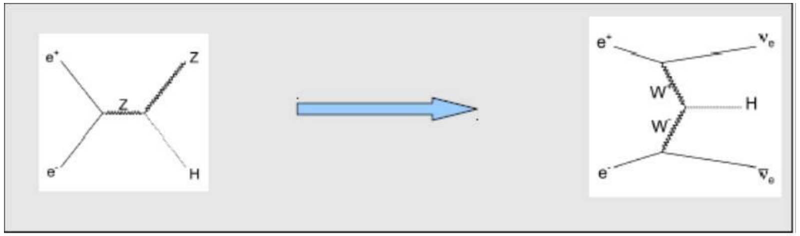
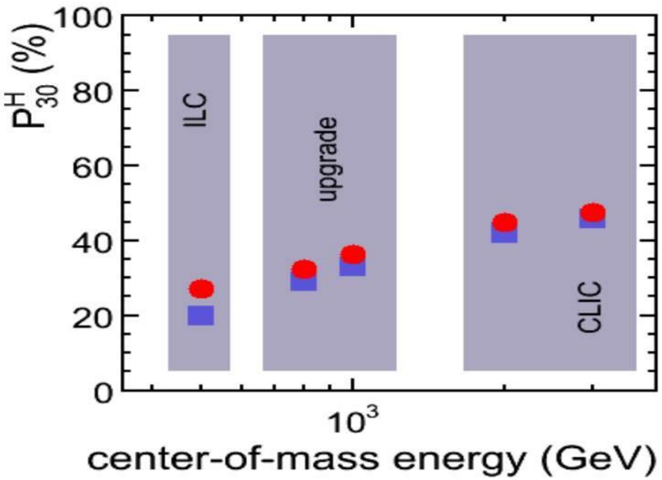




2009 JINST4 P08002

Good momentum resolution

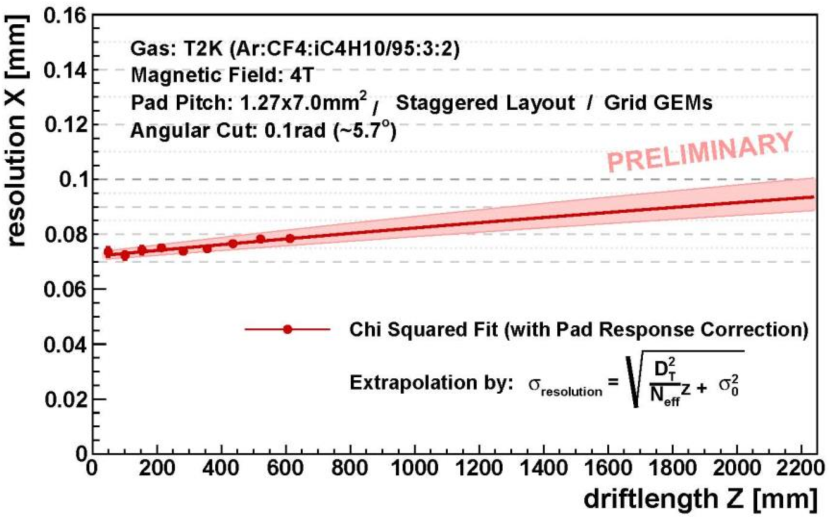
$$\sigma_{1/p_T} \approx \sqrt{\left(\frac{2\times10^{-5}}{\mathrm{GeV}^{-1}}\right)^2 + \left(\frac{10^{-3}}{p_T\,[\mathrm{GeV}]\sin\theta}\right)^2}$$

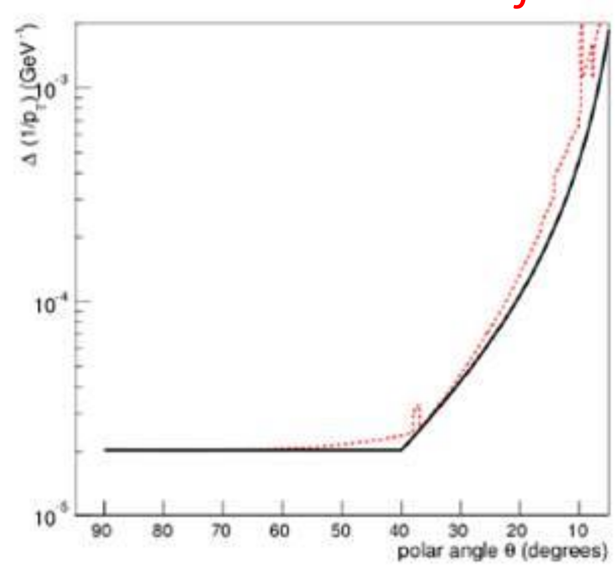
→ *Goal ILD*

$$\frac{\sigma(p_T)}{p_T} = \sqrt{\frac{720}{N+4}}\,\sigma_{r\phi}\,\frac{p_T}{0.3BL^2},$$

Gluckstern formula for N equally spaced layers
(N>10, no Multiple Scattering)
Lever arm L perpendicular to magnetic field B

Degradation at small angle due to the reduction of L





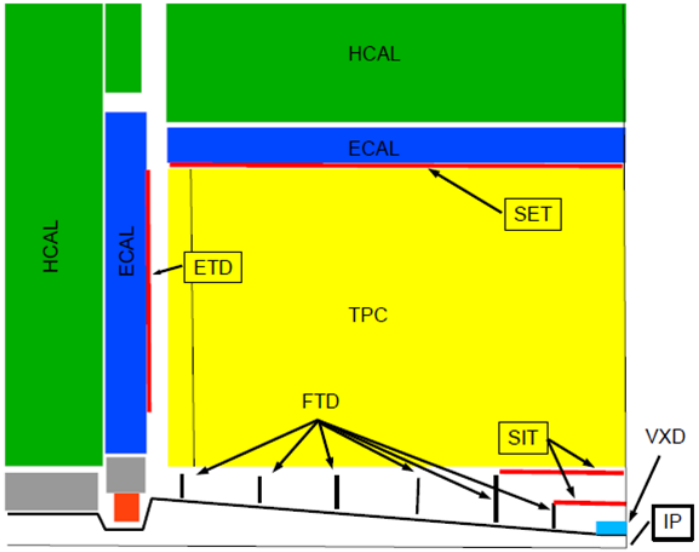
TPC resolution is dependent of drift length

ILD 100GeV muons
(dashed line: simulation; contonuous line:Gluckstern)

Note also that
$\Delta(1/p) \sim \Delta(1/p_t) * \sin\theta$

Good momentum resolution

Real layout ILD inner part



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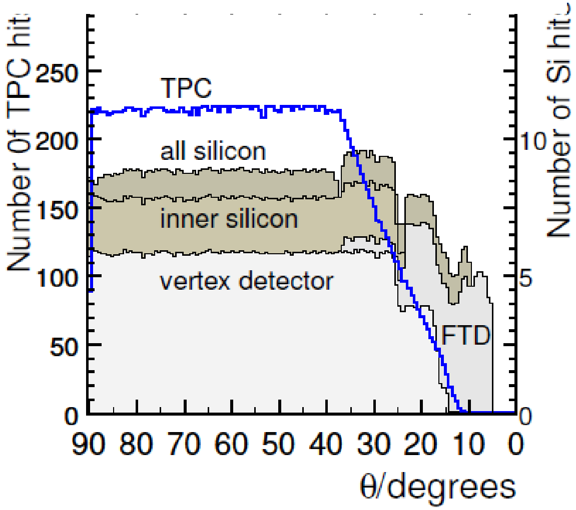
(ideal)



Complex tracking system:

– $\sigma_{r\phi}$ not uniform

- at angles<40º, N decreases, added to shorter L

- forward tracking, N<10, $\sigma_{r\phi}$~7μm

Multiple scattering contribution depends on the material budget. Equals the other term at p~50GeV, at large angle

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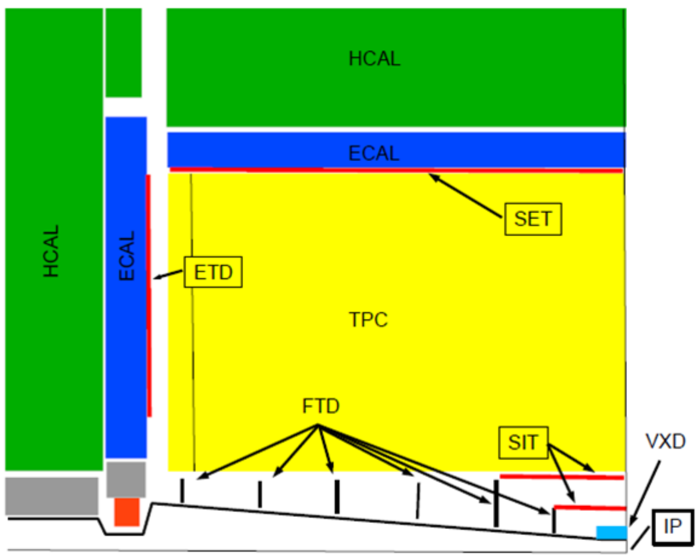

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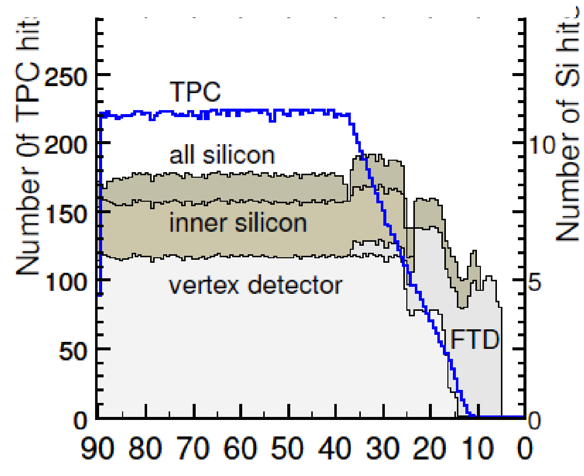

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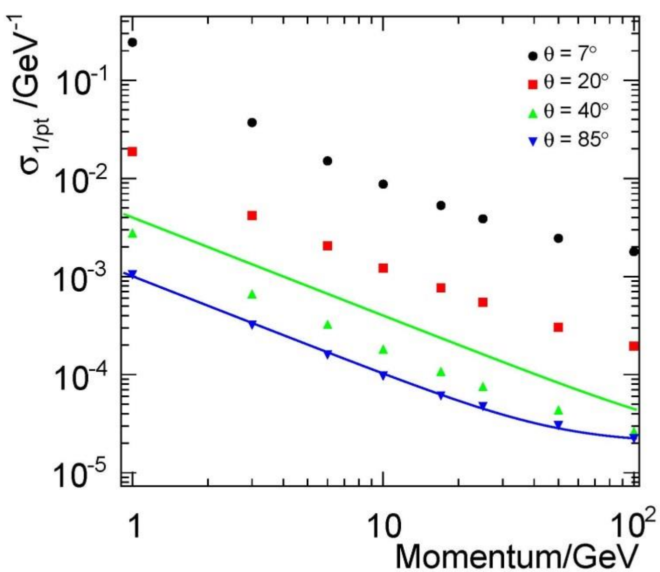

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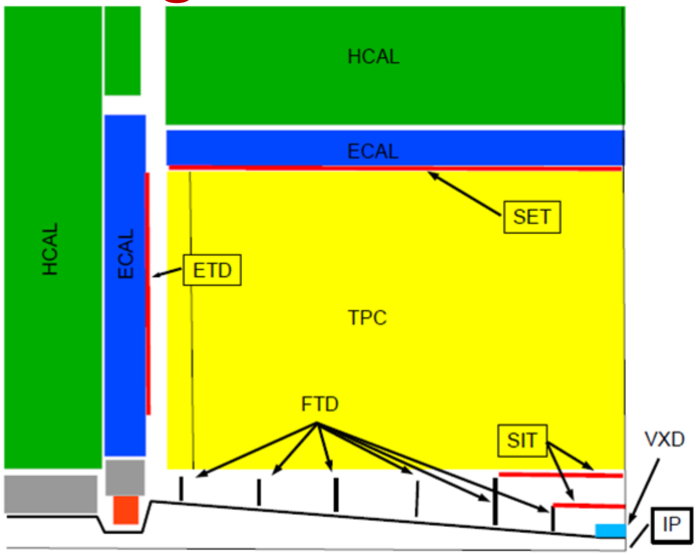
Tracking



ILD Heresy

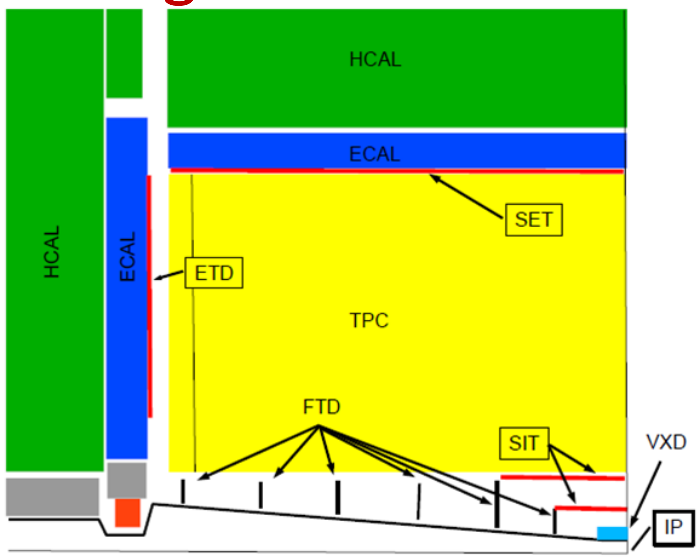
★ Could we live without the SET ?

★ Does the ETD bring anything to ILD ?

DESY, May 29th 2013 Mark Thomson

First question to be carefully analysed

Tracking



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SET, ETD provide precise space points, added to TPC points.

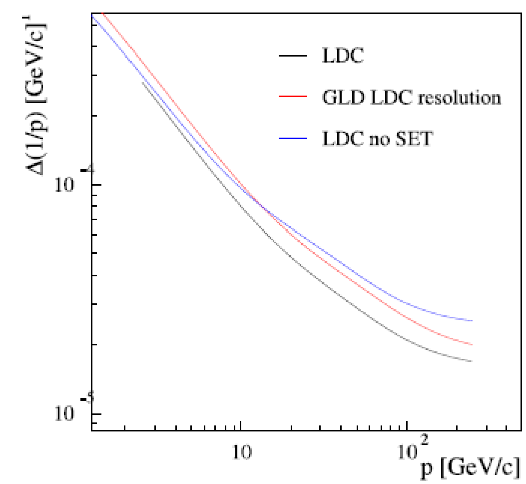
ETD resolution degraded by TPC end plate

SET, ETD improve matching efficiency TPC-ECAL

SET, ETD add material budget in front of ECAL

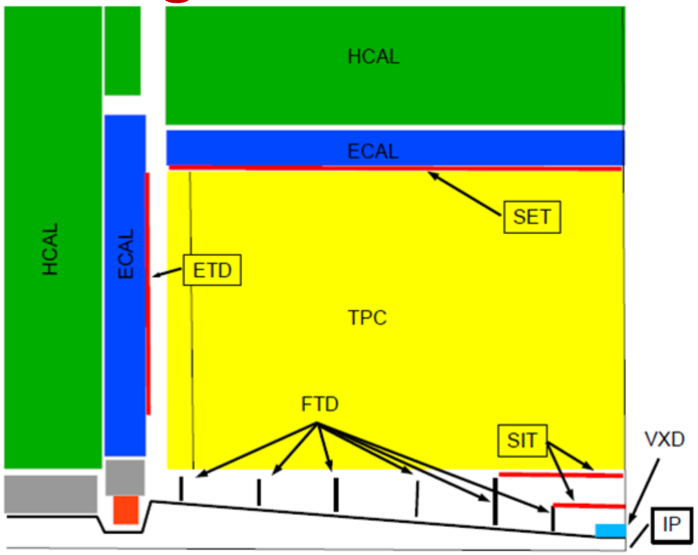
SET provides time stamping (also SIT)

SET, ETD cost is ten times the cost of inner tracking



Mikael Berggren (DESY) Cambridge 2008

Tracking



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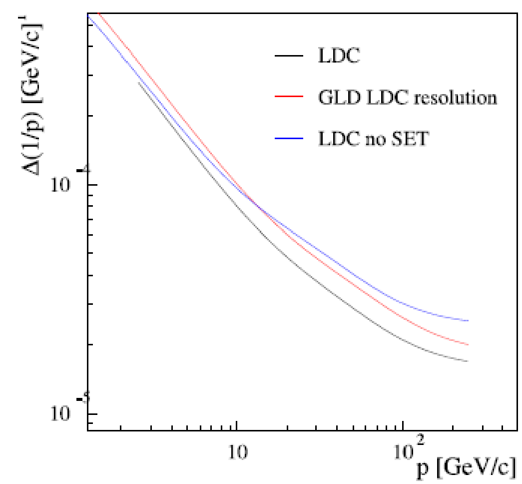

Mikael Berggren (DESY) Cambridge 2008

To answer the question it is needed to analyze it with a realistic ILD layout. Calorimeter people input is very important

Tracking

- SIT, TPC, SET
- There are two important quality functions for the tracking using this configuration:
  1. REDUNDANCY
  2. INTERNAL CALIBRATION
- Unfortunately, these are difficult to quantify, and thus difficult to optimize.

The good timing resolution of the silicon detectors relative to the time between bunches in the ILC together with the high spatial precision helps in time-stamping tracks and assigning them to a given bunch within an ILC bunch train.

- The time-stamping in ILD is found to be precise to ~ 2 ns (to be compared to ~ 300 ns between BXs at the ILC) so that the bunch crossing which produced the track (the T0) can be uniquely identified.

Good impact parameter precision

$$\sigma_{r\phi} = 5 \oplus 10/(p[\text{GeV}]\sin^{\frac{3}{2}}\theta)\,\mu\text{m}$$ → *Goal ILD*

barrel

Forward- backward

$$\Delta d_0 = a[\mu\text{m}] \oplus \frac{b \times \frac{L}{R}[\mu\text{m}]}{p[GeV]\cos^{3/2}\theta}.$$

- *The distance to the interaction point (IP) of the innermost hit goes as ($\sin^{-1}\theta$, $\cos^{-1}\theta$) in the (barrel, forward) tracking*
- *Multiple scattering is proportional to square root of material thickness in X_0*
- *Finally, b is multiplied, in the forward tracker, by the ratio of the IP distance along z (L) of the first disk to the inner radius of the barrel tracker (R)*

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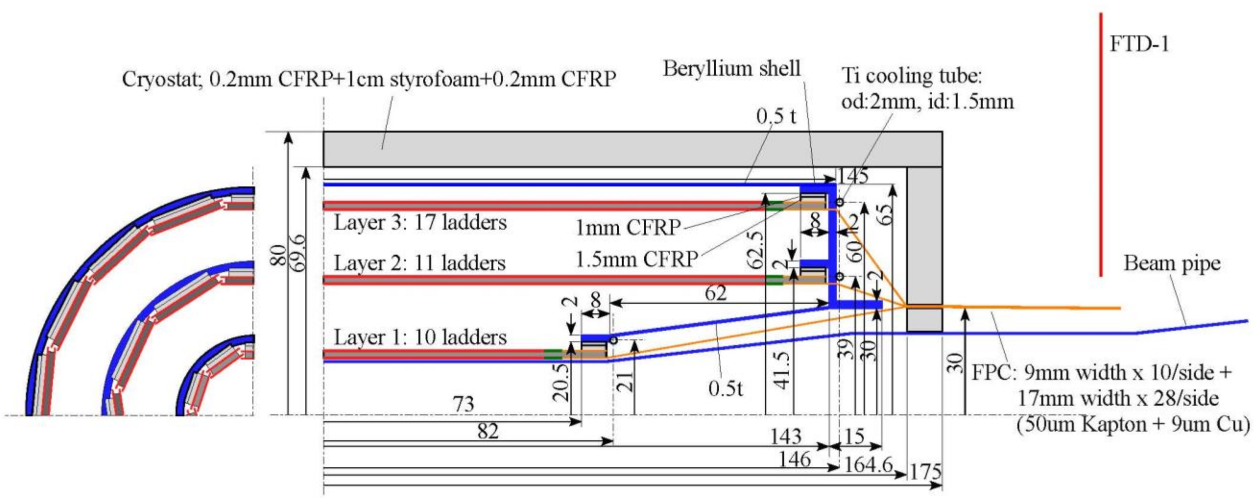
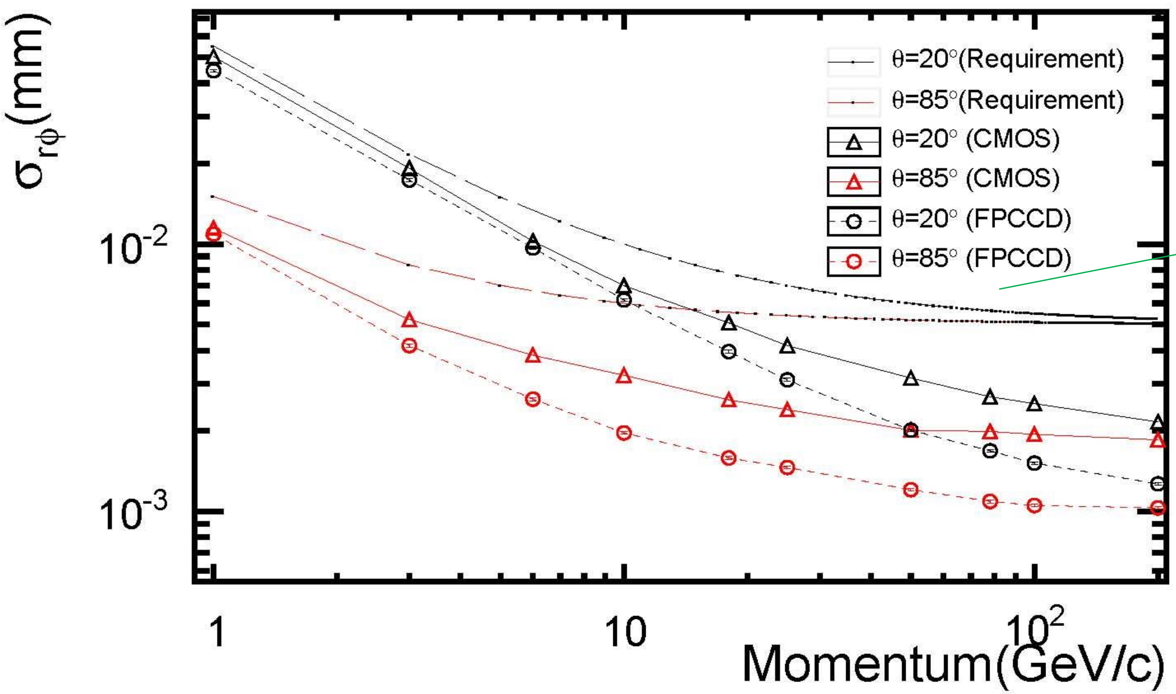


Limited by the background near IP

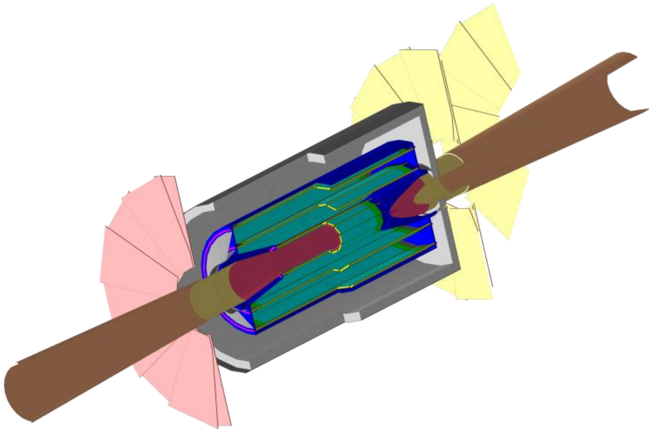
The gap between barrel and end cap limited by mechanics and services

Vertex detector in DBD

	R (mm)	|z| (mm)	|cosθ|	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100



Performance goal achieved in barrel



Questions related to the vertex detector optimization

Q1. Is the outer radius of 60 mm optimal?

The fact that changing the pixel size of outer layers from 5um to 10um does not affect the impact parameter resolution suggests that the outer trackers (SIT and TPC) are working as the "outer layer" of the vertexing system. That implies the outer radius of the VTX could be reduced without degrading the impact parameter resolution.

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Q2. What is the impact of the performance of outer trackers (SIT and TPC) on the impact parameter resolution?

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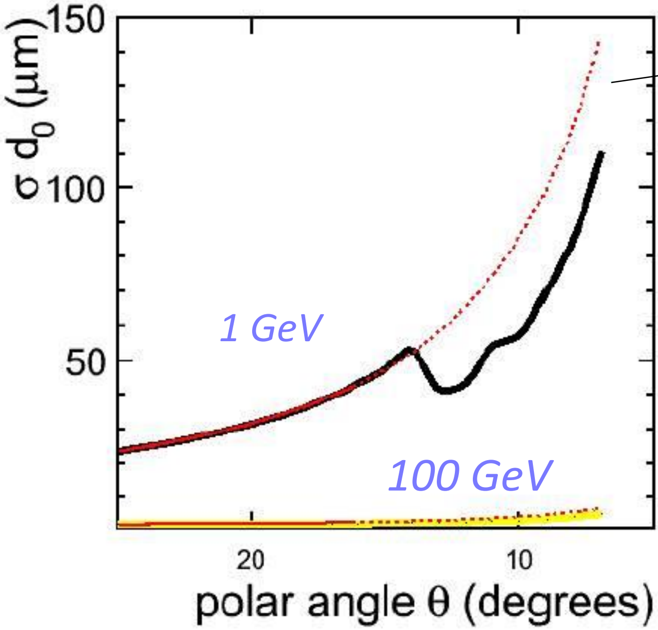
Q3. What is the impact of spatial resolution and material budget of the vertex detector on the physics performance?

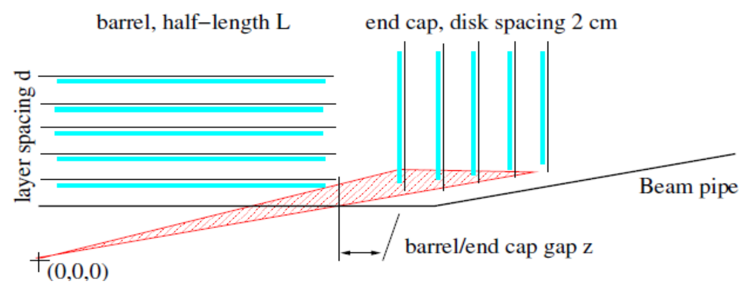
It is clear that better spatial resolution and less material budget of the VTX (inner layers) gives better impact parameter resolution. However, it has not been demonstrated well how much the better IP resolution improves physics output. Physics potential as a function of these parameters should be demonstrated. Effect of the material budget of the end plate, support shell, cryostat, and cables should be studied combined with the outer trackers. → (see later…)

Good impact parameter precision

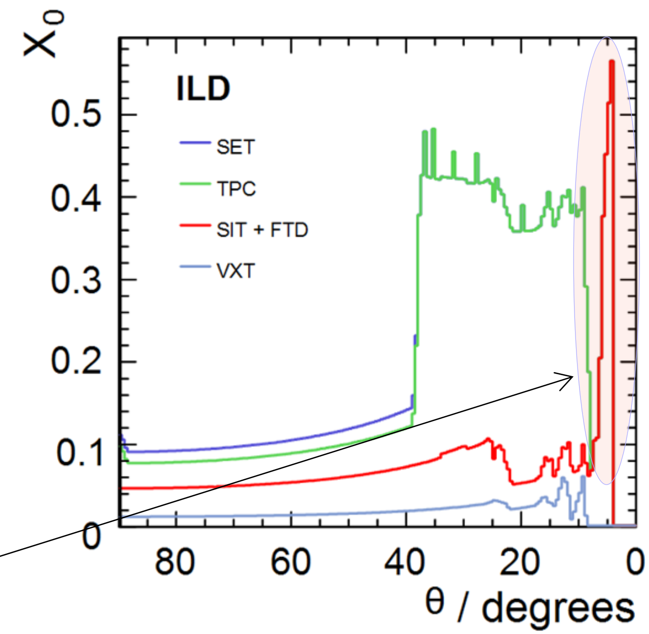


Functional form, toy detector with 0,12% X_0 per layer, 3 μ spatial resolution in $r\phi$ and z

*JINST **8** T06001 2013*



Realistic material budget can degrade notoriously the impact parameter resolution



Mainly vertex cables, services… (not FTD)

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Engineering challenges:

Beam pipe as thin as possible

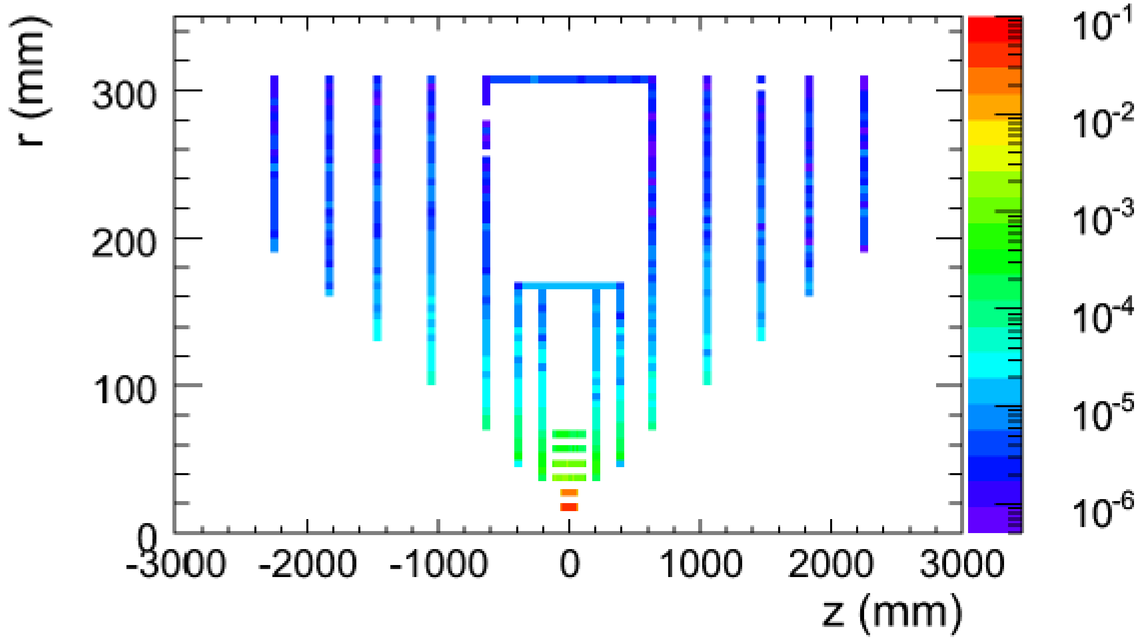
Careful optimization of the services and support structures of the barrel vertex detector to avoid a.m.a.p. the line of sight between the IP and the innermost disk

Routing of the barrel vertex detector cables and services over the end-cap

Good pattern recognition

OCCUPANCY

Detector element	Hit density ($hits/mm^2/BX$)
VXD1	3.2×10^{-2}
VXD6	2.4×10^{-4}
SIT2	4.0×10^{-5}
FTD1	10^{-3} - 10^{-5}
FTD7	1.0×10^{-5}



FTD1 (ee→tt) average

$$1 \times 10^{-4} \frac{\text{hits}}{\text{mm}^2} + 1.6 \times 10^{-4} \frac{\text{hits}}{\text{mm}^2\text{BX}}.$$

FTD1 (ee→tt) peak

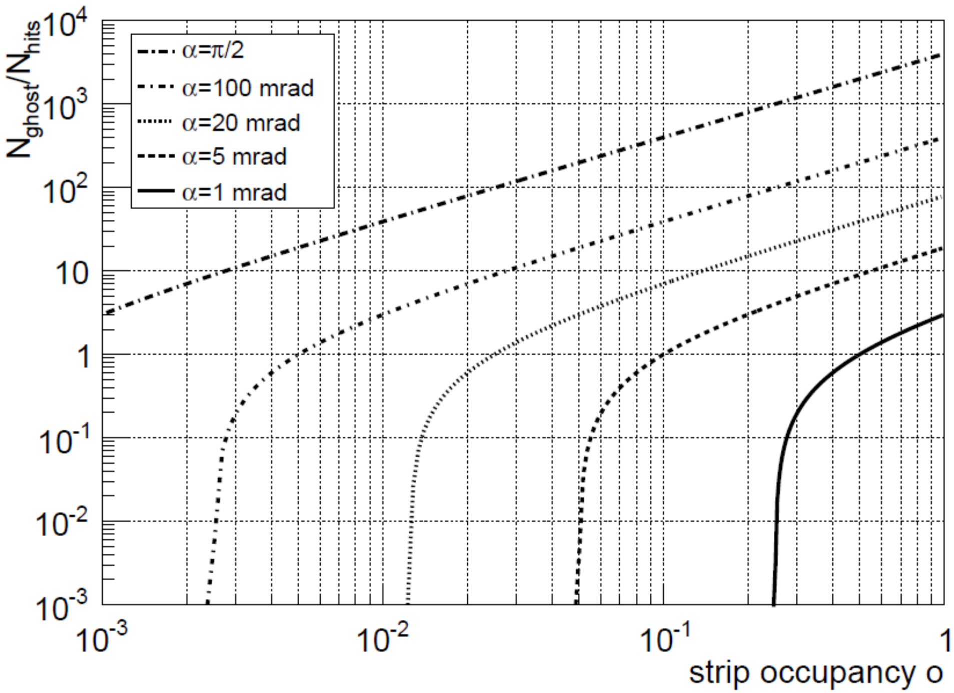
$$1 \times 10^{-2} \frac{\text{hits}}{\text{mm}^2} + 1.6 \times 10^{-3} \frac{\text{hits}}{\text{mm}^2\text{BX}}.$$

Pixels of 25*25 μm^2 in the most inner region allows robust pattern recognition for a readout time of 50 μsec (about 100 BX)

JINST **8** T06001 2013

Good pattern recognition

Microstrip detectors in the forward tracker have radially oriented strips. To constraint the second coordinate with a low proportion of ghost hits, an stereo angle α of about 100 mrad will be used



*100*100 mm^2 sensors with 25 μm pitch*

$$\sigma(r\phi) = \frac{\sigma}{\sqrt{2}\cos(\alpha/2)},$$

$$\sigma(r) = \frac{\sigma}{\sqrt{2}\sin(\alpha/2)}$$

α= 100 mrad → σ(r) = 20 σ (space point resolution of the detector)

Moderately precise r-measurements should be needed in all the forward tracking layers to have a robust pattern recognition

*JINST **8** T06001 2013*

More questions related to the vertex (and tracker) detector optimization

Q4. What is the minimum momentum to be reconstructed with high efficiency from the viewpoint of physics?

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At 250GeV, beam background shape could be different from 500GeV, and the VTX/beam pipe configuration could also be different from the design for 500GeV/1TeV.

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The data size of the VTX is huge. The strategy of handling these large amount of data should be clarified.

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Does the ILD design provide robust tracking down to 6 degrees?

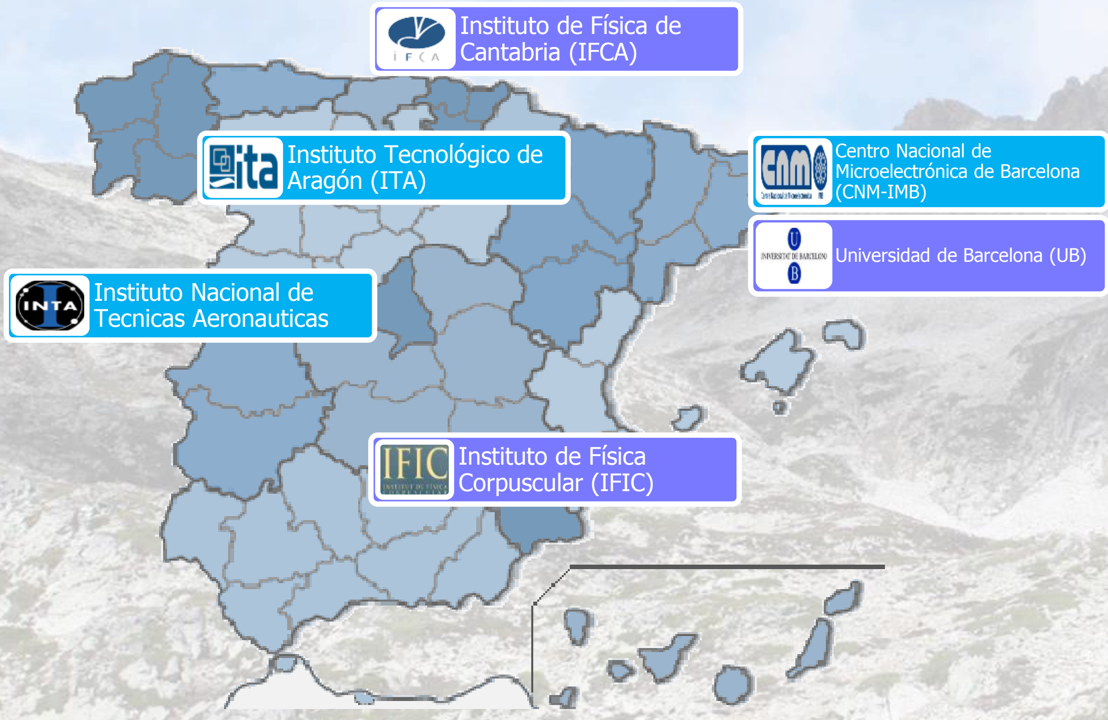
The CLIC answer: no!

Redesign prompted by larger background (inner radius 1.5 cm → 3 cm)

2-disk pixel system extended to 3 double layers

(See : Dannheim, Vos, Simulation studies for the layout of the vertex and tracking regions of the CLIC detectors, LCD-2011-031)

A FAST-TRACK OF THE FORWARD TRACKER STATUS (more information on I.Vila and F. Arteche talks)



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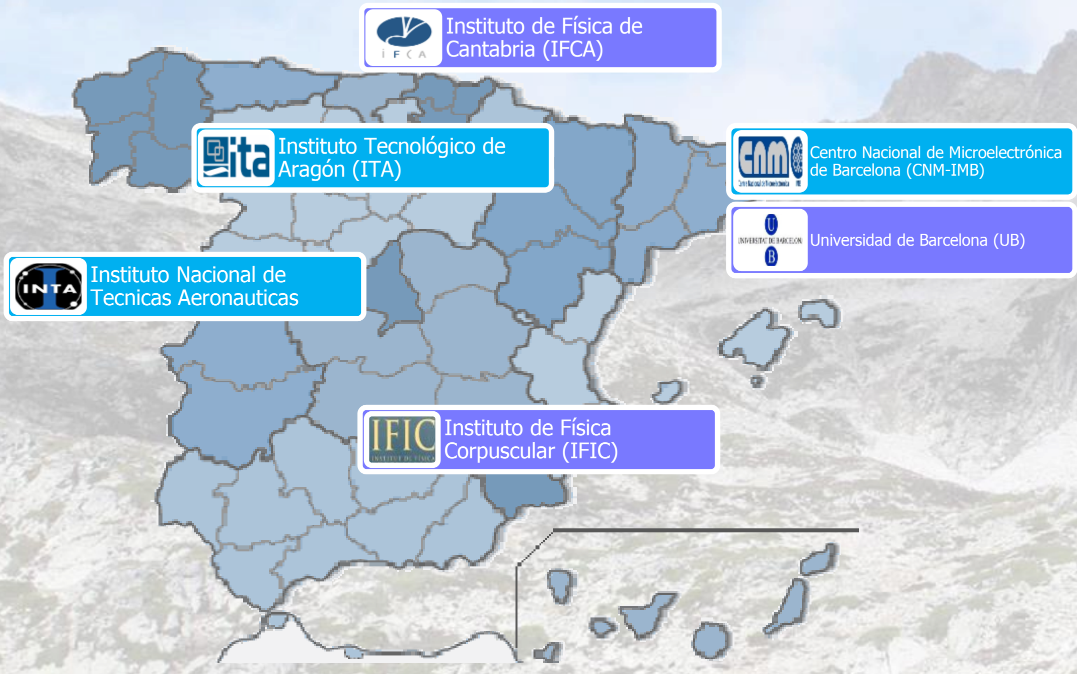


CONSIDERATIUM:

Most of the developments made could serve also for the barrel tracker system.

Anyway there are differences which should be considered in a realistic way

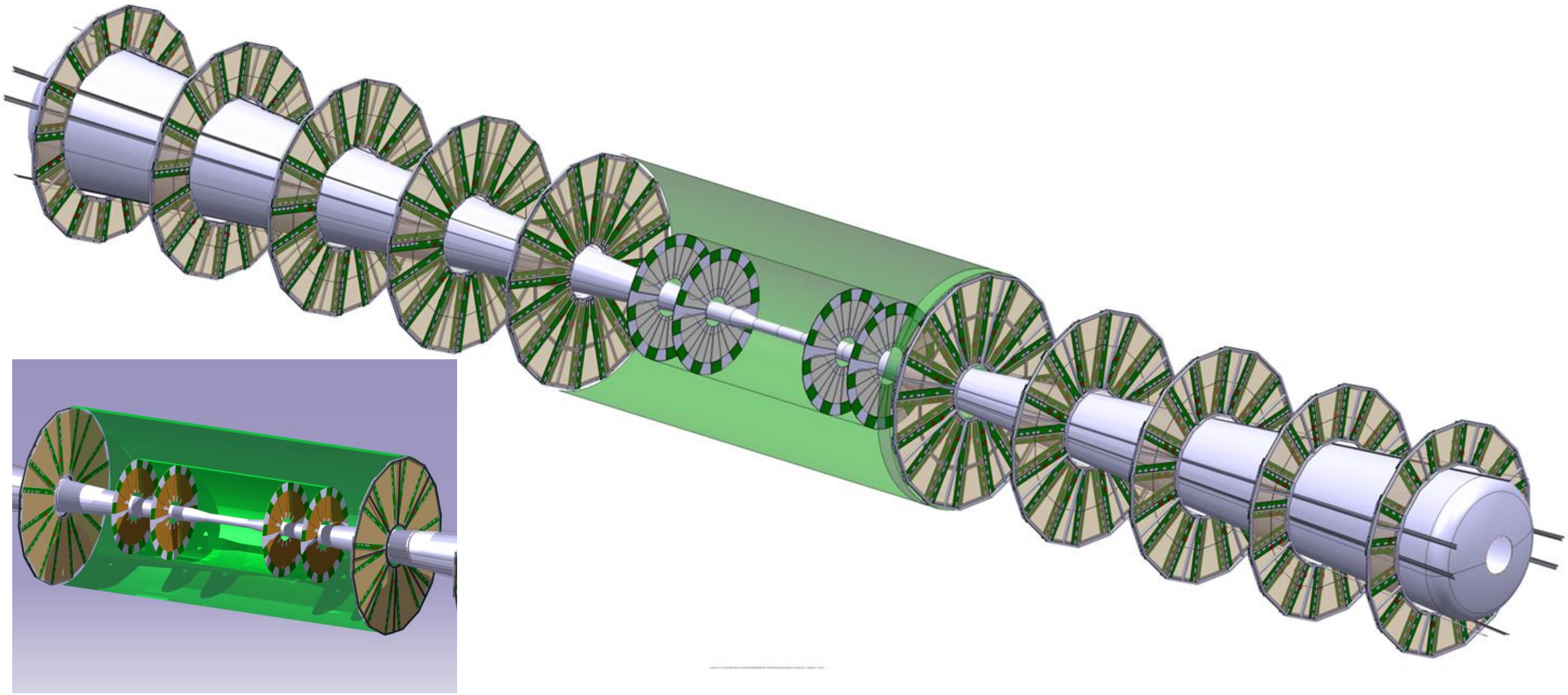
DESIDERATUM:

To reorganize the silicon tracker system as a unique system

FORWARD TRACKER STATUS

***Baseline sensor**: conventional microstrip sensor with integrated signal routing in a second metal layer.*

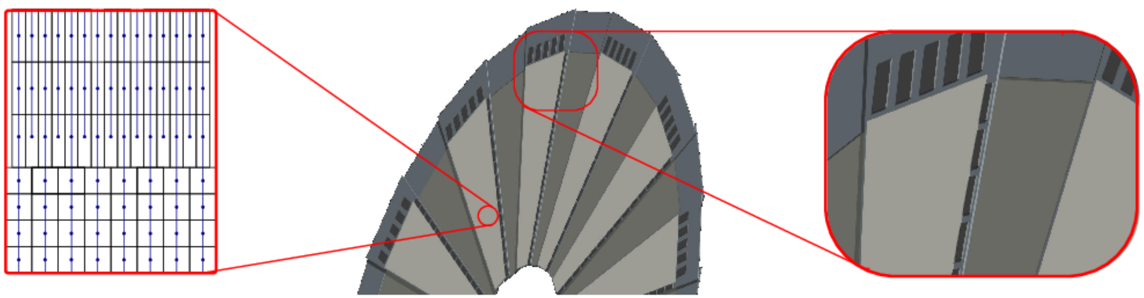
***Baseline operational unit**: petal (sensor+standard hybrid board(s) with readout, powering and data link circuitry.*

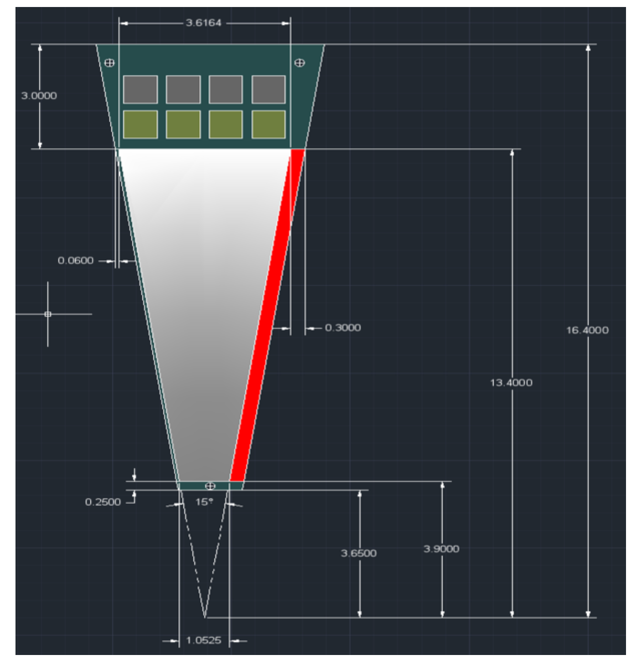


R&D on future technologies (see I. Vila talk)

DEPFET @ LC disks

- LC detector concepts require pixelated disks
→ vertex detector end-cap in SiD, Forward Tracking Disks in ILD
→ adapt DEPFET all-Si "ladder" design to "petal" geometry





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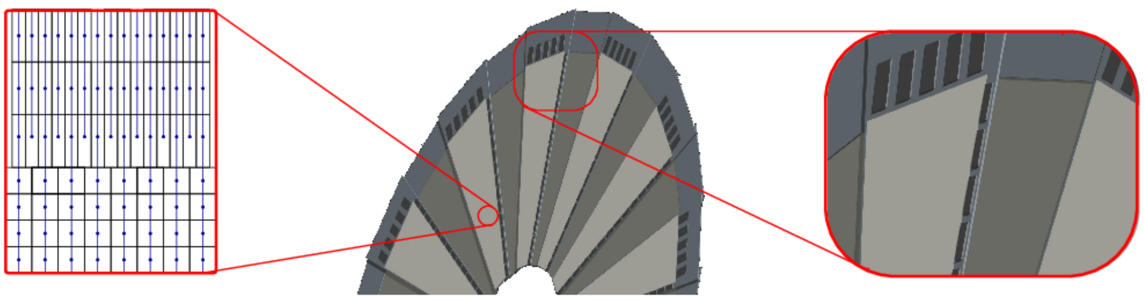
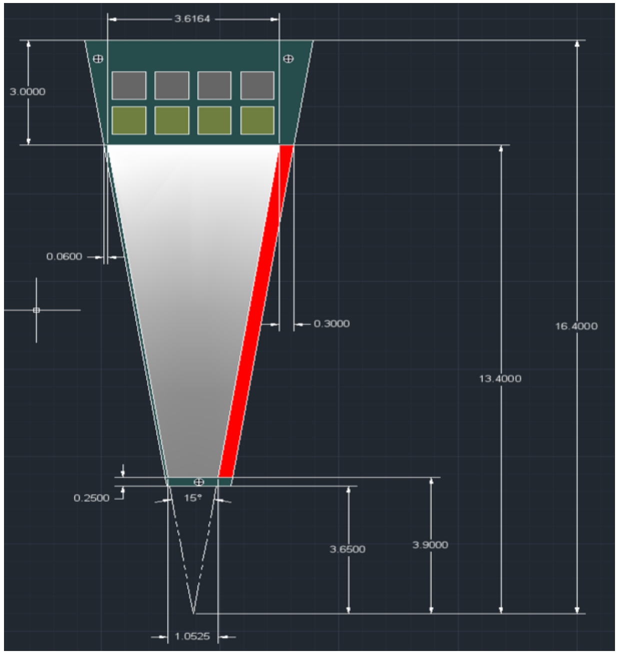
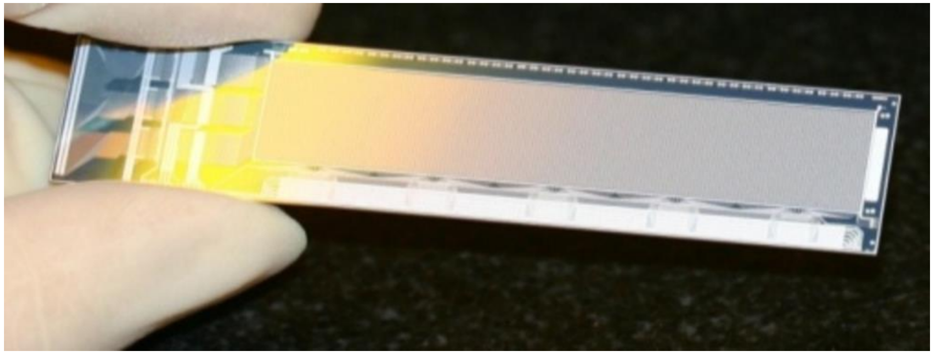




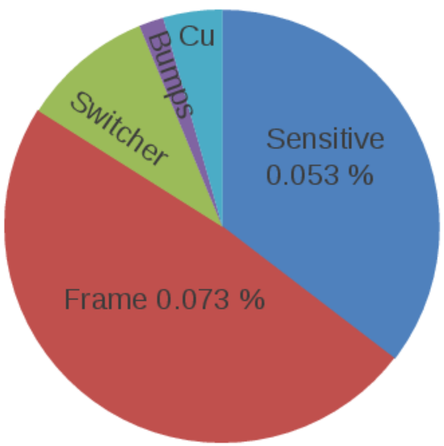
- ***Working on fully engineered design + mock-up***
- *Hoping to learn:*
  - *Sensor: feasibility of layout with variable pitch & length*
  - *Ancillary: length of switcher lines, load on DCD...*
  - *Mechanics: self-supporting frame*
  - *Cooling: air flow through disks*
  - *Physics: assess performance of this design*

DEPFET @ LC disks, Material budget



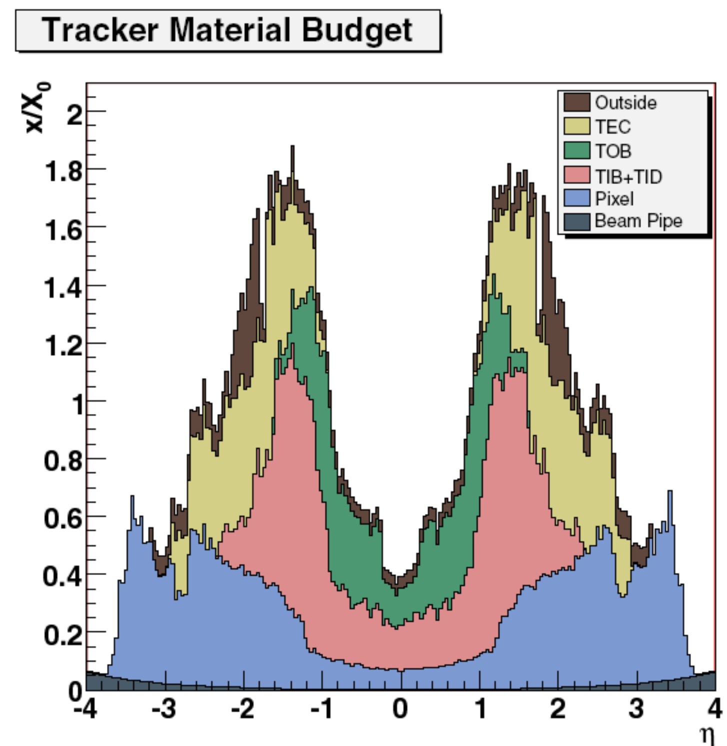
Integrate!

Amplification stage in sensor
Support structure in sensor
Signal and power lines on sensor
Electronics on sensors



Sensitive	0.053 % X_0
Frame	0.073 % X_0
Switcher	0.015 % X_0
Cu layer	0.007 % X_0
Bumps	0.003 % X_0
Total ladder	0.15 % X_0

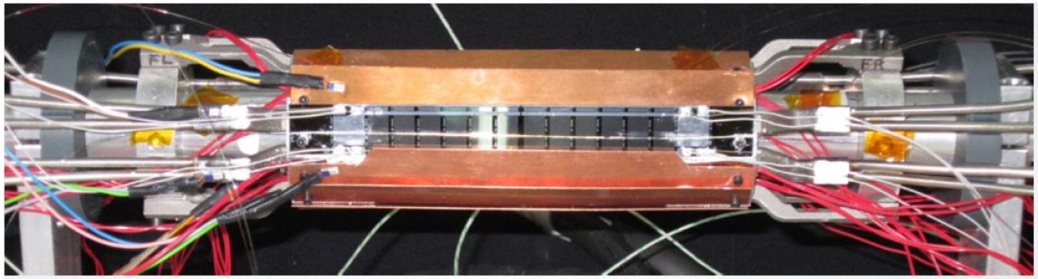
Material budget close to LC goal!!!



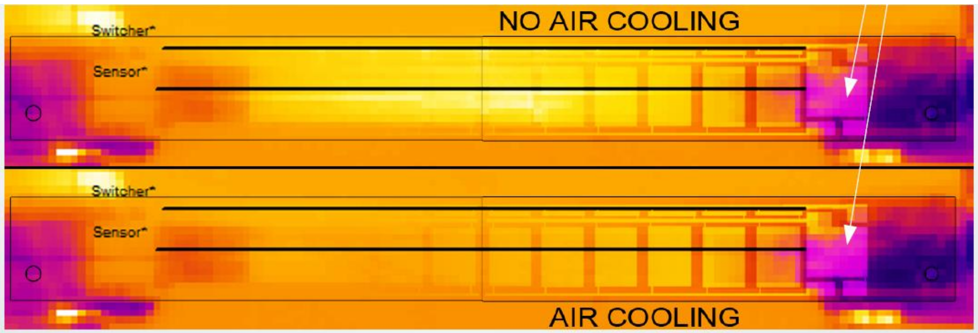
Big leap wrt to LHC...

Admittedly not a fair comparison

COOLING



Valencia PXD Mockup



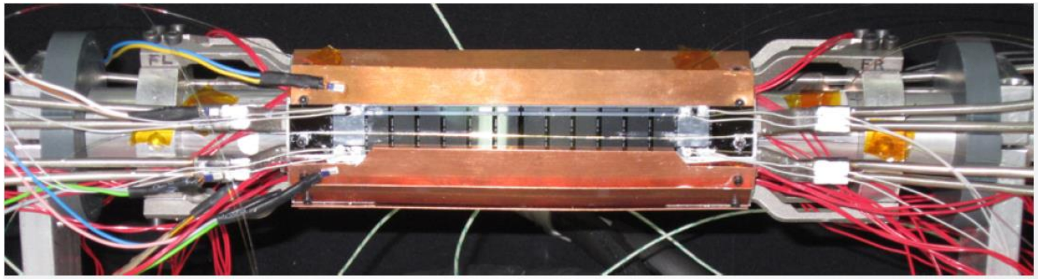
Sensor T	Ambient T = 25ºC	
Without convective cooling	T_{MAX}=~40ºC	ΔT=~15ºC
With convective cooling	T_{MAX}=~25ºC	ΔT=~5ºC

BELLE II (IFIC-IFCA DESY May 2013)

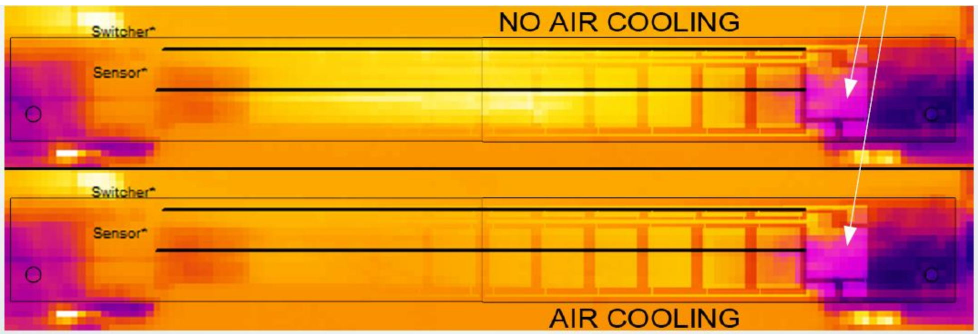
- Cooling of a working fine pixel sensor works properly
  - Combining contact and convective cooling
- No vibrations observed at the pressures studied for cooling

- <u>ILD</u>
  - Naively ~900 to ~1080 W total
  - ~4 to 5 W with power pulsing (ideal 1:200 duty cycle)
  - No active cooling due to angular acceptance requirements
    - Convective cooling (performance demonstrated in Belle II)

COOLING



Valencia PXD Mockup



Sensor T	Ambient T = 25ºC	
Without convective cooling	T_{MAX}=~40ºC	ΔT=~15ºC
With convective cooling	T_{MAX}=~25ºC	ΔT=~5ºC

THERMAL MANAGEMENT:

- Needed more effort to characterize innermost disks

- Fabrication mock-ups, measurements and simulation

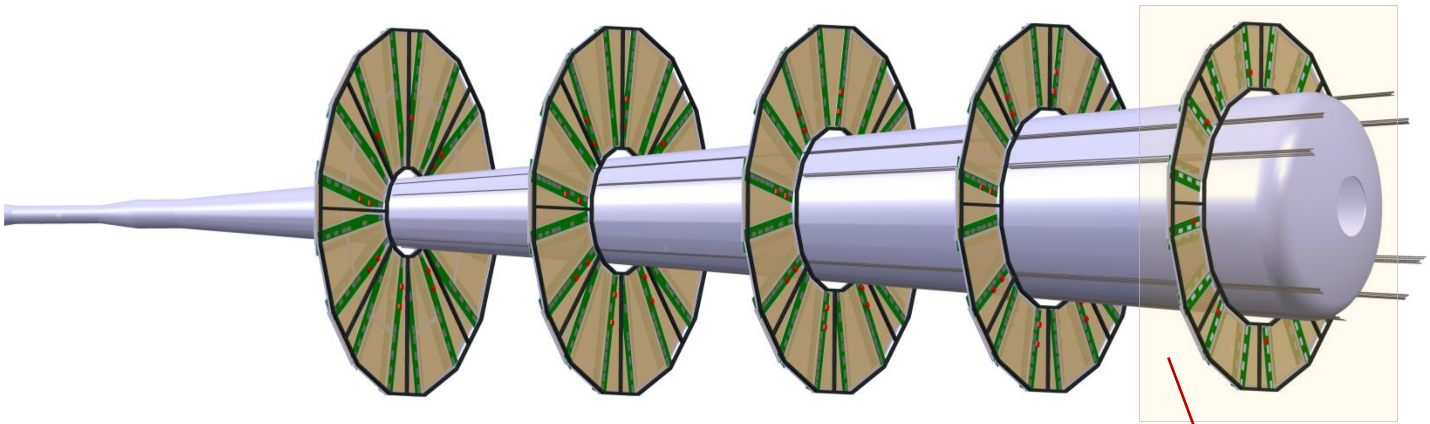
- We have instalations

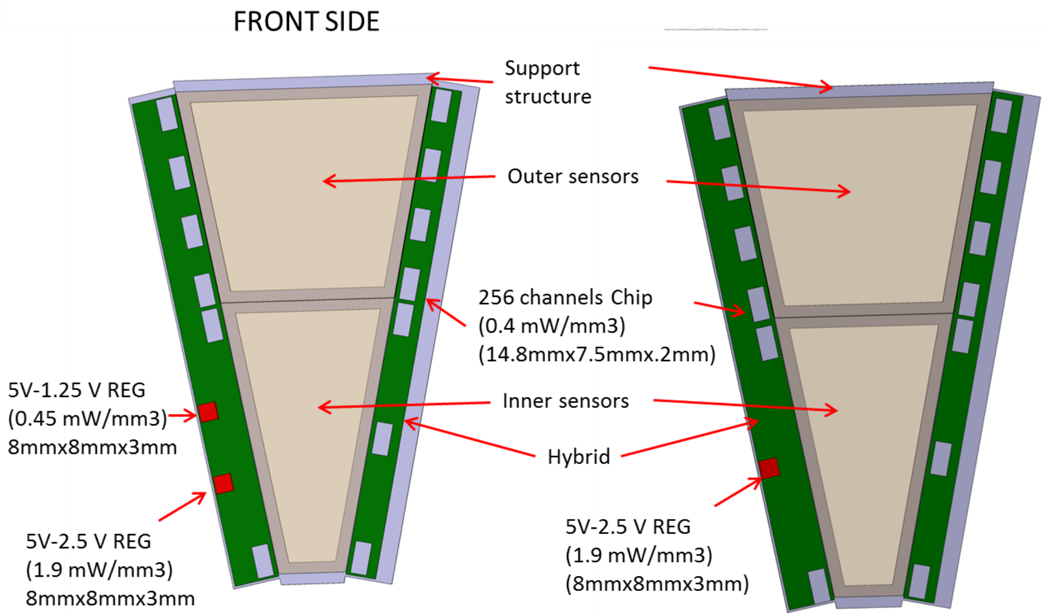
BELLE II (IFIC-IFCA DESY May 2013)

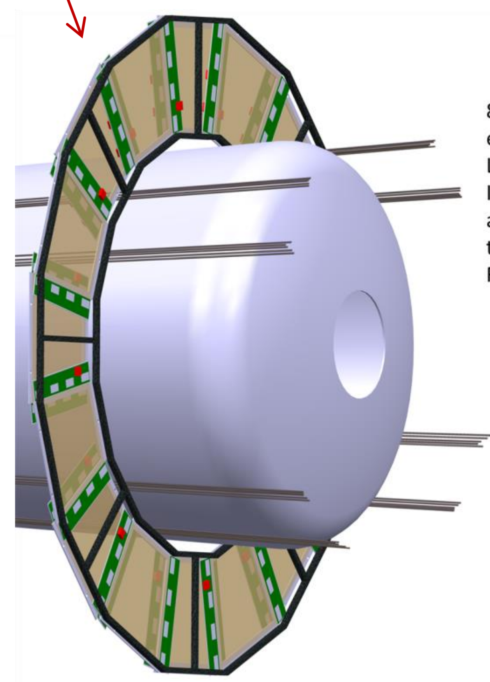
- Cooling of a working fine pixel sensor works properly
  - Combining contact and convective cooling
- No vibrations observed at the pressures studied for cooling
- ILD
  - Naively ~900 to ~1080 W total
  - ~4 to 5 W with power pulsing (ideal 1:200 duty cycle)
  - No active cooling due to angular acceptance requirements
    - Convective cooling (performance demonstrated in Belle II)

FORWARD TRACKER STATUS

MECHANIC,CABLES





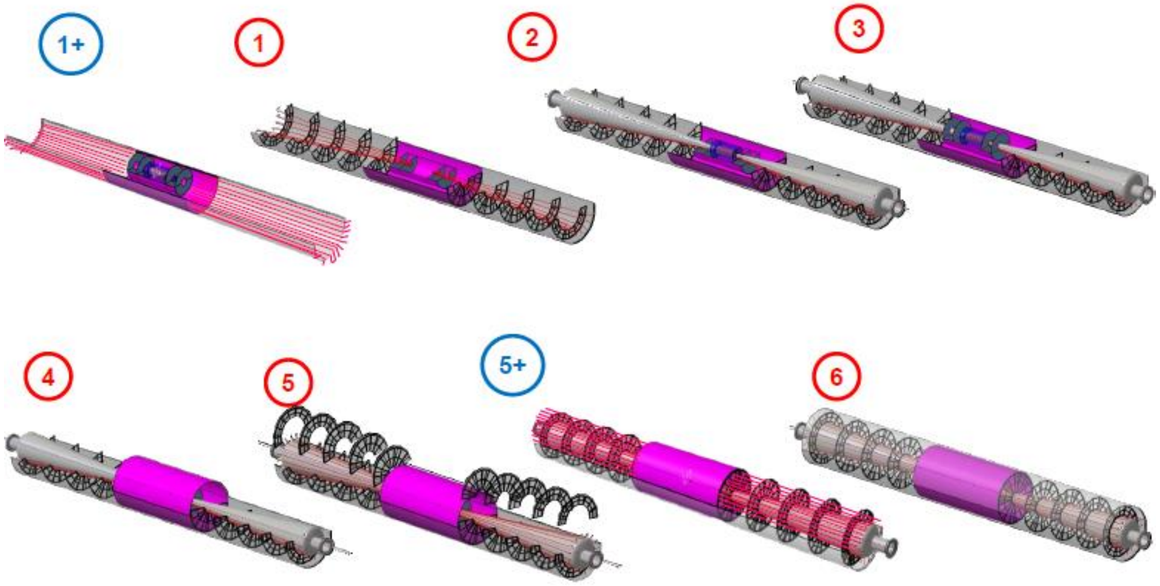


8 cables bunches each composed of 5 LV and 5 HV cables. In total 40 LV cables and 40 HV cables at the outer part (only FTD3-7.

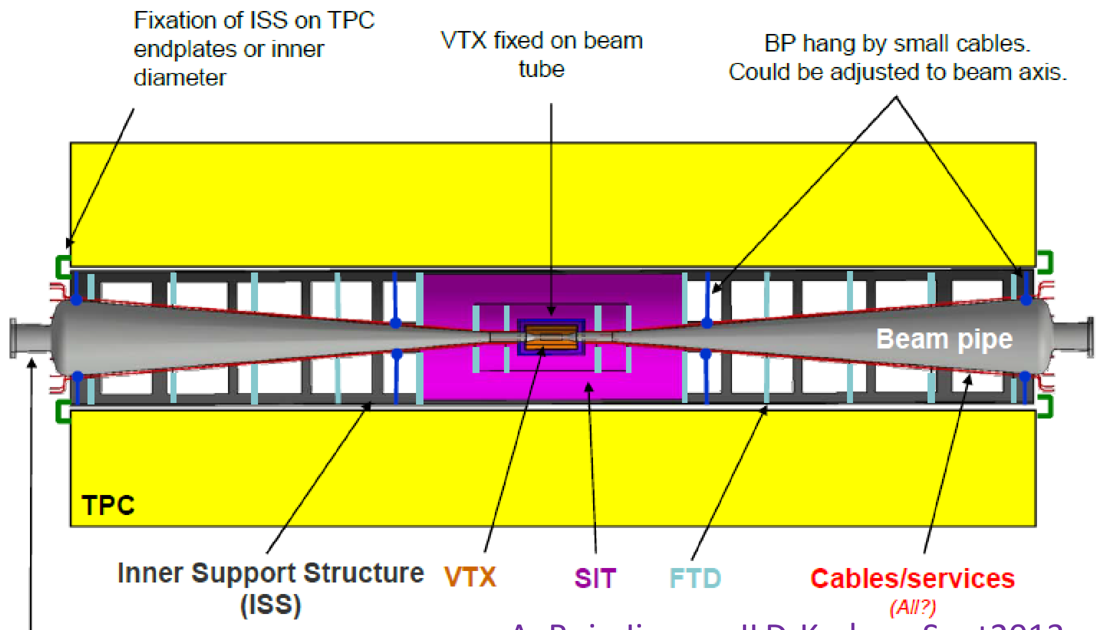
STUDY, PROGRESSING

FORWARD TRACKER STATUS

ASSEMBLING



STUDY, PROGRESSING

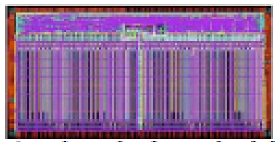


FPA2008-04122-E FPA2008-05979-C04-02 AIDA

2007 2008 2009 2010 2011

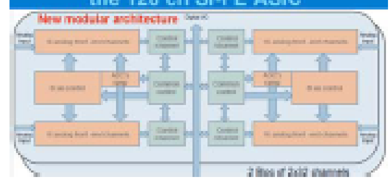
Start of collaboration with IN2P3
Design of the digital part

SiTR-88-130UMC

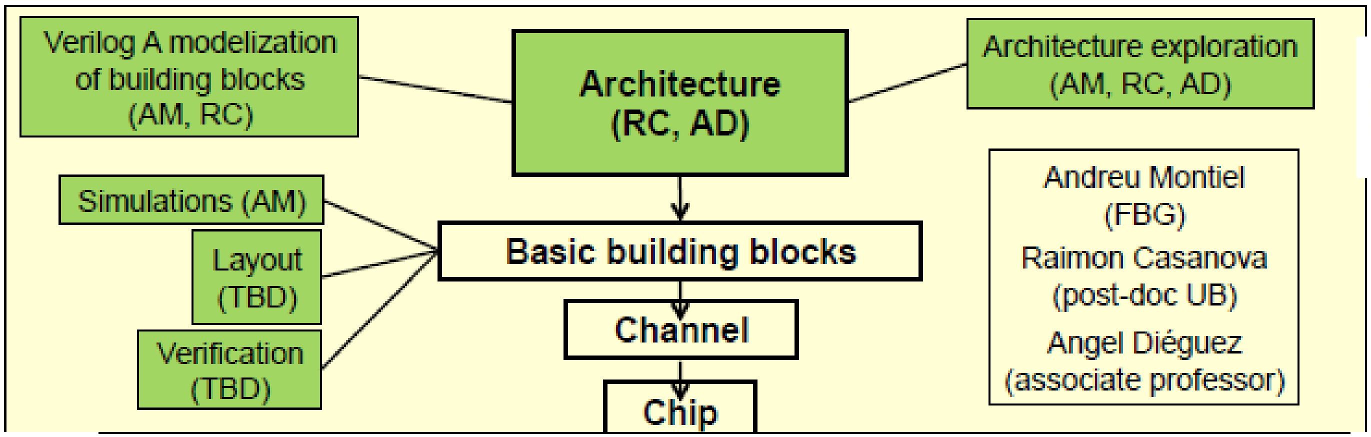


(1st mixed signal chip)

Definition of new architecture



Complete new design (responsability of UB)



AIDA

Dr. Ángel Diéguez adieguez@el.ub.edu
Electronics Departament, University of Barcelona

VLSI Design Group

Department of Electronics
Universitat de Barcelona

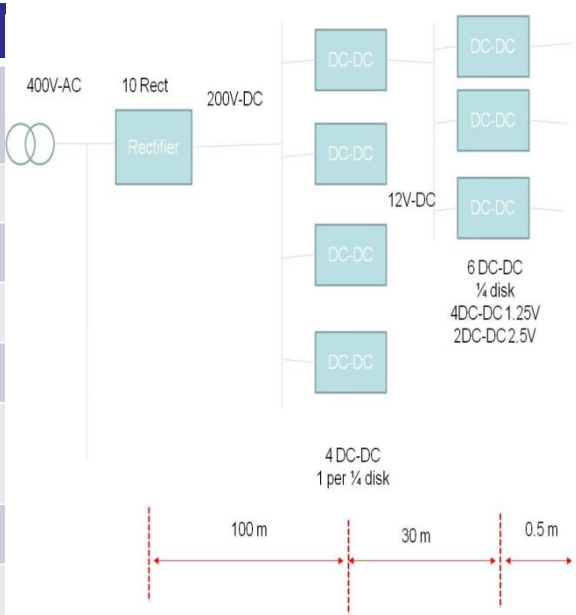
In an initial phase. Much work to be done
There are possible fall-back solutions

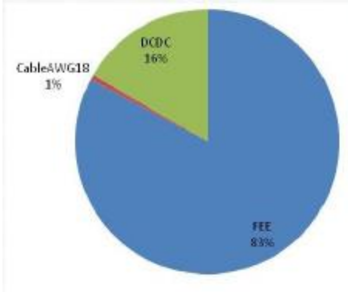
POWER SYSTEM

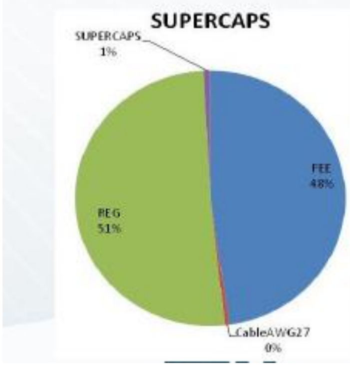
There are several topologies that may be used for FTD.

- DC-DC-based power distribution
- Super-capacitor based power distribution

	DC-DC	Super-caps
Power dissipation	228 W	395 W
EMI phenomena	Yes	No*
RAD tolerant	Yes	?
Material budget	(240 DC-DC) ?	(80 SC) ?
Reliability	?	?
Power pulse applications	Not frequent	Yes
Installed power	1.4 kW	0.48 kW
Primary PS	≈ 36 W	≈ 15 W
Mains protection (UPS effect)	No	Yes





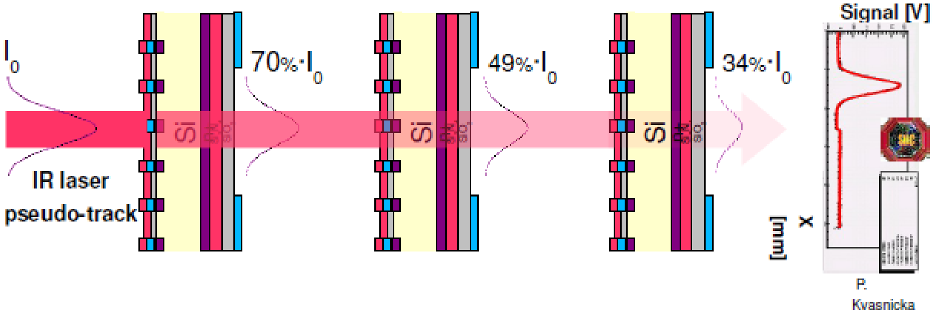


WORK ONGOING SATISFACTORILY

See F.Arteche talk

ALIGNMENT

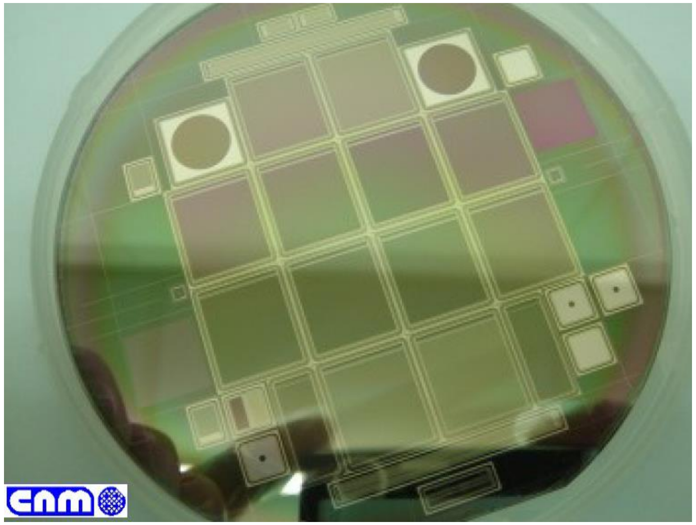
• Laser tracks can be used by a hardware system to align the tracker

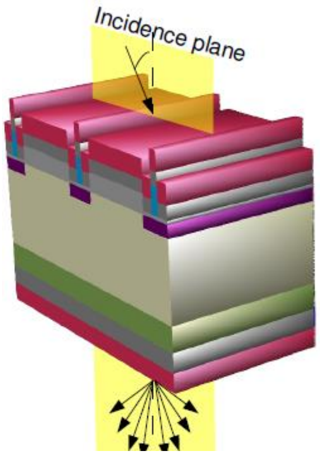


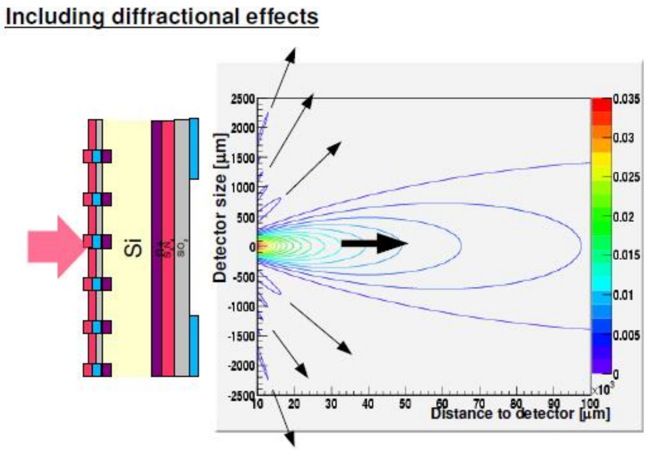
Improved InfraRed transparent microstrips detectors for tracker alignment

• First implemented by AMS I, then AMS II and CMS

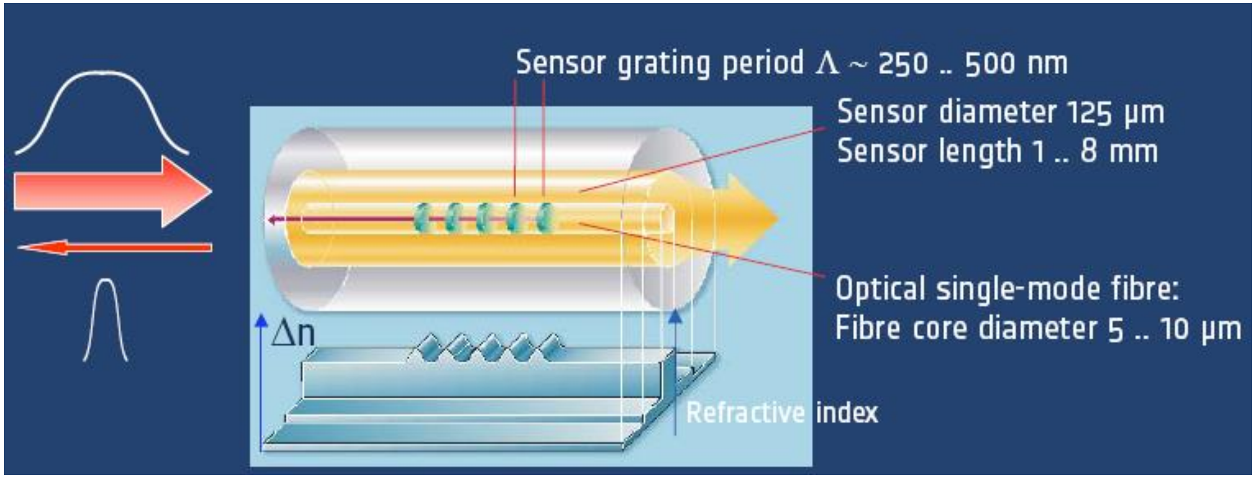
WELL ADVANCED

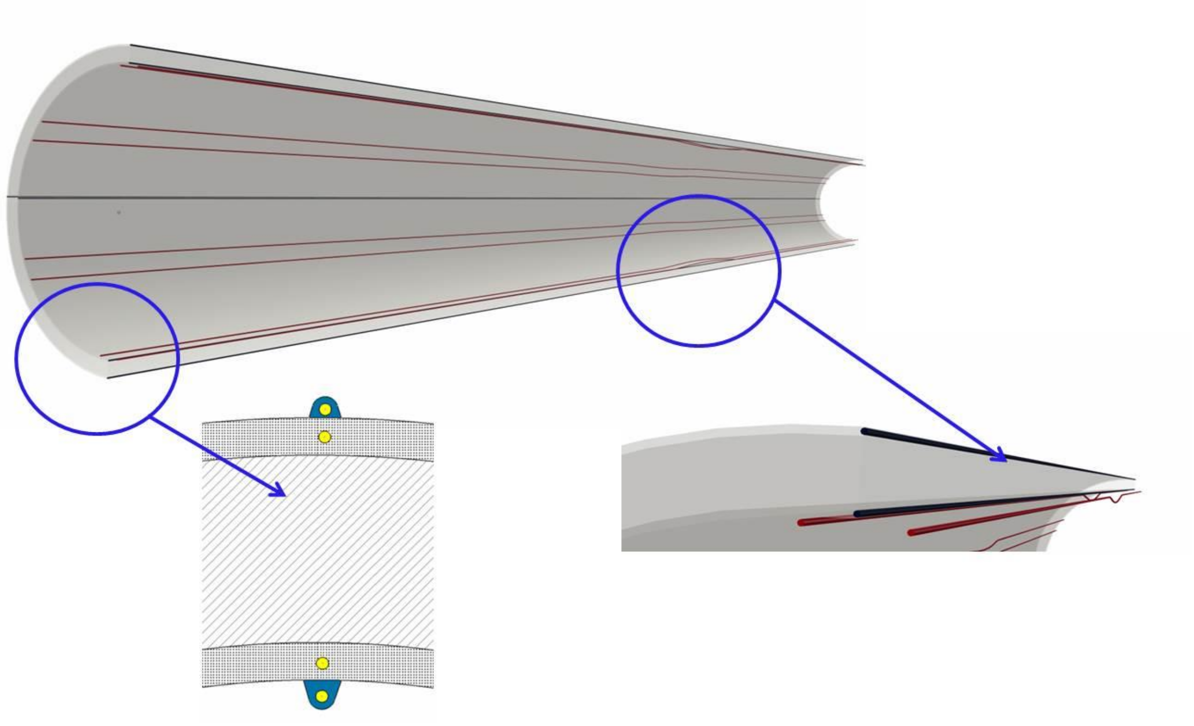






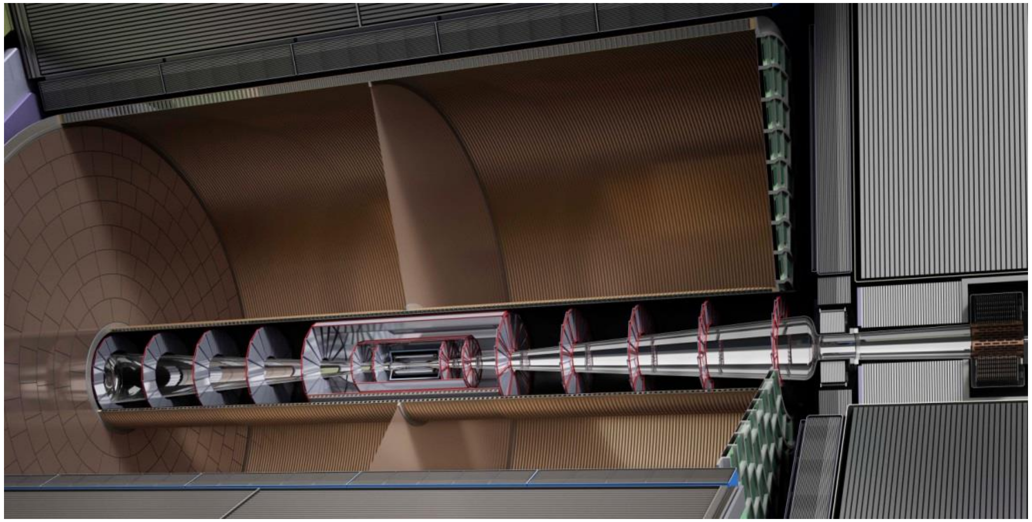
Real Time Structural and Environmental Monitoring

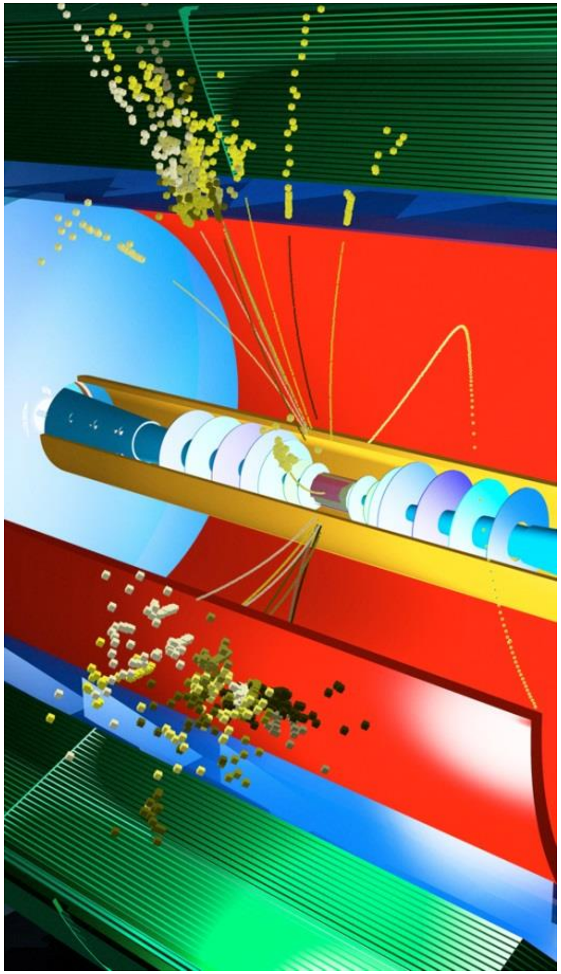




PROGRESSING

OPTIMIZATION





Study to optimize design in a meaningful way:

- samples: some signal with jets (tt), pair production and $\gamma\gamma \rightarrow$ hadrons (ILD MC team?)
- design: provide alternative designs (Spanish LC network)
- technology choice?: no, assume generic performance parameters in DBD
- analysis: ad-hoc task force (joint venture of tracking software team + Spanish LC network?)

Lack of manpower

Costs

Costs

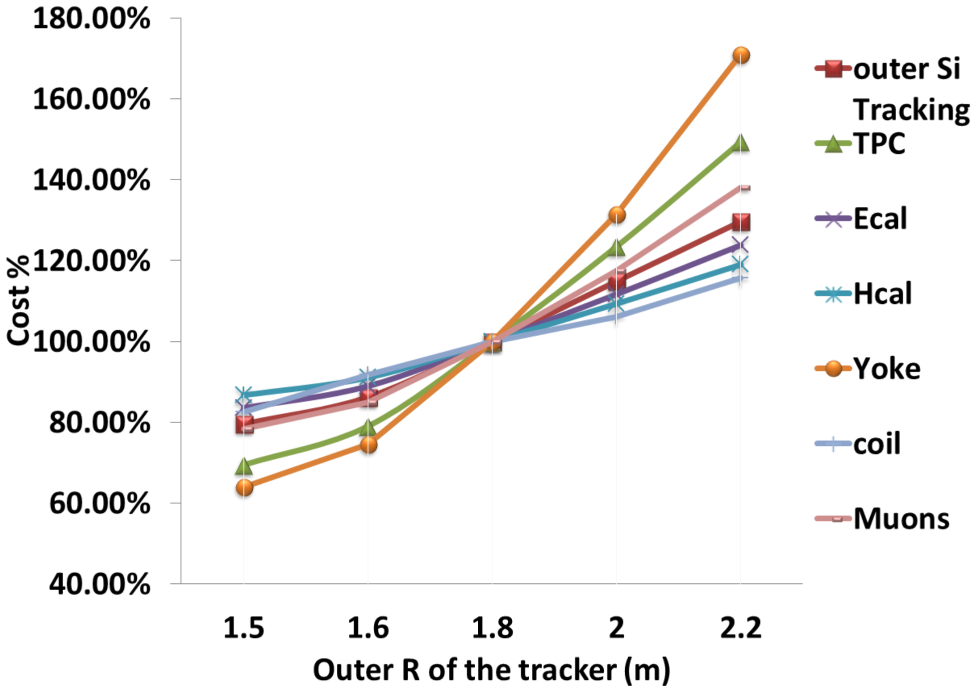
- One way to reduce overall costs is to reduce the size

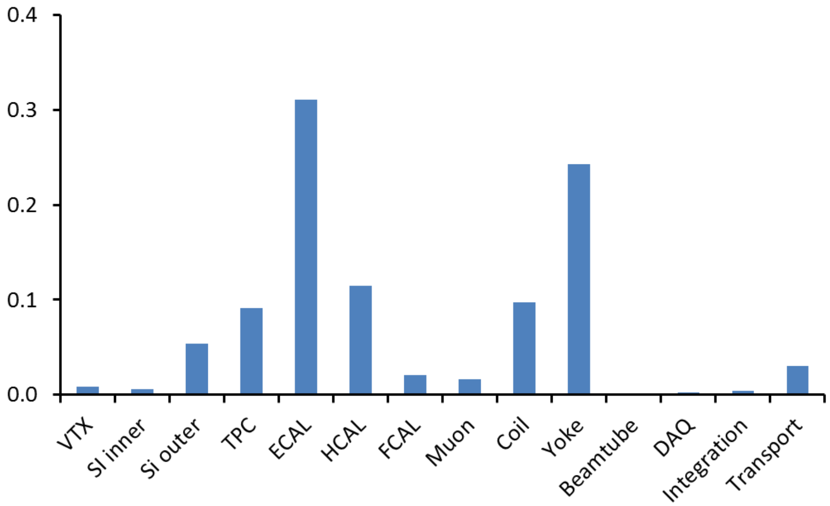
Costs

- One way to reduce overall costs is to reduce the size
- Reducing the size of ILD by 10% (to 1.6 m for the tracker) saves about 20% for the tracking, 15% for Ecal, 15% for Hcal, 15% for the coil, and 30% for the yoke.

20% x 15% ≈ 3% for the tracking,
15% x 30% ≈ 4.5% for the Ecal,
15% x 10% ≈ 1.5% for the Hcal,
15% x 10% ≈ 1.5% for the coil, and
30% x 25% ≈ 7.5 % for the yoke.

about 100M€ altogether





Costs

- 100M€. Does this make sense? Yes, of course, but...
- What happens to the performance?
  - Vertexing ≈ unchanged.
  - Momentum resolution ≈ 20% worse.
  - Particle flow resolution ≈ ? (depends on the what happens to the Ecal granularity)
  - Coil is the size of CMS‘s, new tooling doesn‘t cost much, but experience with 4T?

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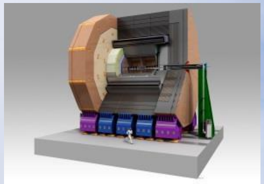
  - Coil is the size of CMS‘s, new tooling doesn‘t cost much, but experience with 4T?
- Bottom line:
  - Mainly a question for Ecal granularity
  - And performance
  - An old wisdom: don‘t save money in the wrong place



TR@cking in ILD

We are approaching the goal !

BACKUP

_Power distribution system

– Currents consumption of Strip – FTD

	MIDDLE PITCH									
FTD	FTD3		FTD4		FTD5		FTD6		FTD7	
	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT
Nº STRIPS PER Module (2sensors)	4096	2560	4096	2560	4608	3072	4608	3584	4608	3584
Chips per petal	52		52		60		64		64	
Optical links per petal	1		1		1		1		1	
I2.5 (A) per Petal	2.56		2.56		2.8		2.92		2.92	
I1.25 (A) per Petal	1.18		1.18		1.34		1.42		1.42	
I per petal	3.74		3.74		4.14		4.34		4.34	
I per disk	59.84		59.84		66.24		69.44		69.44	

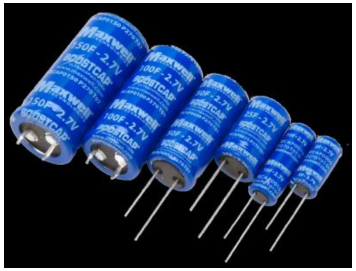
TOTAL Mstrip- FTD Current	**649 A**

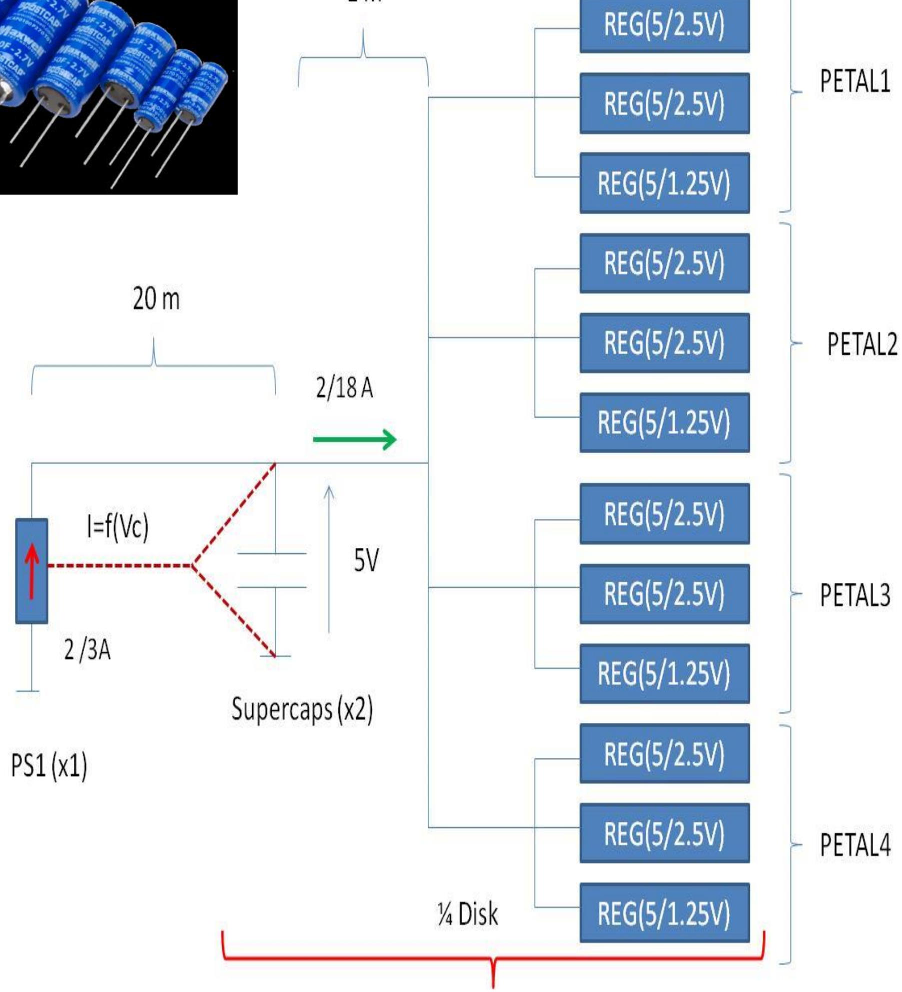
2.1 Powering schemes: DC-DC-based Power System

- Example (1/4 disk) : Power values per group:
  - Routing inside each petal:
    - 6 DC-DC converters
      - 4 DC-DC (12V - 2.5V)
      - 2 DC- DC (12V- 1.25V)
    - Max out current per DC-DC less than 3 A (low transients)
    - Short cabling – Less than 1 meter (low voltage drop)
  - Outside petal (1 cable per ¼ disk)
    - 1 DC-DC per power group
      - 200V – 12V
    - Max out current per DC-DC less than 3 A
      - Transients attenuated by the DC-DC
  - Outside experiment
    - 1 AC-DC per disk
      - 400V 50 Hz – 200V DC
    - Max current per cable less than 1 A

Powering schemes: Supercapacitor based PS

- This power system is based on :
  - **Supercapacitors**
    - Pulse power
  - **LV regulators**
    - Stabilize FEE voltage
  - **Current source**
    - supercapacitor voltage controlled
- To absorb transients related to power pulsing system.
  - Keep transients locally at FEE level.





Powering schemes: Supercapacitor based PS

- Power values per ¼ disk (power group)
  - Routing inside each petal
    - 3 Regulators
      - 2 REG (5V -2.5V) / 2.92 A Pk – 0.29A
      - 1 REG (5V- 1.25V) / 1.42 A Pk – 0.15A
    - Max out current per petal (16 petals) – 4.34 A / 0.434A)
    - Short cabling – Less than 1 meter (low voltage drop) ?
    - 2 Supercapacitors per (1/4 disk) – C=75 F / V=5 V / Imax=18 A /Imin=2
  - Outside petal - ¼ disk
    - 1 Cable per disk
    - Max out current per cable around 2/3 A (defined by FEE)
  - Outside experiment
    - 1 Current source per ¼ disk
      - IDC = 2/3 A
- A similar number of HV cable will be considered to keep the same granularity
  - 1 HV cable and HV power unit per ¼ disk

4. Conclusions

- A first radiation test campaign has been carried out to validate super-capacitors for HEP applications.
- 5 Super-capacitors
  - Maxwell, Nesscap and Panasonic (10F & 25F)
- Tests have been performed based on constant current
  - Normal operation (2.7A, 5A)
  - Stress operation (10 A and 16 A)
  - ERS,C and T have been measured
- There was not found big difference on the main characteristics and SC performance
  - No stoppers have been found
- More tests and analysis are planned
  - Temperature & Higher dose.
  - Annealing effects

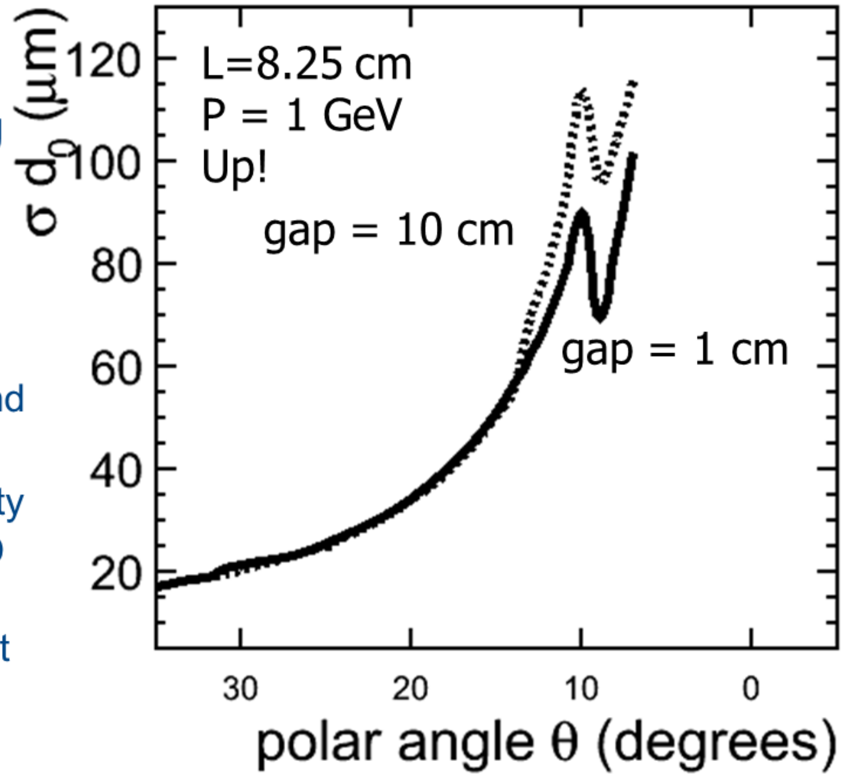
Zgap between the FTD1 and VTX

Comparison z_{gap}

Minimize the gap! *

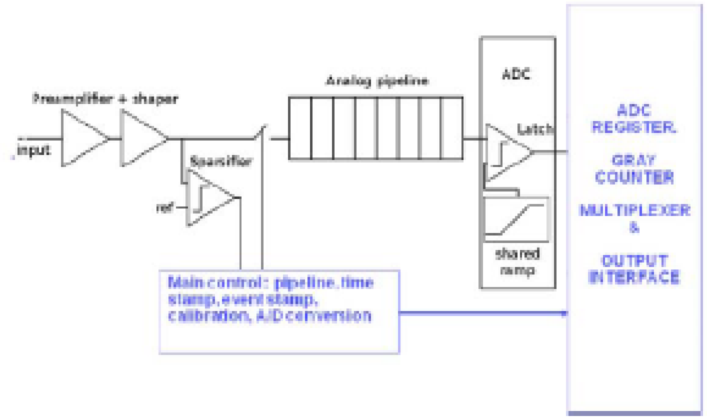
But: if we route the services along the beam pipe, the forward vertexing performance is terrible and essentially insensitive to z_{gap}

* In ILD the distance between VXD and innermost FTD is close to 10 cm. This clearance is motivated by the possibility to fit in a VXD cryostat. If a "cold" VXD technology is chosen, a short gap implies one has to install the innermost disks inside the cryostat.



Front End Electronics

- In AIDA-WP9 a readout chip for Si-microstrips for ILD is being developed by UB with 65nm process
  - ✓ Designed:
    - *T indep current source*
    - Amplifier in the preamplifier
    - Preamplifier, shaper
  - ➢ *To be designed*
    - Analog pipeline, Ramp or SAR ADC,
    - Discriminator, sparsifier, digital logic, I2C/SPI, LVDS, …



Concurrent designs with 65nm process:

- 65nm process is used in the development of the DHP together with Bonn Univ. in the framework of DEPFET collaboration for Belle II
  - ✓ Designed, fabricated and tested:
    - *T indep current sources, current-mode DAC*
  - ➢ *Designed*
    - T sensor

One module of each FTD disk will be composed by four petals (16 sensors) in order to reduce cables. For each module we will have eight LV 5/2.5 regulators, four LV 5/1.25 regulator and two supercapacitors. Each disk will be by a power system of 16 W. The power to two supercapacitors will be transmited usin an AWG 16 cable . The conexión from the supercapacitors to the LV regulators will be done by and AWG16 cooper cable too. For each module we will have too one HV cable (AWG25) and one optical cable. So for each module there will bee four cooper cables with a total section of 3.03 mm2 and for each disk 16 cables with a total section of 12.12 mm2.

Per module we will have:

2 LV cables (AWG 16) for supercapacitors powering

2 HV cables (AWG 24) for sensors polarizing

1 fiber optic for results transmision

In the next table can be seen the total numbre or cables and cooper section going outside the FTD. Only is taking into account the ustrip FTD cables (it must be added vertex, SIT and pixel FTD-s cables)

	FTD3	FTD4	FTD5	FTD6	FTD7
Fiber optic cable	4	8	12	16	20
Nº HV cables (AWG 24)	8	16	24	32	40
Nº LV cables (AWG 16)	8	16	24	32	40
Total cooper section (mm2)	12.092	24.184	36.276	48.368	60.46