HCAL R & D

- AHCAL
- SDHCAL
- Conclusions

Katja Krüger

ILD meeting

Krakow, 24 September 2013

HELMHOLTZ ASSOCIATION

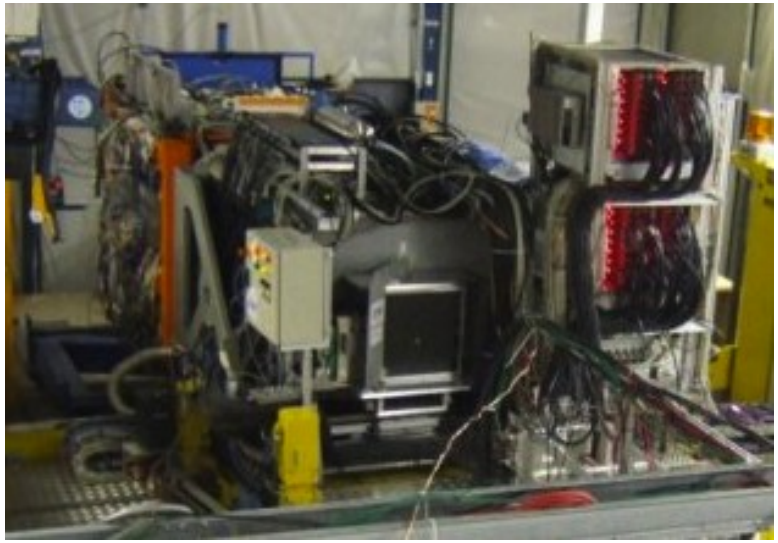
CALICE Calorimeter for ILC

Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

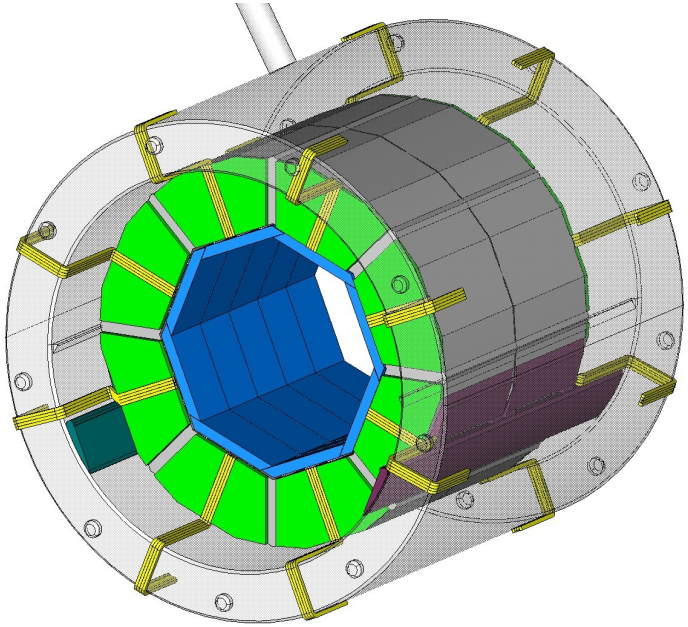
DESY

AHCAL Status

- capabilities of a highly granular scintillator-steel (or tungsten) calorimeter successfully demonstrated with the “physics prototype”:
  - validation of Geant4 simulation
  - validation of PFA performance
  - 7 journal publications + additional 9 Calice Analysis Notes

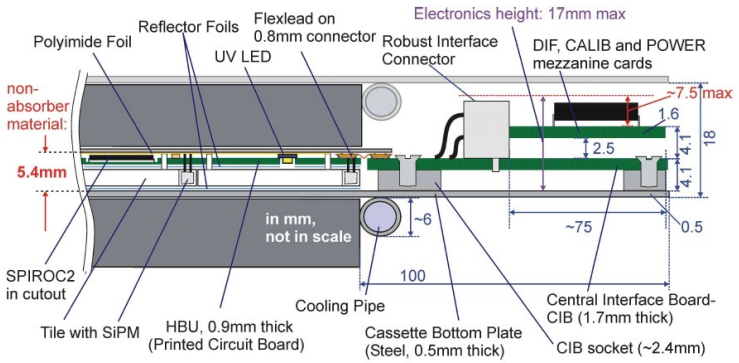


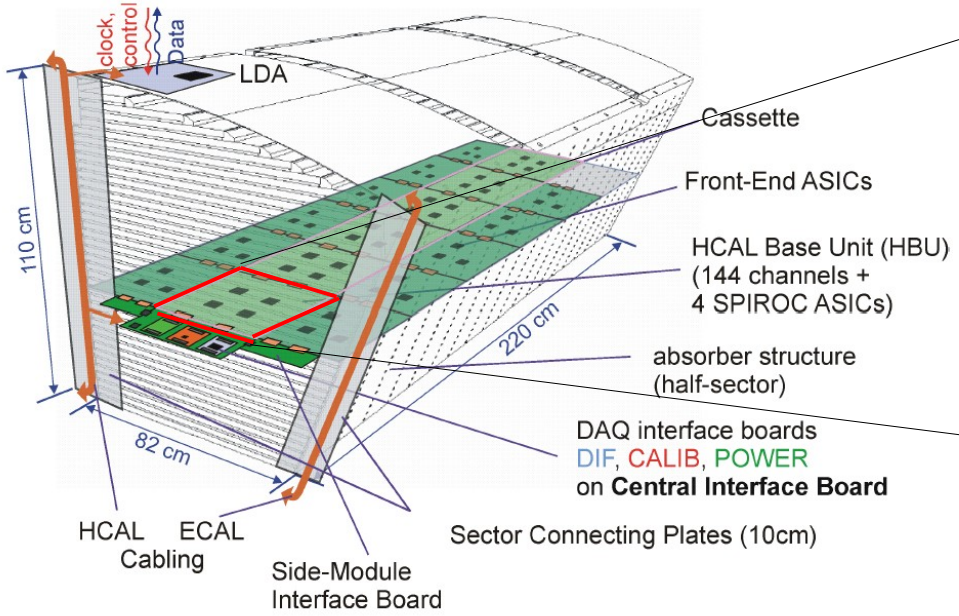
- goal for the “engineering prototype”: develop, build and test a prototype scalable to the full ILD layout
  - integration of electronics into active layers
  - realistic infrastructure: cabling, cooling, DAQ

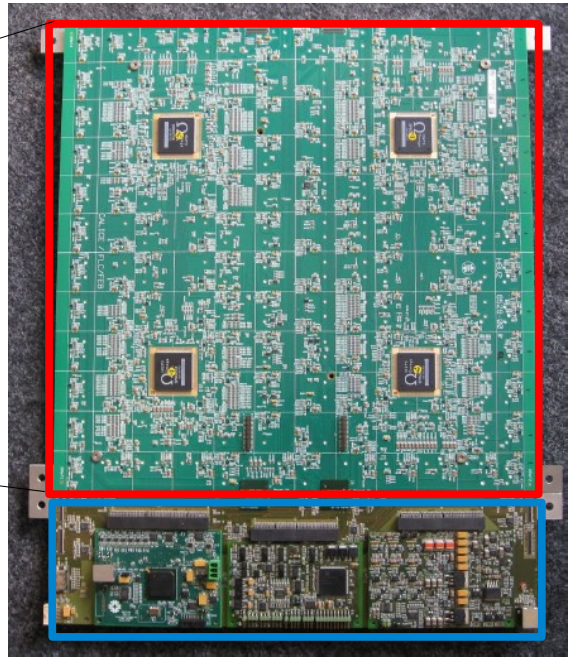


AHCAL engineering prototype: Integrated Electronics

- HCAL Base Unit: 36*36 cm^2, 144 tiles, 4 SPIROC2 readout ASICs
- Central Interface Board: DIF, Calibration, Power for 1 layer
- 5.4 mm active layer thickness
- 1 layer has up to 3*6 HBUs

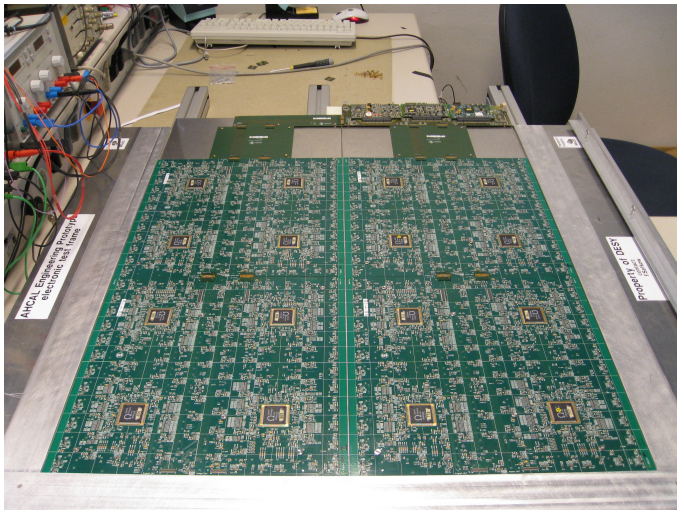


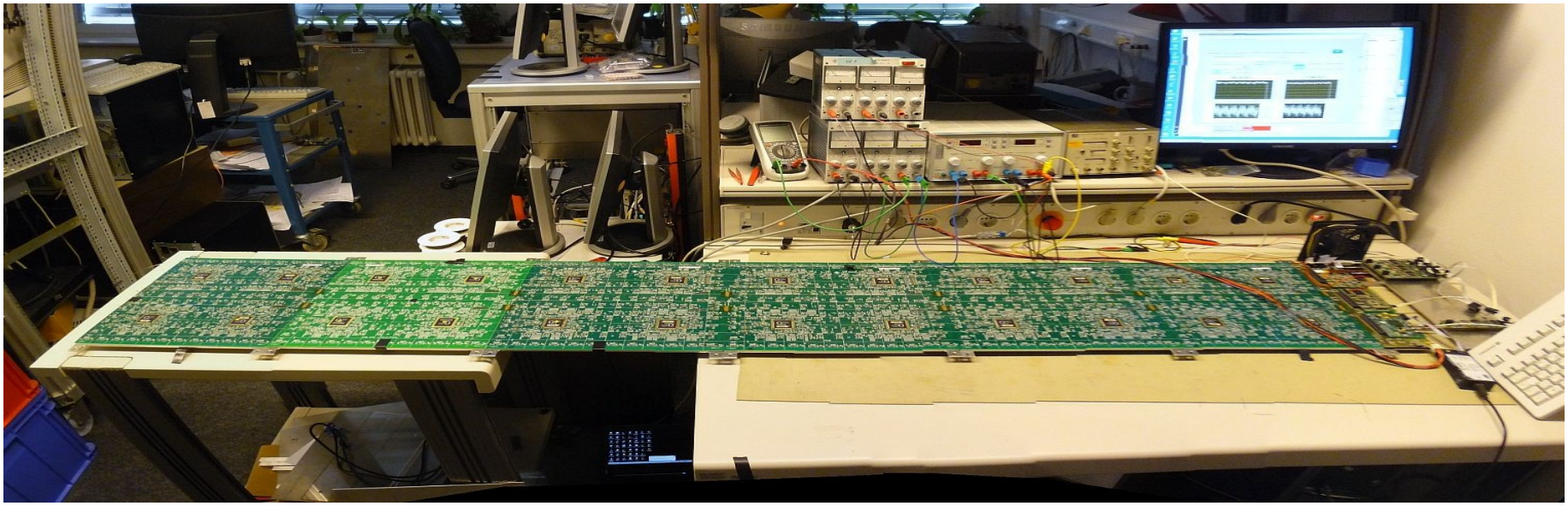




AHCAL engineering prototype: Layer Integration

- single HBUs extensively tested and calibrated in lab, cross checked in DESY testbeam
- operation of a full slab with 6 HBUs in the lab
  - started tests of power pulsing with a full slab
- operation of 2*2 HBU layer in CERN testbeam

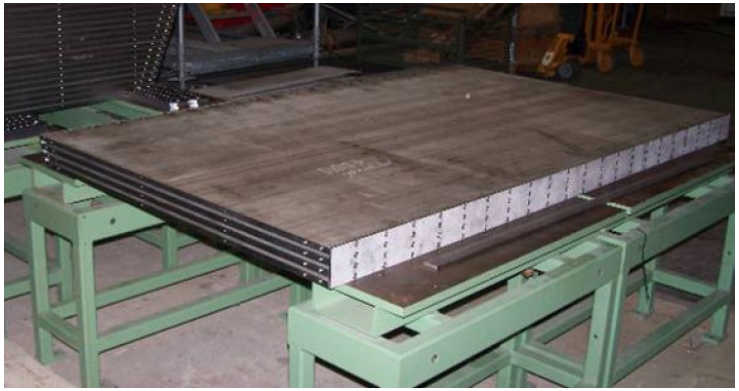




AHCAL engineering prototype: Stack Integration

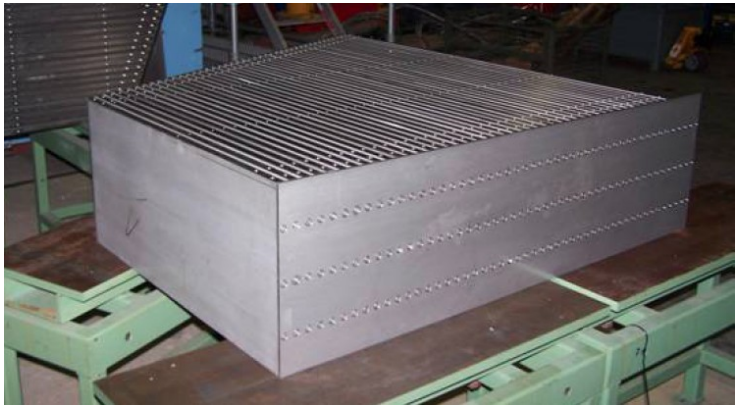
layer-wise integration solved, still to test:

- power pulsing
- mechanics & heat dissipation of 6 HBU-length layer



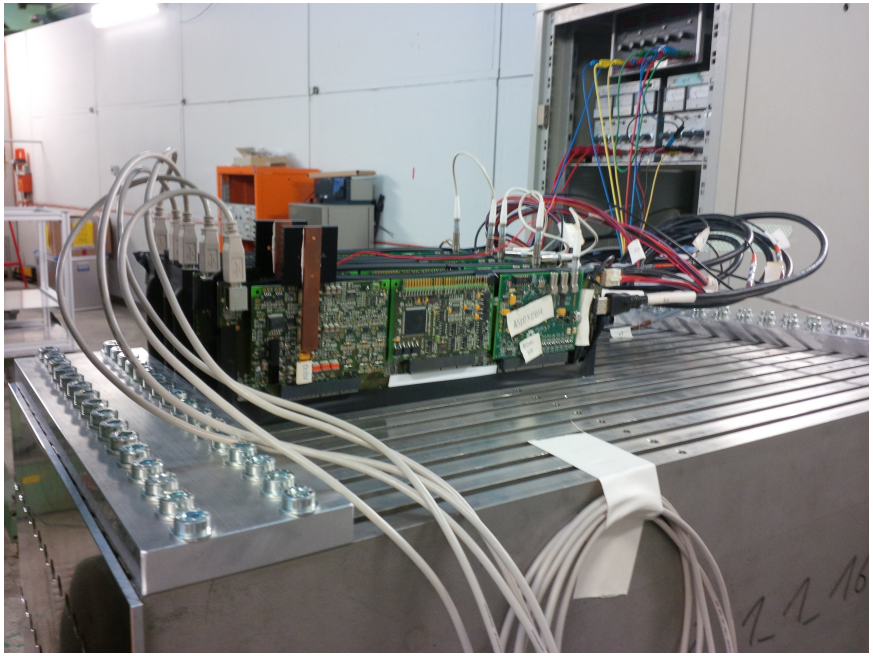
now working on stack integration:

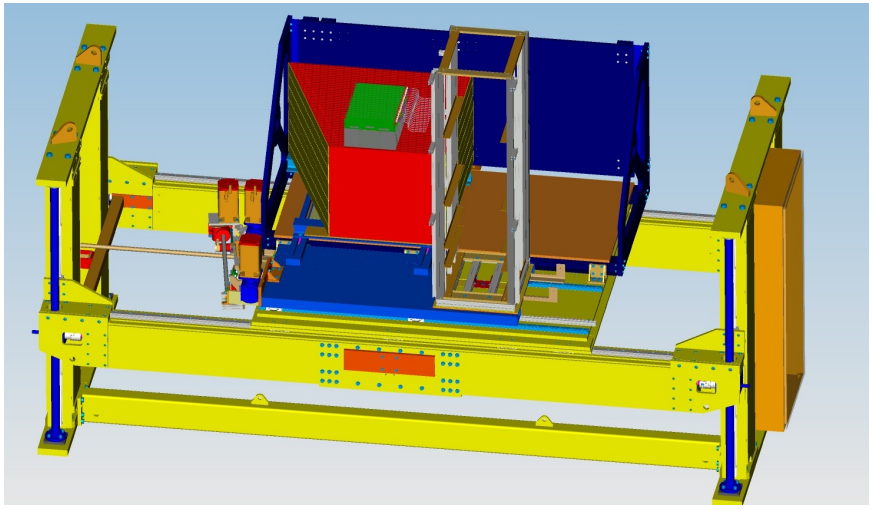
- mechanics:
  - absorber stack (+ air stack)
  - cassettes
- multi-layer DAQ
- infrastructure: power supply and cooling



AHCAL Mechanics: Stacks

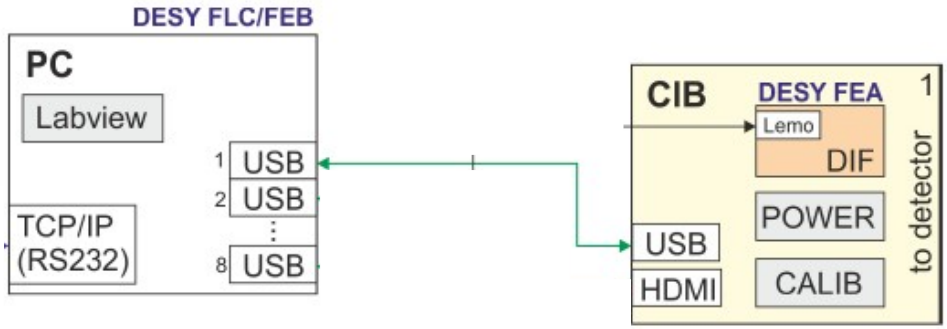
- ILD-like absorber stack for 15 layers (EM showers) installed “permanently” in DESY testbeam 22
- preparation of big EUDET stack (2 HBU deep, 1/3 of a ILD barrel sector)
  - nearly $1m^3$
  - will fit hadronic stack of 40 layers of 2*2 HBUs





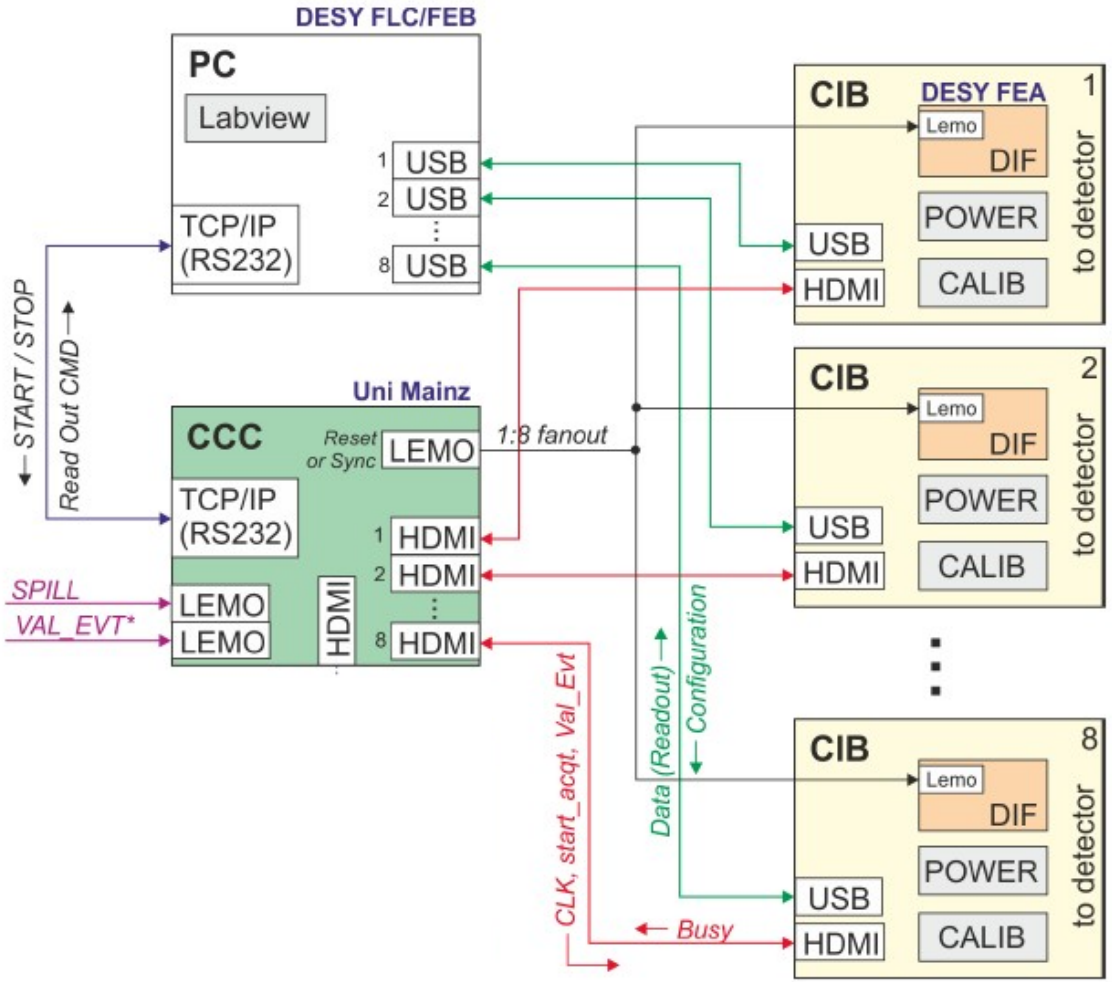
Progress towards a multi-layer AHCAL/ScECAL DAQ

- starting point: 1 layer DAQ (PC with Labview, 1 CIB) successfully operated in lab and testbeams



Progress towards a multi-layer AHCAL/ScECAL DAQ

- starting point: 1 layer DAQ (PC with Labview, 1 CIB) successfully operated in lab and testbeams
- status: Clock- and Control Card (CCC) included, fast signals via HDMI
  - operated successfully with 5 AHCAL layers
  - operated successfully with 2 ScECAL + 2 AHCAL layers



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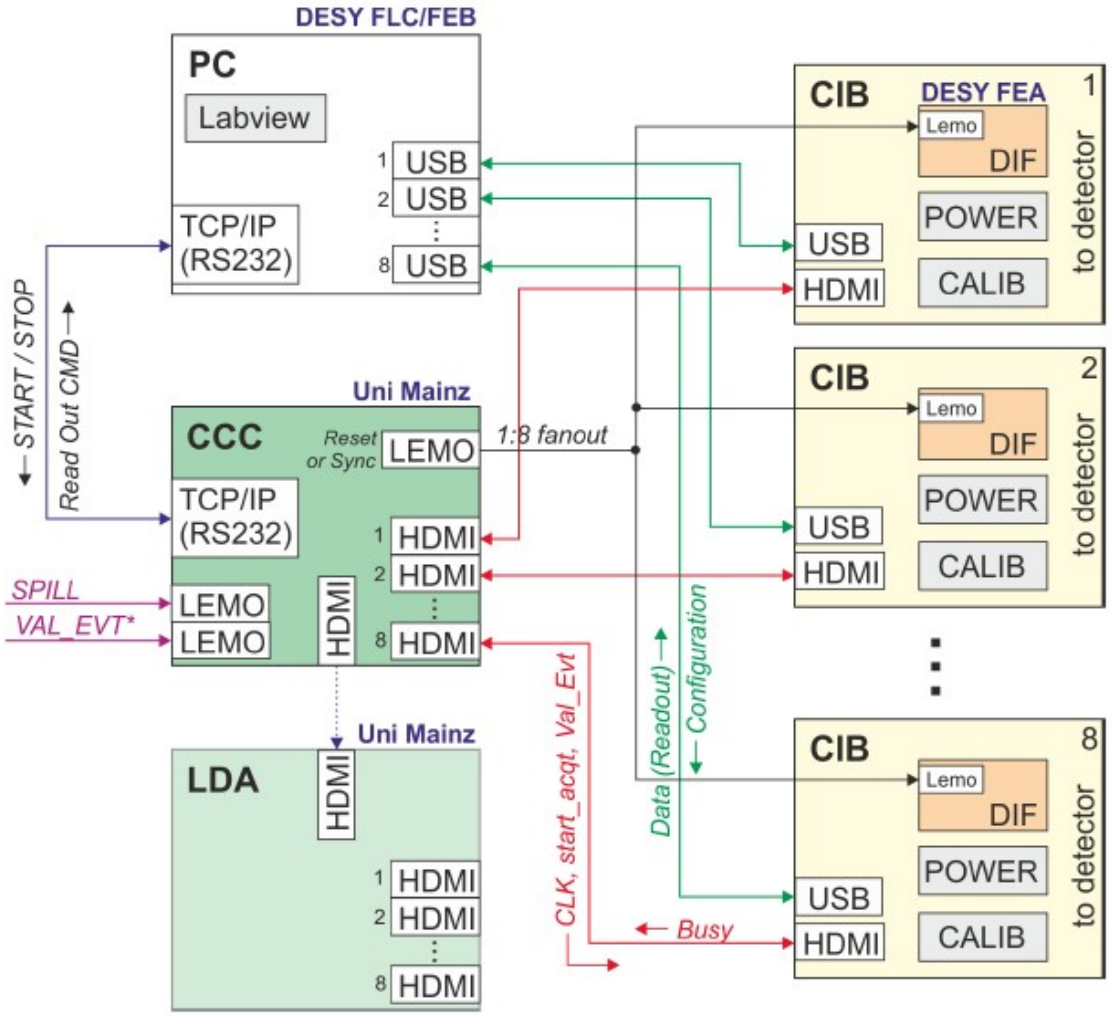
- starting point: 1 layer DAQ (PC with Labview, 1 CIB) successfully operated in lab and testbeams
- status: Clock- and Control Card (CCC) included, fast signals via HDMI
  - operated successfully with 5 AHCAL layers
  - operated successfully with 2 ScECAL + 2 AHCAL layers
- todo:
  - LDA integration
  - switch to data transfer via HDMI
- compatible with CALICE DAQ, can be used by other detectors



AHCAL Stack Integration: Infrastructure

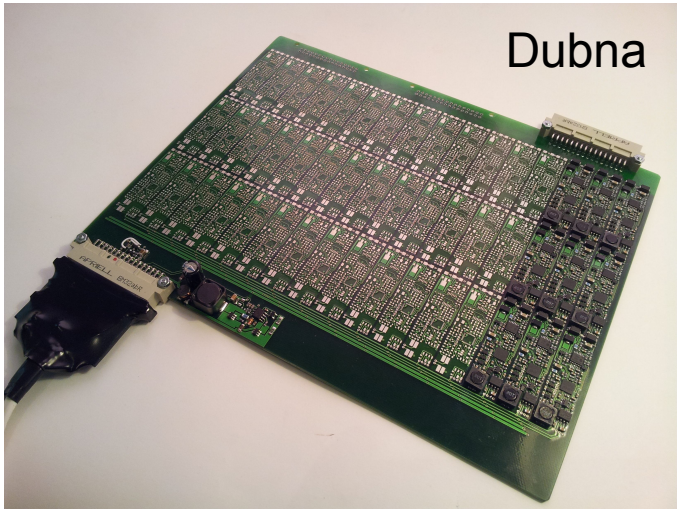
Power supply and distribution

- dedicated, low-cost system, scalable to ILD size, is being developed at Dubna
- ordered short-term solution for testbeams: commercial system usable for up to 16 layers
  - easily upgradable to 48 layers
- started design of power distribution box

Cooling

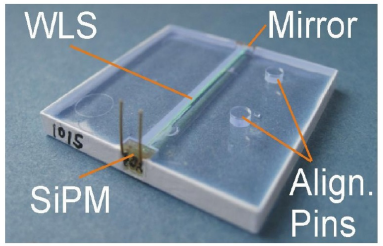
- started design of cooling system fitting into the barrel-endcap gap of ILD

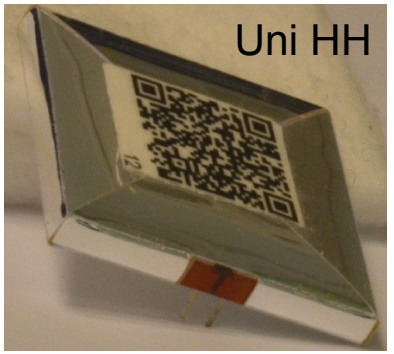
power supply

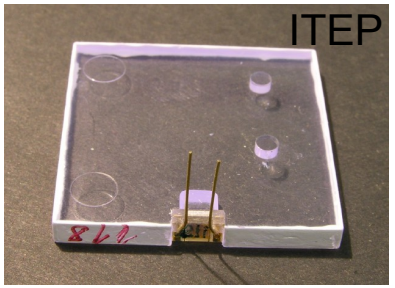


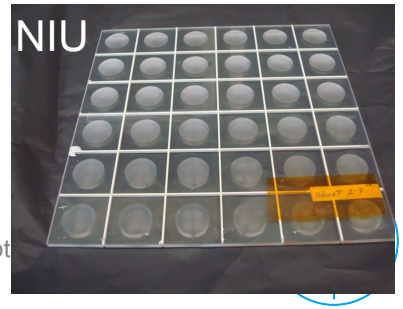
Going mass production: more tiles+SiPMs

- **4 HBUs** fully equipped with tiles+SiPMs + **1 HBU** partly equipped exist and have been used in testbeams already
- for **8 HBUs**, Uni HH produced direct-readout tiles + next generation SiPMs, are being tested now, HBU PCBs exist
- for 2 HBU ITEP direct-readout tiles+SiPMs
- 1 HBU with surface-mount megatile+MPPCs being tested at NIU
- for 4 HBUs, expect Hamamatsu MPPCs from Japan, ITEP agreed to produce direct-readout tiles
- testing several different options now, but for practical reasons will need to converge to 1 or 2 for larger prototypes



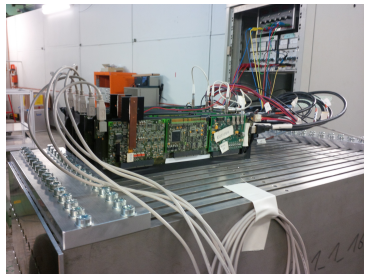


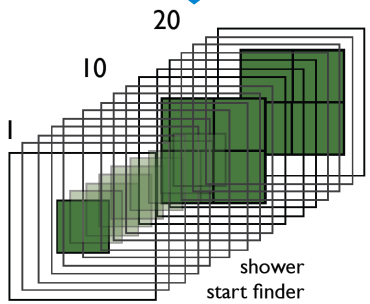


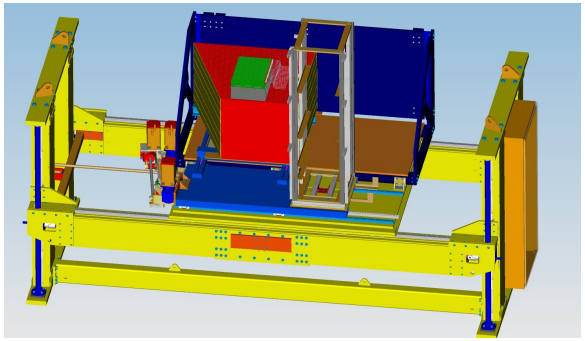


AHCAL Schedule

- 2013/2014:
  production, calibration and test of new hardware
- beginning of 2014:
  measurements of EM showers in the small ILD-like stack (11±2 layers)
  - commissioning of full multi-layer DAQ
- 2014/2015:
  first measurements of hadrons with a “shower start finder” and a few 2*2 HBU layers
  - EUDET stack: sector integration of cabling & cooling in ILD geometry
  - first test of the full system
- longer term: fully equipped 1m^3
  - step into larger scale production and quality assurance

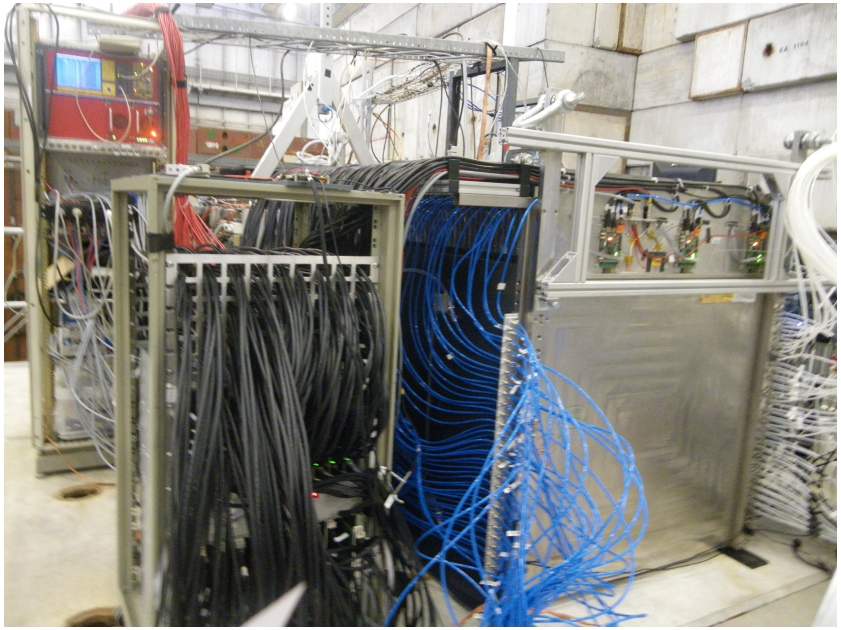




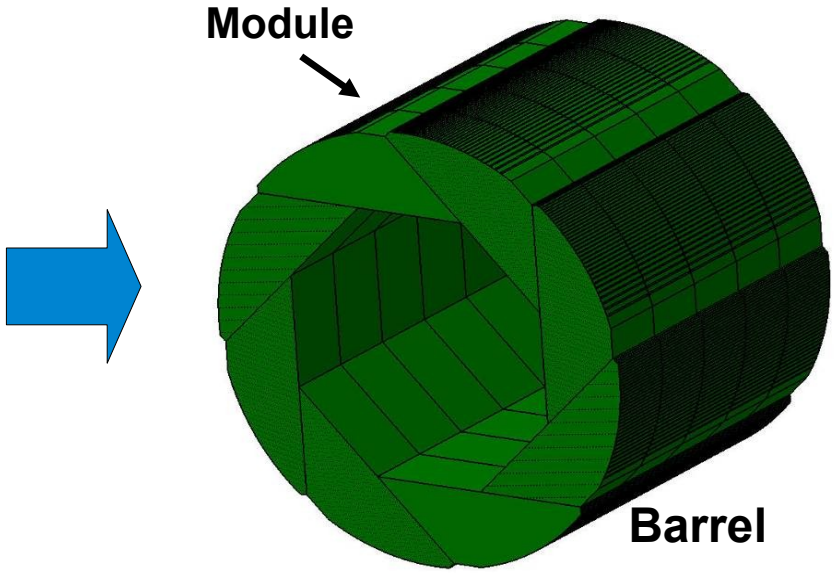


SDHCAL Status

- $1m^3$ prototype with 48 GRPC layers realised as technological demonstrator:
  - electronics integrated in active layers
  - power-pulsed
  - data analysis ongoing, first results very satisfactory
  - tests of several Micromegas layers

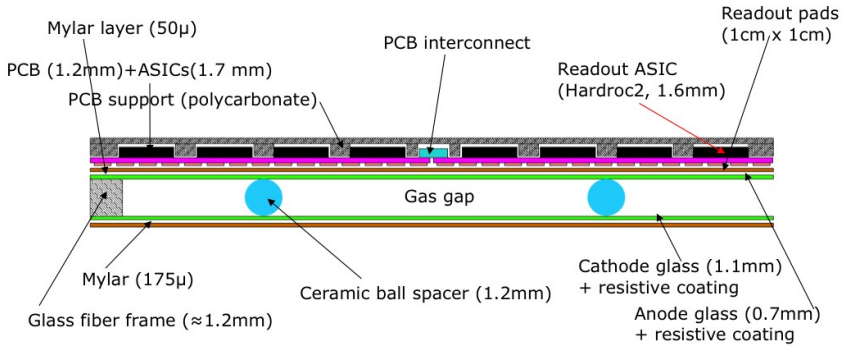


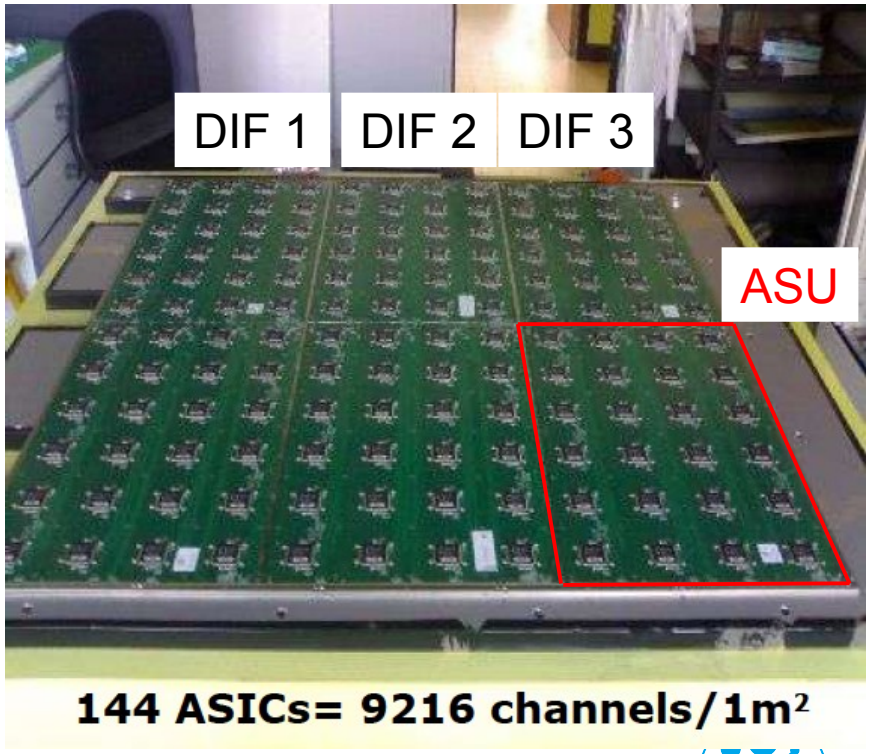
- needed to demonstrate scalability to full ILD layout:
  - large GRPC detectors
  - mechanical structure for Videau geometry
  - optimised PFA



SDHCAL: Current Layer Layout and Plans

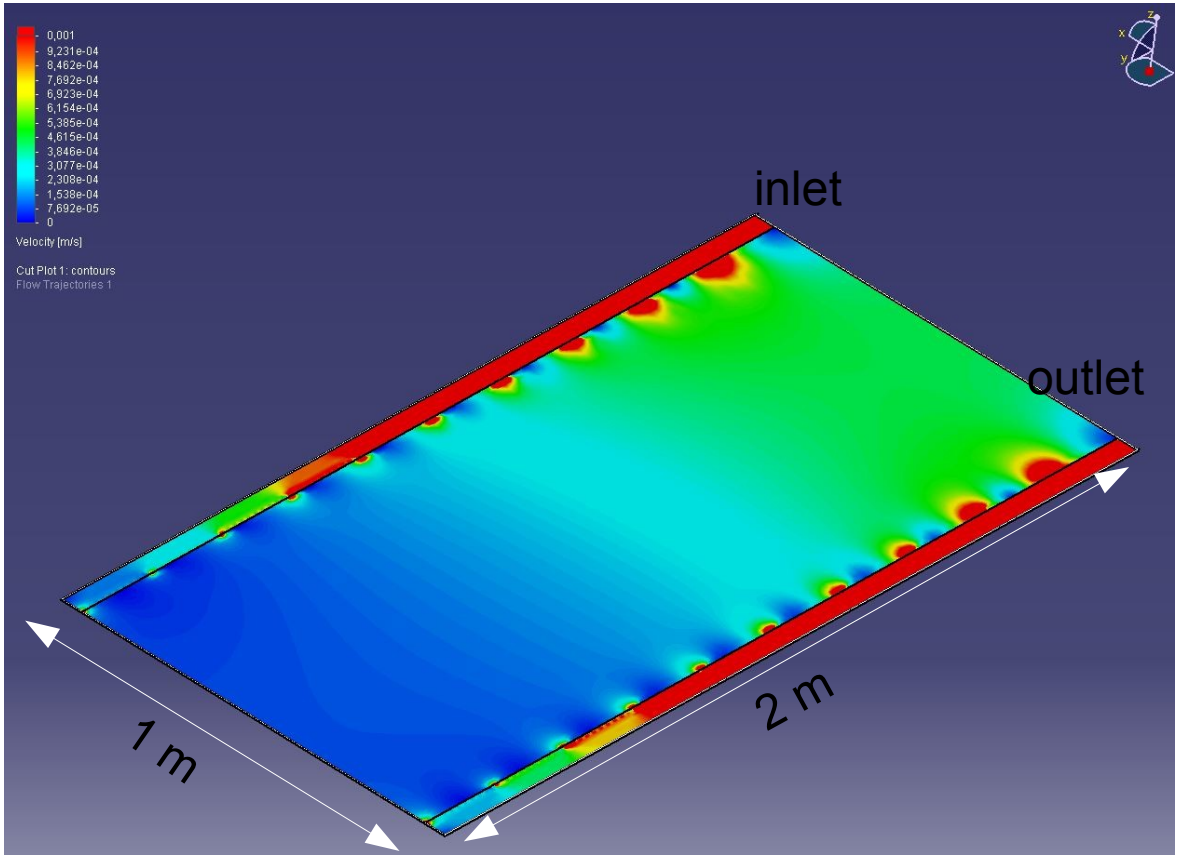
- have demonstrated layers with integrated electronics of 1 m^2
- next steps:
  - build few very large GRPC detectors (2-3 m^2): gas circulation system, thickness…
  - improve on the readout electronics (3rd generation ASICs)
  - design a new ASU capable to read the large GRPC
  - develop a new DIF (low power consumption, reduced size, new functionalities)
  - build a small mechanical prototype to host the few large chambers





SDHCAL: Large GRPC for ILD

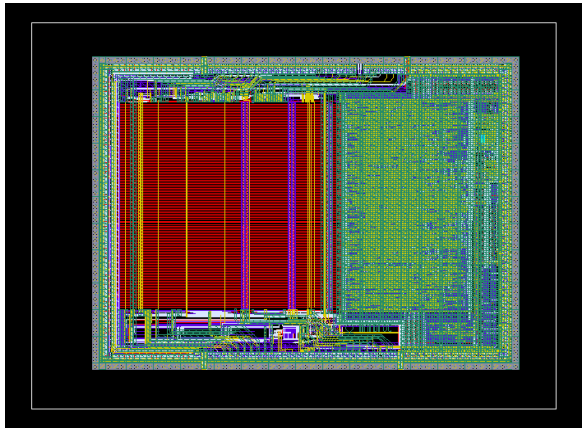
- for ILD, GRPC with a surface of up to 3 m^2 are needed
- intend to build a 2 m^2 GRPC (glass are already there)
- currently studying the gas distribution system to ensure a good gas renewal
  - scaling from 1 m^2 to larger surface needs more study to ensure fast gas renewal



SDHCAL Readout Electronics: 3rd Gen. ASIC HARDROC3

2nd generation ROC ASICs:

- auto-trigger, power pulsing

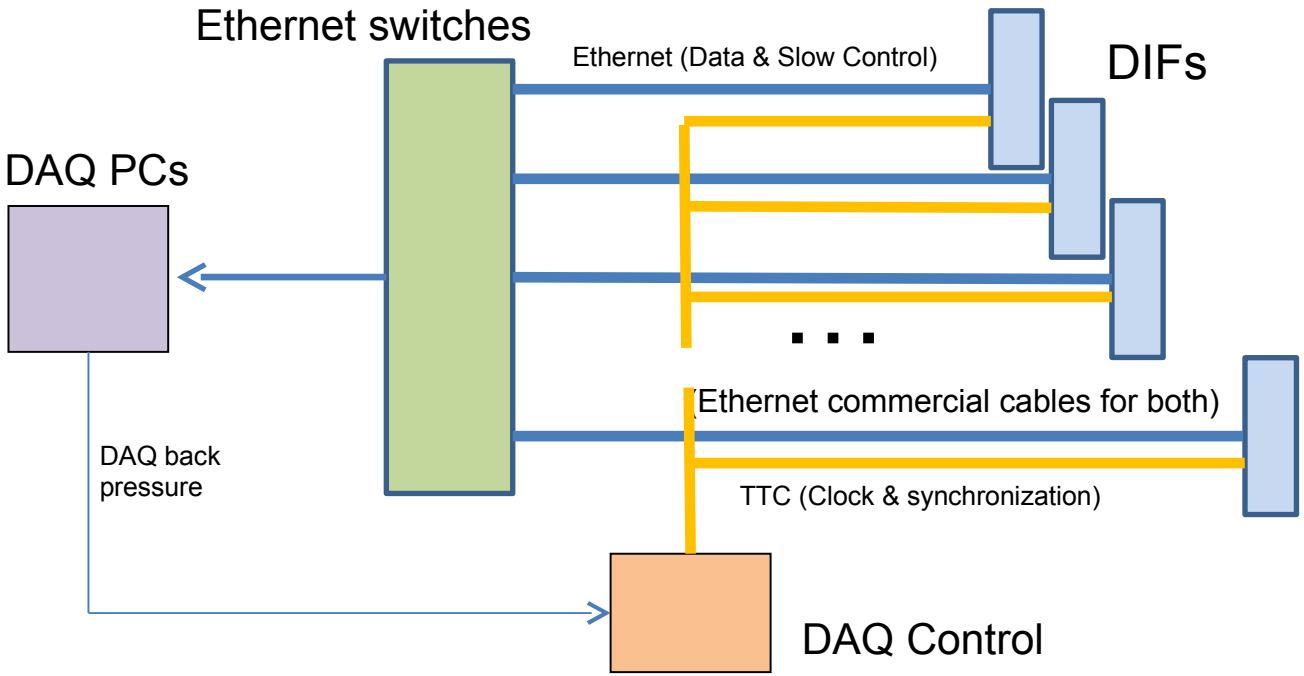


3rd generation ROC ASICs:

- independent channels (= zero suppression)
- digital part much more complicated
- new slow control (triple voting) using I2C link
- new PLL:
  - input frequency 2.5 MHz → output frequency: 10, 20, 40, and 80 MHz
  - need to distribute only slow clock to ASUs
- HARDROC3 is the demonstrator for all 3rd gen. ROC chips (SKIROC, SPIROC, …), same digital part for all
- HARDROC3 received in June 2013
- test board is designed and being produced
- tests to start soon

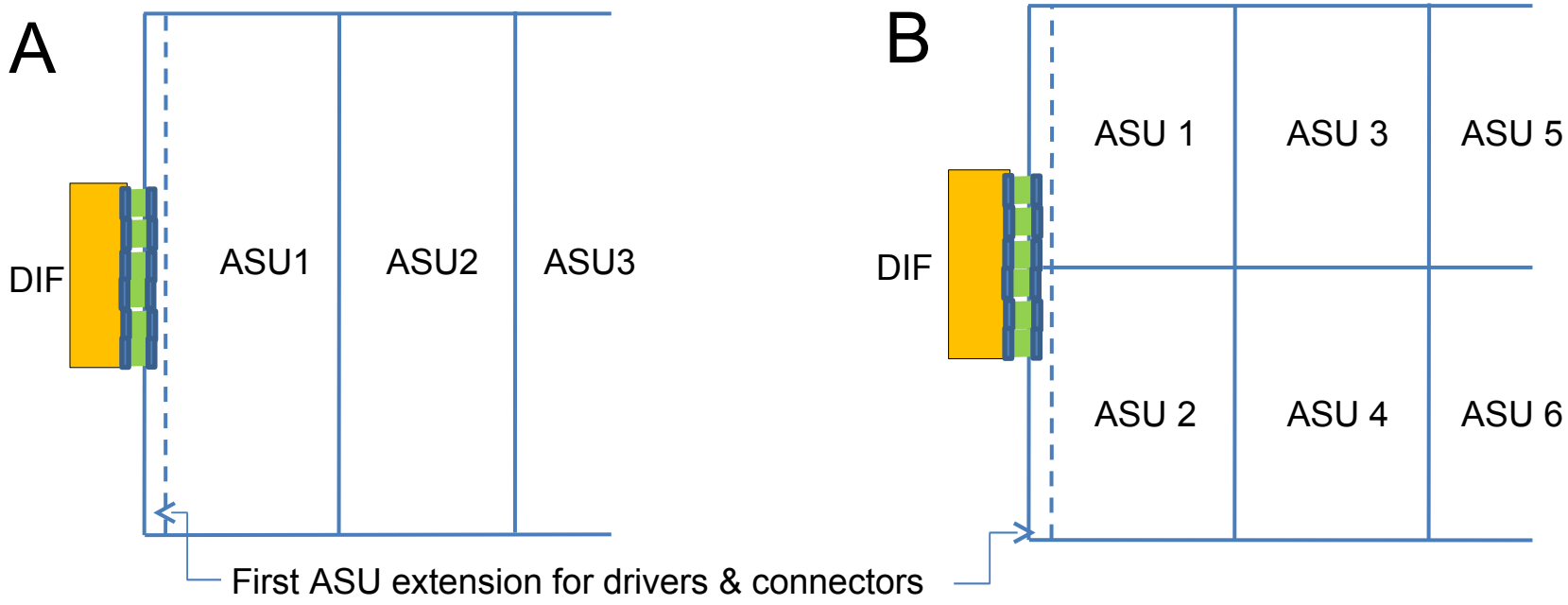
New SDHCAL DAQ architecture

- only one DIF per plane (up to 432 HARDROC3 chips)
- slow control through the new I2C bus
- data transmission to DAQ by Ethernet using commercial switches
- clock and synchronization by TTC
- USB 2.0 for debugging



SDHCAL: New ASU Layout Options

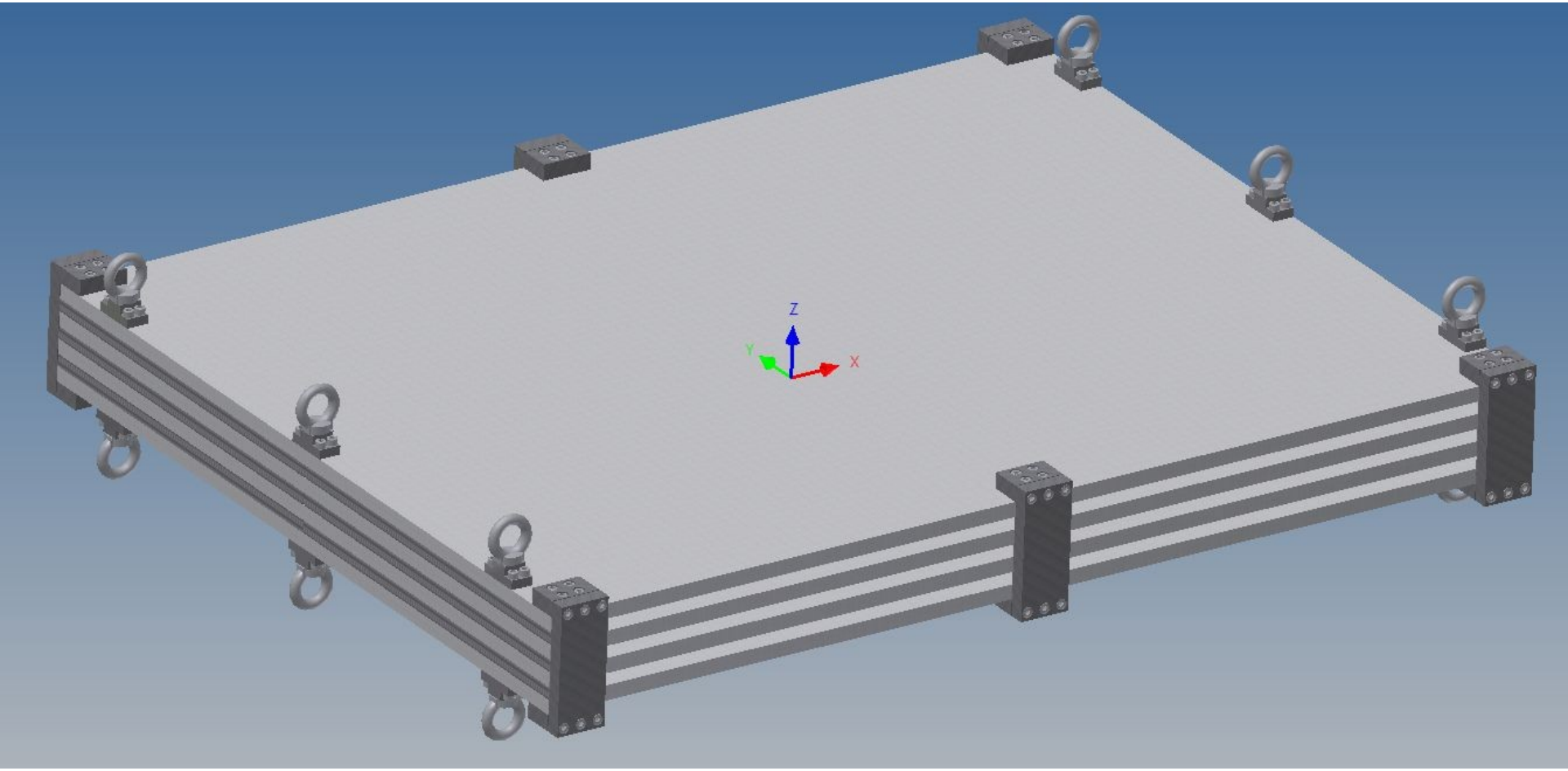
only one DIF per plane → rearrange ASU boards in the plane to reduce the number of connections between the DIF and the plane



- option A: looks more risky because of 1m long ASU boards
- option B: need to send common signals twice (one per slab)
- both options: first ASUs will have extension to host the connectors and the buffers for driving the long lines

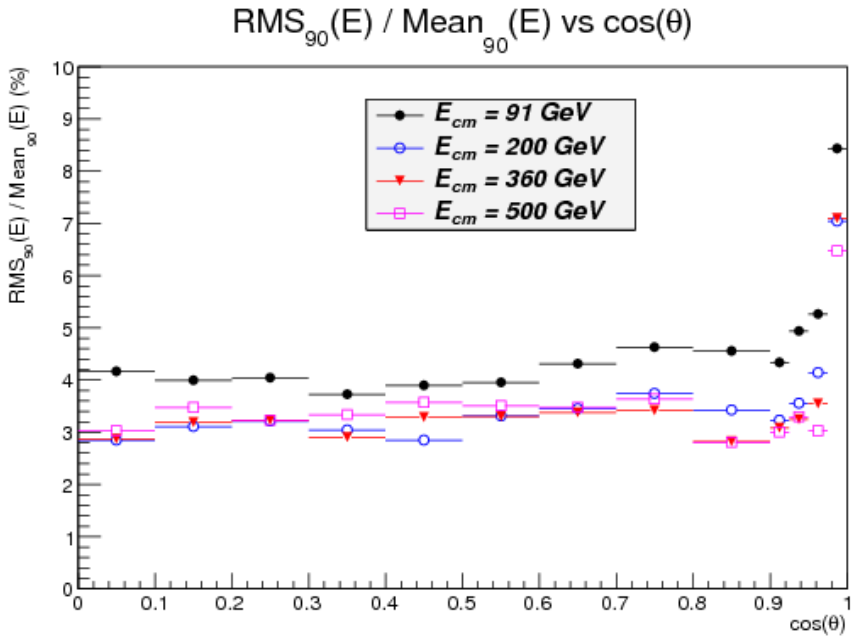
SDHCAL: Large Self-supporting Mechanical Structure

> design of large self-supporting structure for 3 layers



SDHCAL: Optimisation of Particle Flow

reasonable jet reconstruction
with non-optimized Pandora PFA



- energy reconstruction:
  - $E_{old} = \alpha N_1 + \beta N_2 + \gamma N_3$
  - $E_{new} = \alpha(N_{shower})N_1 + \beta(N_{shower})N_2 + \gamma(N_{shower})N_3$
- Neural Network
  - use the hadronic shower shape
- SDHCAL radius:
  - collaborate with ECAL people
- cell size (?), more bits (3?)

Conclusions

AHCAL

- successful operation of physics prototype, validation of simulation and PFA
- successful tests of one layer with integrated electronics
- for ILD-ready detector, working on:
  - multi-layer DAQ
  - beam tests with small EM stack and large EUDET stack (1/3 of ILD barrel sector)
  - integration of infrastructure (cooling, cabling) into sector stack
  - larger scale production & quality assurance

SDHCAL

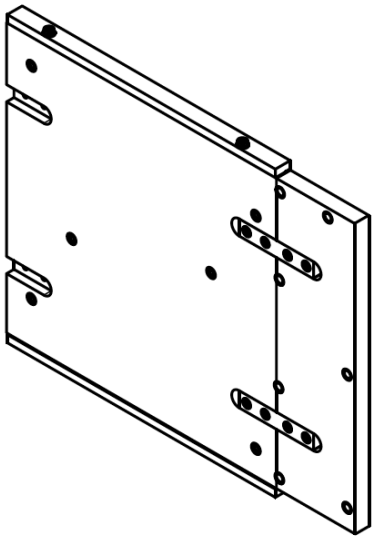
- successful operation of prototype with integrated electronics & power pulsing
- for ILD-ready detector, working on:
  - development of large GRPCs
  - tests of 3rd generation readout chips & corresponding changes in DAQ and electronics
  - mechanics for large chambers
  - optimisation of PFA

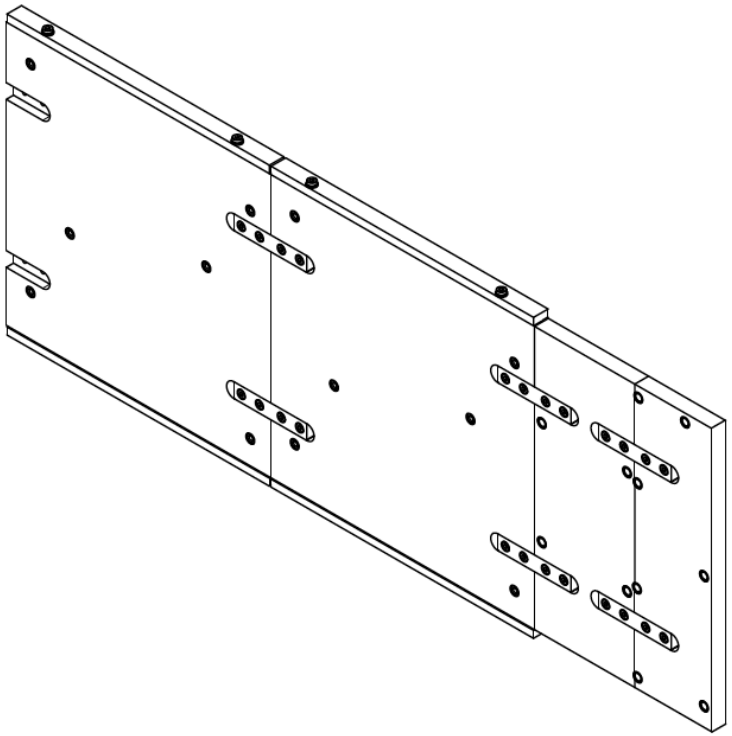
Many thanks to all AHCAL and SDHCAL colleagues providing material and feedback, especially Felix and Imad!

Backup

Mechanics: Tool for Quality Control of Cassettes and HBUs

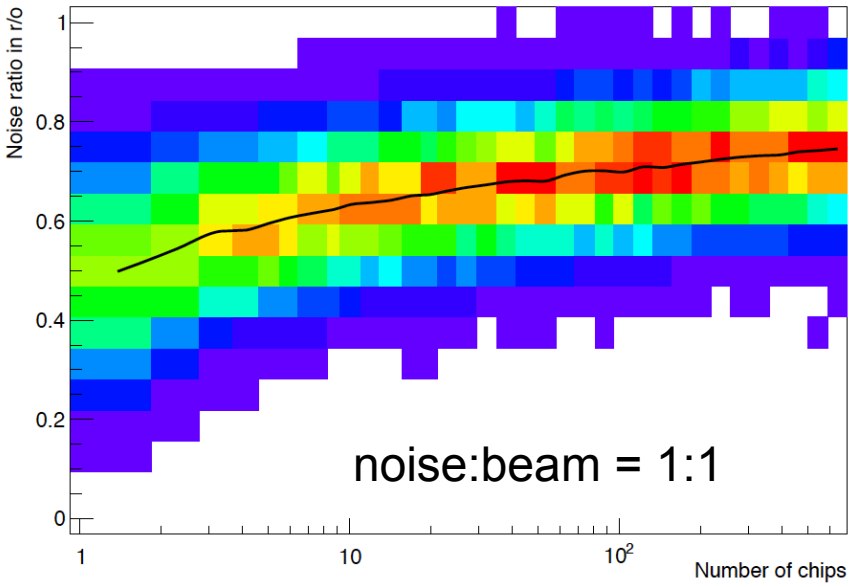
- modular tool to check dimensions
  - of cassettes and their pins
  - of HBUs and their holes
  - of additional boards: CIBs, SIBs, extenders
- parts designed and ordered





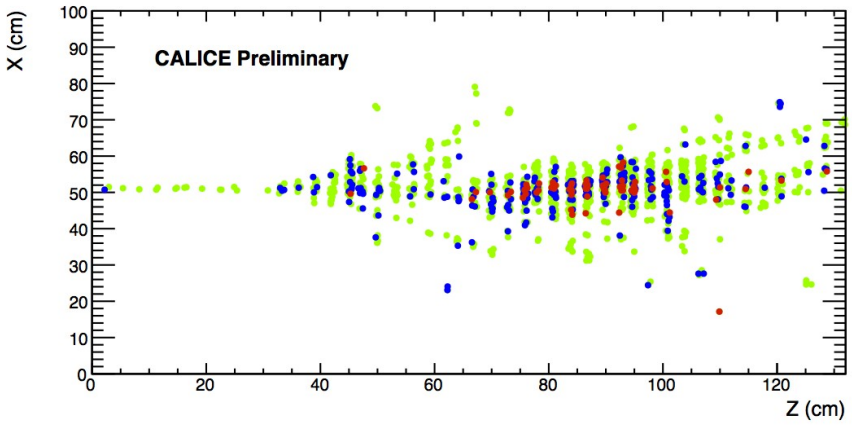
Other ASICs needed? (SPIROC2d or SPIROC3)

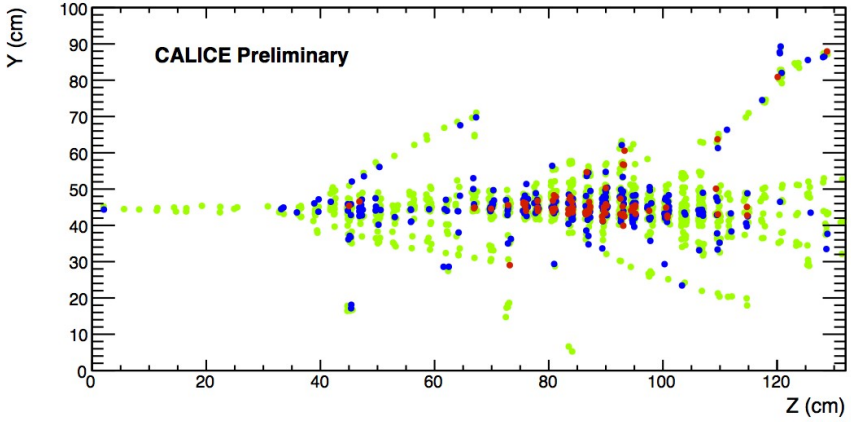
- started to look into rate dependency of fraction of noise events
  - for now focus on sequence
    - EM stack (<60 chips)
    - HCAL with shower start finder (~100 chips)
    - 1m^3 HCAL (600 chips)
  - plan to check simulation also for ILD calo
- fraction of useful events is OK with SPIROC2b for EM stack and HCAL with shower start finder



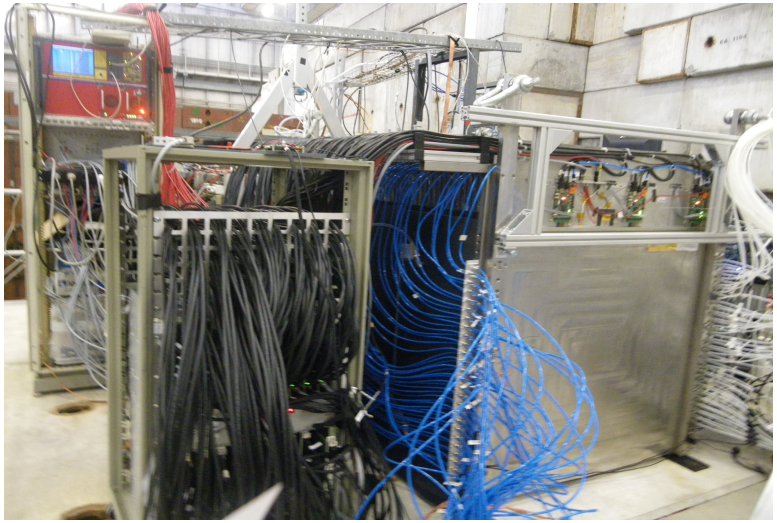
- data taking possible, but with non-optimal efficiency for 1m^3 HCAL with current SiPM noise rates, possible solutions:
  - close the validation gap
  - zero suppression (only the triggered channel read out, not all 36 channels on a chip)

Semi-Digital HCAL



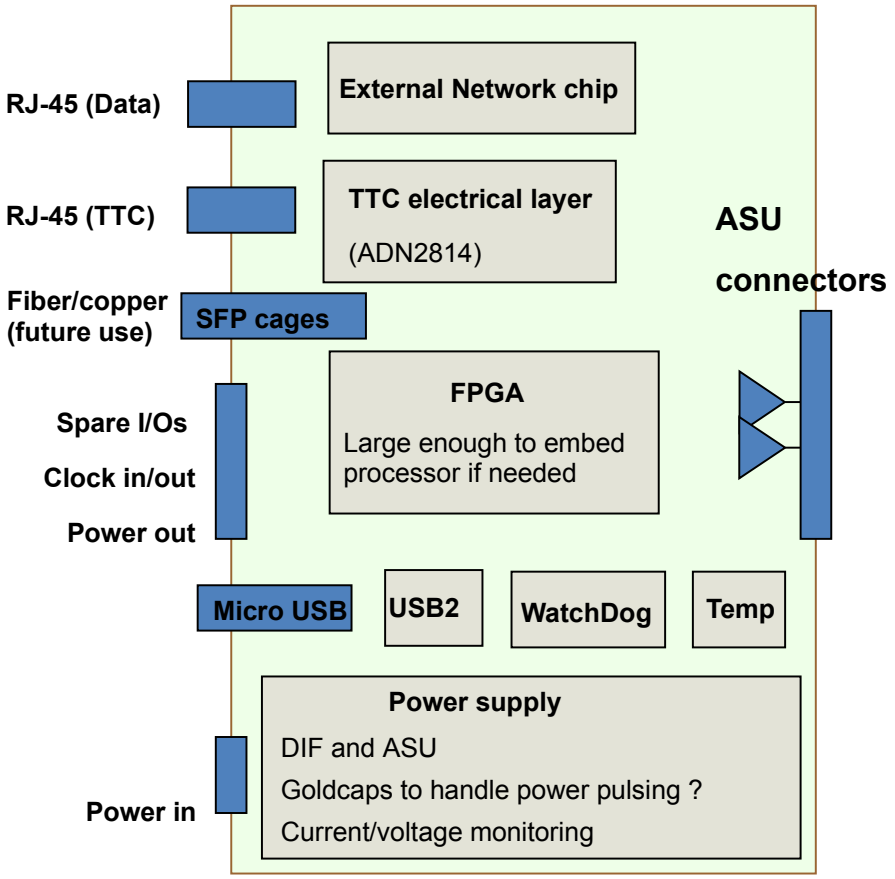


- Glass Resistive Plate Chambers
- 1*1 cm^2 pads
- read-out: 2 bit (semi-digital)

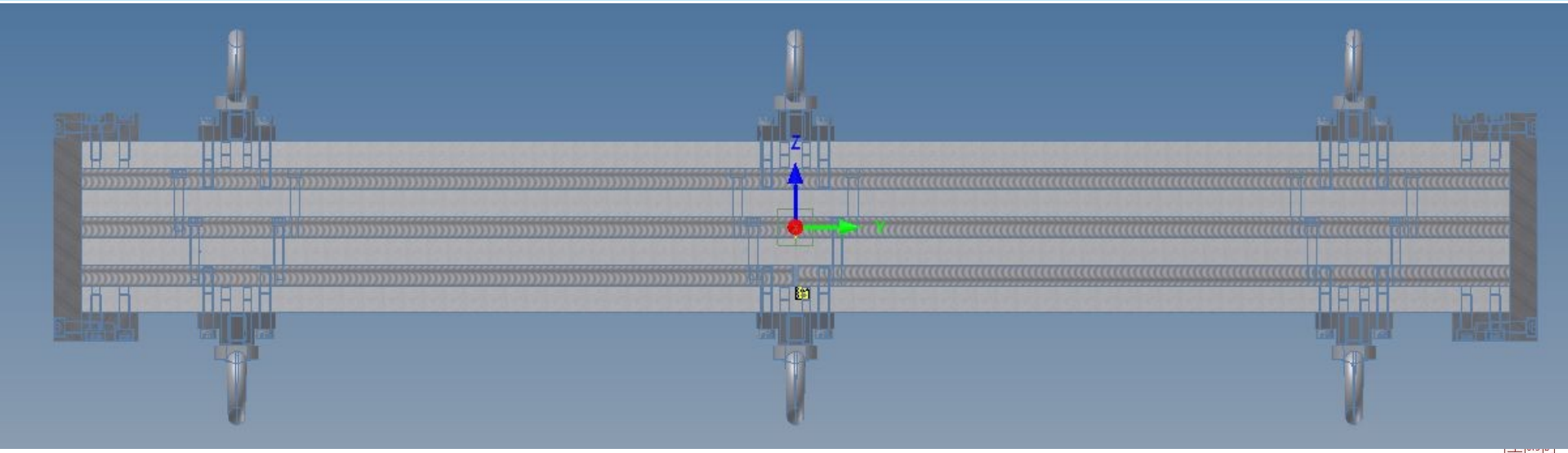


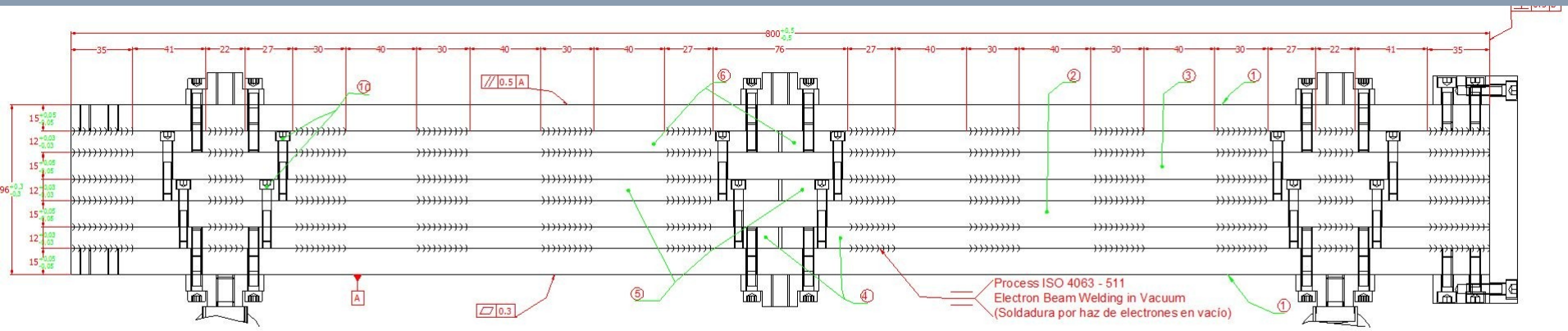
DIF: Designed for ILD SDHCAL

- Only one DIF per plane. For the maximun lenght plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmision to DAQ by Ethernet using comercial switches for concentration
- Clock and syncronization by TTC
- USB 2.0 for debugging



Self-supporting Mechanical Structure

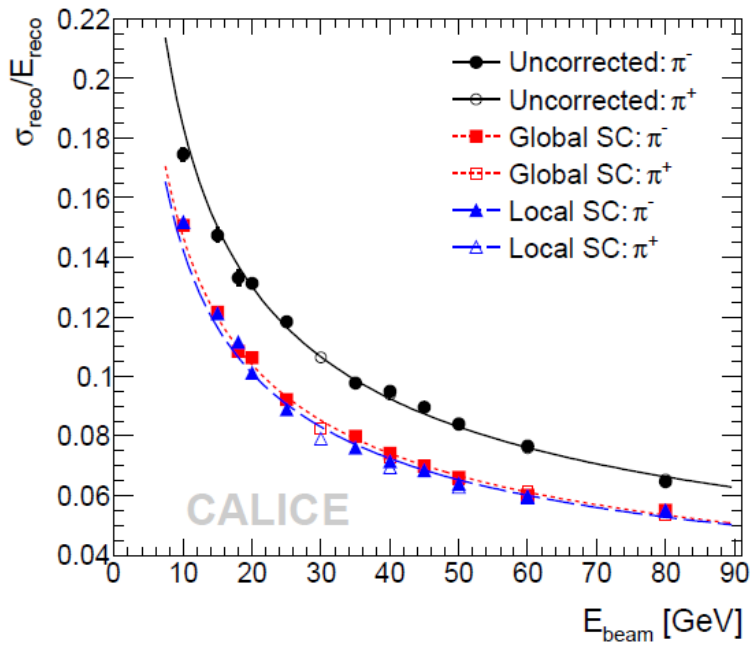




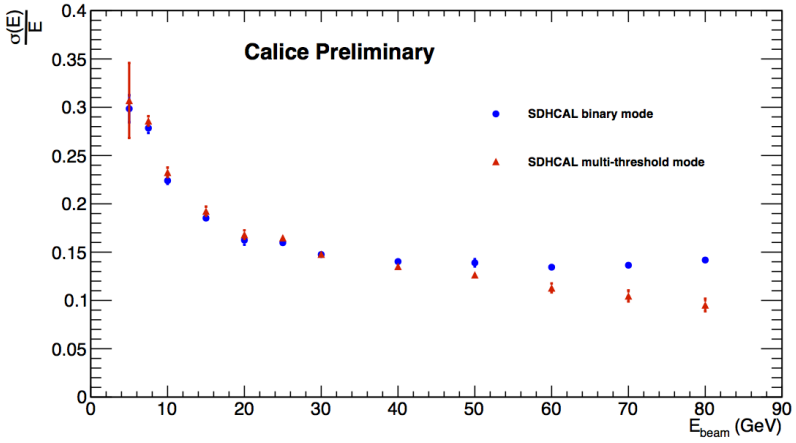
Made by Electron Beam Welding proccess in Vacuum.
Welding deep of 5 mm.

Energy Resolution for Hadrons

AHCAL



SDHCAL



Software Compensation improves stochastic term:
58%/√E → 45%/√E

Resolution with **1** or **3** thresholds

3 thresholds improve resolution at large energies