
# ECAL R&D

24.9.2013

ILD Meeting in Krakow

Yuji Sudo (Kyushu University)

# Outline

- Power pulsing
- ROC (ASIC) chips

- Si ECAL

- test beam
- development of daq electronics
- Si sensor study

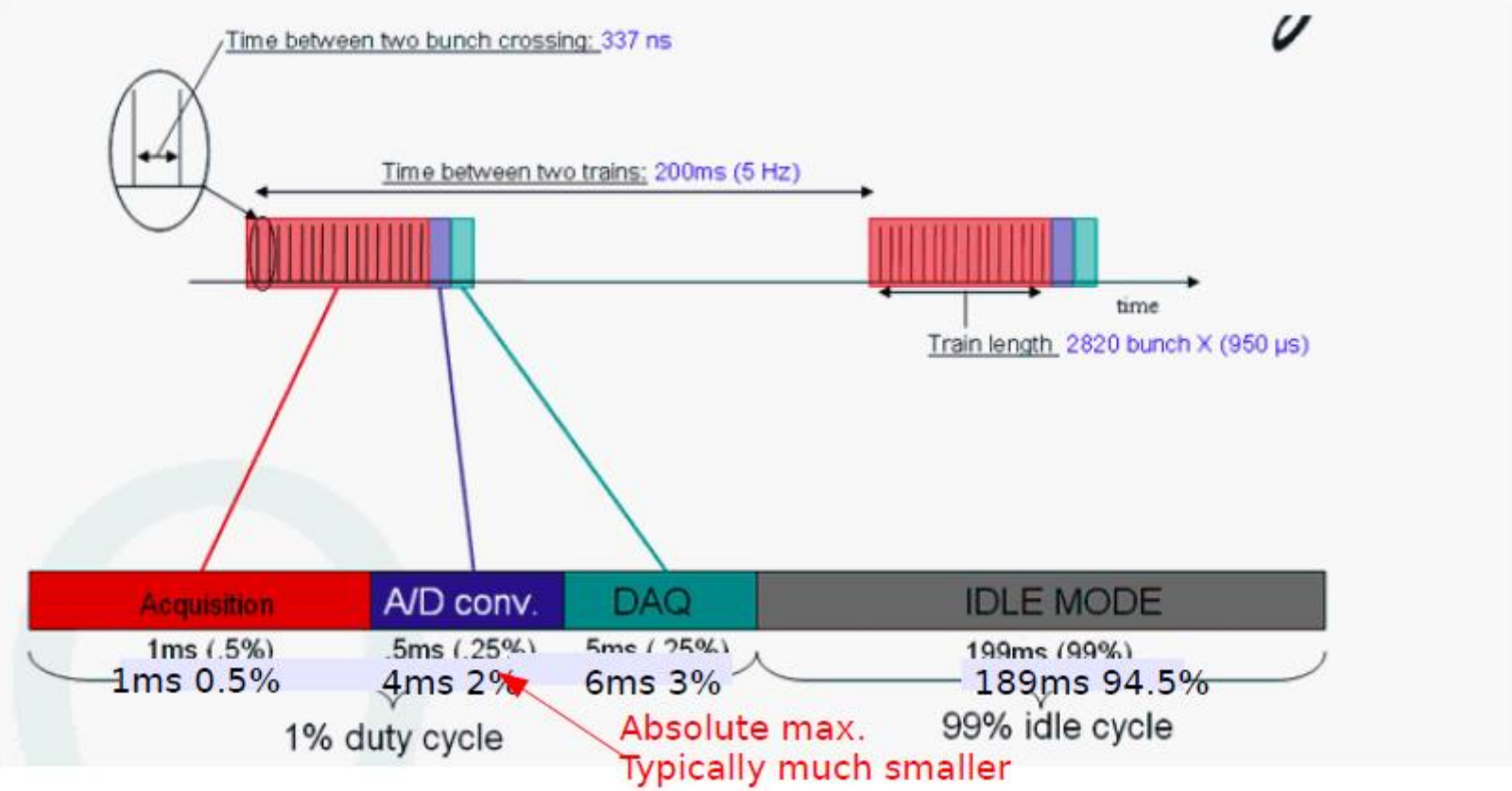
- Sc ECAL

- test beam
- MPPC (PPD) study
- scintillator design

- Hybrid ECAL

- optimization with simulation

# Power Pulsing




- Electronics switched on during > 1ms of ILC bunch train and immediate data acquisition
- **Bias currents** shut down between bunch trains
- Mastering of technology is essential for operation of ILC detectors

  Measurements for SKIROC ship 1.7 mW ⇔ 27 µW/ch

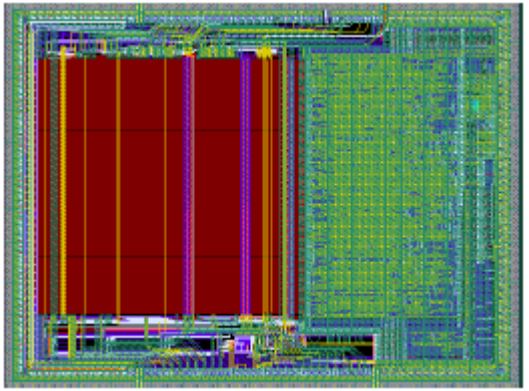
# ROC Chips

- 2nd generation ROC chips
  - Auto-trigger, analog storage, digitization and token-ring readout, common DAQ
  - Power pulsing : <1 % duty cycle

It is useable for test , but it is not demonstrated to be scalable to final project

- 3rd generation ROC chips
  - **Independent channels (= Zero suppress)**
    - 64/36 address pointers
    - ReadOut, BCID, SCA (Spiroc and Skiroc) management

    **=> Digital part much more complicated**
    - SCA depth: 8 instead of 16
    - New TDC with no dead time



**- HARDROC3** ( AHCAL, ScECAL, SDHCAL)
= AIDA Milestone

After HARDROC3 → other ROC3 chips

# Si ECAL

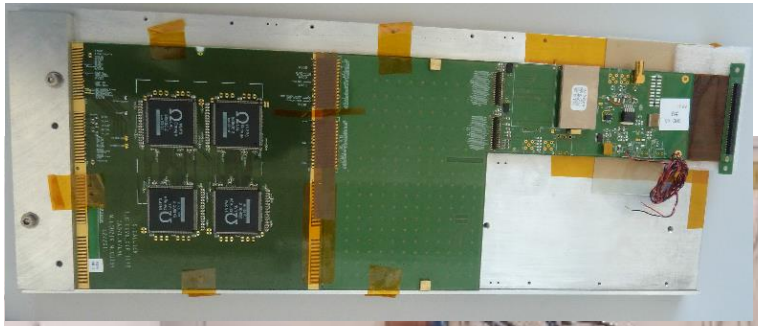
# Si ECAL Technological Prototype

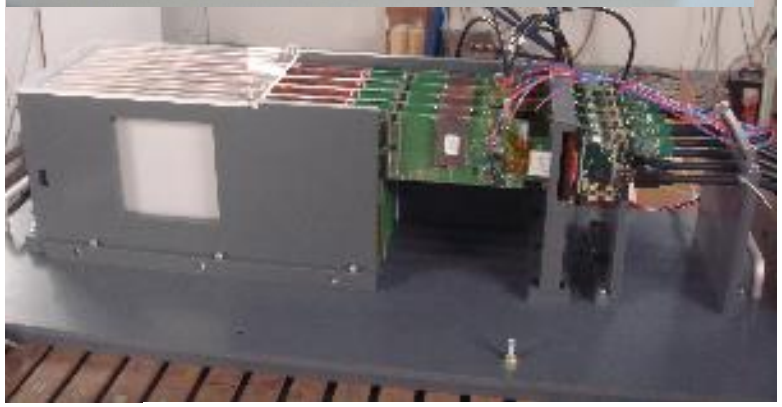
- Integrated front end electronics
- Small power consumption (PP)

FEV8

SKIROC2 64ch/chip, 4 chips/slab

1 Si Sensor/slab



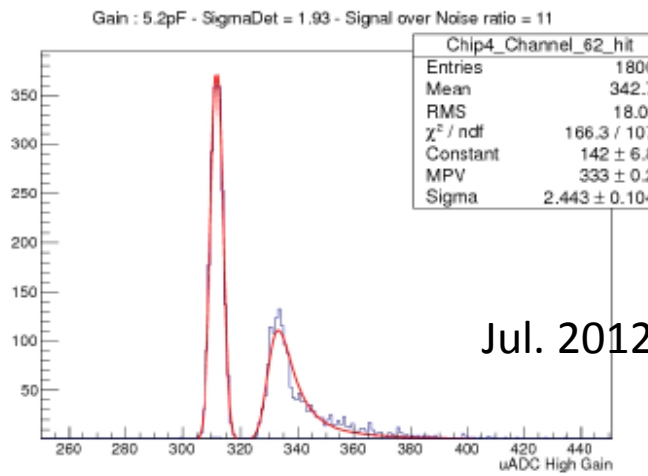


Test beam in

2012 Jul. : 6 slabs, noPP operation

- Nice MIP signal, good separation
- S/N ~ 10

S/N = (MPV - pedestal)/(RMS of pedestal)




Jul. 2012

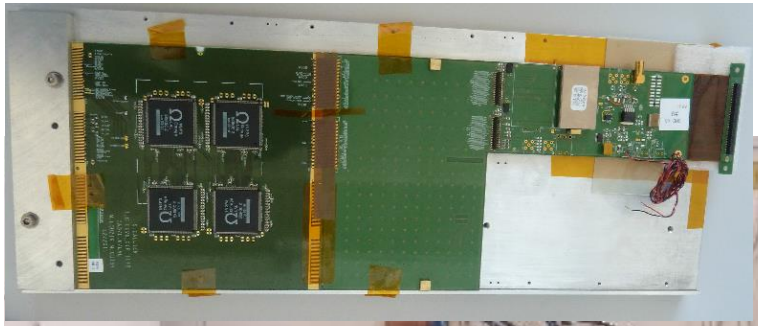
2013 Feb.: 7(8) slabs, successfully operat

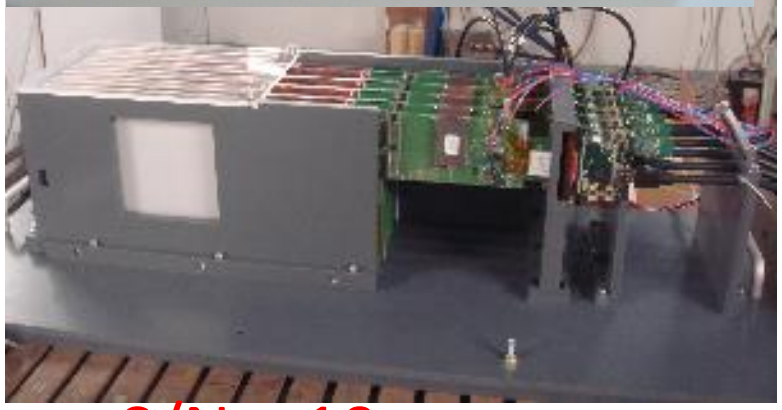
issues of SKIROC instability w

1 slab, tested inter connectio

# Si ECAL Technological Prototype

- Integrated front end electronics
- Small power consumption (PP)





FEV8
SKIROC2 64ch/chip, 4 chips/slab
1 Si Sensor/slab

Test beam in
2012 Jul. : 6 slabs, noPP operation
- Nice MIP signal and good separation : S/N ~ 10

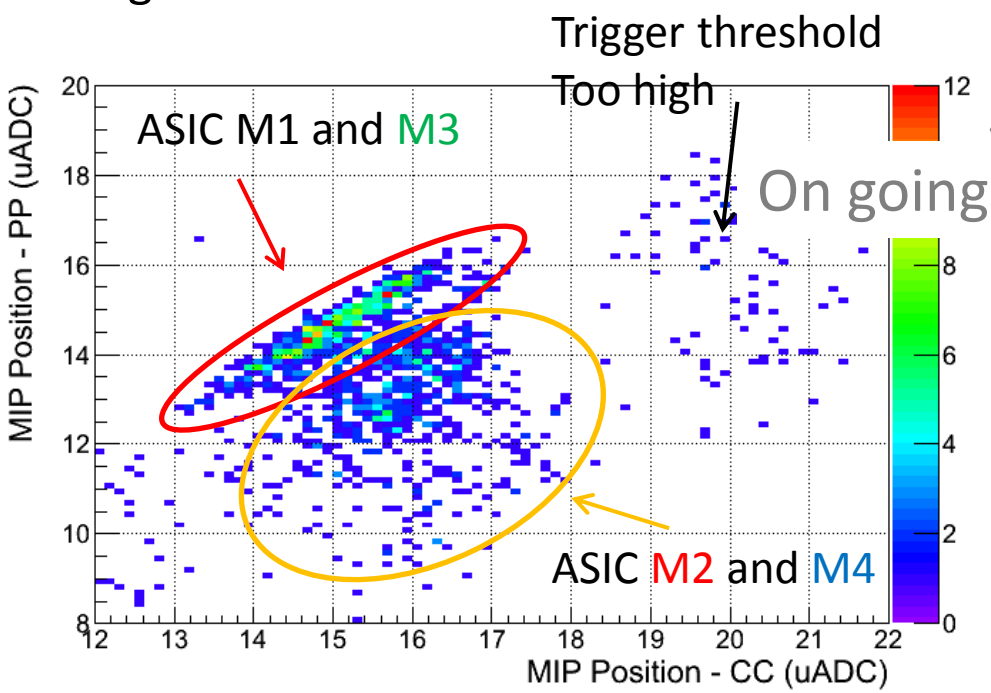
2013 Feb.: 7(8) slabs, successfully operated in PP mode,
issues of SKIROC instability was found in CC & PP.
1 slab, tested inter connection in B field

2013 Jul. : 6(7) slabs, tested with new data aggregator (GDCC)

# Comparison CC/PP – Energy calibration

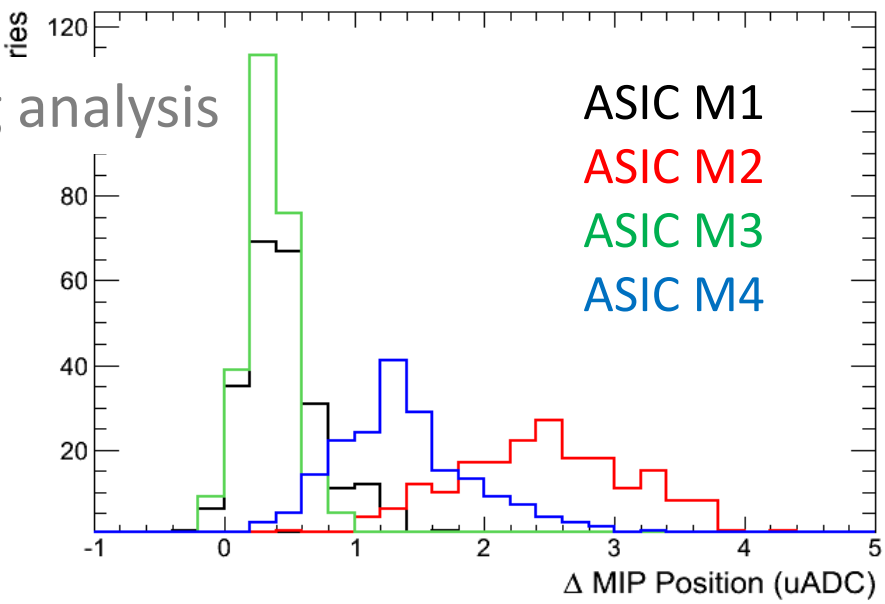
Fit energy distribution: Landau convoluted with a Gaussian

Sigma of the Gaussian is fixed to the noise




Jul. 2013

On going analysis




- MIP position shift of M1 and M3 due to pedestal shift.

One of the reasons for large ΔMIP between CC & PP of M2 and M4 is

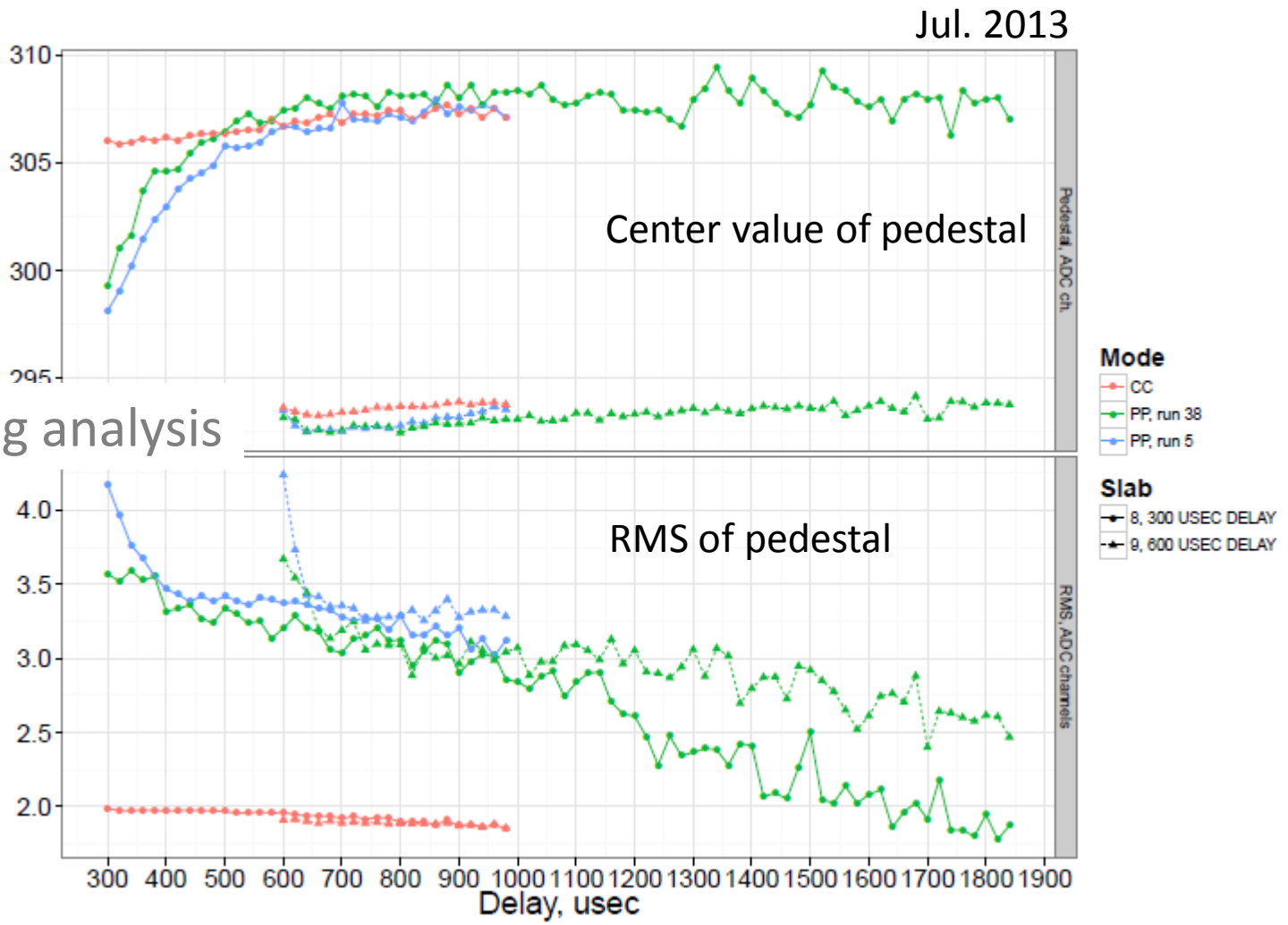
- digital lines are very close to ASIC2 M2 and M4.

→The activity of digital lines disrupts ASICs M2 and M4.

We are still working on this issue.

# Stability of SKIROC in PP Operation

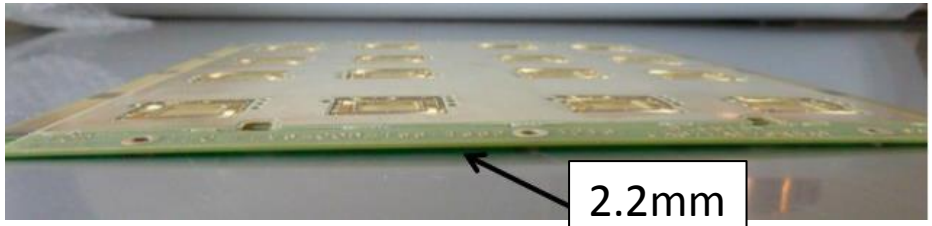
- After spill start, center value of pedestal drifts during ~500 μs
- RMS approaches CC value in > 2 ms.




On going analysis

# FEV R&D

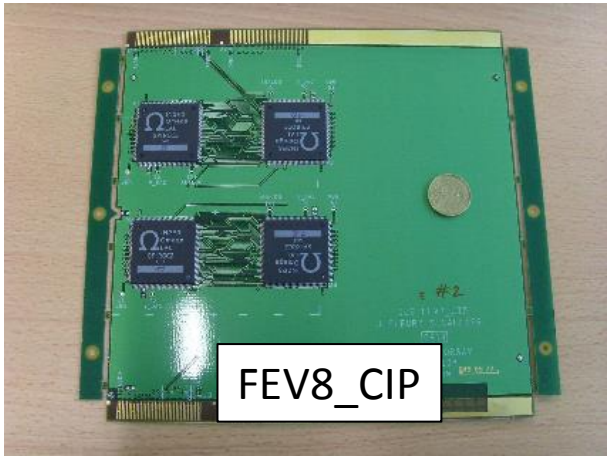
- FEV_COB (Chip On Board): in the DBD, 1.2 mm thick




FEV8_COB – first COB type
~1.3 mm thick, bad flatness
FEV8_COB has been testing

- COB has mechanical tolerance problem …

- FEV_CIP (Chip In Package): thicker than COB, good flatness
- Allows us to realize a number of very useful tests
- We used FEV_CIP for test beam




- FEV8 → FEV9
- Good planarity COB is produced by EOS (Korean company)

- FEV7_COB - Test production at EOS company

~1.2 mm PCB with good flatness

- We will pick up contact this autumn

to arrange FEV8_COB production

# Long slab setup « 10 ASU »

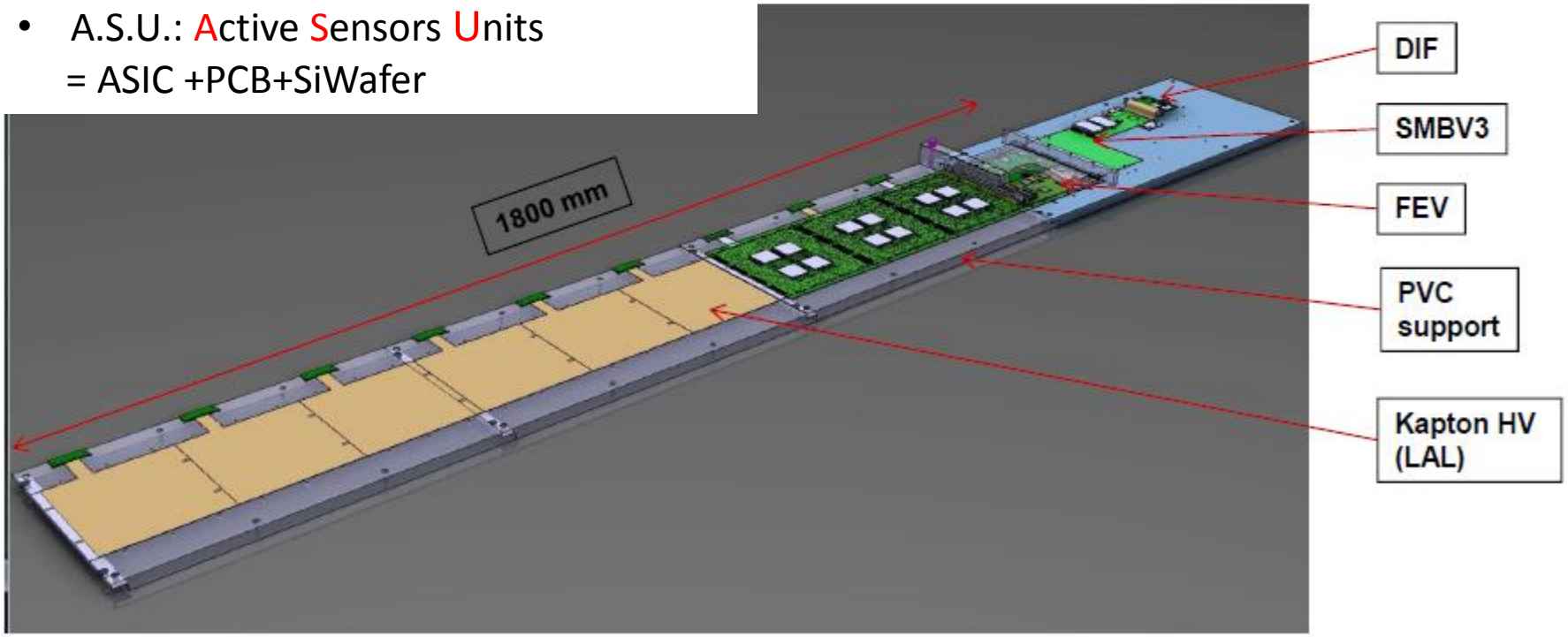
⇨ **The goal:**

1.0 – inter-connection of 10 FEV

- Realize a test bench to verify inter-connections and data taking on 10 ASU
- Keep a possibility to easily disassemble it in order to move to a test beam

A layer is composed of several short ASUs

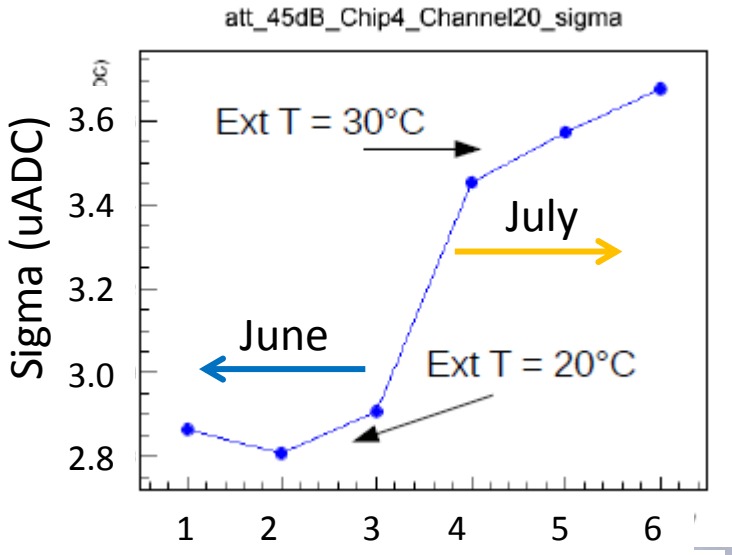
- A.S.U.: Active Sensors Units
  = ASIC +PCB+SiWafer

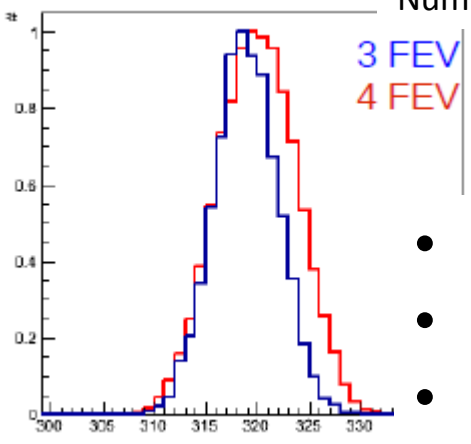


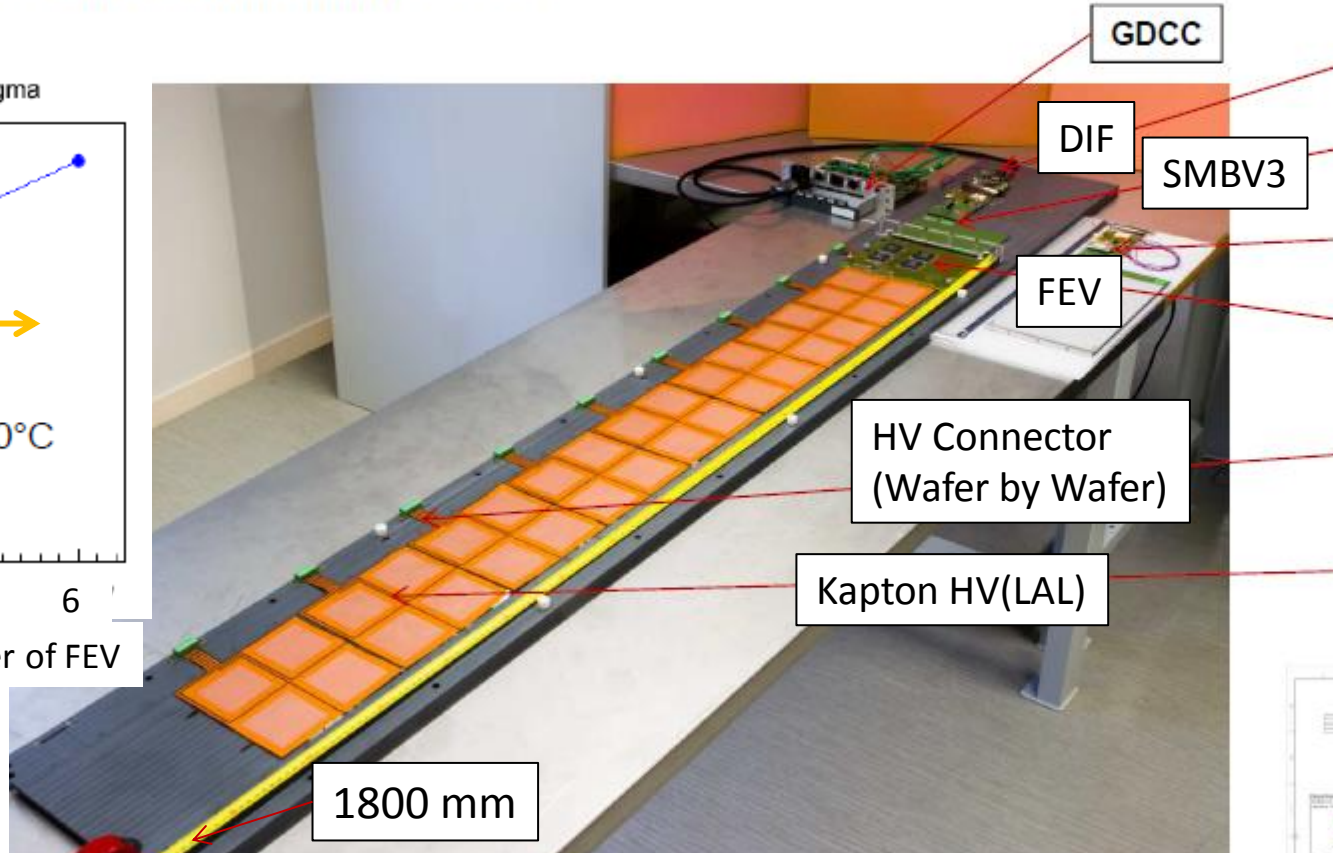
# Long slab setup « 10 ASU »

⇨ **Our realization:**

*1.1 – inter-connection of 10 FEV*



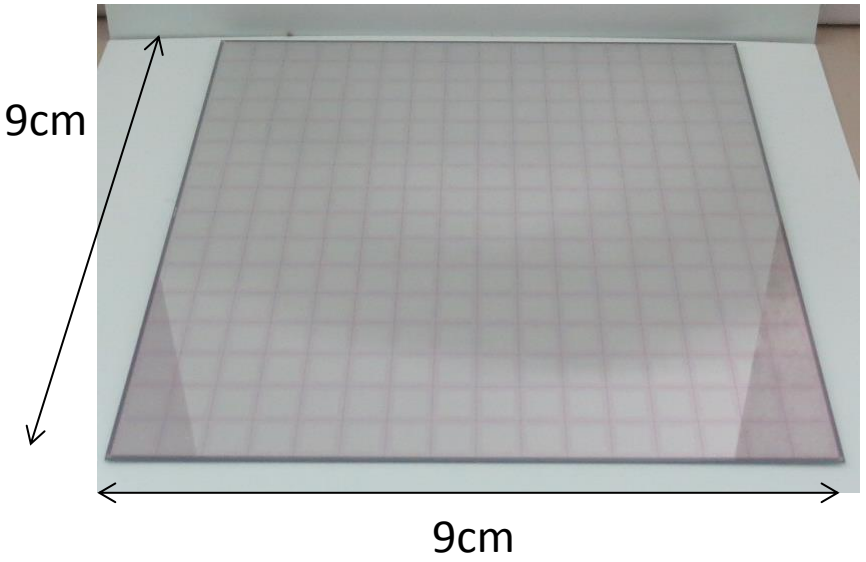



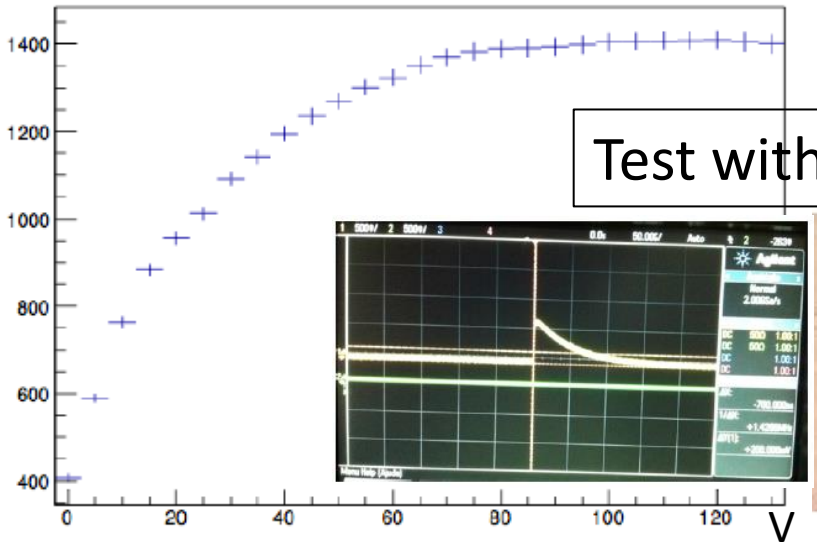




- RMS of injected signal is increased 0.1 (uADC)/FEV
- Temperature has bigger effect on RMS than # of FEV
- We are working on Long slab study

# Si Sensor Test

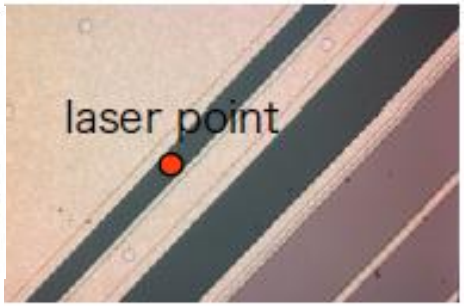
- Produced by Hamamatsu Photonics K.K
- 16x16 = 256 pixels in total
- Pixel size : 5.5x5.5mm$^2$
- Thickness : 320 μm

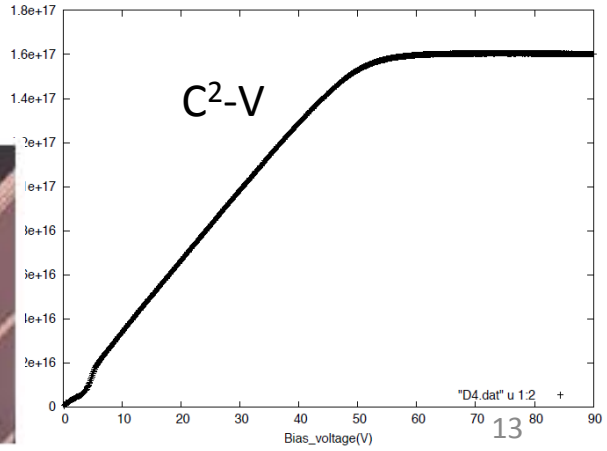



Test with IR laser





# Next Si Sensor from HPK

We will receive new sensors in the next month

No guard ring

Full depletion voltage: min 20 V , Max 120 V

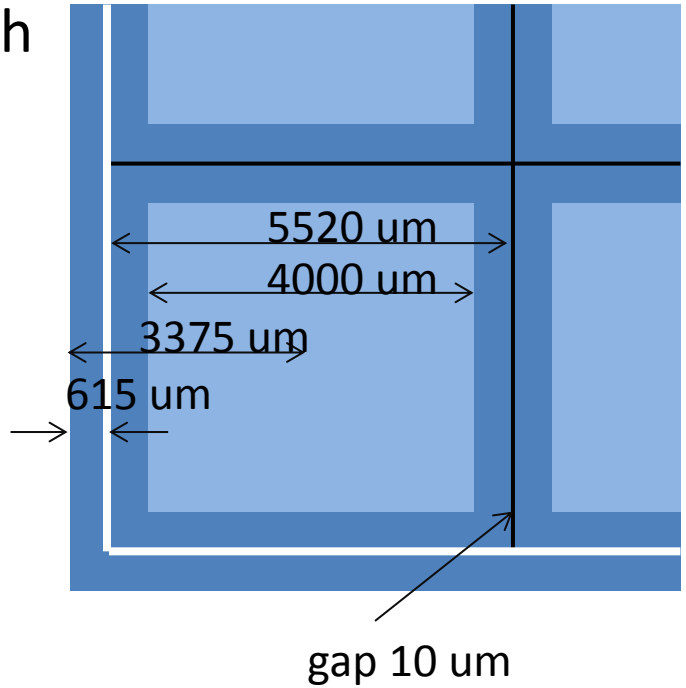
Device type : $P^+$ pixel on N substrate

89.7 x 89.7 mm

Thickness 320+-15 um

# of pixels 256

Pixel size : 5520 um




# Price Estimation by HPK

If we order 300k – 400k pieces,

- 31000 Yen/sensor ~ 240 Euro/sensor
- ~ 3 Euro/$cm^2$ (1Euro = 132.38 Yen 20.09.2013)
  ~ 4 \$/$cm^2$

# ScECAL

# ScECAL Technological Prototype

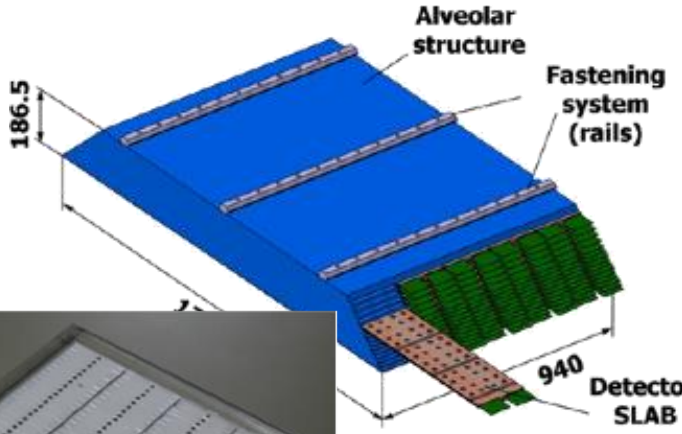
- scintillator strip : 5mm x 45mm x 2mm

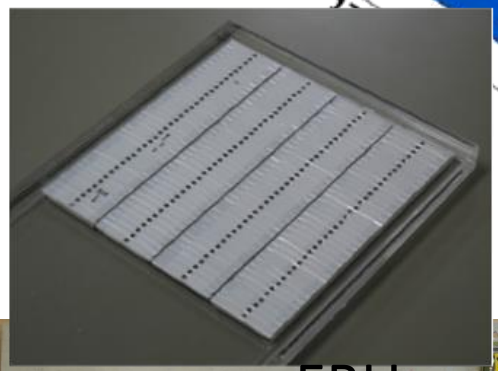
read by MPPC directory

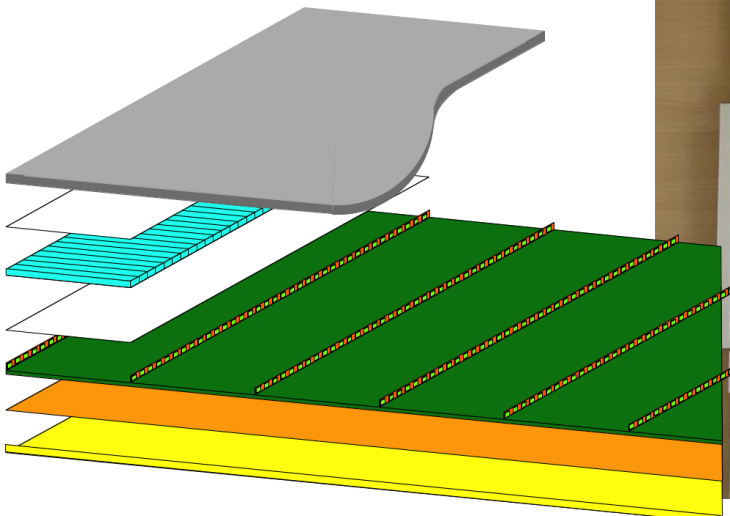
- embedded read out ASIC layer
- SPIROC2b

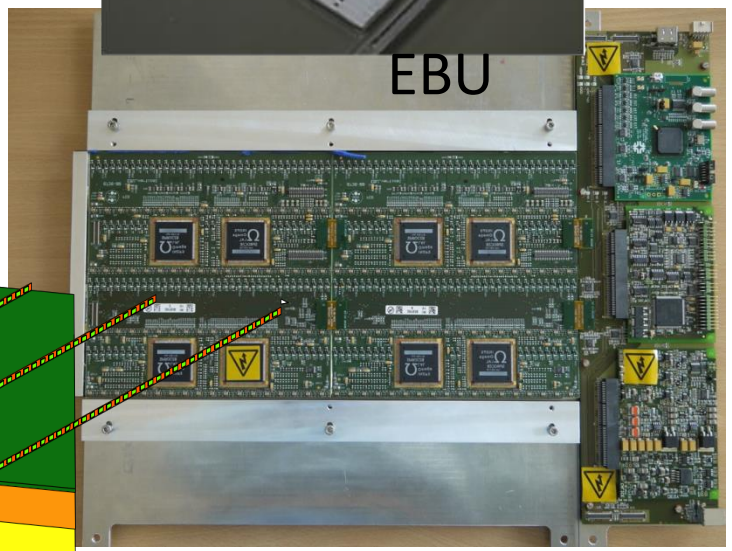
Thanks for the AHCAL group support

We could take beam data.







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- scintillator strip : 5mm x 45mm x 2mm

read by MPPC directory

- embedded read out ASIC layer
- SPIROC2b

Thanks for the AHCAL group support

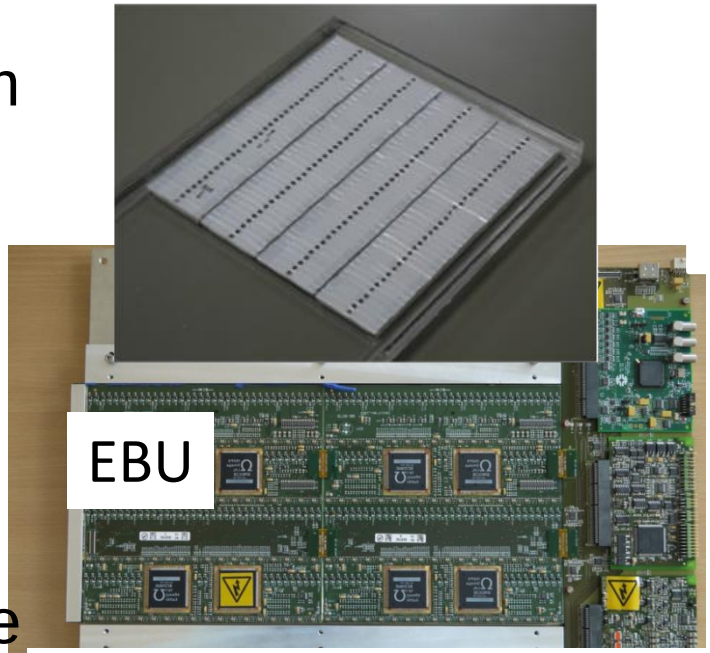
We could take beam data.

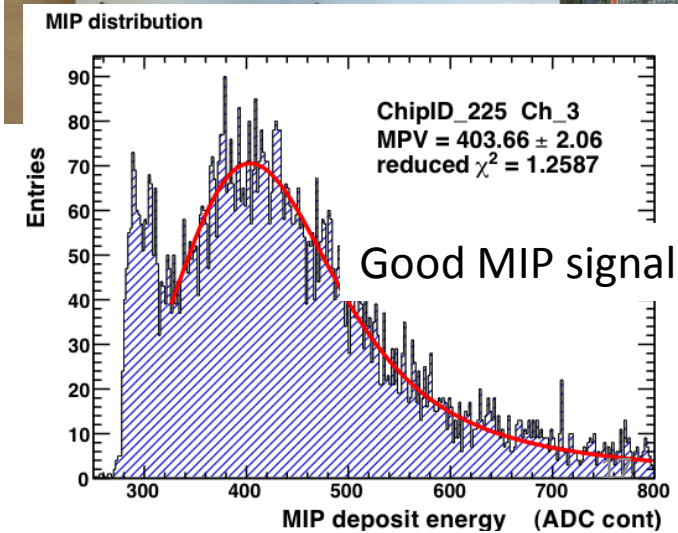
- Nice MIP signal

but not completely separated from Noise

- signal looks broader
- signal is different sci.(photon) and Si (e)
- We need individual threshold setting

We are still working on it.



# Technological Prototype TB

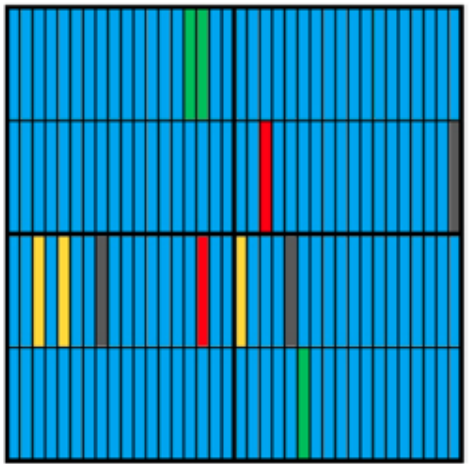
- LED calibration > 90%
- MIP calibration > 80%
- Practical 5x5mm cells
- Pseud-shower development

Next step

- power pulsing
- synchronized DAQ

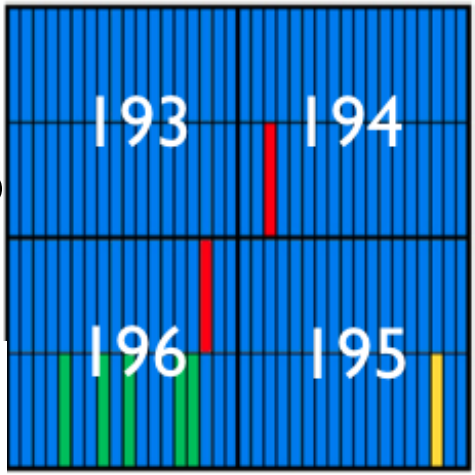
Forward layer result @DESY

LED



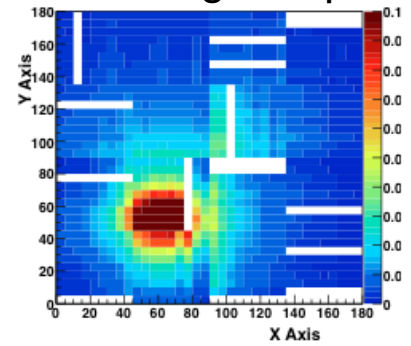
Forward layer result @DESY

MIP




EM shower profile in XY :

0.7X0 tungsten plate * 2

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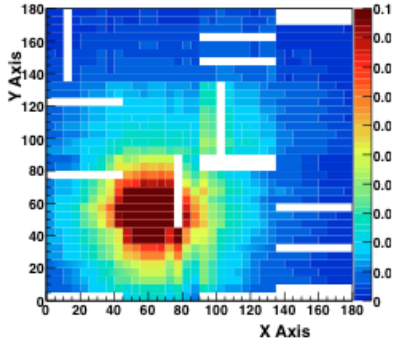


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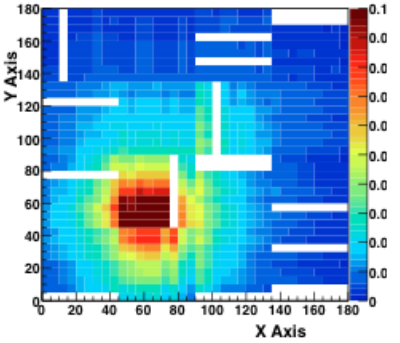




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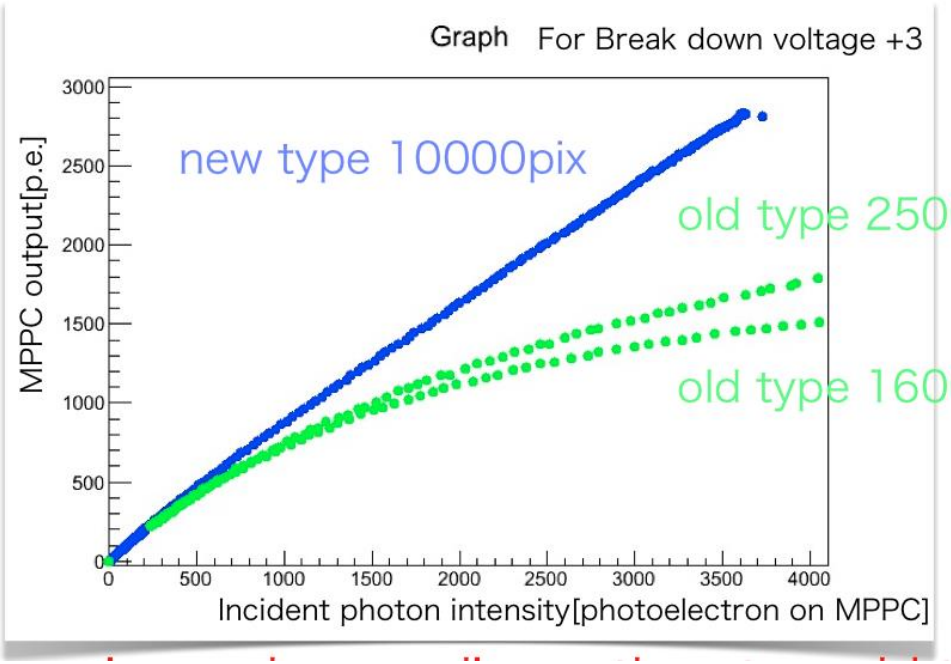
# MPPC

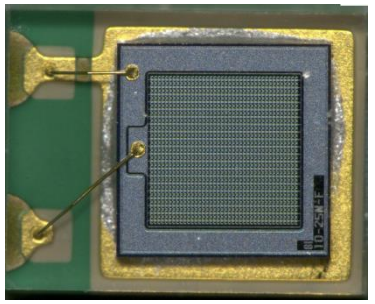
- MPPC is one of PPD manufactured by HPK

Up to 10000 pixel – 10μm pitch

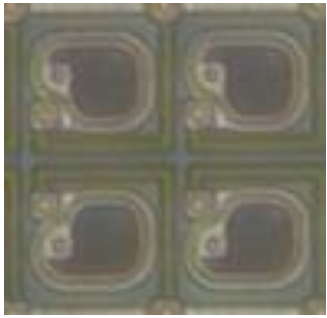
→ Large dynamic range



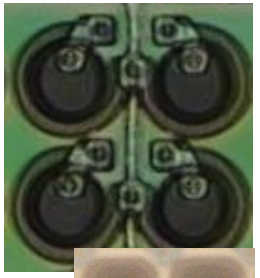

1mmx1mm



1600pix.
25μm pitch

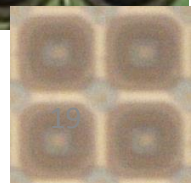


2500pix.
20μm pitch



4400pix.
15μm pitch

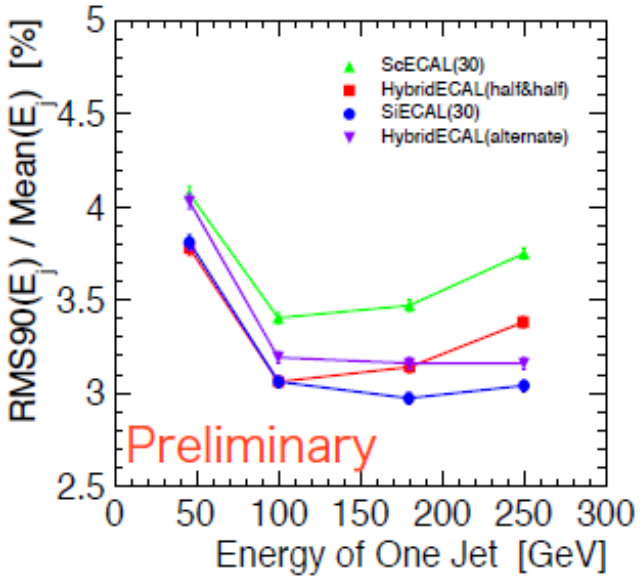
New!



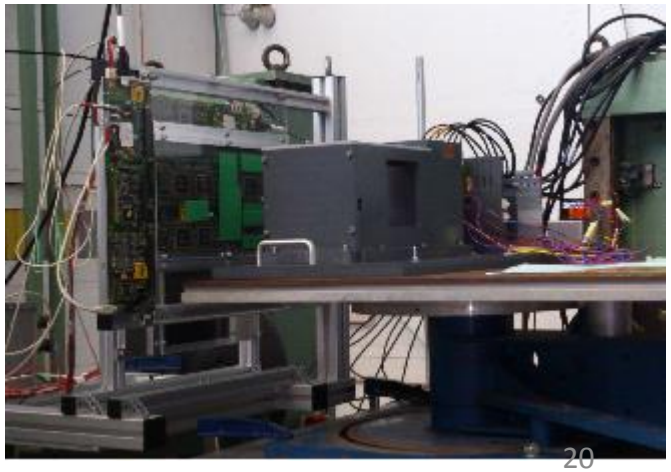
10000pix.
10μm pitch

# Hybrid ECAL

same module thickness




- Hybrid ECAL is a one of the possible option to reduce ECAL cost.
- Jet energy resolution of Si-Sc alternate structure Hybrid is 0.1 – 0.2 worse than Si ECAL result.
- Optimization study is in progress.
- We could try Si and Sc ECAL synchronized data taking at TB in July 2013.
  - analysis is difficult because these daq systems are different…



# Scintillator Strip Design

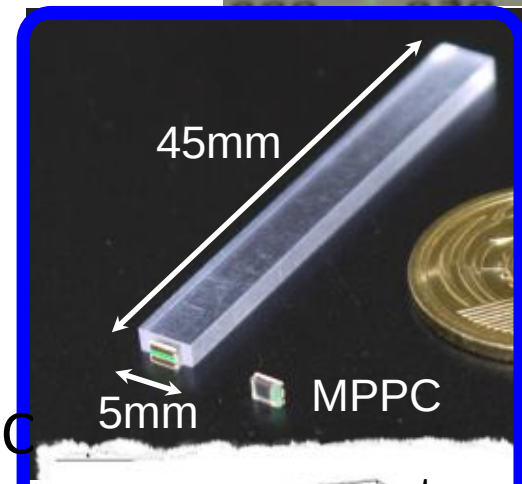
Physics prototype : 3mm thick x 10mm x45mm

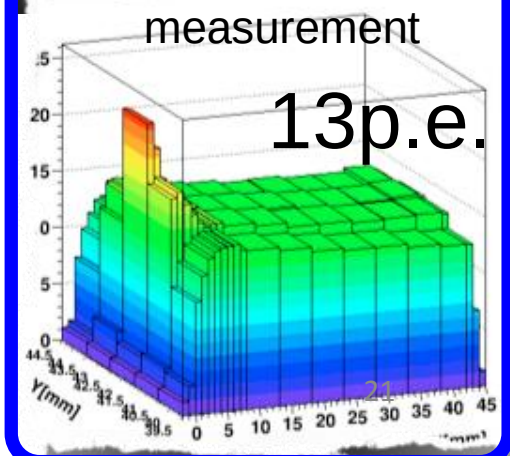
Tech. prototype : 2mm thick x 5mm x 45mm

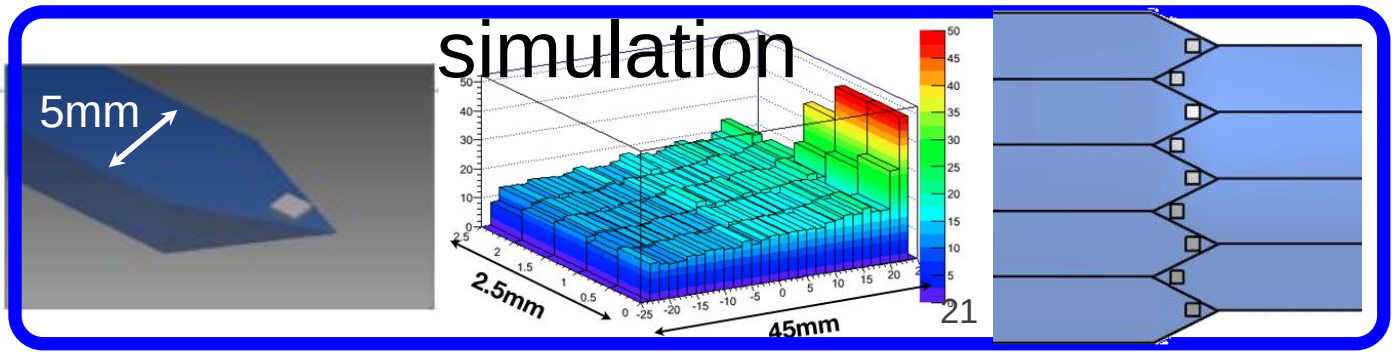
Aiming 1mm thick Scintillator

- Homogeneity is still a problem,
  but we are working on it.

Direct coupling makes non-uniformity in front of MPPC
→ Optimize sci. design



# Summary

We took useful data with technological prototype.
- we faced several difficulties on during operation of tech. prototype and found solutions.

We have to understand more deeply our current tech. prototype.
In parallel, we are preparing many things for the next step
ROC2 → ROC3
FEV8 → FEV9
Short slab → Long slab
Si sensor and MPPC R&D
Scintillator design
Improve DAQ software and hardware

# Backup

# A generic DAQ system for the CALICE calorimeters (Technological Prototypes)

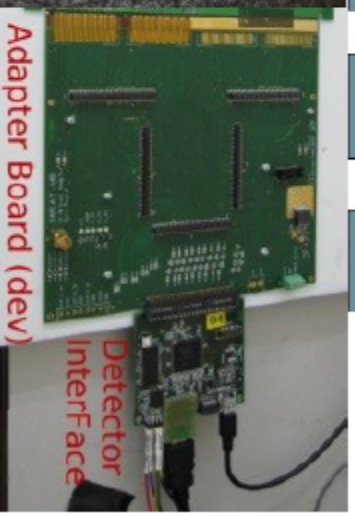
**Standard**

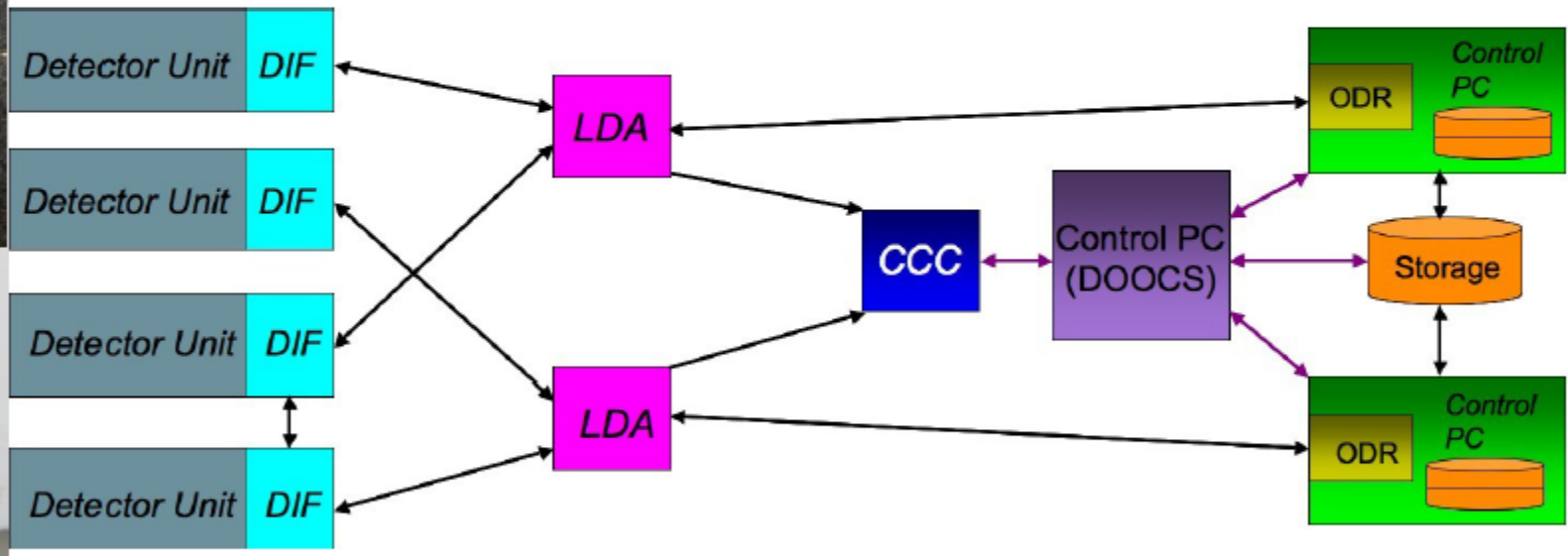
HDMI connectors
LVDS
GBEthernet
Optical links

**Generic**

FPGA

**Scalable**



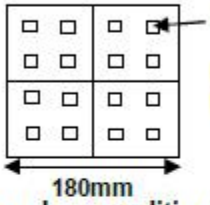

**DAQ chain established using SPIROC and FEV7_CIP**
**Since 1st quarter of 2012 SKIROC and FEV8_CIP**
**-> beam test in March 2012 at DESY**

# ECAL / Thermal flux inside modules

## TEST and simulation on old design

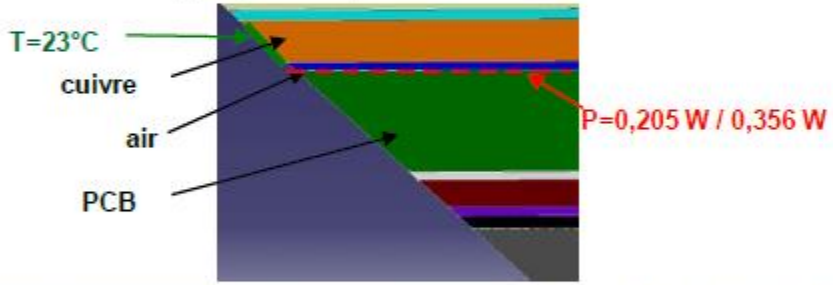
**Inlet**

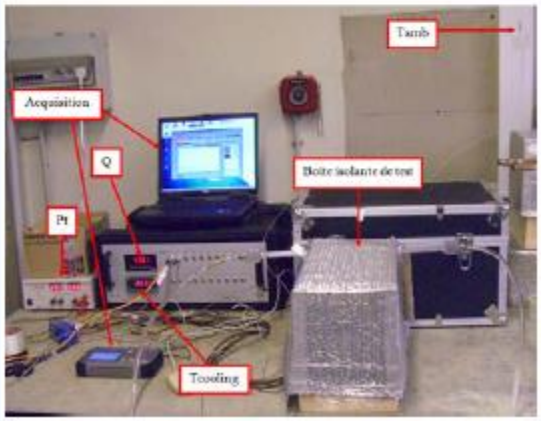
**Power on PCB = 0,205 W / 0,356 W**

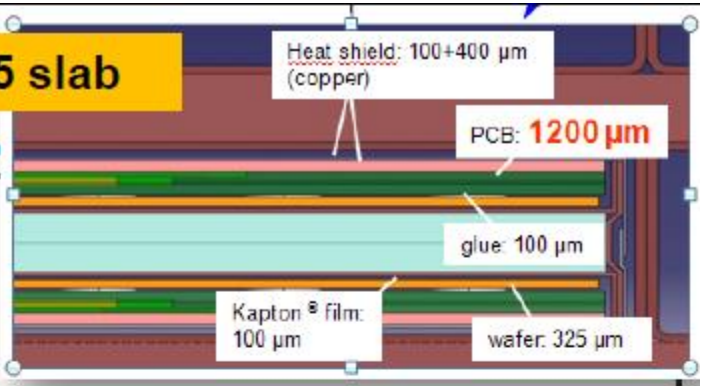



Barrel : (1,6.10-3*16)/180*1445=0,205 W
EndCap : (1,6.10-3*16)/180*2500=0,356W

Boundary condition T = 23 °C beginning of the copper plate
Air between copper plate and pcb is in the model




**Results**

**Barrel : (1.5m)**

**ΔT = 2,2°C**

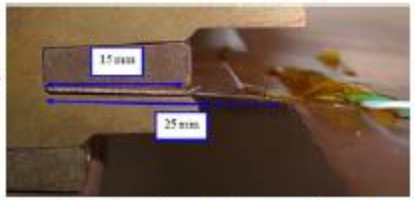
**End Cap : (2.5m)**

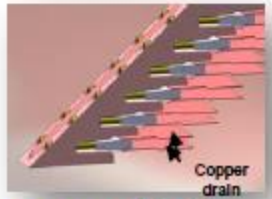
**ΔT = 6°C**

**Conclusion**

**Low T° gradient -> cooling system suitable**
**Cooling front –end (front of slab sufficient)**

Confirmation: **25 mm** free opening in DIF for extraction of cooling system



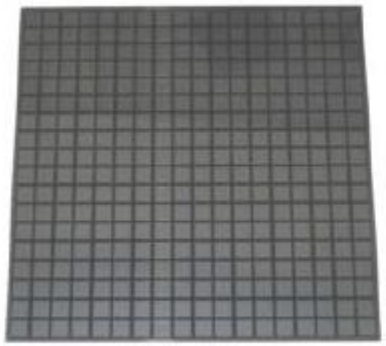



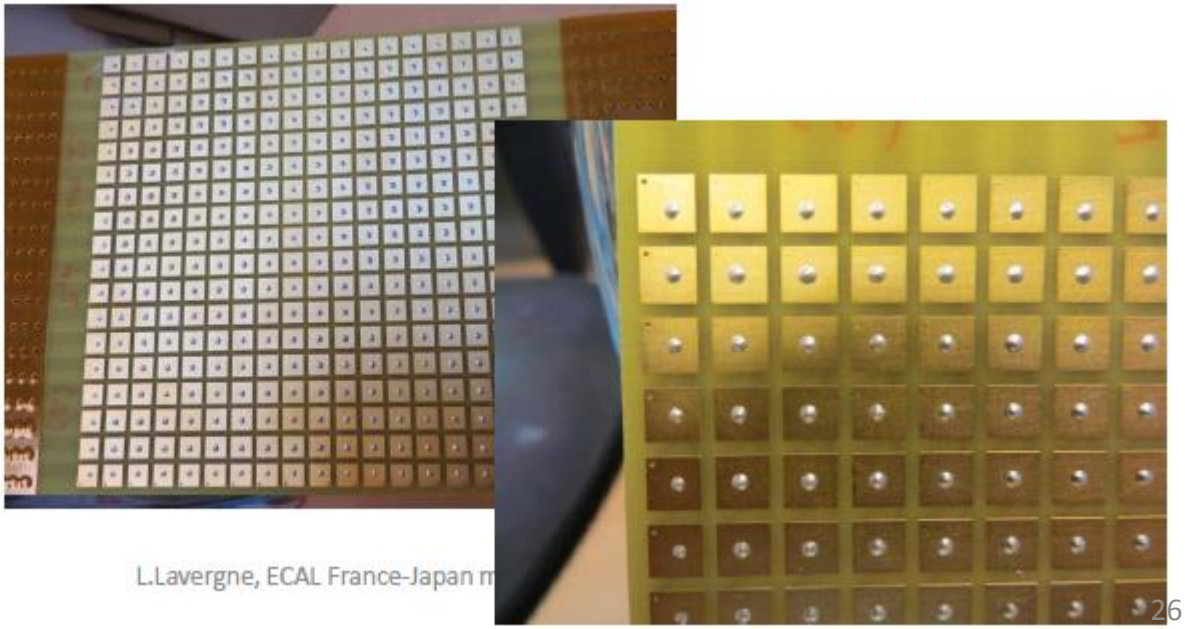

**Copper plate / heat exchanger link**

# Gluing

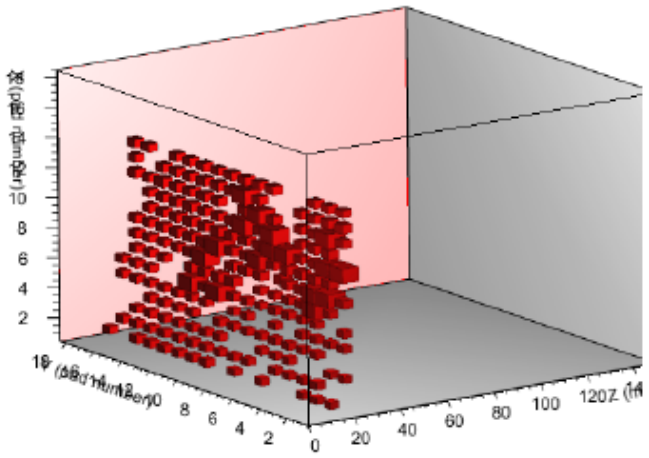
- The automated gluing process is now functional for the beam tests prototypes, reproducible and controlled (for one sensor per PCB).

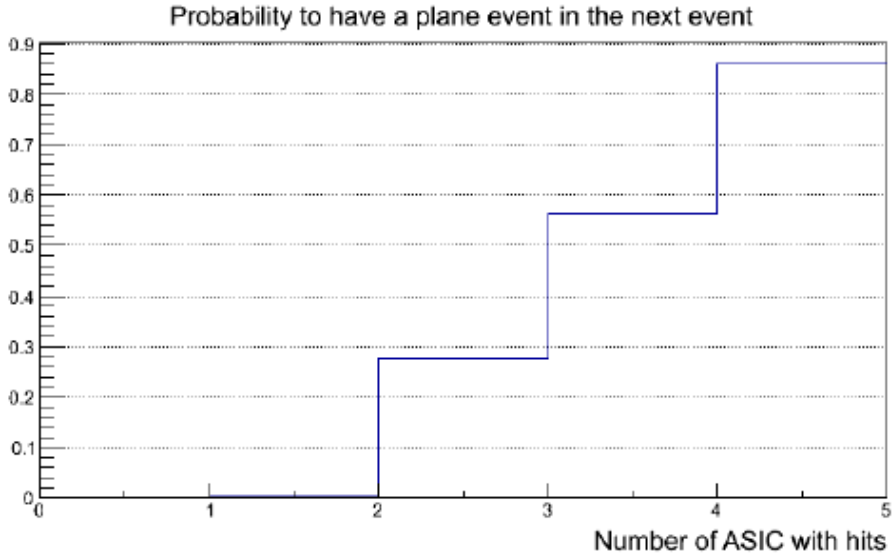
  The next step is to glue 4 sensors on a PCB, using automated positioning





# Plane Event in PP operation






PA is referenced to the analog power supply

→Instabilities of power supply makes fake events

- some digital part connected to analog power supply line

What we have to do

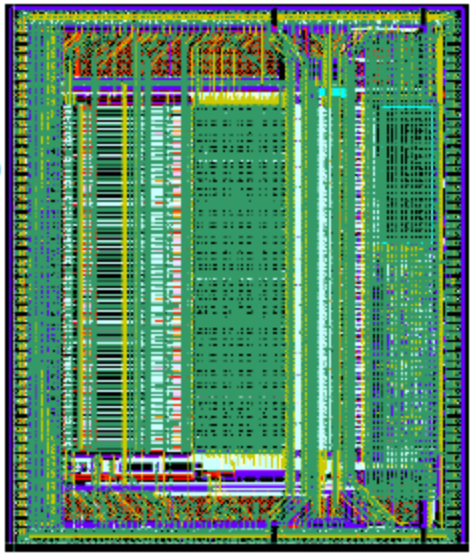
-- We underestimated the instability

→ bigger decoupling capacitors on VDDA

-- We found a few mistake of power supply line connection

→correct power supply lines of digital and analog part.

# SKIROC 2



- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: **1 Mip (4fC)→ 2500 Mip**
  - Shaping time of 180ns
  - Mip/noise ratio > 10
- Auto-trigger on 1/2 MIP (2 fC)
  - MIP/noise ratio on trigger channel >10
  - Fast shaper : ~30 ns
  - Auto-Trigger on ½ MIP
- Analog memory for time and charge measurement : depth = 15
- 12 bit-ADC, 4k internal memory
- Daisy chain readout
- Low consumption : ~25 µW per channel (in power pulsing mode)

# DAQ electronics: GigaDCC

Link Data Agregator (LDA):

- difficult to maintain firmware (Xilinx licence is needed for Ethernet interface, current version is obsolete; understanidng of packet management requires reverse engineering)
- not sufficiently reliable (grounding, shielding, connections)

Gigabit Data Concentrator Card (GDCC) will replace LDA. Same software, reuse of some hardware parts.

# GDCC

**LDA : Xilinx's GEMAC IP bloc is obsolete : code is no more supported.**

- Only used for desktop test benches.

**GDCC is now the replacement board (ECAL)**

- **Can work at high SPILL rate (>100Hz, kevt/s)**
- Mezzanine for DIF connectors : allow future changes
- Discrete fan-out for clock and trigger
- Cost : ~1500€ proto (note: LDA prod =1600€)
- Have just received V1 (V0 had some layout errors)

GDCC firmware will be improved

- Preliminary $GDCC_{LDA}$ firmware is acceptable and implements all LDA functions
- Will add / rewrite functions :
  - UDP/IP
  - New & simplified FSM
  - Robust MUX & buffers
  - Synchronous structures
  - Removal of UK serial link under study

Still need mechanics to hold cables and pay attention to cabling
+ Reset system base on arduino board
Software components are to be improved

- Packet capture (some losses, negligible @10Hz spills)
- Framework Integration (XDAQ...)
- "Failsafe" procedures

# FEV8

We used FEV8_CIP until now (CIP = Chip In Package)

COB (Chip On Board = naked die bonded on the board) version exists but has flatness issue = problem to glue the sensor.

Improvements to be done concerning FEV8:

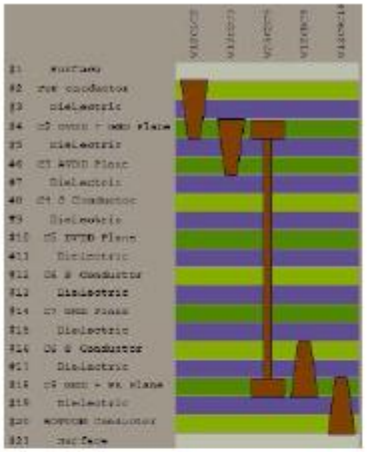
- FEV8 is referenced to GND while chip reference is 3.3V (nobody checked this…)
- On FEV8 some digital power supplies of the chips are wired to the analog supply
- The board has 4 chips only
- CLK lines are not good at long length

So, we took decision to design a new version : “FEV9”

- With a new version of adapter board (power supply, line drivers)
- Packaged chips : 400 balls BGA
- Fix reference, decoupling
- 16 chips
- Transmission lines for 2m & ~80 chips

The board is being routed (finished by the end of the week)

# FEV8 → FEV9



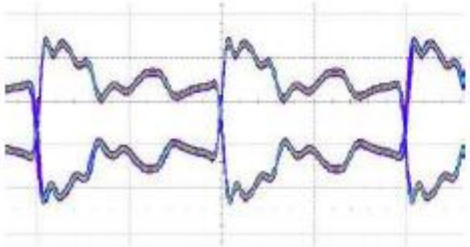
Symmetric stack will improve flatness, good for wafer gluing

Analogue signals shielded with AVDD

Digital traces shielded with GND and kept away of analogue (as much as possible)

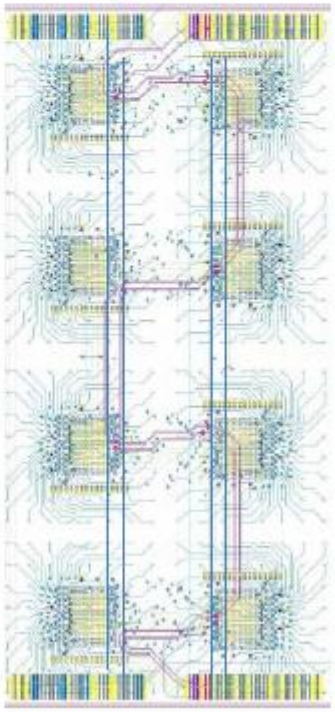
FEV9 1st version will implement two partitions of chips with differential signals routed with 2 options : straight lines (needs 2 times more buffers & connectors) or snake line (maximize load)

FEV9b is planned

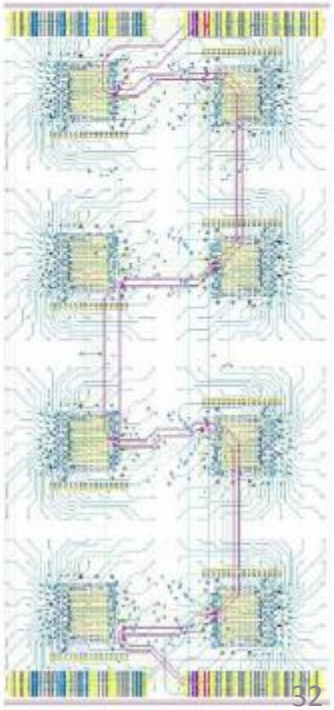


Measuring at the end of 2 FEV8…

Option 1



Option 2



# TB July 2013

## What has been done (only the lowest gain)

with 6 slabs
(nobody beleived 7th was "configurable", start with 6 slabs, bad consequence of democracy)
everything in power pulsed and continuous modes:

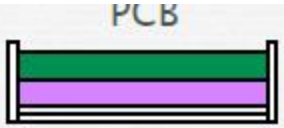
- MIP position scan (9 points)
- showers with 5 x 4.2 mm W (first layer without W) at 1,2,3,4,5 GeV

with 7 slabs

- MIPs (center point only)
- 6.3x3 mm (in front) + 6x4.2 mm W (between layers) only at 2 GeV
- 6.3x3 mm (in front) at 2 GeV
- spill frequency scan 5-100 Hz (nominal point - 10 Hz)
- combined Si-Sc run at 2 Hz, only spill synchronization (not BX)

No trigger delay scan (delay=130 as in Feb'13)

- Slab made by LLR : U shape
- EBU contains scintillator sensors and read out electronics including SPIROC2b
- mechanical combination photo

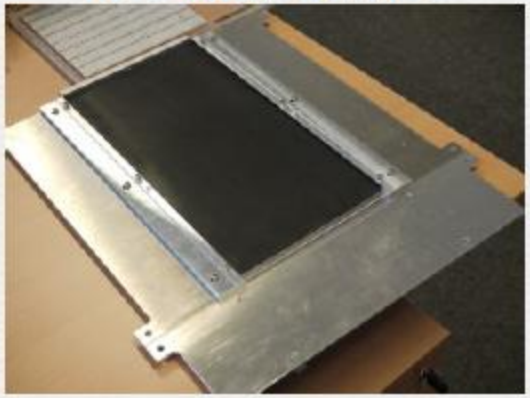


U-struc.

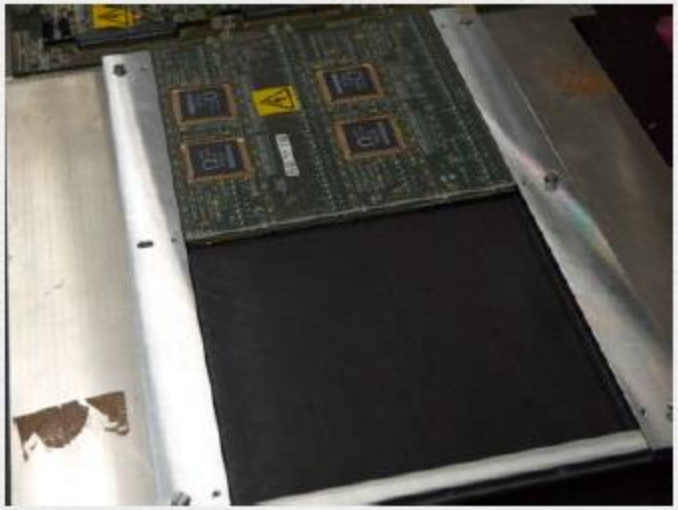
EBU

18x18cm2

U structure



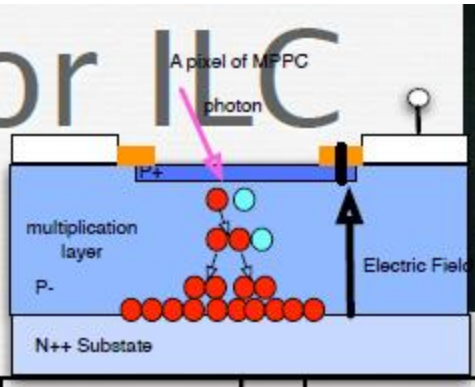
EBU in U

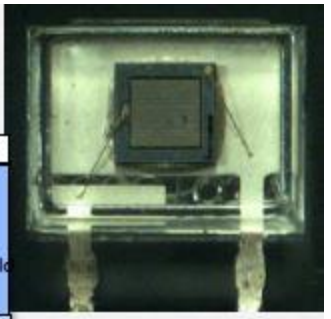


2

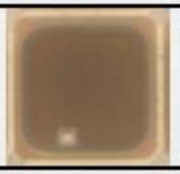
# MPPCs for ILC

- in 1mm x 1mm active area
- >= 1600 pixels



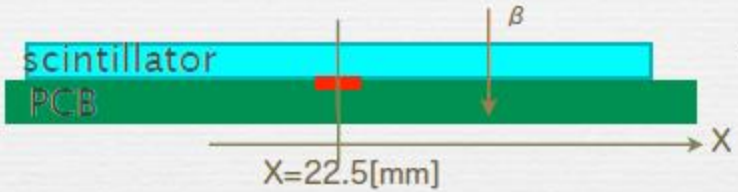



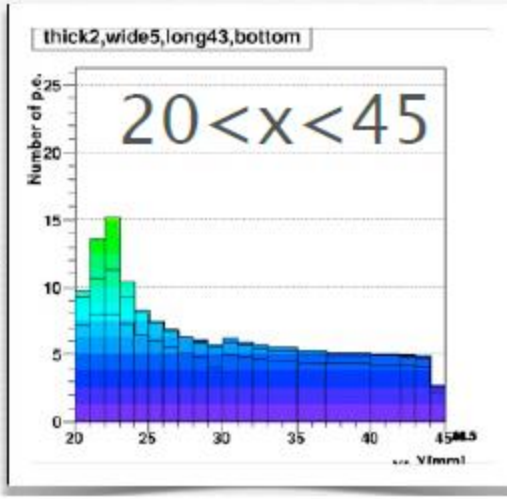
ILC-package

| Npixels | pitch (um) | gain ($10^5$) | C(fF) | old PR | new MR |
|---|---|---|---|---|---|
| 1600 | 25 | 2.7 | 17 |  |  |
| 2500 | 20 | 2.0 | 12 |  | X |
| 4400 | 15 | 2 | 10 |  |  |
| 10000 | 10 | 2 | 5 | X |  |

# strip read out vs uniformity

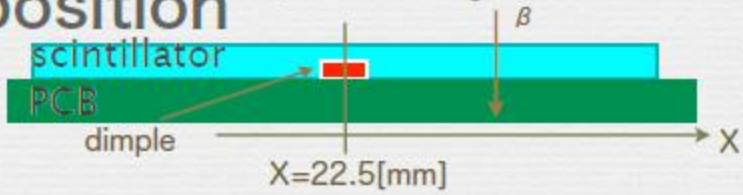
- MPPC on the PCB board
- simplest : Np.e. ~5 : too small
- PCB is in  a hole

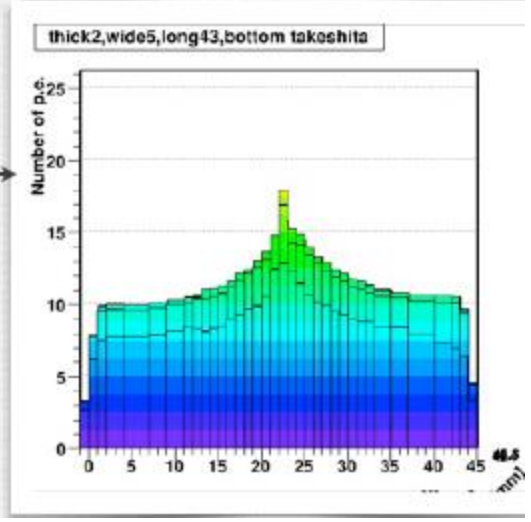



with a dimple, MPPC is soldered easily

- Np.e. ~10, except MPPC position

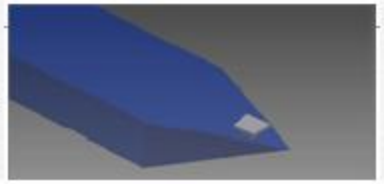


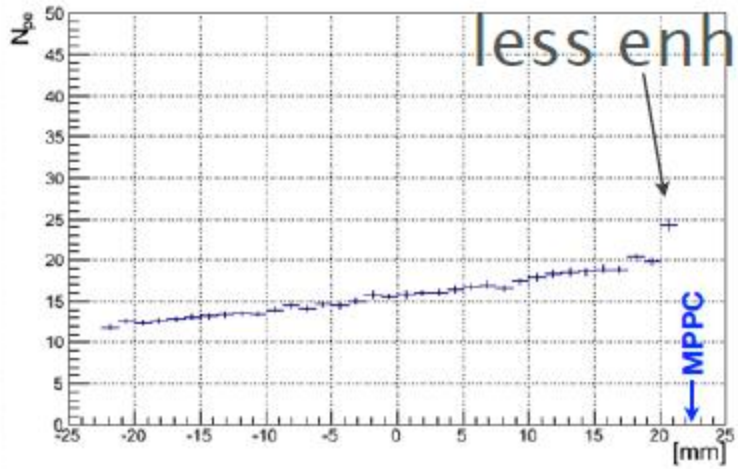



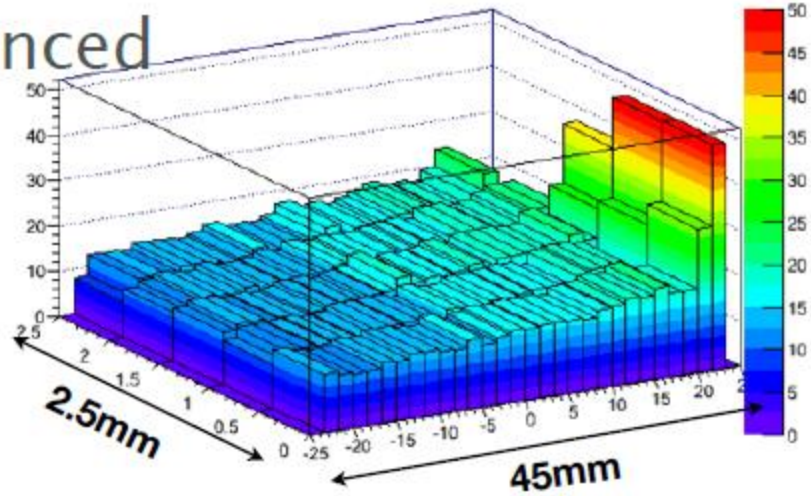

- we will test it

# scintillation light sim. cont.

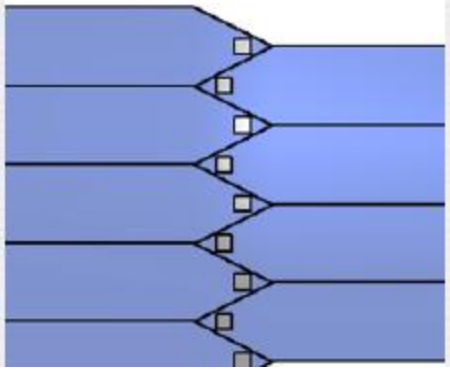
yet another strip idea






amount of scintillation light seems to be enough
homogeneity is good
installation looks promising



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# ScECAL Technological Prototype

- scintillator strip : 5mm x 45mm x 2mm

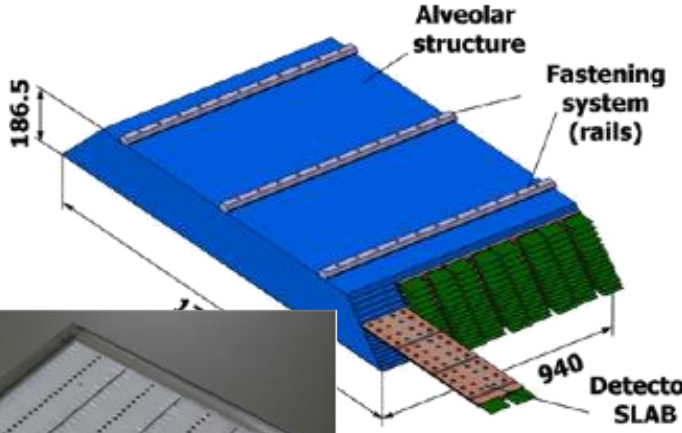
read by MPPC directory

- embedded read out ASIC layer
- SPIROC2b
- Nice MIP signal, but

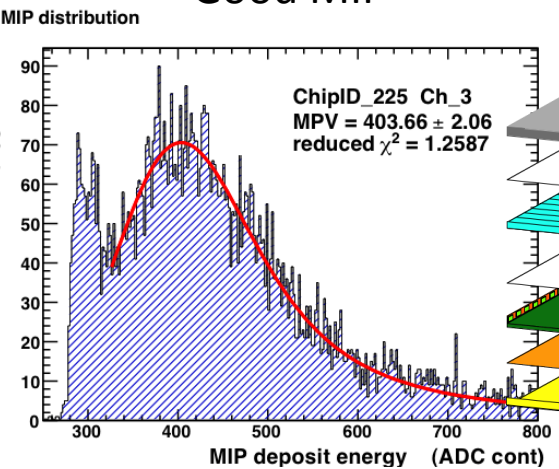
not completely separated from Noise

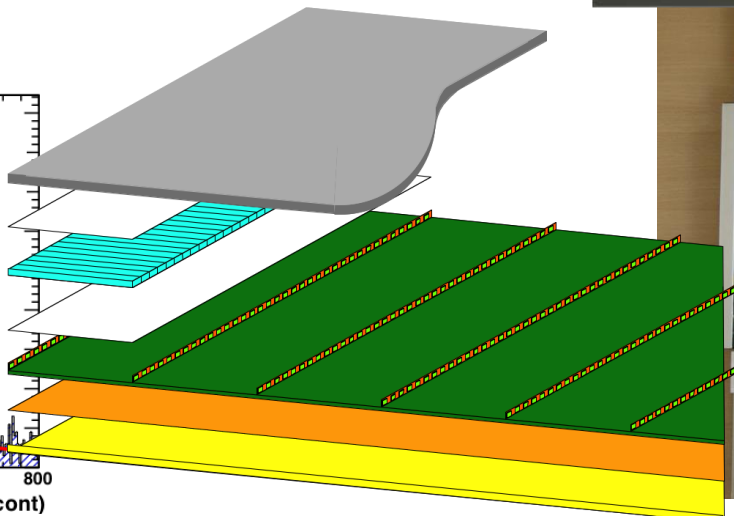
Thanks for the AHCAL group support

We could take beam data.




Good MIP



EBU