SiW ECAL optimisation in simulation

Trong Hieu TRAN

Laboratoire Leprince-Ringuet, Ecole polytechnique, CNRS/IN2P3

Summary of works done by:

Shion Chen, Daniel Jeans, Sachio Komamiya, Chihiro Kozakai

University of Tokyo

Trong Hieu Tran

LLR, Ecole polytechnique

Outline:

- Introduction
- PCB thickness
- Guarding size of the sensors
- Effect of dead pixels
- Number of layers

ILD meeting

Cracow, September 2013

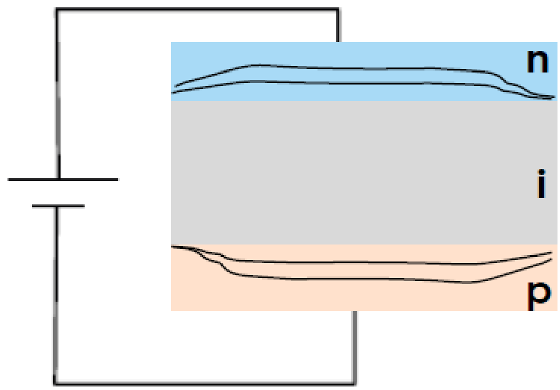
Introduction

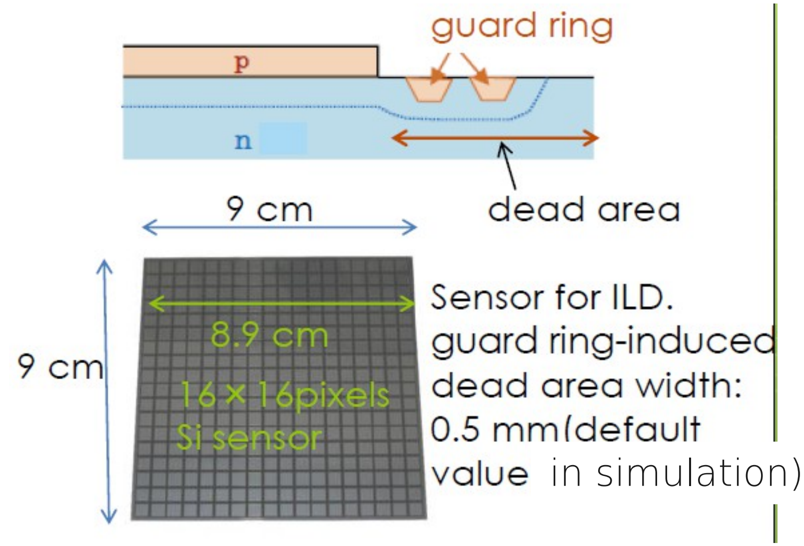
- **Motivation**
  - ILD is costly, especially SiW ECAL (~30% ILD's price)
  - SiW ECAL cost mainly due to: large sensitive area, large number of channels
  - Many studies of cost-effectiveness were/being realised
- **Options**:
  - Reduce ECAL number of layers
  - PCB thickness
  - Guard ring size
  - Effect of Si sensor dead area.
  - ...

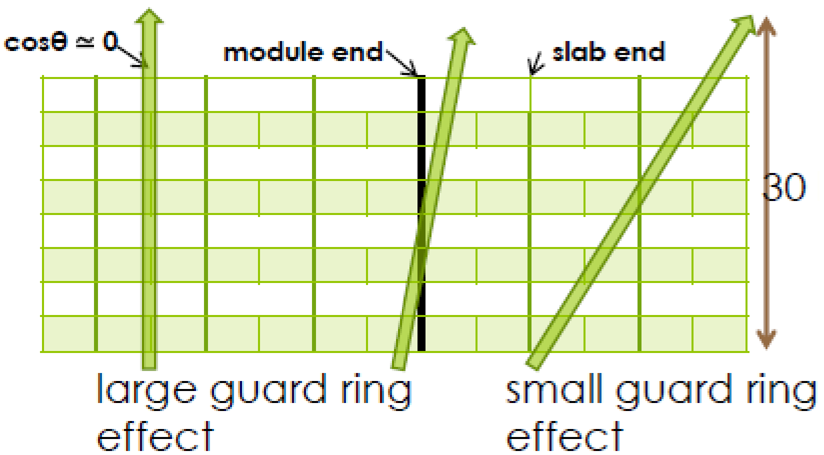
- All studies are done with Mokka & Marlin framework.
- Detector performance estimated via jet energy resolution (JER) with jets recontructed by PandoraPFANew.
- ILD model: ILD_o1_v05 (DBD)

Guard ring in SiW Ecal

- Sensor is matrix of PIN diodes
- Guard ring prevents surface leakage current → decreases dark current and improves high voltage stability
- Study how geometrical inefficiency affects JER resolution





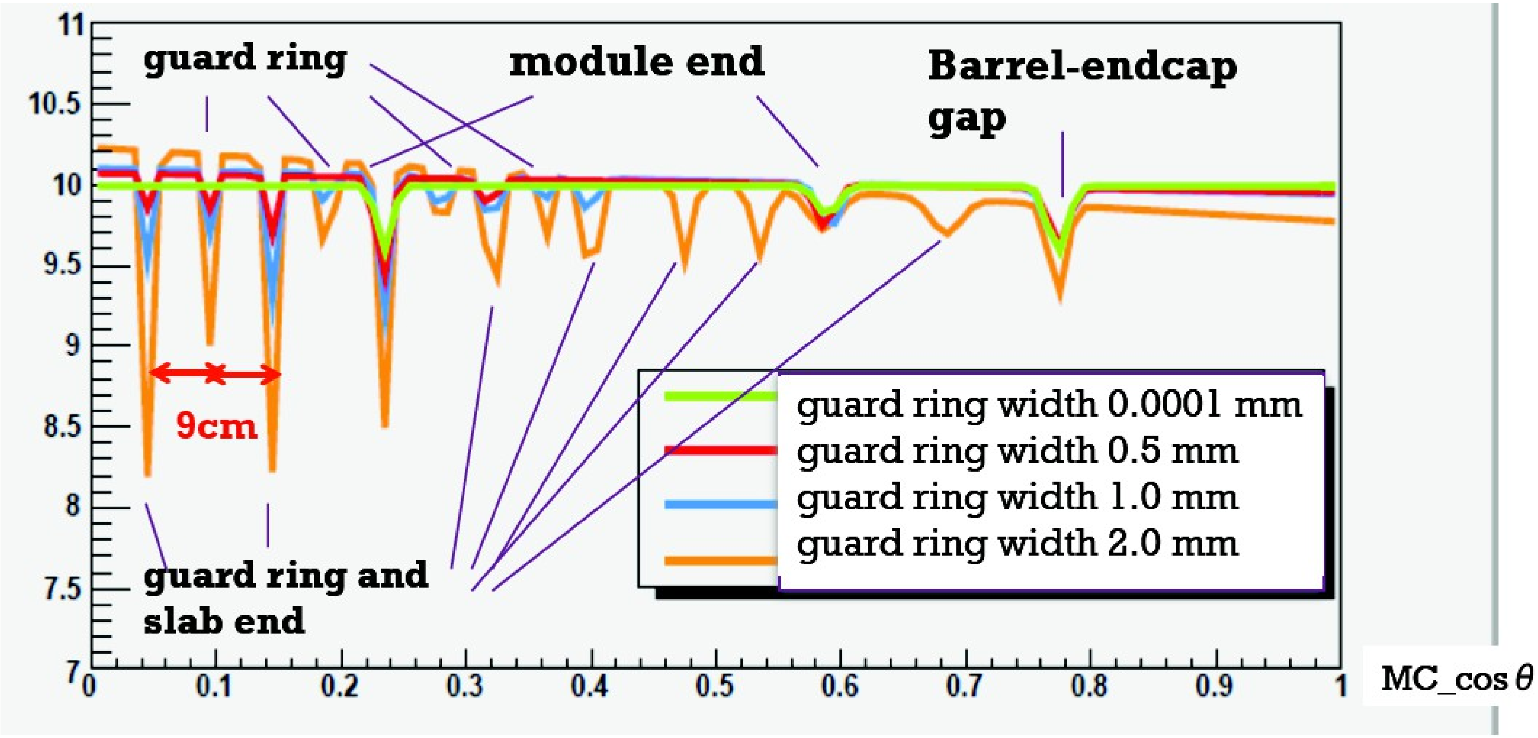


- Energy loss in gaps is compensated by simple theta angle correction

Guard ring in SiW Ecal: energy correction

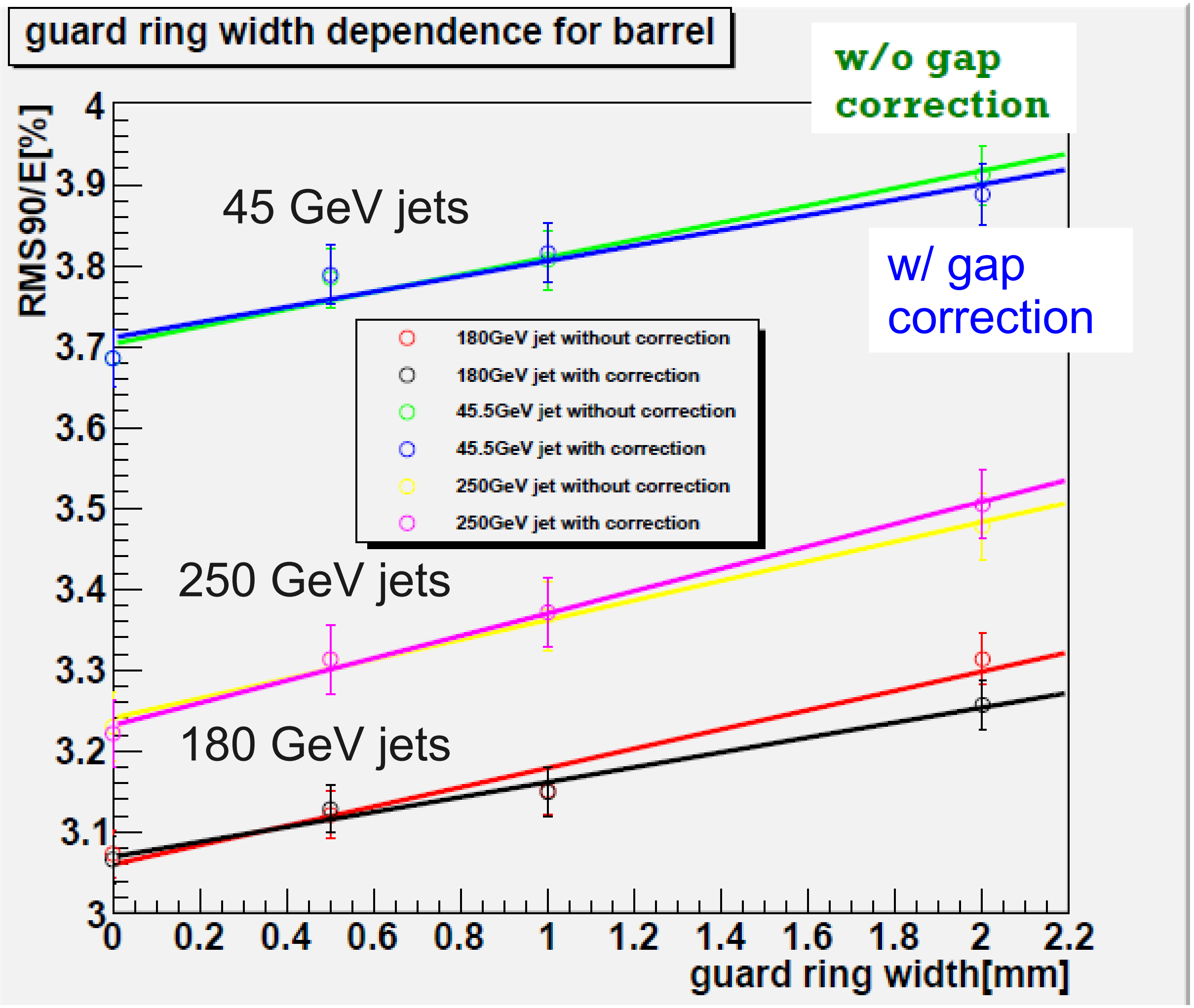
- Energy decreases in gaps between slab sensors, alveolars, at module ends and barrel/endcap gap.
- Direction resolution for θ of 3.3×10^{-4} rad. Sufficient to give a correction by θ.
- Correction is determined by gaussian+linear fit of simulated response to 10 GeV photon
- Energy drop ~10% @ 1.0mm, ~20% @ 2.0mm

10 GeV photons



JER with different guard ring widths

- Z → uds events (Z decaying at rest). JER estimated by RMS90 method.
- Linear dependence of JER with 6% difference between 0 mm and 2mm widths
- Angular correction also helps resolution

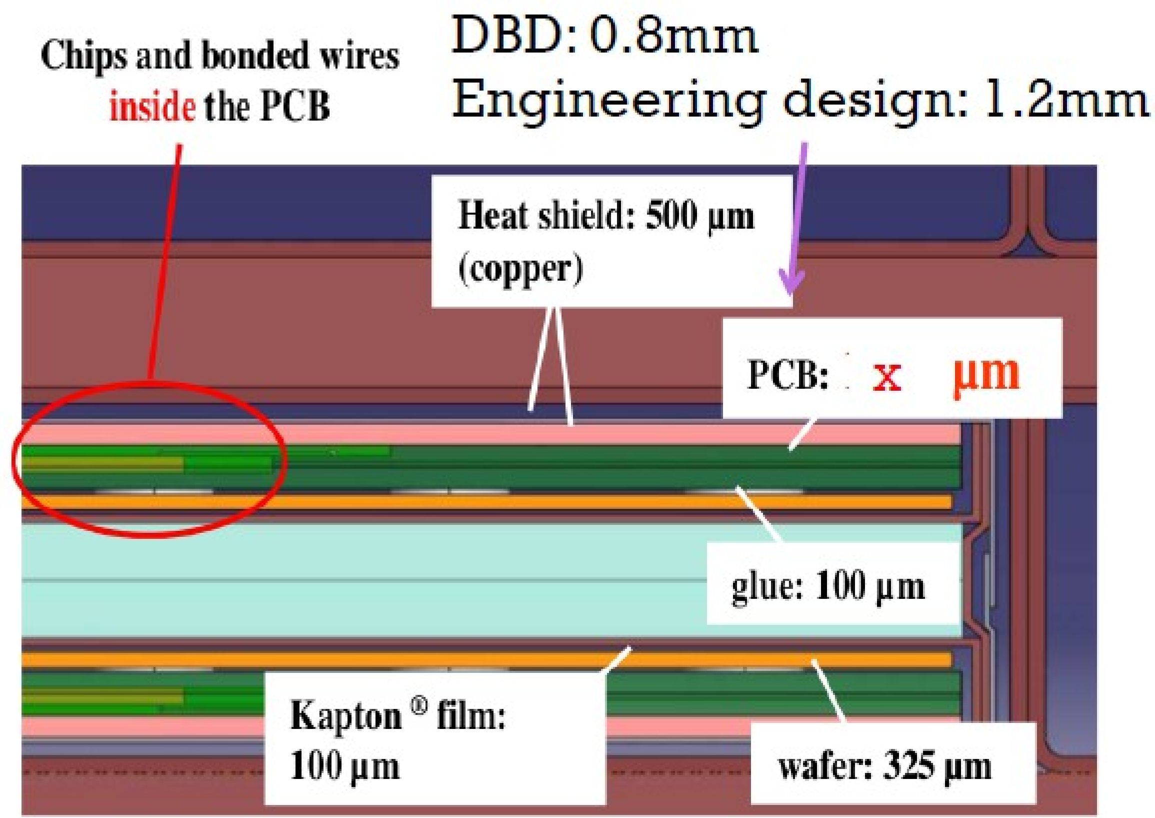


PCB thickness

PCB thickness

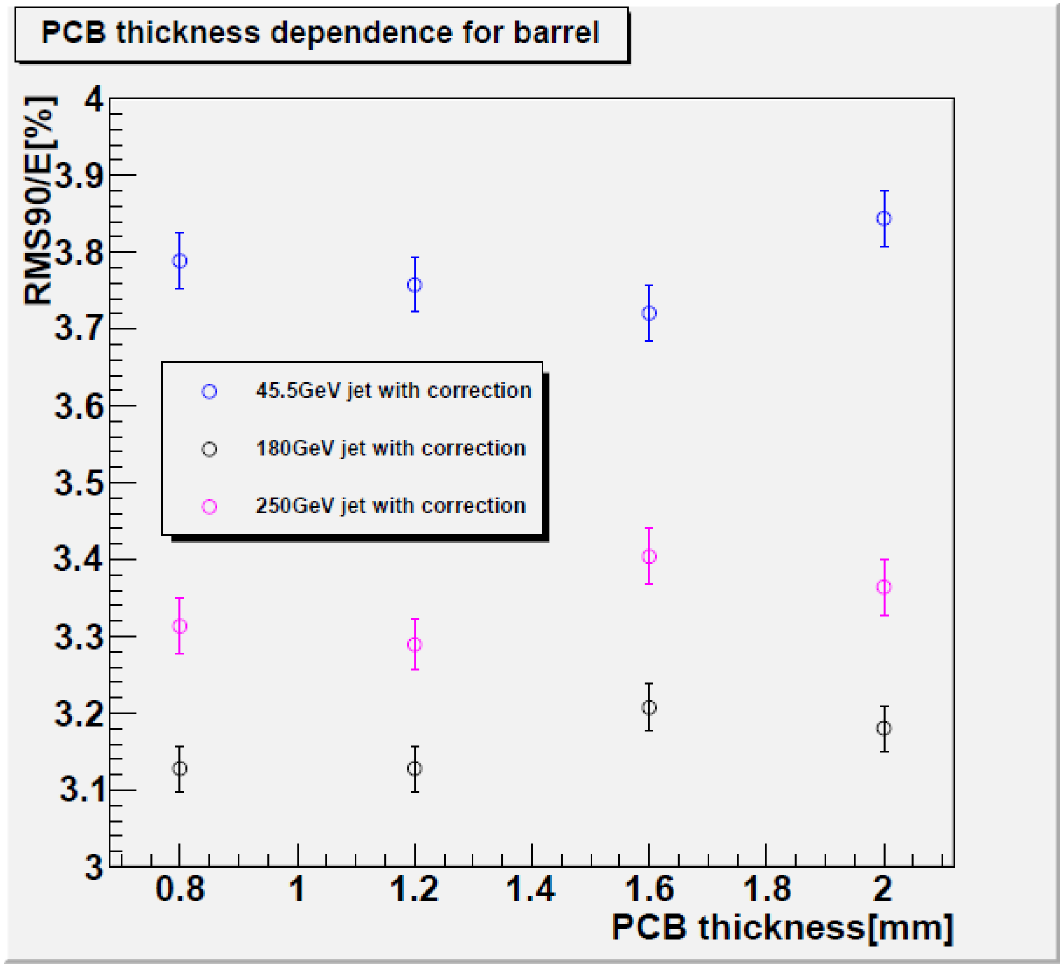
- Increases lateral shower size
- More overlap of particle showers
- Confusion increases → JER is expected to be worse at high E

- Thin PCB is preferable for performance but technologically difficult and expensive



PCB thickness: effect on JER

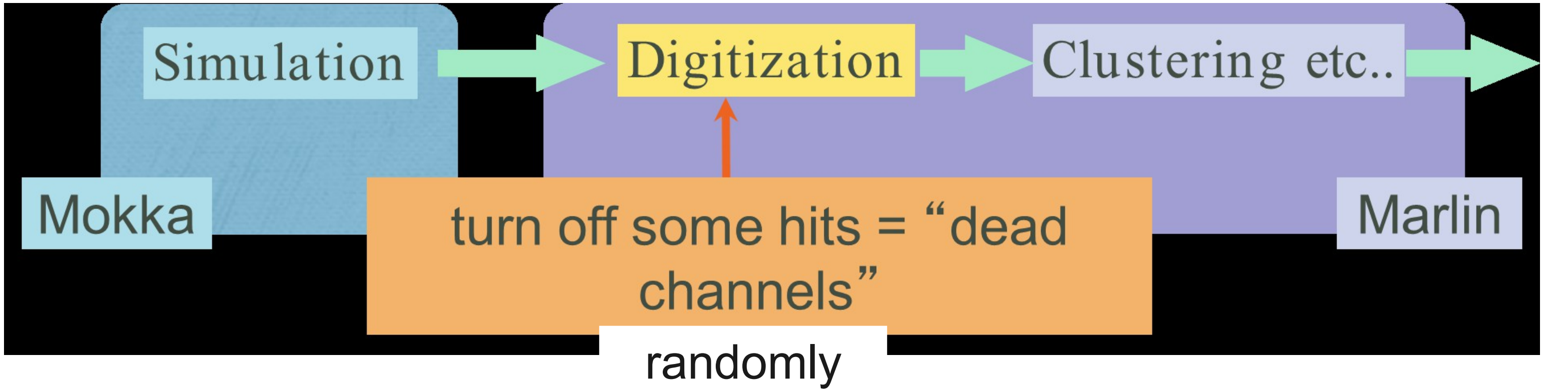
- The rest of modules remains the same as default ILD model
- → Whole detector size is bigger than default
- No significant dependence of JER on PCB thickness is observed



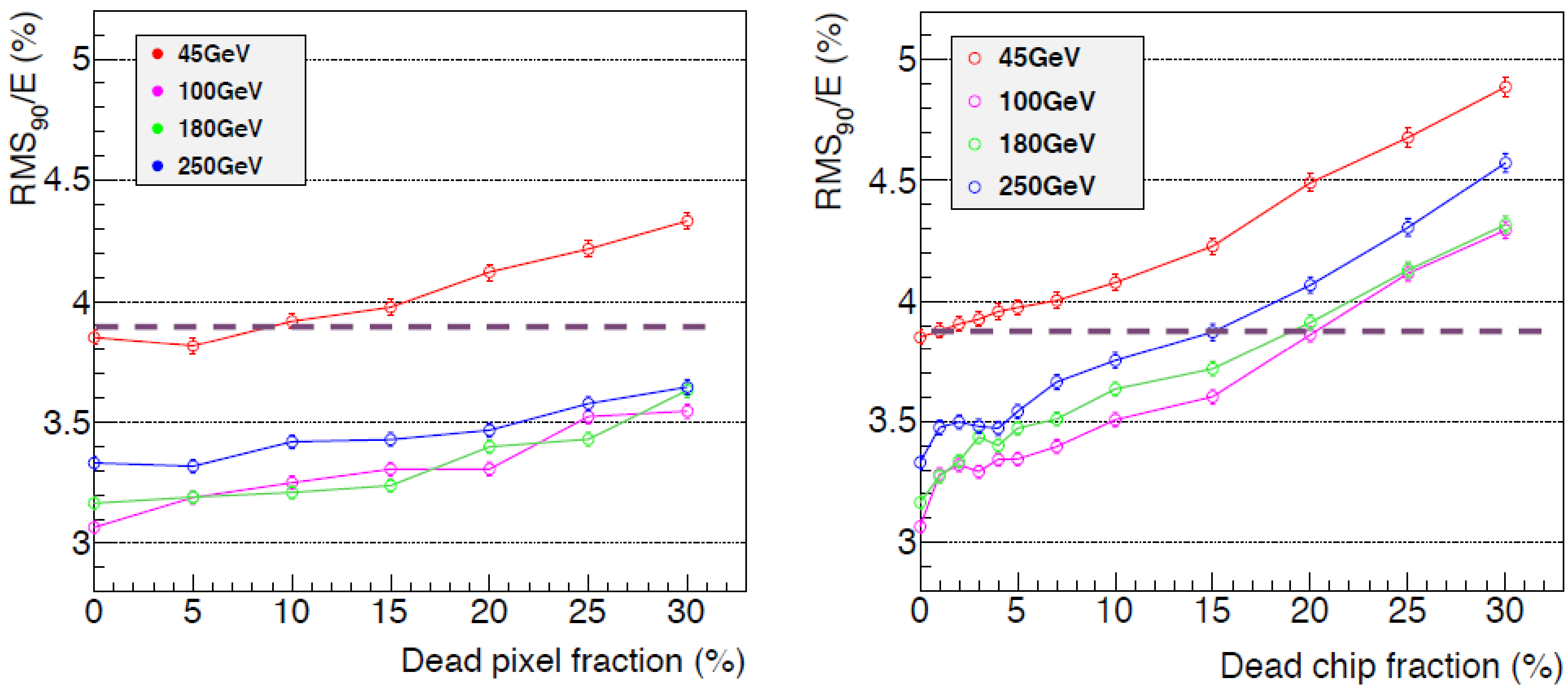
Dead channel effect

Dead channel effect

- If a few % dead cell is OK, we can increase yield for Si sensor and reduce cost.
- Some of the readout chip may be broken during construction or experiment
- Study procedure:



JER dependence on dead pixels / chips fraction



- Almost negligible effect with 10% of dead pixels
- Small effect with 5% of dead chips
- ECAL resolution degrades due to decreasing sampling fraction, but weak effect on JER.
- No serius breakdown. PFA is very robust against dead channels.

Number of layers

ECAL number of layers

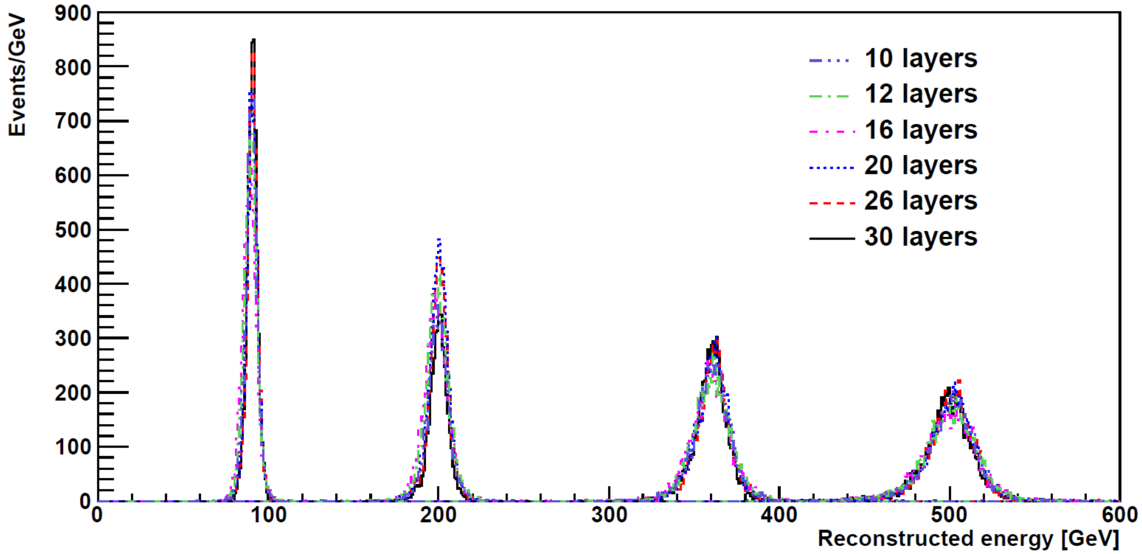
$$S_{\text{Si}} \propto \frac{[\pi(R_{\text{TPC}}+e)^2 - \pi R_{\text{TPC}}^2]}{e_1} \times L_{\text{Barrel}} + \frac{\pi R_{\text{TPC}}^2 \times e}{e_1}$$
$$= \frac{2\pi R_{\text{TPC}} \times e + \pi e^2}{e_1} \times L_{\text{Barrel}} + \frac{\pi R_{\text{TPC}}^2 \times e}{e_1}$$

S_{si} : total Si surface
R_{TPC}: TPC radius
e_1: layer thickness
e : total thickness of all layers
L_{barrel} : Barrel length

- Five alternative SiW-ECAL models have been studied for baseline detector ILD_o1_v05
- In all models: the same total W thickness and 1:2 between inner:outer W layers

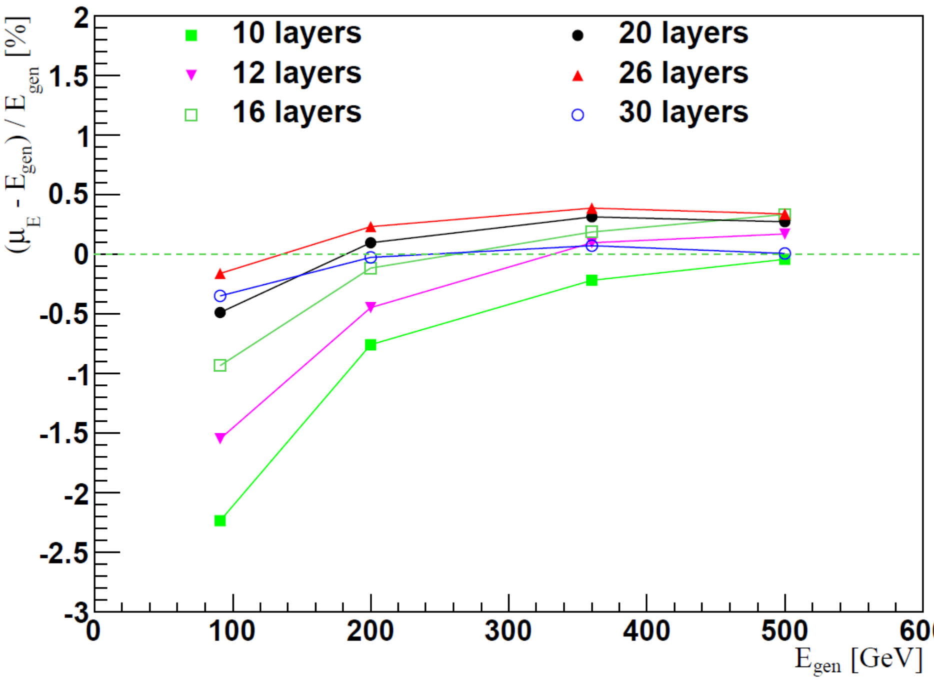
ECAL model	W layers	Layer thickness (mm)
30 layers	20 9	2.1 4.2
26 layers	17 8	2.4 4.8
20 layers	13 6	3.15 6.3
16 layers	10 5	4.0 8.0
12 layers	7 4	5.32 10.64
10 layers	6 3	6.65 13.30

JER vs ECAL number of layers

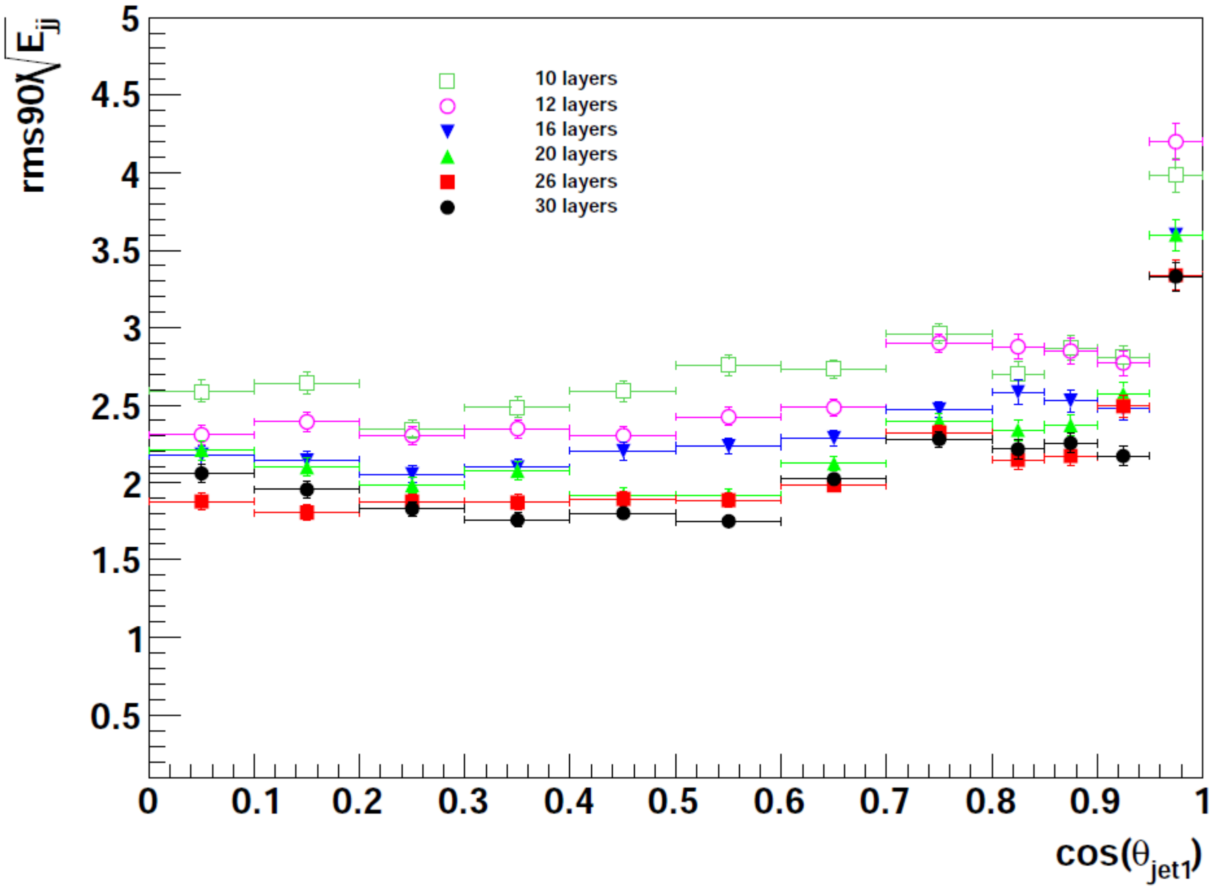


- Reconstructed jet energy for all ECAL models and for events at c.m. energies 91, 200, 360, 500 GeV

- Residual $(E_{rec}-E_{true})/E_{true}$ shown in% as a function of E_{true}
- Linearity within 0.5 % for 30-26-20 layers and significantly degrades for other ECAL models



Jet energy resolution vs cos(θ_jet)



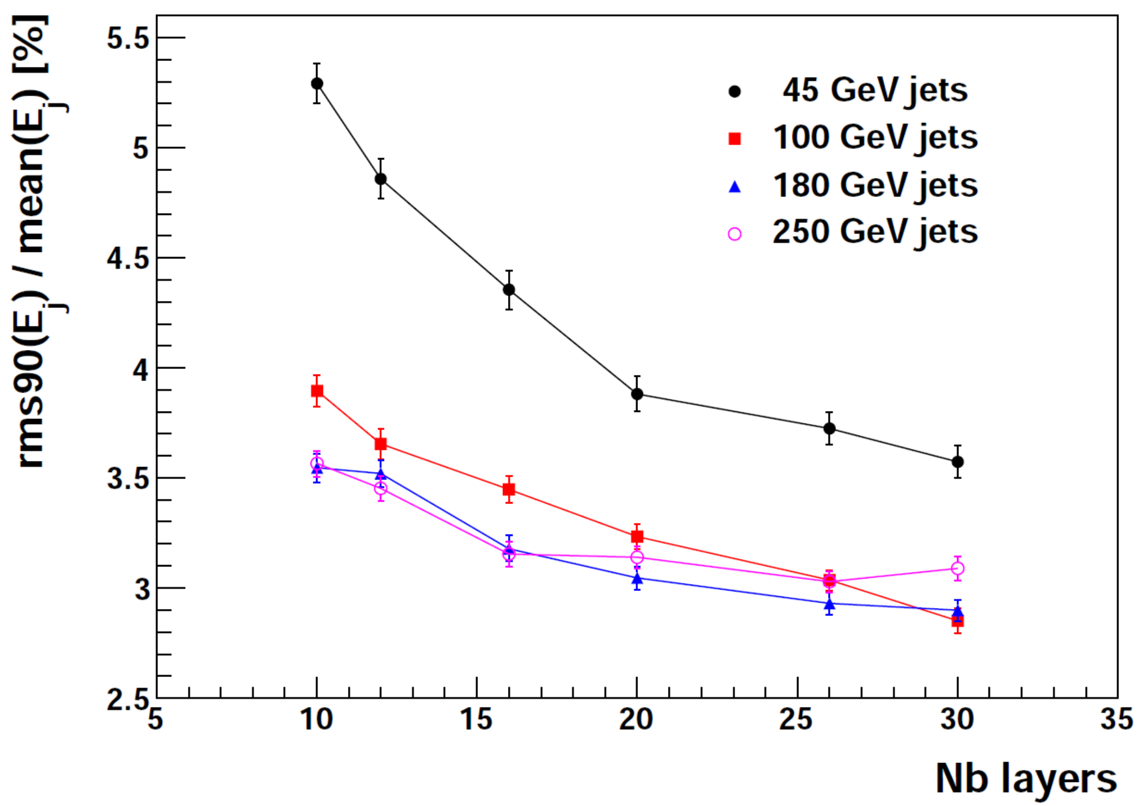
- Jet energy resolution presented in function of cos(θ) of first jet
- No significant problem found among full region of cos(θ)
- Example for Z→uds 91 GeV sample

Jet energy resolution

- Single JER as a function of number of layers for 91, 200, 360, 500 GeV Z → u/d/s.

- 9% of degradation when going from 30 to 20 layers for the worse case, 45 GeV
- effect is less important for higher energies

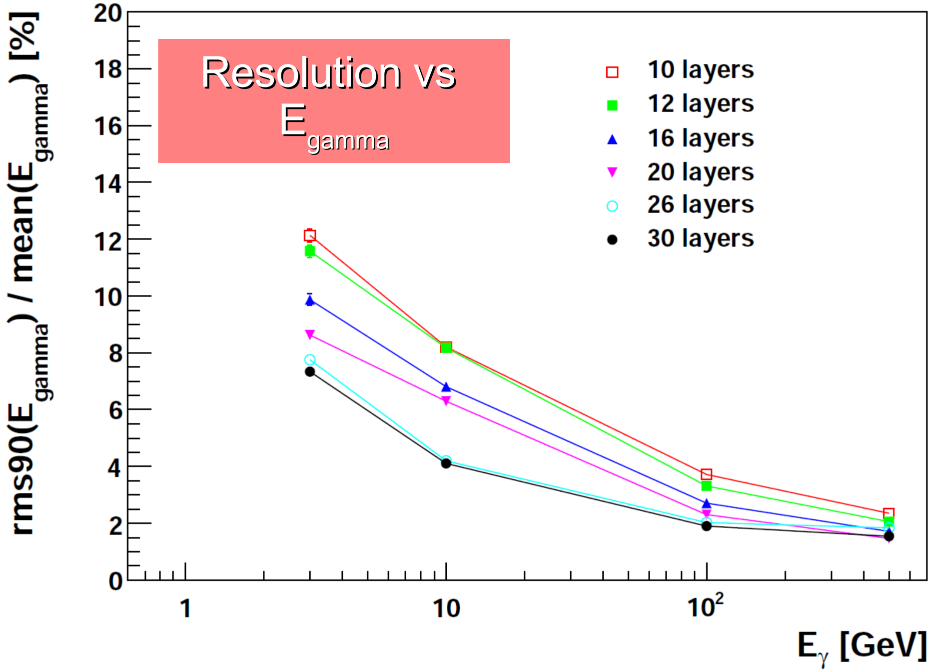
A cut |cos(theta_jet)| < 0.7 is applied to avoid the Barrel/Endcap overlap area

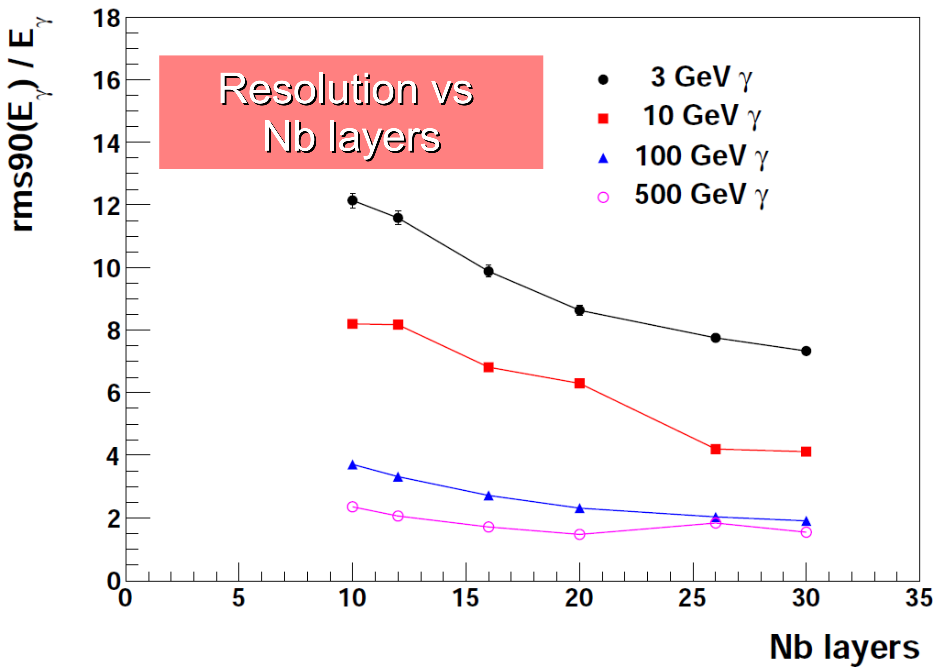


The error bars are taken from a fit.

$$\frac{\mathrm{rms}_{90}(E_j)}{E_j} = \frac{\mathrm{rms}_{90}(E_{jj})}{E_{jj}}\sqrt{2}$$

Photon energy resolution





- Photon energy resolution as a function of E_{photon} (left) and N-layers (right)
- Slight degradation observed going from 30 to 20 layers (≤ 9%)
  and quite significant with smaller number of layers (16 downto 10)

Summary

- The effect of guard ring, PCB thickness, dead pixel/chip fraction and number of layers were studied
- Guard ring affects JER linearly, ~6% @ 2mm
- With PCB thickness, no significant JER degradation observed (upto 2mm)
- 10% of dead pixels / 5% of dead chips have very little effect on JER
- ≤ 9% of degradation in JER if we choose to reduce number of layers from 30 to 20

<u>On going:</u>

- Radius and length optimisation