HV/HR-CMOS sensors

(A quick overview from personal perspective, which is biased on ATLAS strips work)

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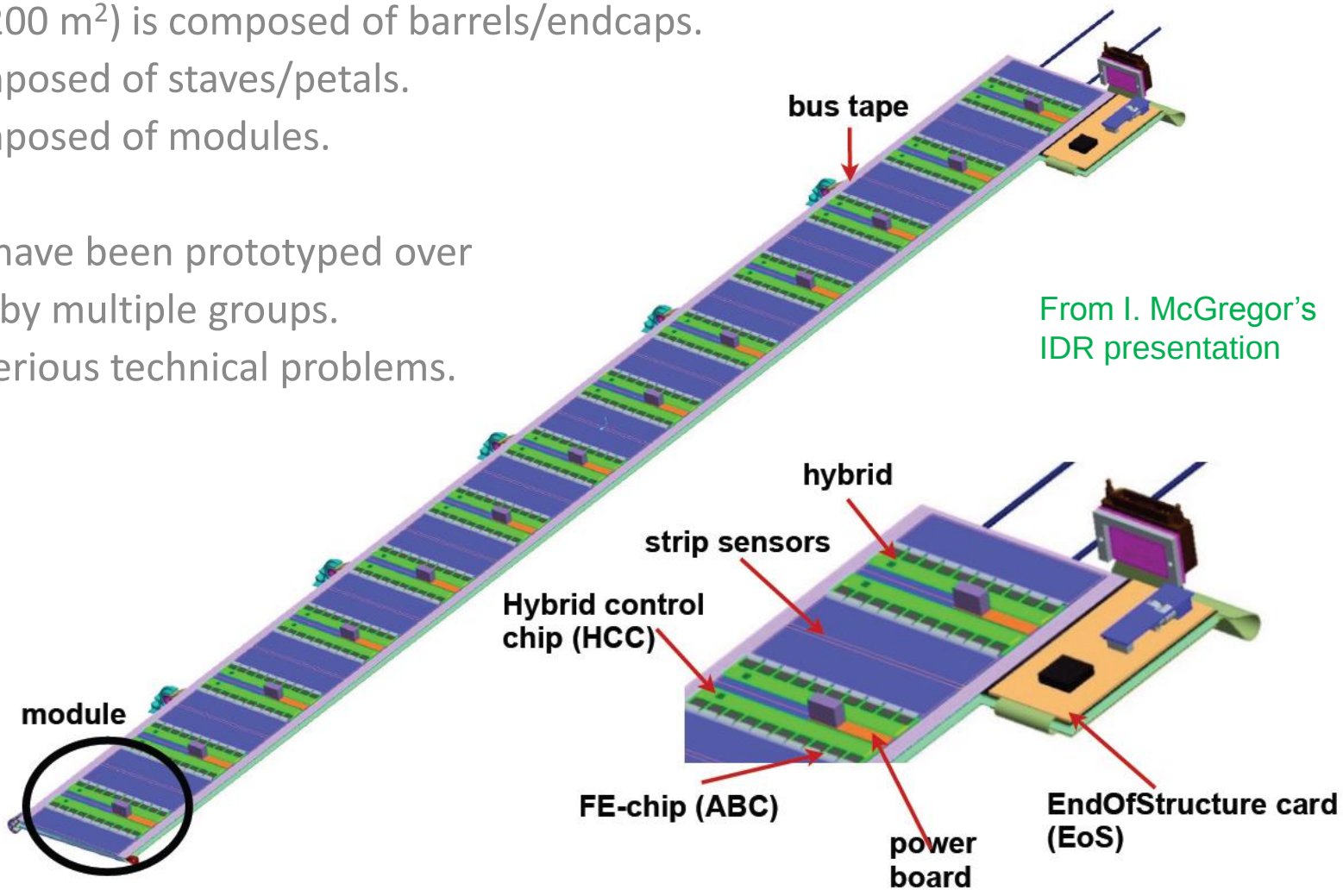
Outline

- Baseline ATLAS strips
- What is HV/HR CMOS
- Technology choices and options
- Recent tests
- Further work

Baseline ATLAS Strip Tracker

The tracker (~200 m^2) is composed of barrels/endcaps.
Which are composed of staves/petals.
Which are composed of modules.

These objects have been prototyped over last >= 3 years by multiple groups.
There are no serious technical problems.



From I. McGregor's IDR presentation

Baseline ATLAS Strip Module

A barrel module from last round of prototyping (with ABCN-250 chips).

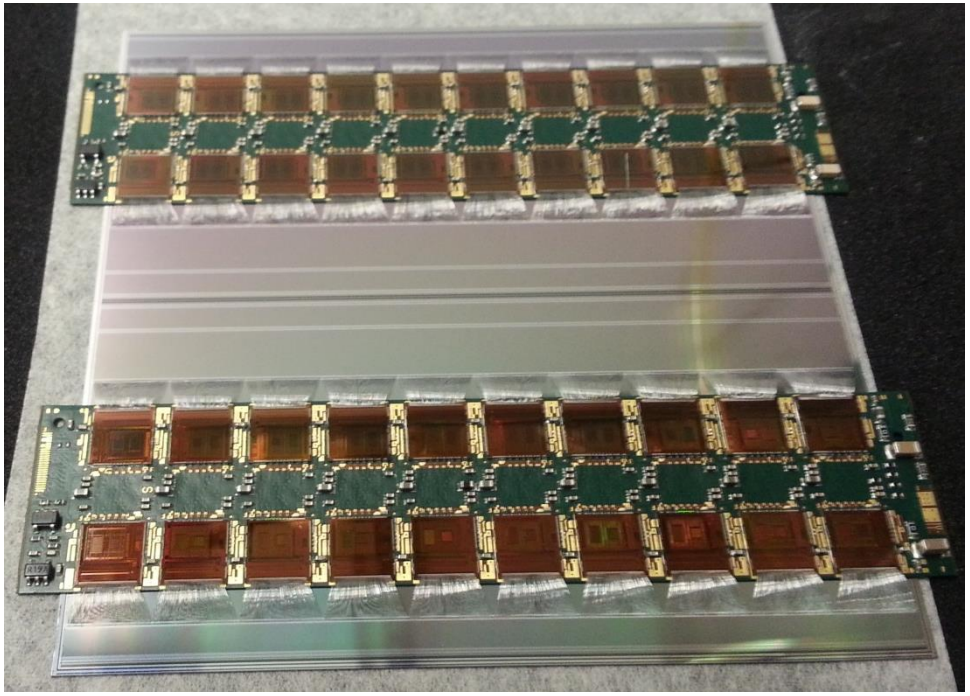
Traditional heterogeneous architecture:

- Separate sensors and readout ASICs.
- Precursor steps:
  - ASIC testing
  - Hybrid assembly and testing
  - Sensor testing.

Differences with current ATLAS SCT modules:

- n-on-p sensor as more rad-hard
- Single-sided module
- Single large sensor
- Direct gluing of hybrid on sensor
- More channels/module (and more modules in production)

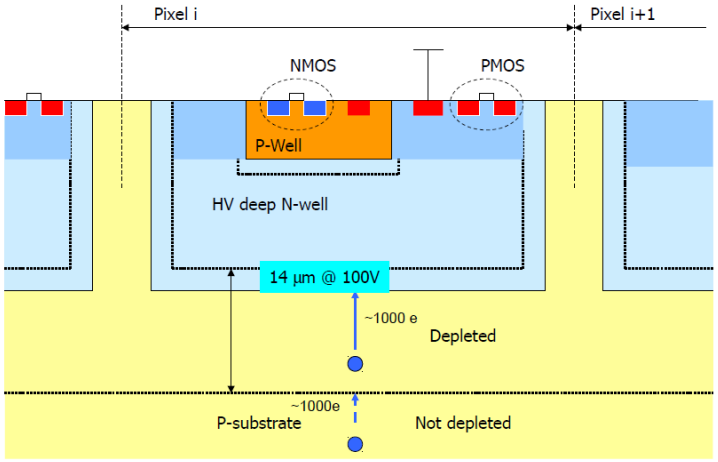
Next round of prototyping is imminent. It features new ASICs, ABC-130, with x2 channels/chip => half the chips and less hybrid area/material.



10x10 cm^2 sensor with 5120 channels; 40 ABCN-250 chips on 2 hybrids

What is HV/HR-CMOS

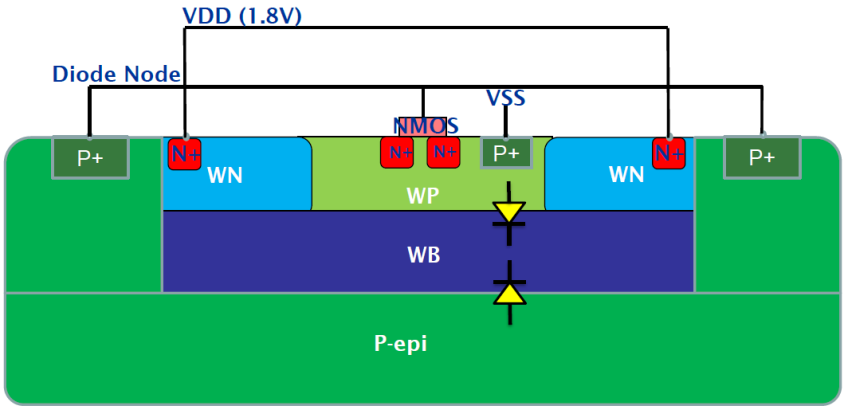
High-Voltage CMOS technology is a variation of standard CMOS process that is frequently used for power devices. Allows for higher-resistivity substrates and ~100 V bias.



CMOS electronics placed inside the diode (inside the n-well)

High-Resistivity CMOS was developed for imaging applications. Features high-resistivity thin epi layers one can take advantage of.

Bottom line: higher V(bias) and ρ than for commercial CMOS, although not as high as for what HEP is used to.



WN: Shallow N-well
WB: Deep N-well (~3µm)
WP: P-well

Two back to back diodes form between WP-WB and WB-Pepi!!

Projects within ATLAS

There are two projects within ATLAS evaluating HV/HR CMOS technologies:

- Pixel demonstrator project
- Evaluation for strip sensor

But there are also other possibilities being pursued to some extent:

- Additional outermost pixel layers
- Muon high-eta extension

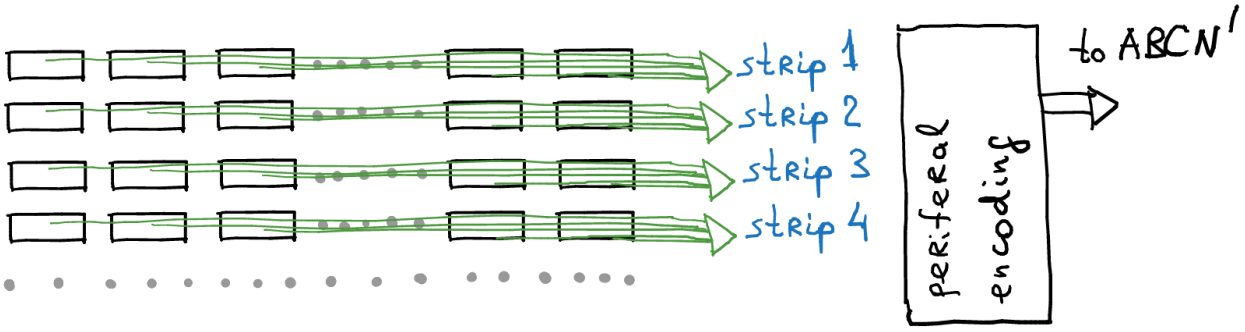
CMOS Strips Introduction

There are two circumstances that forced the current development plan:

- Promising results from HV-CMOS test chips.
- Upgrade schedule which calls for start of sensor pre-production in 3 years.

This lead to a very targeted exploration of the technology:

- A working group was formed that outlined most promising use of the technology as *sensor* replacement:
  - Could still have amplifiers and comparators on chip, but the rest of digital processing, command I/O, trigger pipelines, etc will go into (modified) ABCN.
  - Transmitting high-speed information instead of individual analog signals to readout ASICs.
  - Even though this is a strip system, the active area is *pixelated*, with connections to the periphery that result in longitudinal information.
  - Looking at ~40 μm pitch and 800 μm length of pixel region (better than 74.5 um baseline pitch and 40 mrad crossing angle).
  - Max reticle sizes are ~2x2 cm^2 => Looking into rows of 4-5 chips as basic units (yield performance is critical here).
  - This would take advantage of the rest of the mechanical/cooling/readout/power architecture of staves that was developed for the baseline program over past several years.
- R&D with two foundries is being pursued: AMS and TJ. (Pixel efforts have more, e.g. L-foundry.)



Benefits and Work Plan

Possible improvements compared to the baseline:

- Cost savings due to x2 less area and less cost per area.
- Faster construction due to fewer wirebonds.
- Less material in the tracker.

ATLAS agreed to explore the possible use of the technology, with 3-year plan:

- Year 1: Characterization of basic sensor/electronics properties and architecture
- Year 2: Fabricating and evaluating a large-scale device.
- Year 3: Full prototypes of sensors and ABCN' .

There is a review of progress at the end of each year (breakpoint).

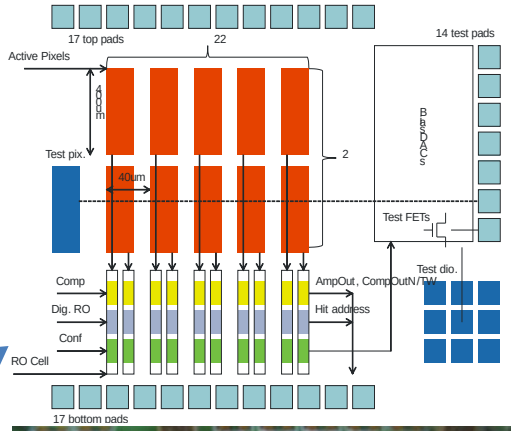
First Year Efforts

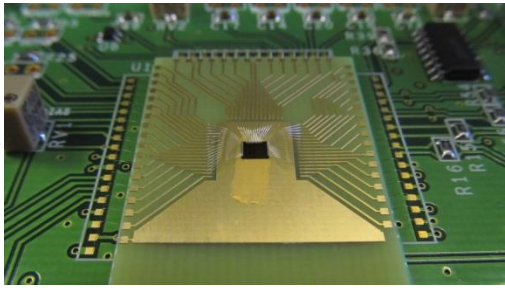
The goal of 1st year work is to understand the properties of signal (radiation tolerance, timing resolution, power, noise), pixel layout, and on-sensor readout architecture.

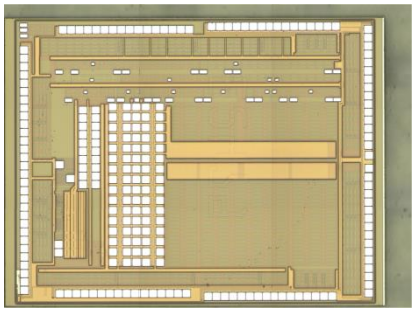
Had 3 chip submissions to figure out basic sensor properties:

- HVStripV1 by Ivan Peric (Karlsruhe/KIT)
- CHESS-AMS by H. Grabas et al (UCSC), A. Dragone et al (SLAC)
- CHESS-TJ by R. Turchetta et al (RAL)

There is a pending AMS architectural submission (SLAC/UCSC/Ivan Peric), to be submitted in March.







Transistors, amplifiers, passive pixel arrays, active pixel arrays

HVStripV1 Tests

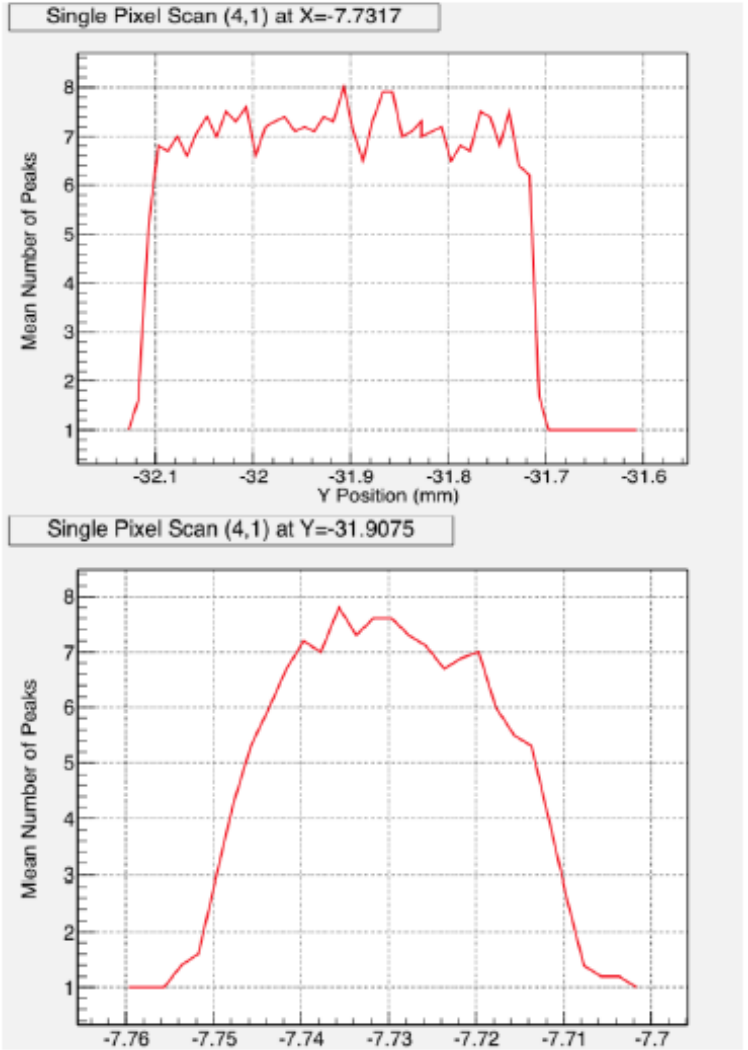
(Not meant to be exhaustive due to numerous on-going studies)

Pixel scan with focused X-rays at

Diamond Light Source:

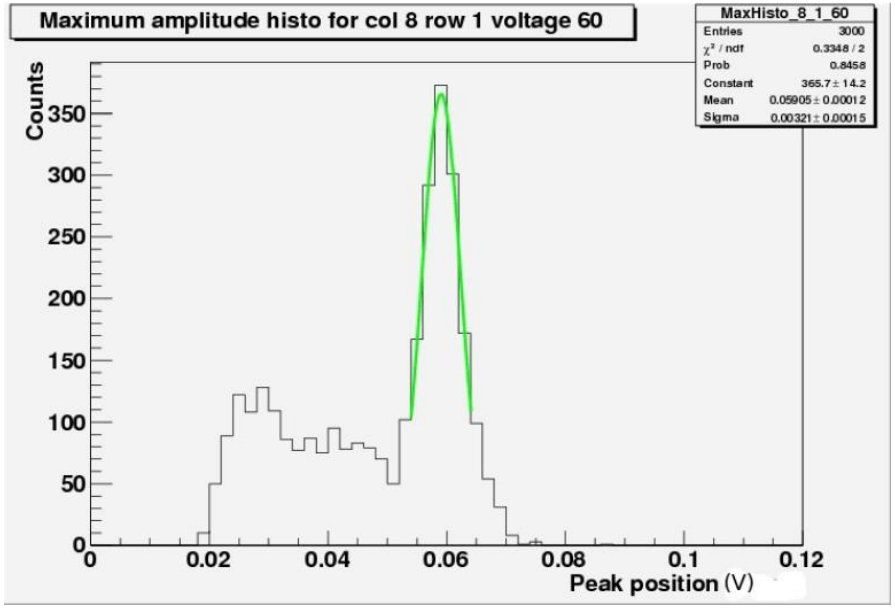
Observe pixel dimensions of

40x400 um^2

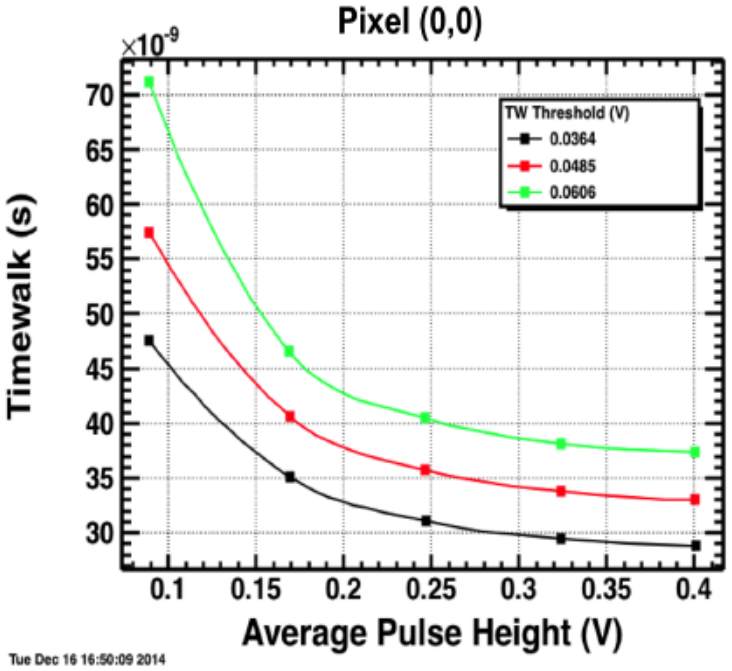


Study by Glasgow/Oxford/RAL/DESY

HVStripV1 Tests (Cont)



Fe-55 peak example

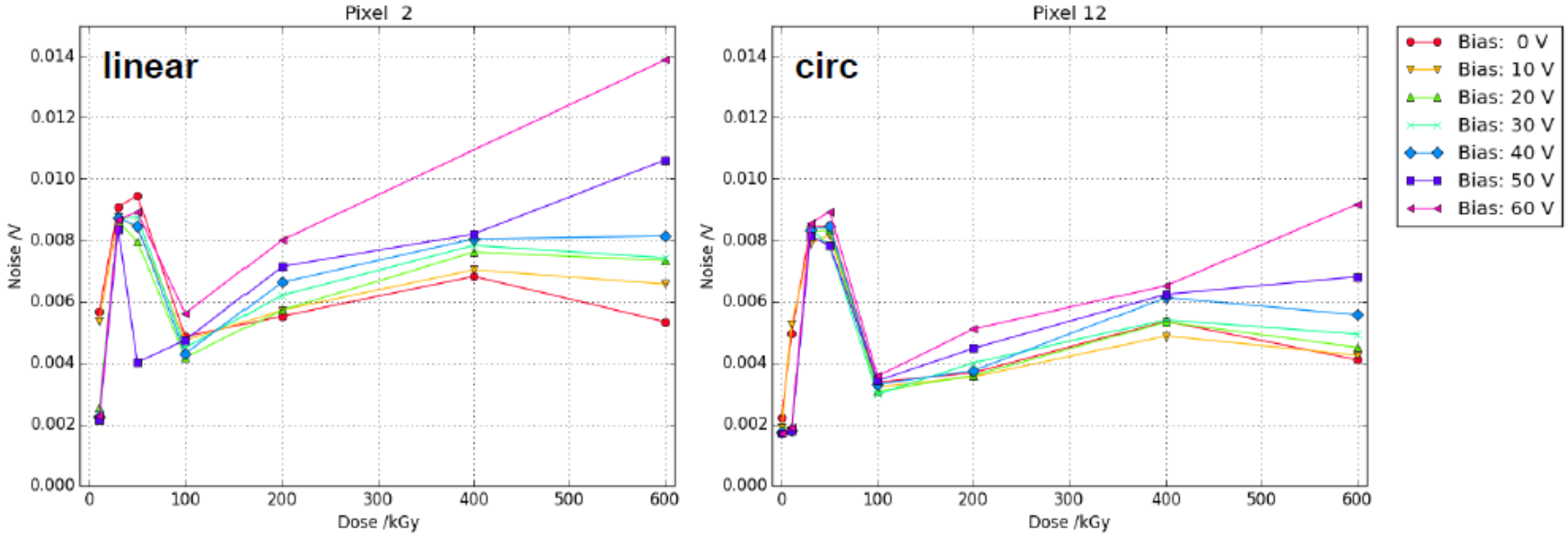


Timewalk study example

Studies by Oxford group
(work by L. Vigani)

HVStripV1 Tests (Cont)

Study of pixel noise dependence on ionizing dose



- Noise of pixels increases with dose at envisaged bias voltage

Studies by R. Eber et al (KIT)

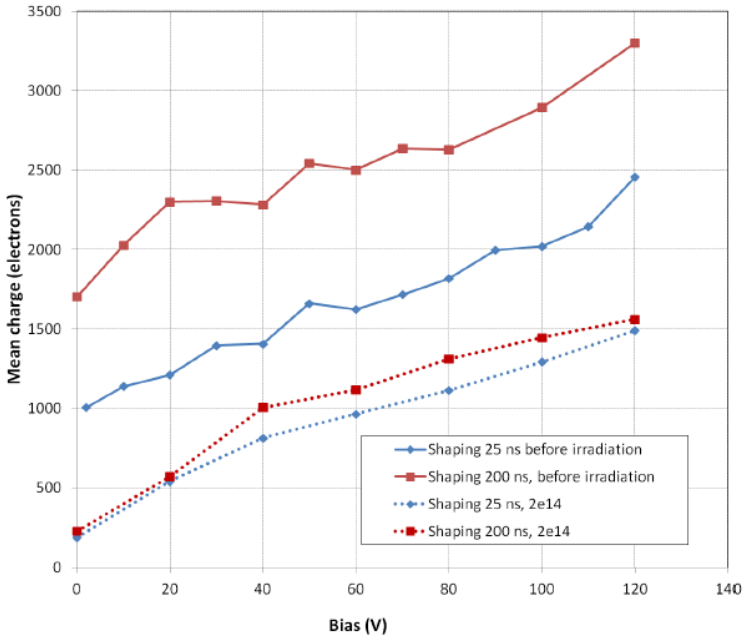
CHESS-AMS Charge Collection with Different Integration Time and Fluence

Measurements on passive pixel array (closest approximation to traditional sensor):

- Less charge at lower integration time due to presence of diffusion component before irradiation.
- Similar values afterward due to attenuated diffusion.
- Decrease at 25 ns int. time is also likely due to diffusion differences, although the onset of trapping is in principle possible.

The studies are continuing. Will be interesting to see results at higher fluence (spec for strips is 2e15 neq/cm^2).

- sample irradiated in TRIGA reactor in Ljubljana to equivalent fluence Φ_{eq} = 2e14 n/cm^2
- annealed at 60 C for 80 minutes



➔at 25 ns shaping about 35 % less charge measured after irradiation at high voltage
➔ small dependence on shaping time after irradiation ➔ small contribution from diffusion

Studies by Ljubljana group (I. Mandic et al)

Further Studies (short term)

The device evaluation is a very active program. The near term intended active studies are:

- Further Neutron Irradiation and charge collection (Ljubljana)
- Gamma Irradiation (UNM)
- Proton irradiation (Oxford, Birmingham)
- Beam tests (proton (Glasgow,Oxford,RAL), electron (DESY))
- Further IV/CV/pixel isolation (SLAC, UCSC)
- Transistors and radiation damage (RAL)
- Amplifiers and threshold matching (UCSC)

It's likely that people will do more!

Conclusions

HV/HR-CMOS technologies are a very attractive form of monolithic sensors.

ATLAS commenced R&D efforts to evaluate them for tracking.

Strip community is in the 1st year of the development, with promising results.

Of course, we'll have to clear several technological milestones to make CMOS sensors a reality for the experiment.

Reference Information

Not meant to be exhaustive, but rather to give leads to several efforts/foundry trials:

AMS: Peric et al, "High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments", NIM A 731 (2013) 131

TowerJazz: J. Crooks et al, "Kirana: a solid-state megapixel uCMOS image sensor for ultra-high speed imaging", Proc. SPIE 8659, Sensors, Cameras, and Systems for Industrial and Scientific Applications XIV

EPC: M. Havranek, T. Hemperek, et al, "DMAPS: a fully depleted monolithic active pixel sensor - analog performance characterization", http://arxiv.org/abs/1407.0641

XFAB: T. Hemperek et al, "A Monolithic active pixel sensor for ionizing radiation using a 180nm HV-SOI process", http://arxiv.org/abs/1412.3973

Workshop on Active Pixel Sensors for Particle Tracking (CPIX14), Bonn, September 2014, http://cpix14.org/