VIP ILC Vertex Chip Status Report

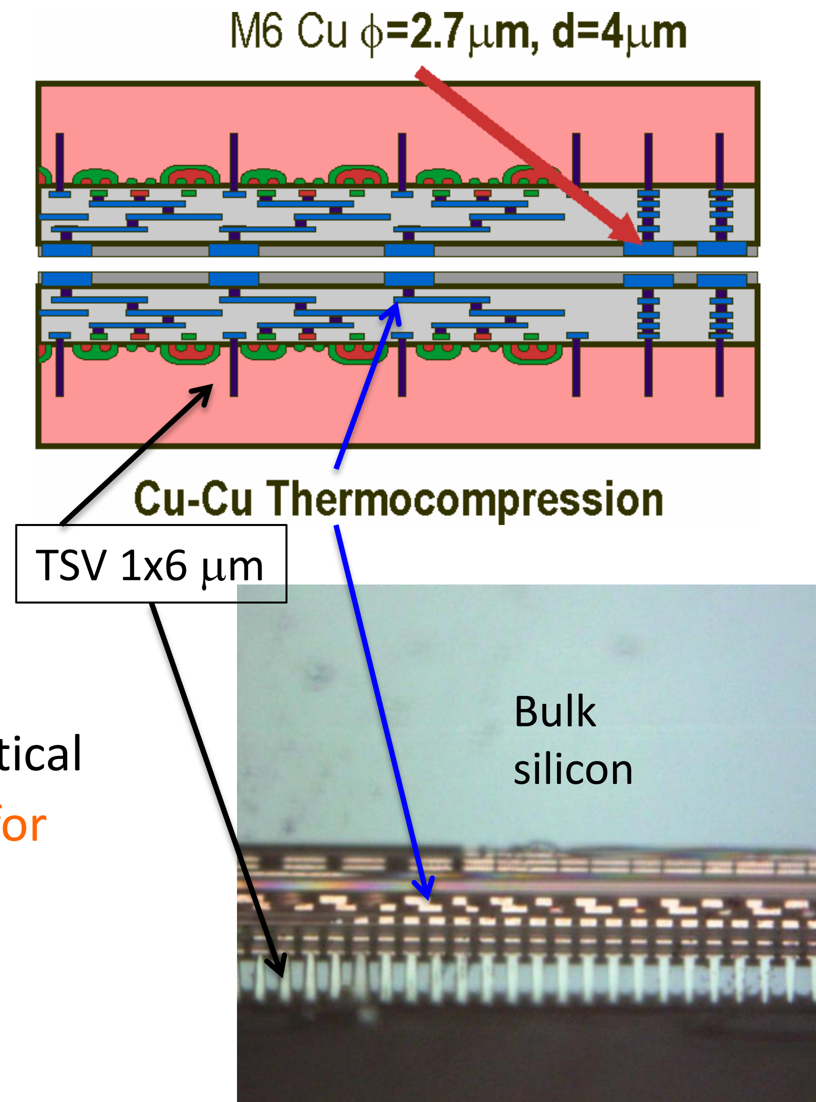
This talk will summarize the status of work to explore integration of sensors and electronics based on "3D" (multi-tier) technology for ILC.

- 3D Technology
- Processes and Designs
- Results of VIP (and VIPIC) chip testing
- Development of tiled arrays
- Conclusions

Presented by Marcel Demarteau
on behalf of Ron Lipton

3D Integrated Circuits

A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity.



Component Technologies:

- Through Silicon Vias (TSV): small diameter vertical connectivity - not only to build chips but also for attaching detectors to readouts
- Bonding: Oxide-, polymer-, metal-, or adhesive
  - Wafer-Wafer, Chip-Wafer or Chip-Chip
- Wafer thinning
- Back-side processing: metallization and patterning

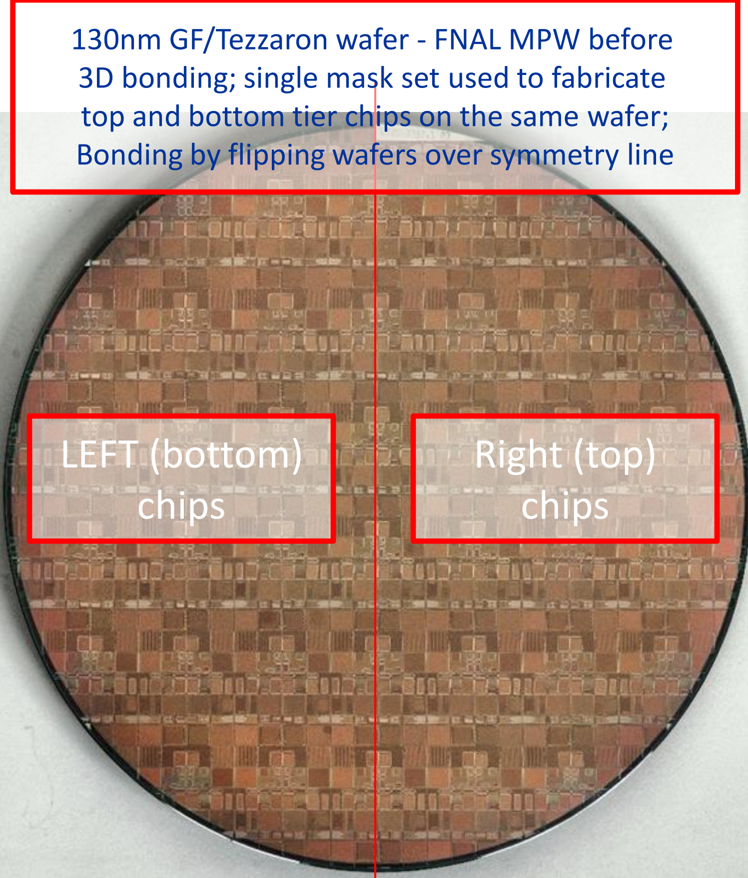
3D For Particle Physics

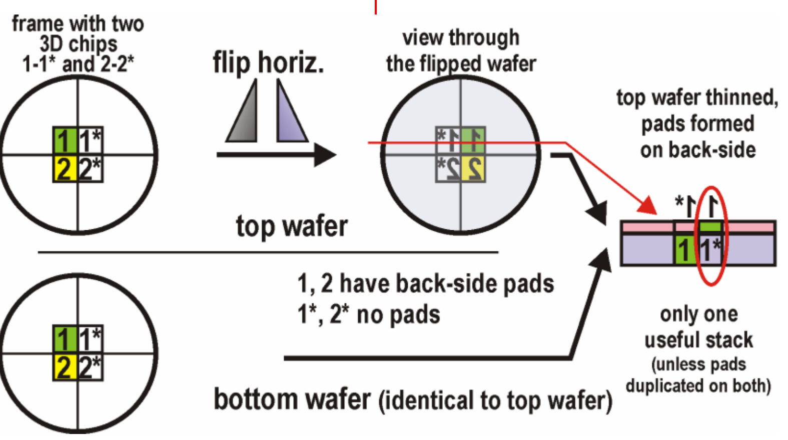
In HEP we care about bonding silicon sensors to complex analog/digital electronics. Technologies associated with 3D integration:

- Enable intimate interconnection between sensors and readout circuits
- Enable unique functionality with innovative circuit/sensor topologies
  - Separate digital/analog/ and data communication tiers
  - Multi-layer micro/macro pixel designs which can provide high resolution with minimal circuitry
- Wafer thinning enables thin, low mass, high resolution, and radiation hard sensors
- Bonding technologies enable very fine pitch, high resolution pixelated devices
- Commercialization of 3D and wafer-wafer bonding can reduce costs for large areas

‘Fermilab’ 3D-IC run

- 3D-IC Consortium established in late 2008, now 17 members; 6 countries: USA, Italy, France, Germany, Poland, Canada + Tezzaron
- Fermilab organized first 3D-IC MPW run for HEP
- Designs in: 05/2009; Chartered (GF) 130nm
  - Fermilab had a role of silicon broker
  - Many challenges in working with cutting edge technology: design mistakes, incompatibility of software tools (Tezzaron not Cadence), lack of 3D oriented verification, handling of databases , shifting foundry requirements (DRC), changing personnel at foundry, slow progress through fab etc.
- MPW frame accepted for fab in 03/2010
- Three FNAL designs: VICTR(CMS), VIP(ILC) and VIPIC(x-ray)

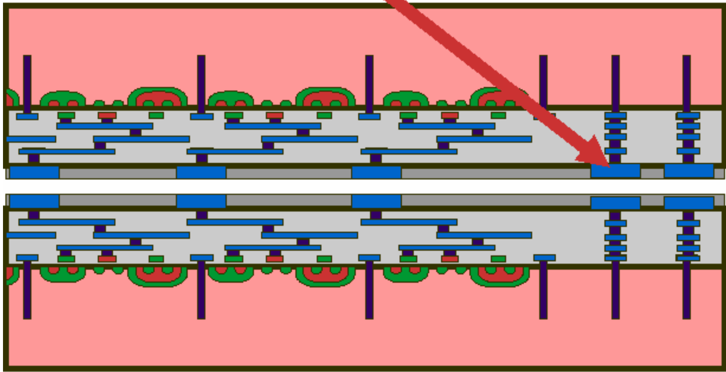




‘Fermilab’ 3D-IC run

Tezzaron / Novati

M6 Cu ϕ=2.7μm, d=4μm

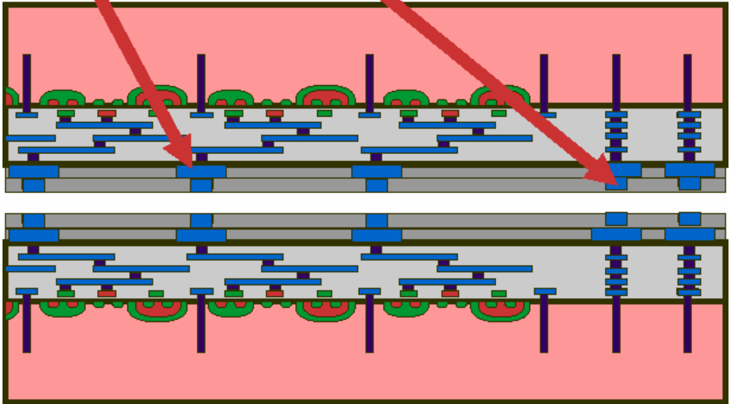


Cu-Cu Thermocompression

Ziptronix / licensed to Novati

M6 Cu ϕ=2.7μm, d=4μm

DBI Cu ϕ=1.2μm, d=4μm

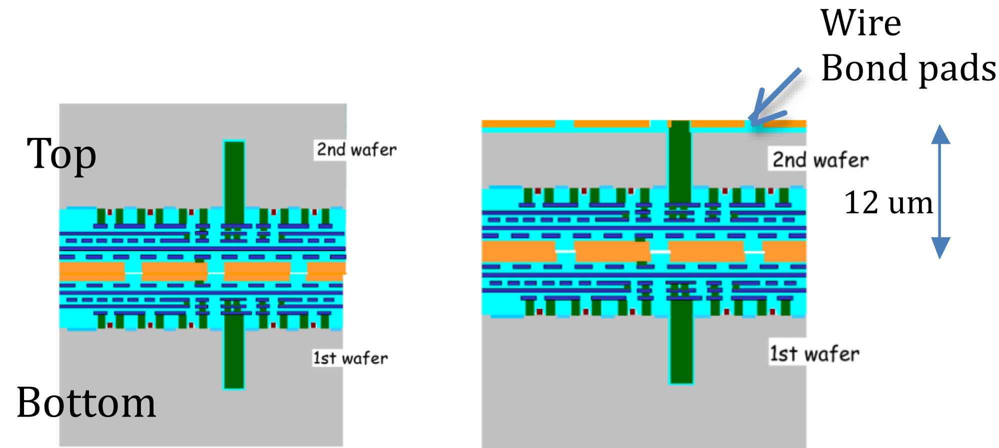


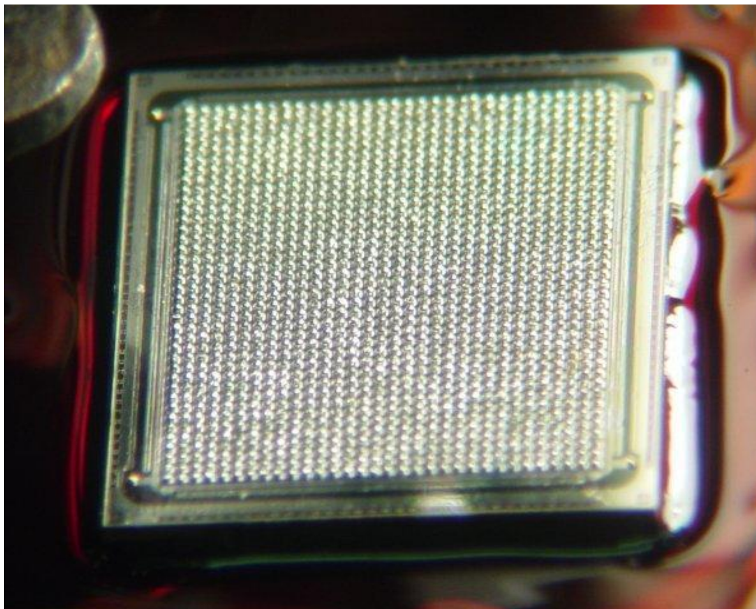
Cu DBI

- Difference between Cu-Cu thermocompression and Cu DBI wafer bonding methods:
  - Cu-Cu not reworkable, bonding established by fusing metal pads, forgiving on surface planarity
  - Cu DBI reworkable shortly after bonding, bonding established by chemically fusing oxide surfaces, must be ultra planar

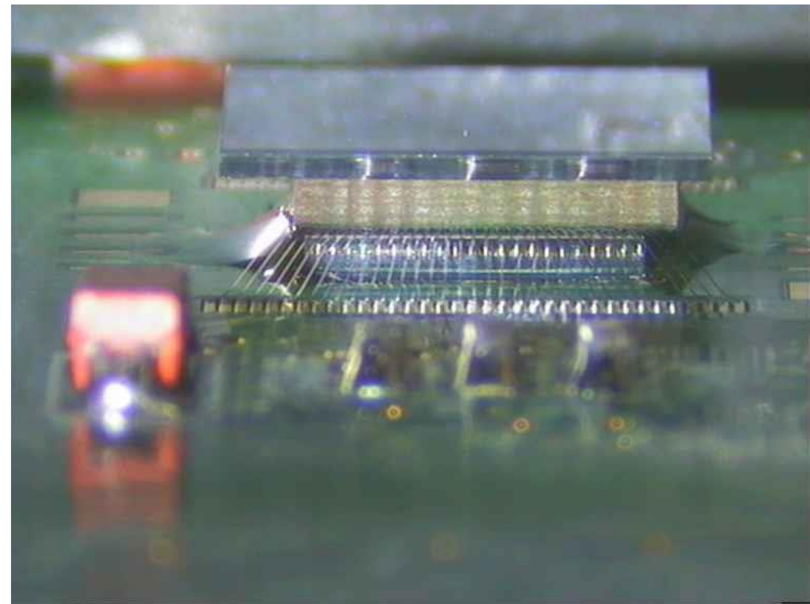
Two-Tier Devices

- Final two-tier face-to-face bonded wafers were delivered in 2013
- VICTR, VIP and VIPIC chips were tested, both bare and with bump bonded sensors (VIPIC).





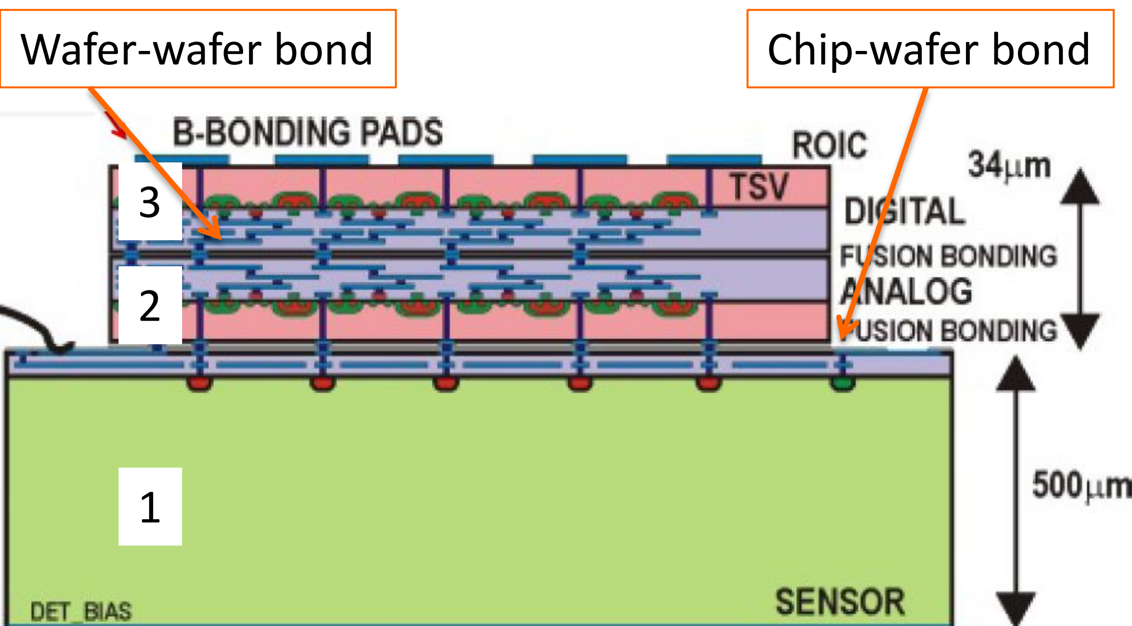
VIPIC with bumps

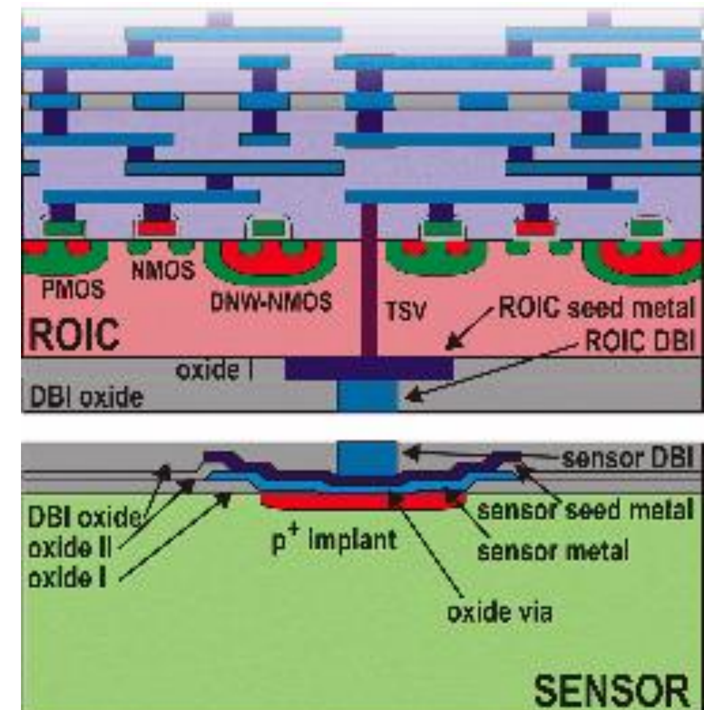


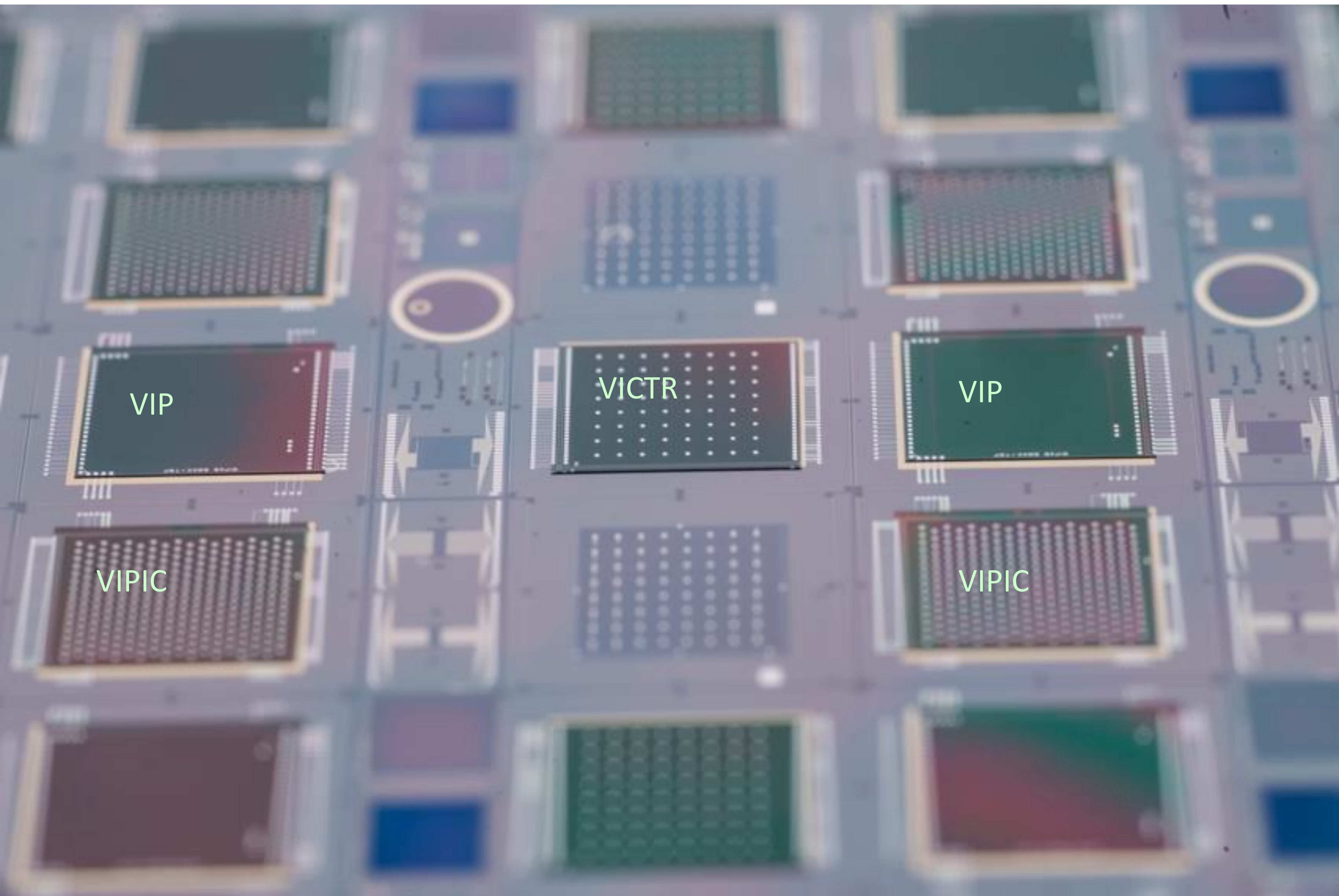
VICTR with top sensor and interposer

Sensor Integration –Three tier devices

- We then chip-to-wafer oxide (DBI) bonded 3D chips to BNL sensors to form three-tier integrated sensor/electronics assemblies – parts received in March 2014
  - VIP(ILC), VICTR(CMS), and VIPIC(X-Ray) assemblies






VIP
VICTR
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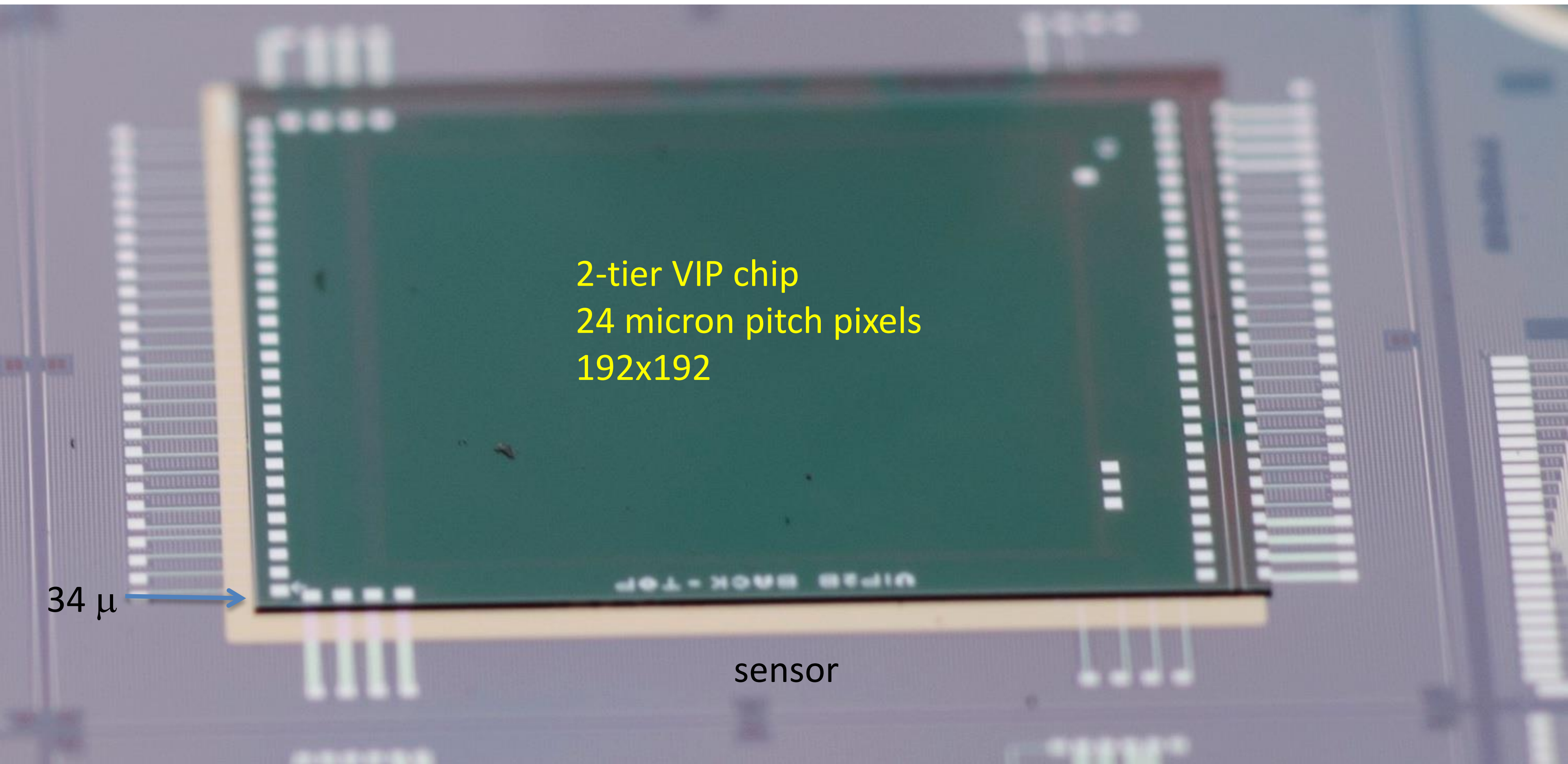
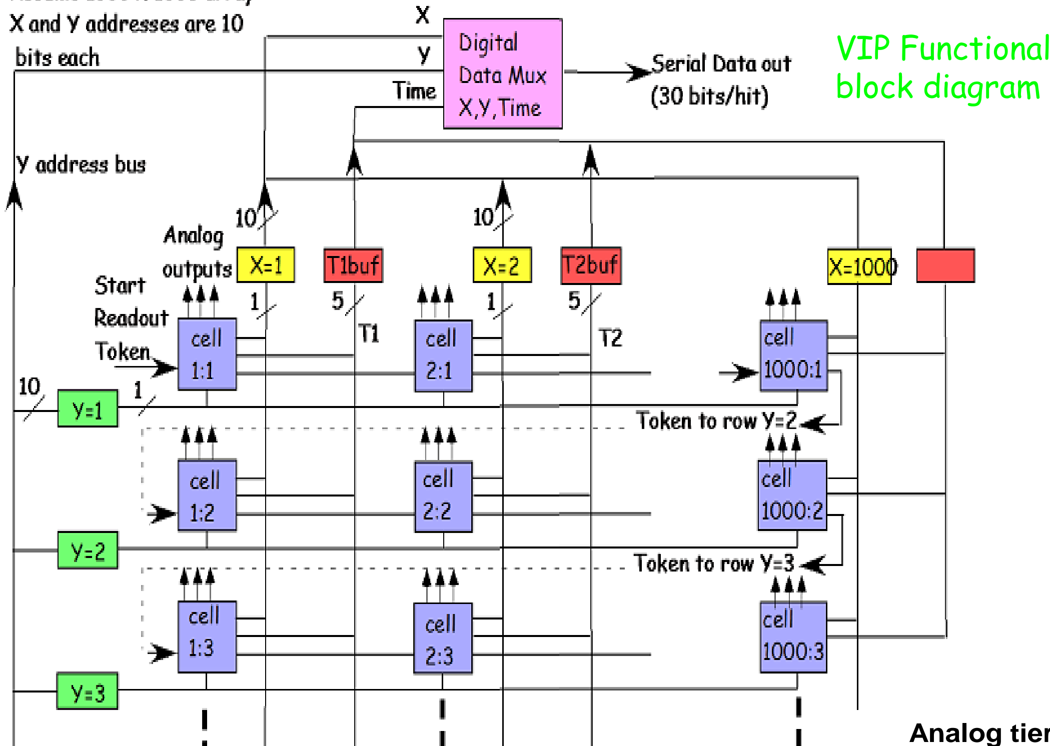
VIPIC

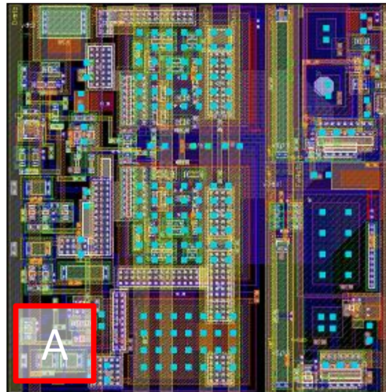
VIP

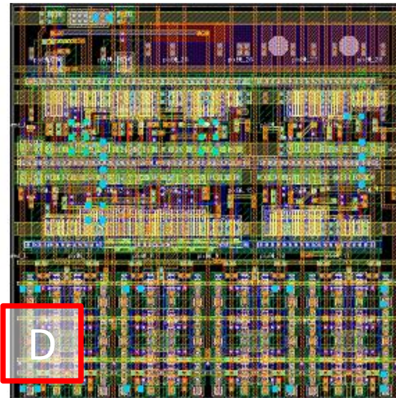


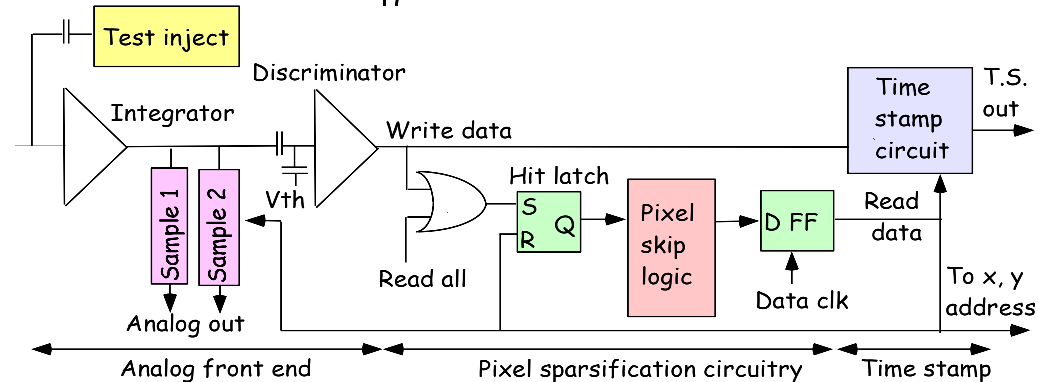
VIP2b ILC Vertex Chip



- **How it works:**
  - 192 × 192 array of 24x24 μm^2 pixels
  - 8 bit digital time stamp
  - Readout between ILC bunch trains of sparsified data
  - Sparsification - token passing scheme
  - Single stage signal integrating front-end with 2 S/H circuits for analog signal output with CDS
  - Analog information available for improved resolution
  - Serial output bus
  - Polarity switch for collection of e^- or h^+







VIP Testing

- Successfully read out all 192x192 = 36,864 pixels
- Token passes through at 189 ps/pixel
- Sees sources
  - noise is not yet carefully measured
  - Time stamping appears to work
- Issues with test pulse masking, odd/even threshold – basically, the chip works well

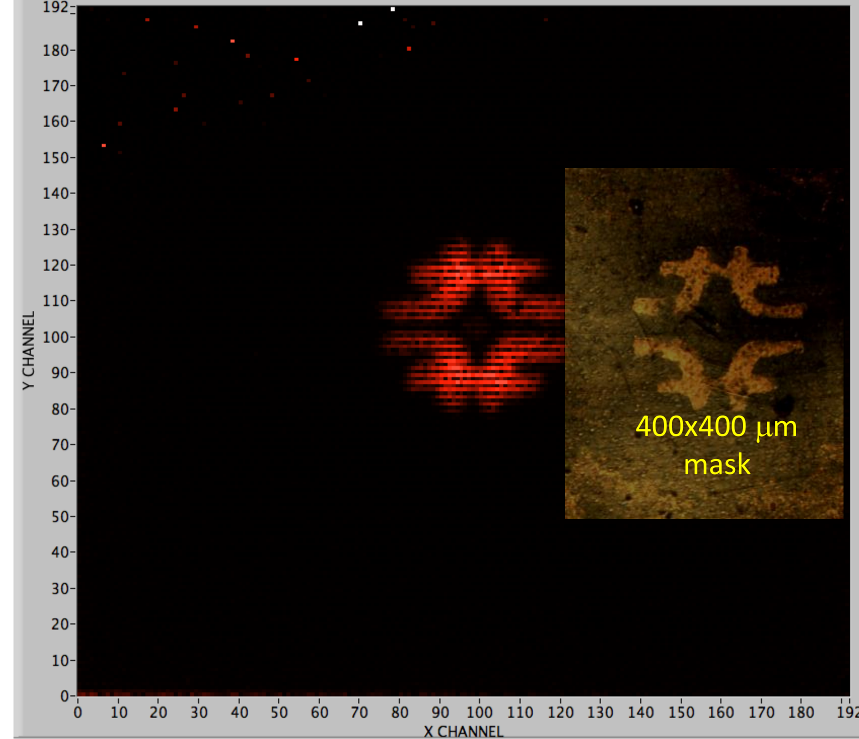
Showing preliminary functional tests now – limited bias voltage – being conservative in initial tests

Collaborators

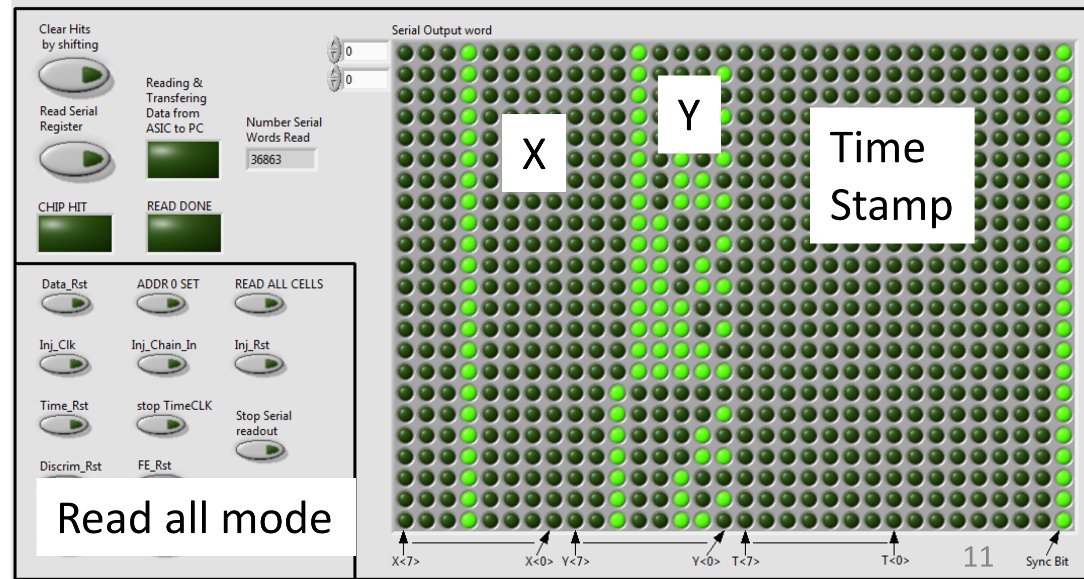
Brown University

Argonne Laboratory

Beam test this summer?



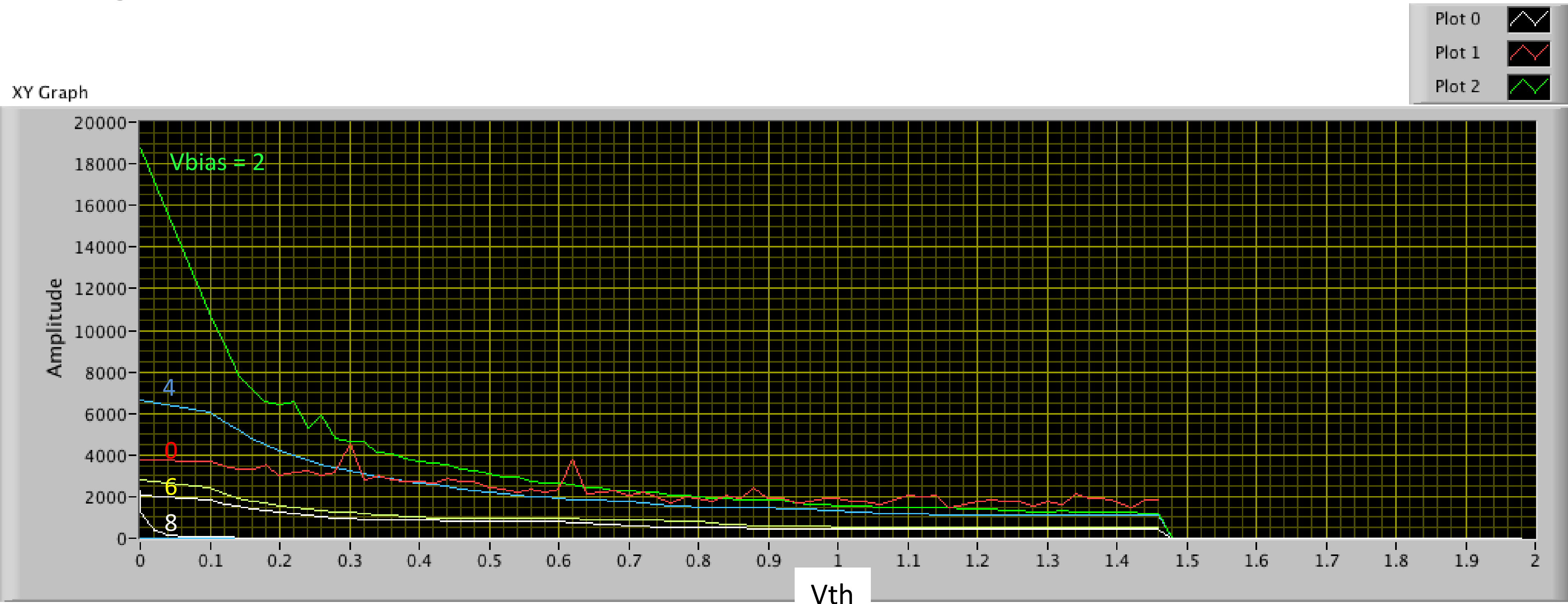
^{109}Cd (~20keV γ) radiogram of tungsten mask



VIP Noise Scans

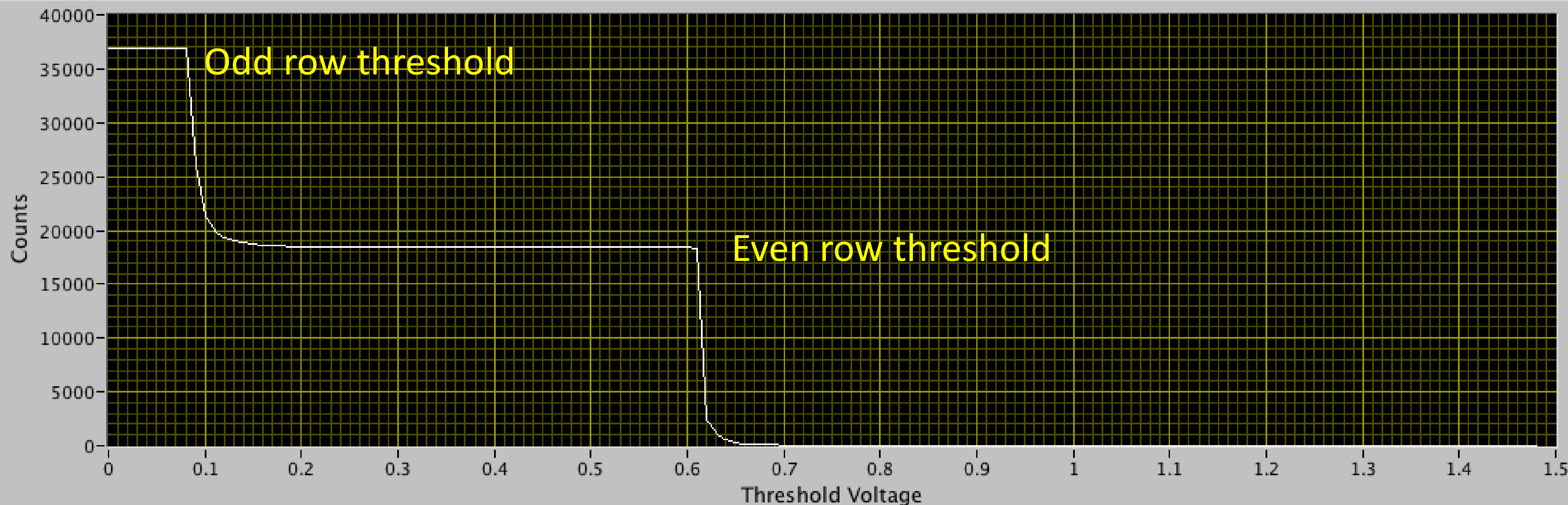
The number of counts versus threshold was measured as a function of bias voltage. There appear to be edge effects which cause noisy channels at the edge of the array. This disappears by V_{bias} = 10V. Full depletion of the 0.5 mm BNL sensor should be about 160V.

The expected decrease in noise occurs after the 0V point (which has anomalously high currents).



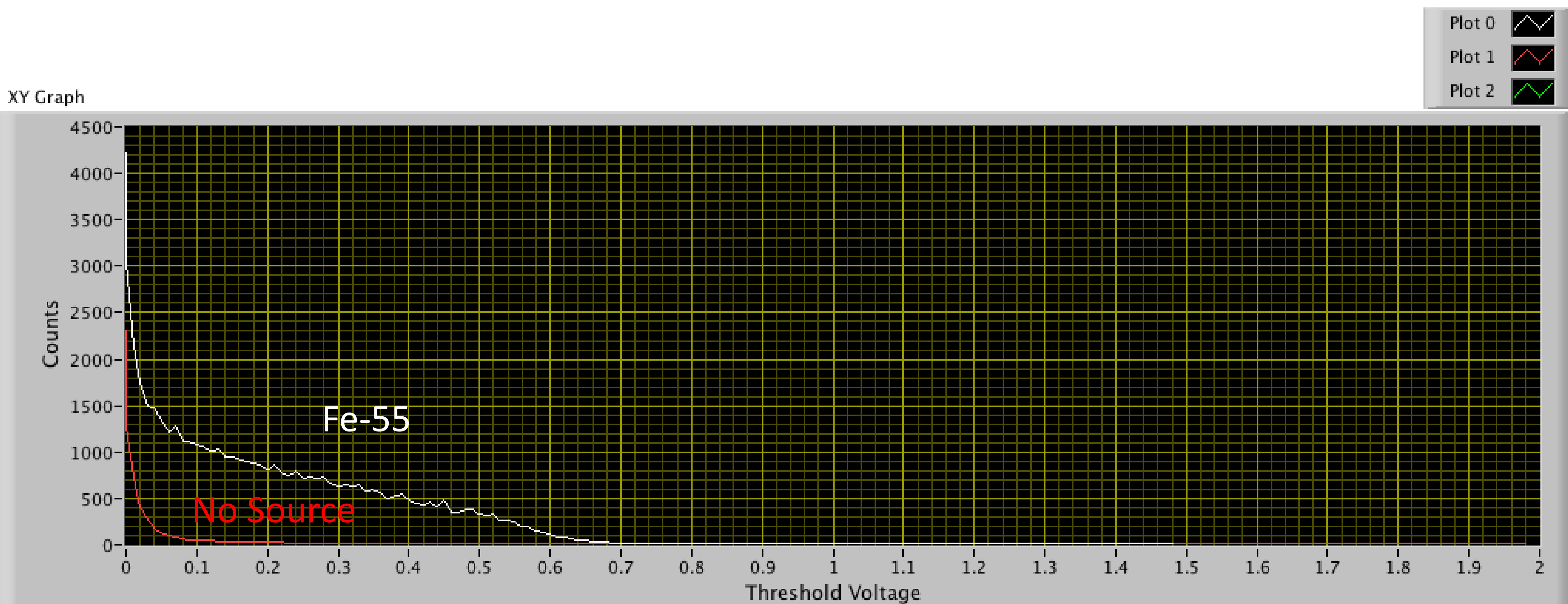
VIP Threshold Scans

The number of counts vs threshold was measured for a bias of 10 V for a constant charge injection value of 0.1 V. Two thresholds can be seen, for the odd and even rows of the device. This is also seen in source images. Threshold is set by a charge injected into the disc. Input – this implies some capacitance differences between odd and even rows.



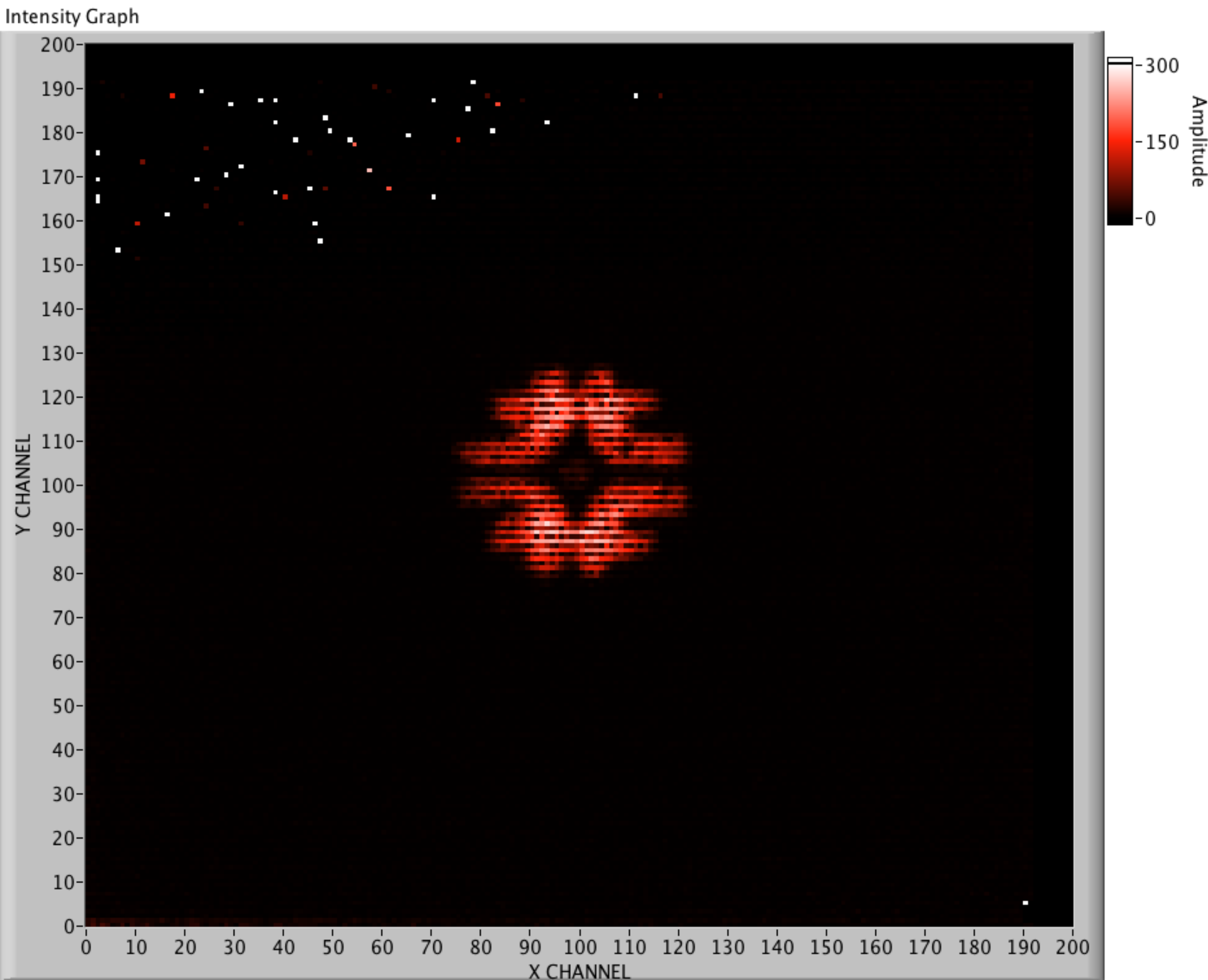
VIP Source Tests

Threshold scan with Fe-55 source. Vbias=10. The threshold is not clean due to low bias and resulting charge sharing among pixels as well as the odd/even threshold difference.



Tungsten mask

400 x 400 micron tungsten mask. Cd^{109} source only channels with <1000 counts/pixel plotted (this removes noisy pixels in unbonded top left corner)



VIP Work to do

- Understand source of odd/even disparity and non-functionality of injection masks
- Test at full depletion
- Test analog sample/hold output
- Measure noise for odd and even channels
- Measure threshold uniformity
- Measure resolution in beam tests

Some of these need to be done channel by channel (for 192x192 channels)

Note: the device works !

Large Area Arrays

We have demonstrated new technologies for chip and sensor interconnect.
For wide applicability we need to address yield, cost and commercial access.
The goal is inexpensive, large area, fine pitch pixelated systems.

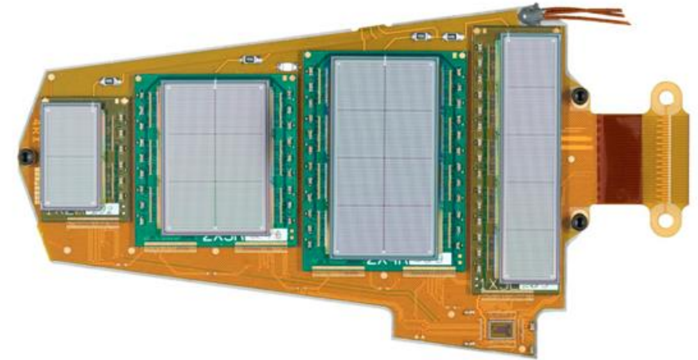
Such systems will be important (crucial) for many applications in HEP, x-ray imaging and Nuclear Physics.

Options:

1. Use the fact that wafer-scale sensors can be fabricated with good yield and bond an array of smaller readout chips to a large sensor
   - Interconnect geometry is a central issue
   - Placement yield limits utility for 3D
2. Fabricate tiles from wafer-wafer bonded devices which can be butted on all four sides to fabricate arrays of arbitrary size.
   - Avoid yield losses and labor in chip-wafer bonds
   - Yield is no longer ε^n

Combining the two 3Ds

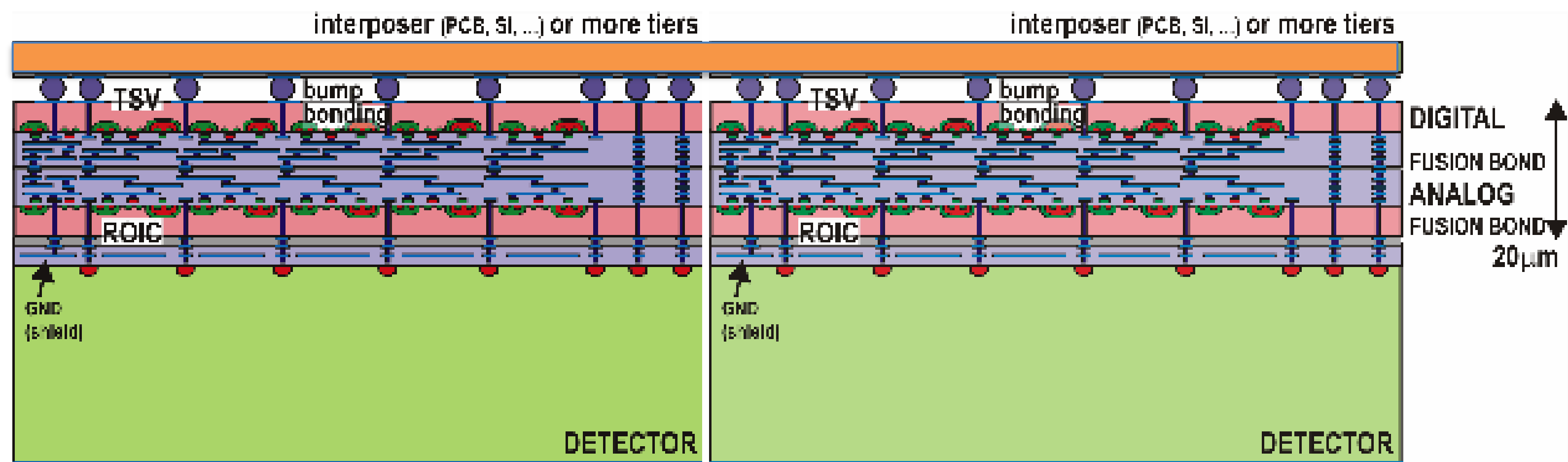
CMS FPIX Plaquette



Goal: Low cost, large area, thin, pixelated sensor planes with no dead regions.

Decouple bond and array yields

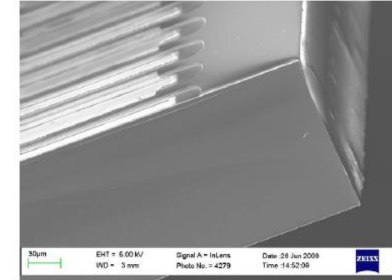
- 3D provides backside interconnect to eliminate peripheral bond connections
- Sensors can be processed to have “active edges” using deep reactive ion etch so assemblies can be tiled.



R. Lipton

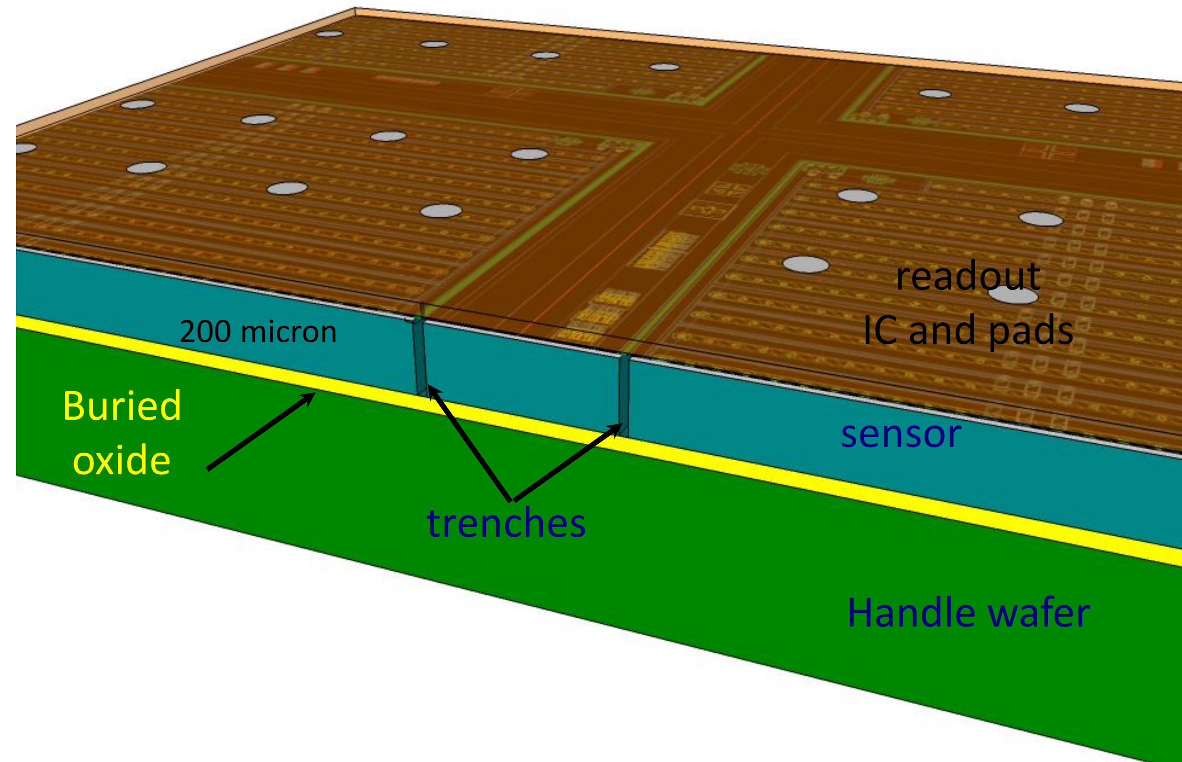
How can we do it with 3D?

VTT Active Edge sensor



Combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.

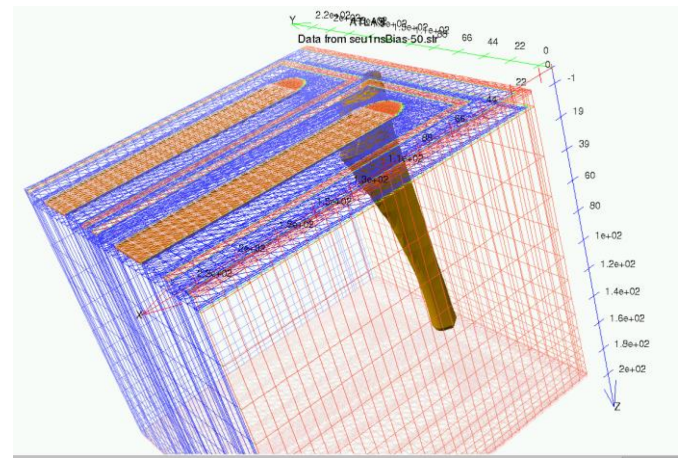
- These tiles can be used to build large area pixelated arrays with good yield and reasonable cost
- Tiles can populate complex shapes with optimal tiling and low dead area
- Only bump bonds are large pitch backside interconnects
- High density and geometrical flexibility



Demonstration Project

A project to demonstrate this technology is underway using:

- active edge sensors from VTT, based on early CMS long/short strip PS
- module designs
- Dummy ROIC wafers from Cornell



Simulation of charge density due to 3.5GeV muon hitting near the edge- study charge collection and edge effects.

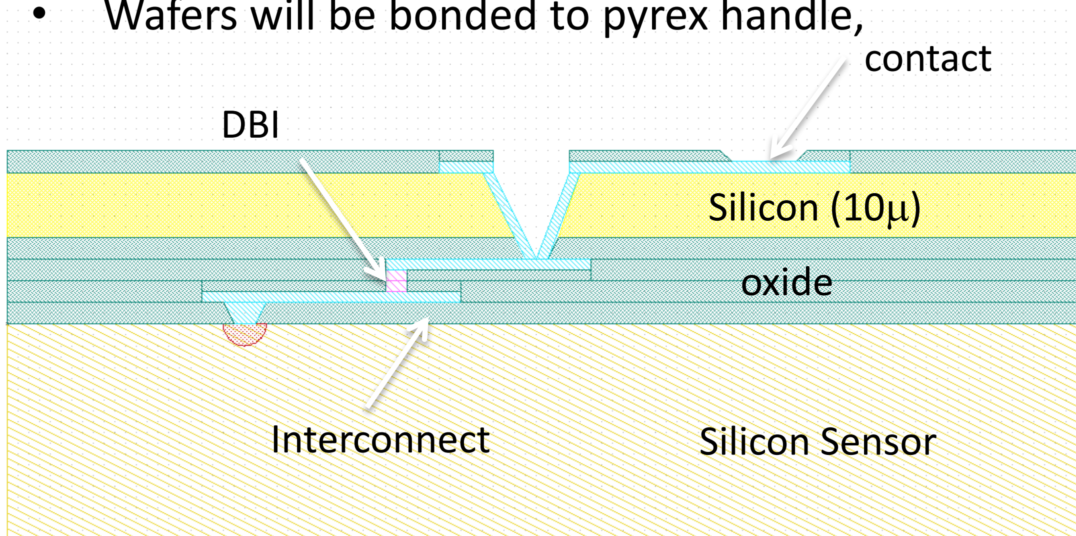
The two have been wafer-wafer DBI bonded by Novati .

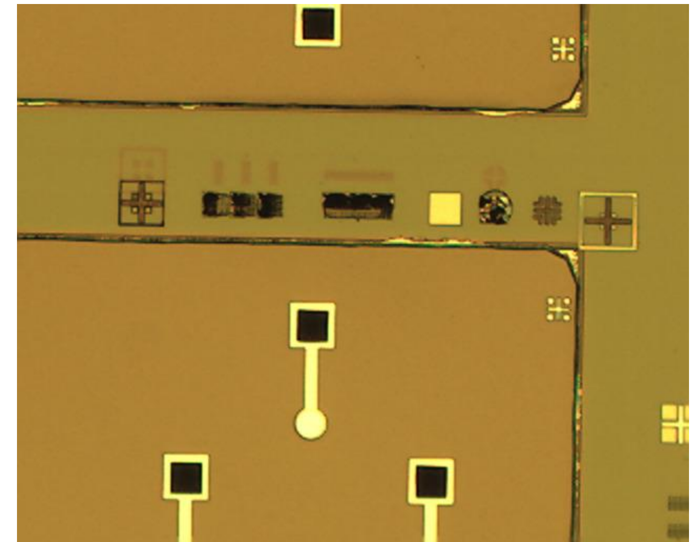
Note that the top contacts are revealed by etching thinned silicon, not TSVs

Active Edge/3D Combination

Status of the demonstration project:

- Active edge wafers fabricated at VTT
- Dummy ROIC wafers fabricated at Cornell
- Etching tests at SLAC to singulate die
- Etching tests at NIU to remove handle
- Wafers bonded, dummy ROIC wafer thinned to 10 microns, metal exposed and top contacts patterned at Novati
- Wafers now at SLAC for singulation etch
- Wafers will be bonded to pyrex handle, most of the silicon handle removed, and etched at NIU
- Die will be bumped onto a PCB, connected to an APV readout system and tested in the Fermilab test beam

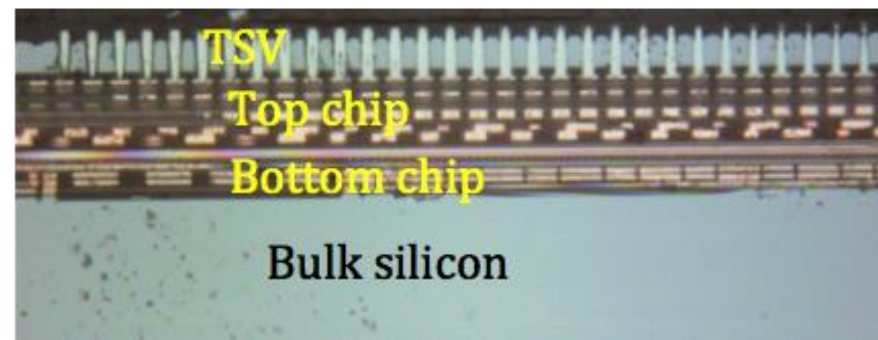




Summary

- We are now able to use 3D technology to combine optimal sensors and readout without many of the compromises inherent in other technologies
- We have demonstrated a commercial process for:
  - 3D wafer-wafer bonding and post processing of two layers of commercial 0.13 micron electronics with 4 μ pitch
  - Chip-to-wafer oxide bonding to sensors with 25-80 μ pitch
  - Reduced noise relative to bump bonding
- We are studying the extension of these technologies to large area devices by combining active edge devices with 3D electronics

3D Process Development

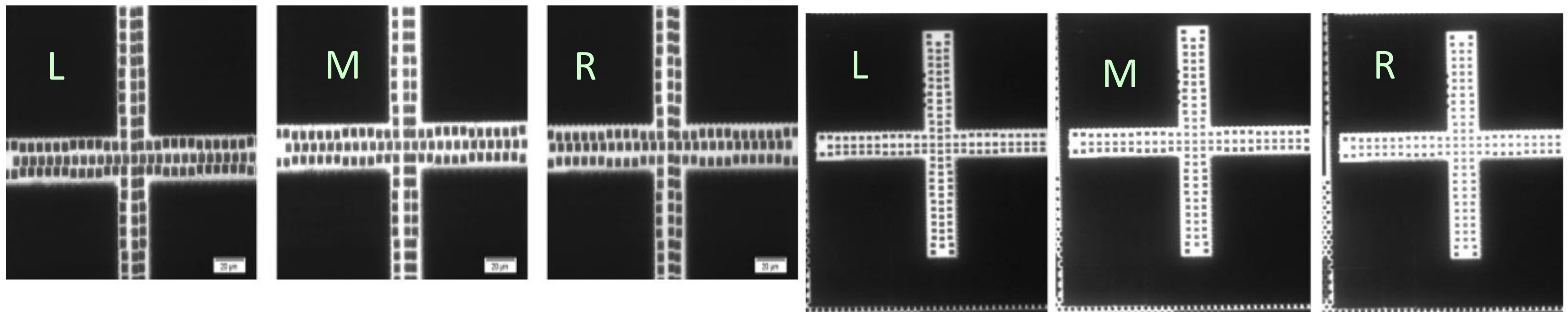


Misaligned Bond Interface in Cu-Cu bonded wafer

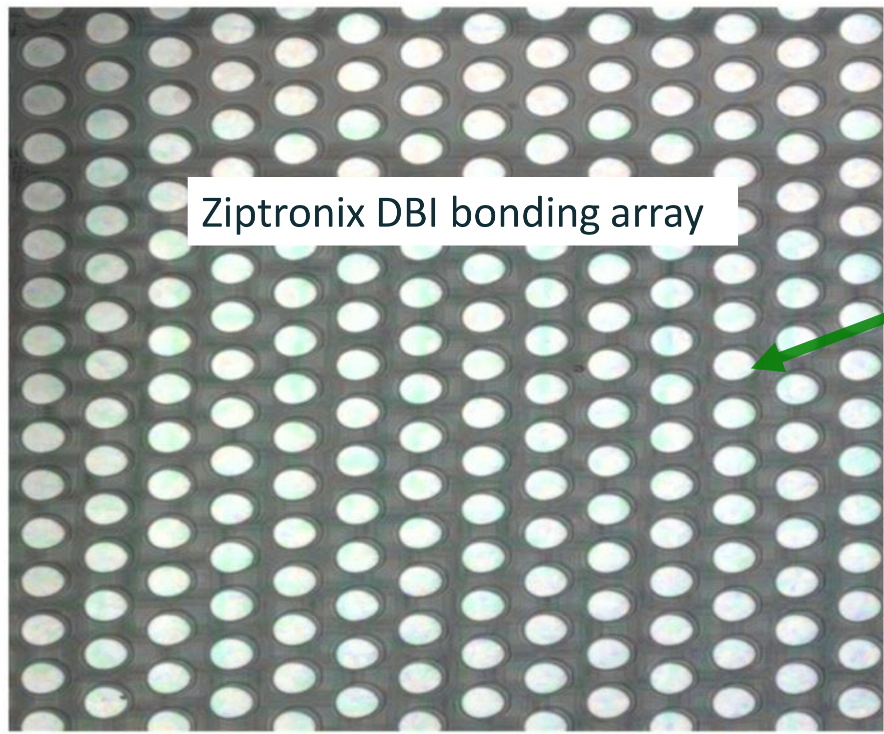
The original Cu-Cu thermocompression bonding technique developed by Tezzaron had several issues:

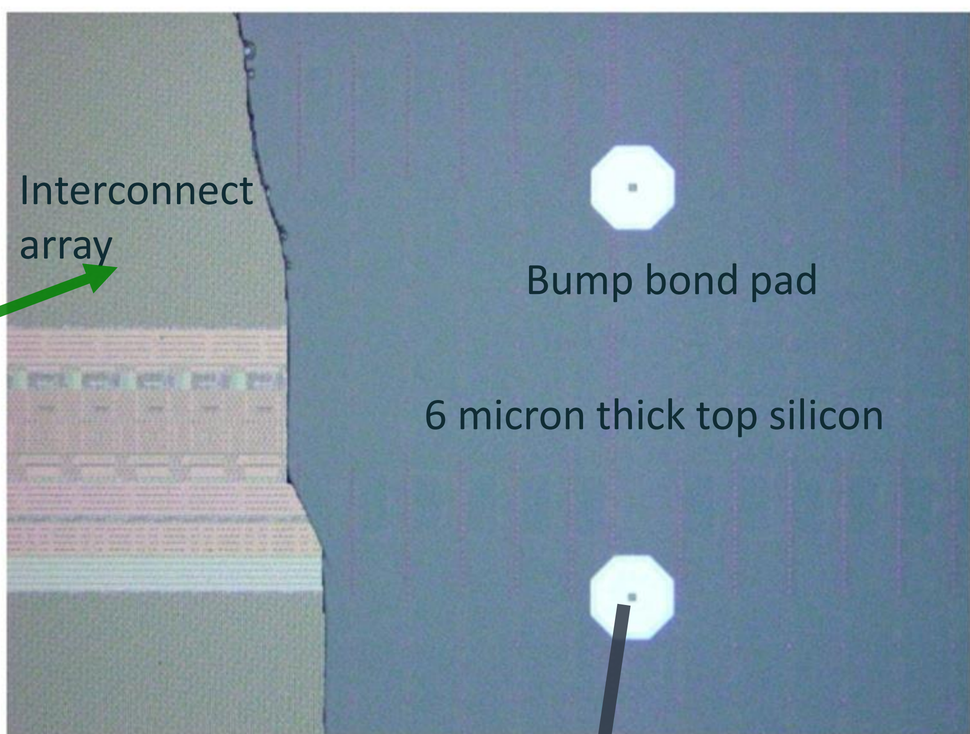
- Aging of top copper
- Wafer misalignment
- (Too) Aggressive design rules - 2.7 μm octagons on a 4 μm pitch
  - alignment between wafers must be better than 1 um

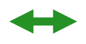
The DBI-oxide bonding process solved these problems.



Cu-Cu **Alignment Keys** DBI

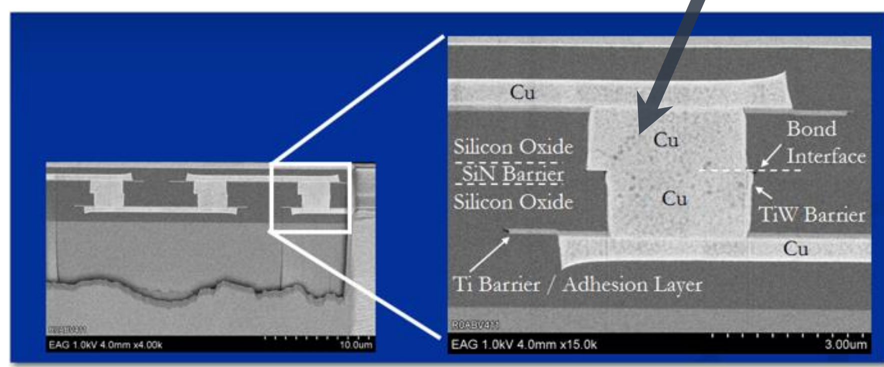


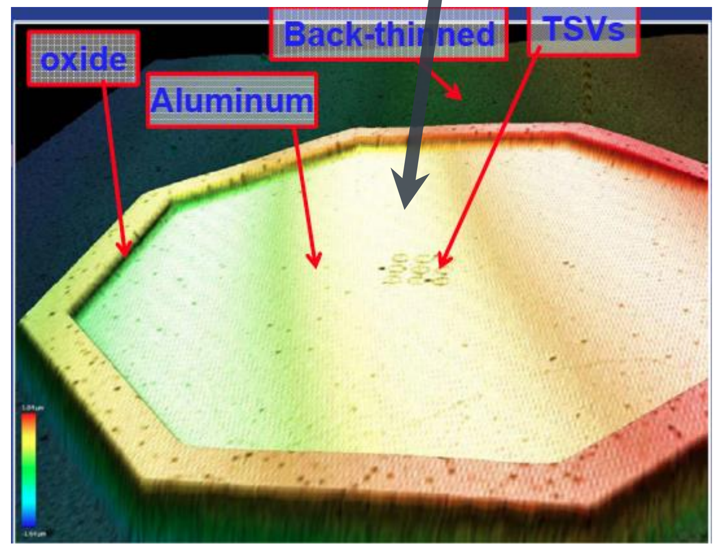




4 micron pitch

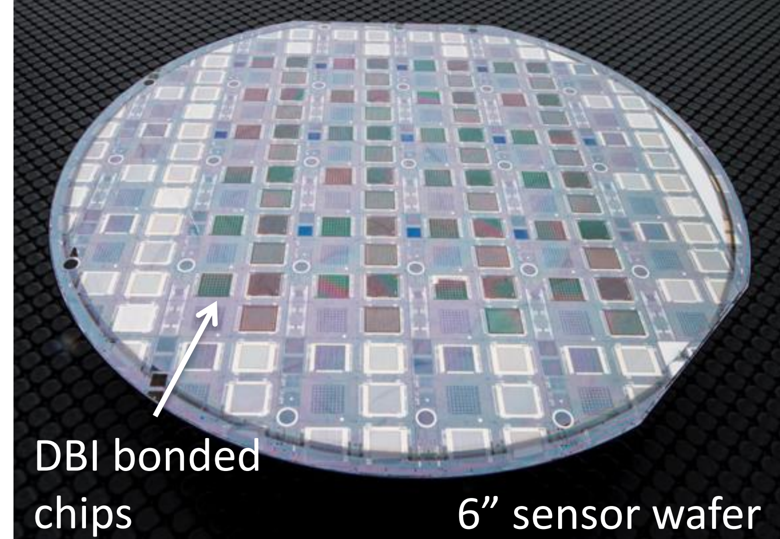
DBI Copper pillars



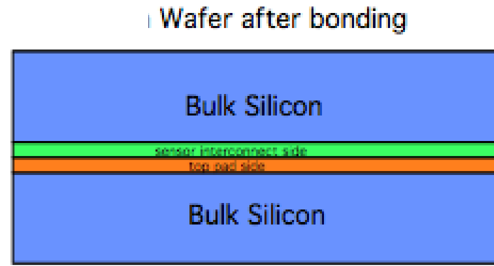


Chip-to-Wafer bond

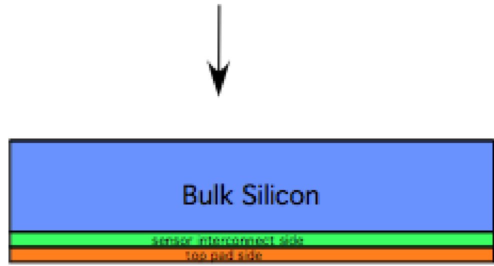
DBI bonding of ROICs (VICTR, VIPIC, VIP) to BNL sensor wafer



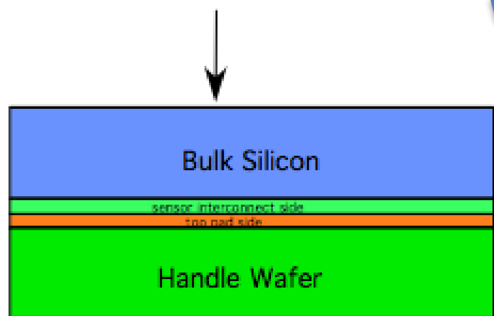
Wafer after bonding



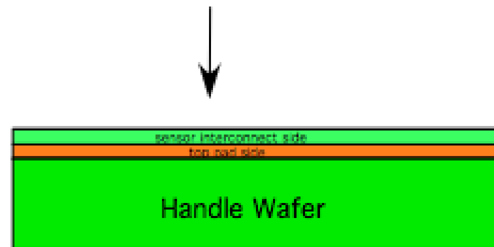
Wafer-wafer 3D Bond



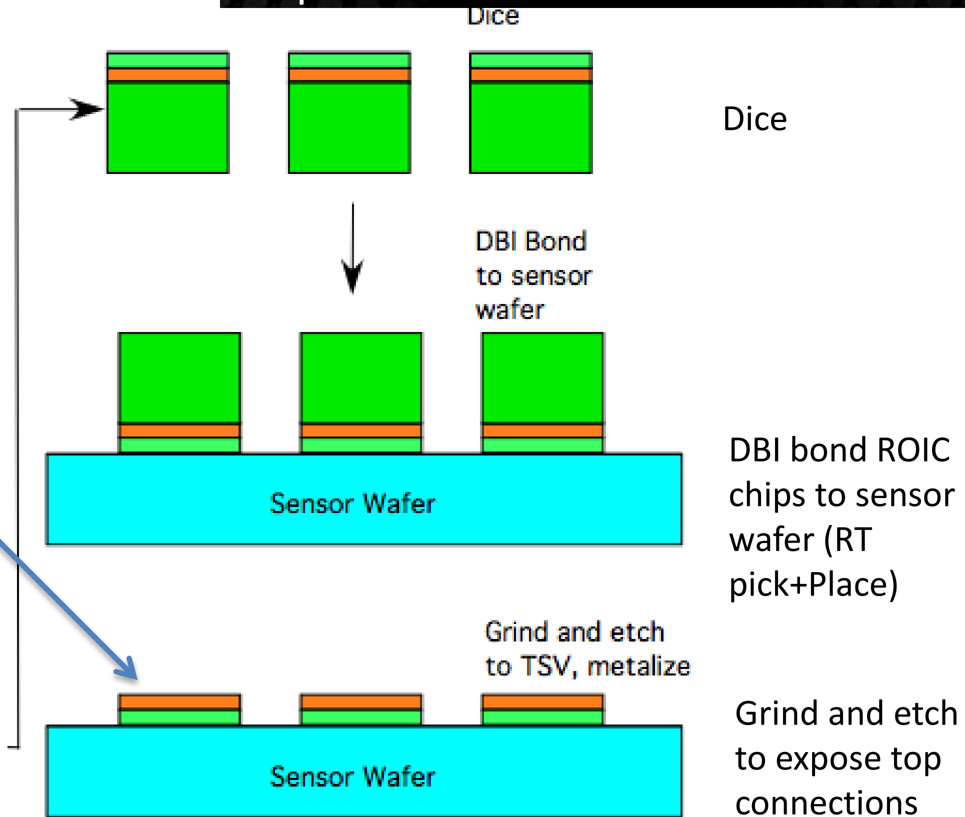
Expose TSVs, pattern Top aluminum



Oxide bond Handle wafer



Expose sensor side TSVs, pattern DBI structures



Dice

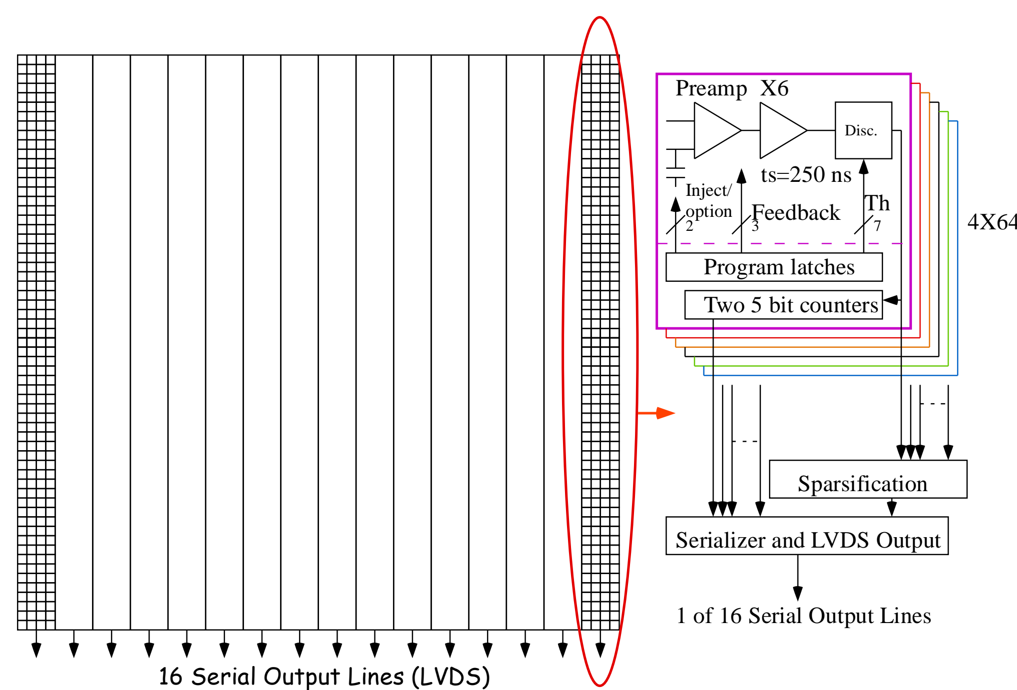
DBI bond ROIC chips to sensor wafer (RT pick+Place)

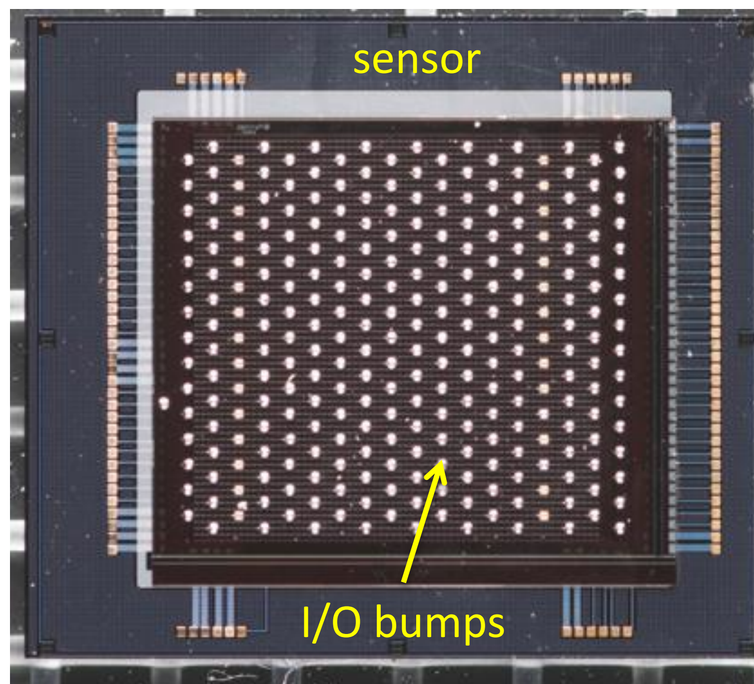
Grind and etch to expose top connections

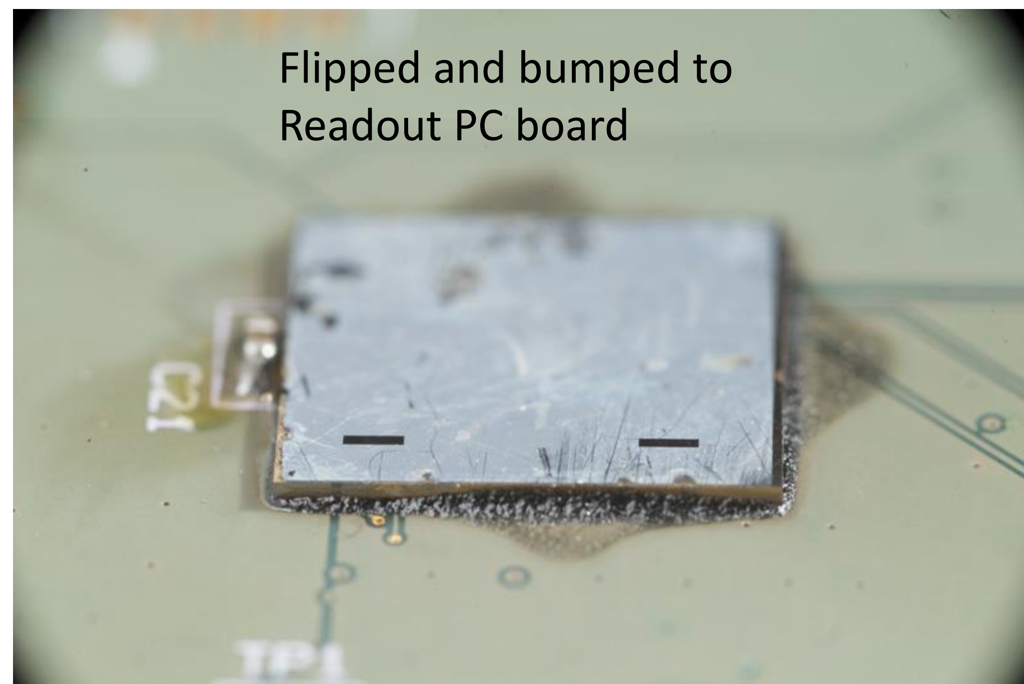
VIPIC

VIPIC is a chip design for X-ray photon correlation spectroscopy with deadtimeless readout

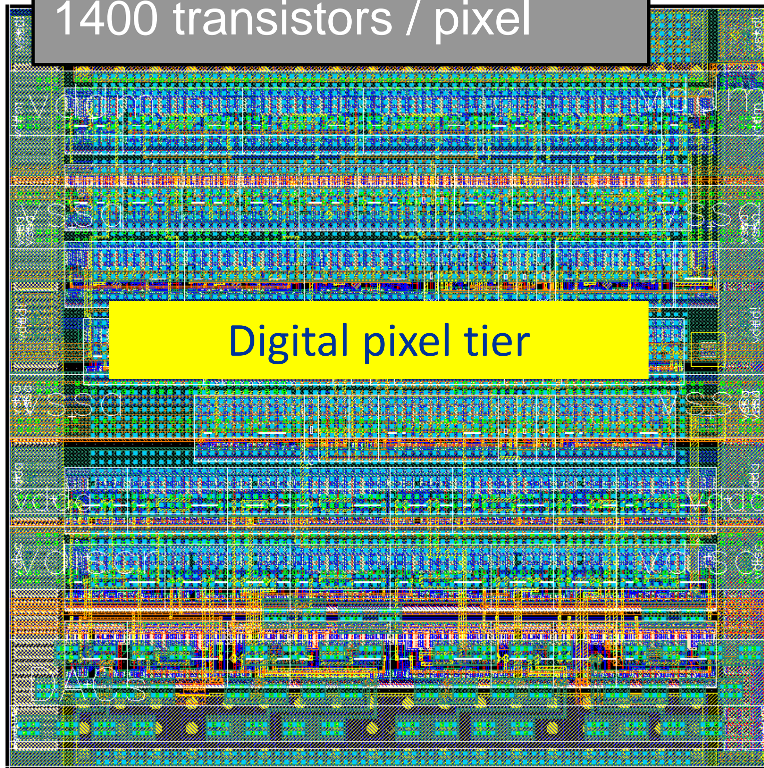
- Separate analog/digital tiers
- 25 inter-tier connections/pixel (64x64 80 μ pixels)

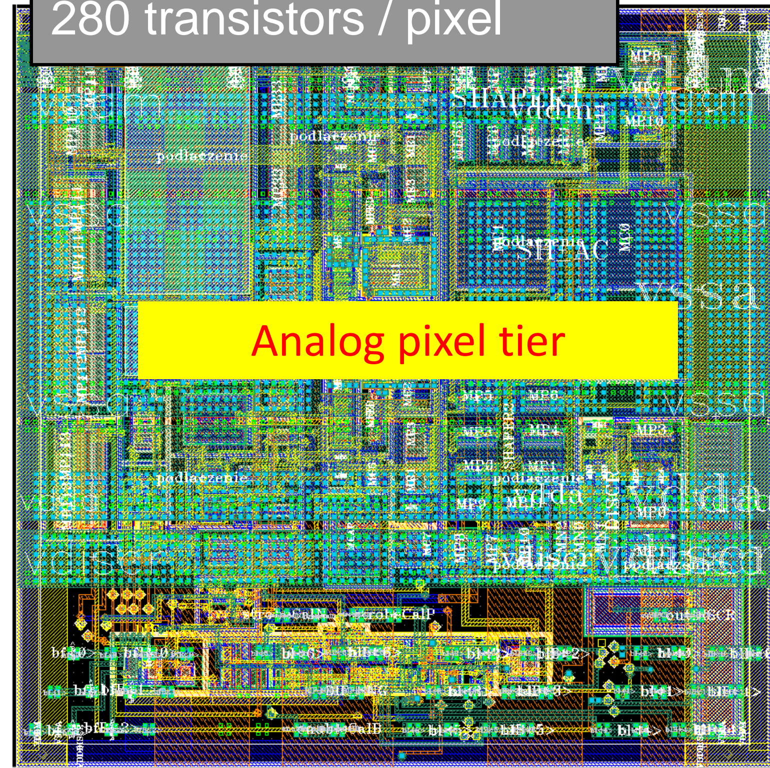






3D-IC: Fermilab designs – VIPIC





- 64 × 64 array of 80 mm^2; shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <<150 e^- ENC
- Two dead-time-less modes of operation (64 × 64 matrix / in 16 sub-matrices of 4 × 64 pixels):
  - timed readout of hits acquired at low occupancy (address and hit count) σ_t~1μs
  - imaging – counting of events
- Sparsified readout with priority encoder circuit (hit pixel address readout only)

VIPIC Sensor results

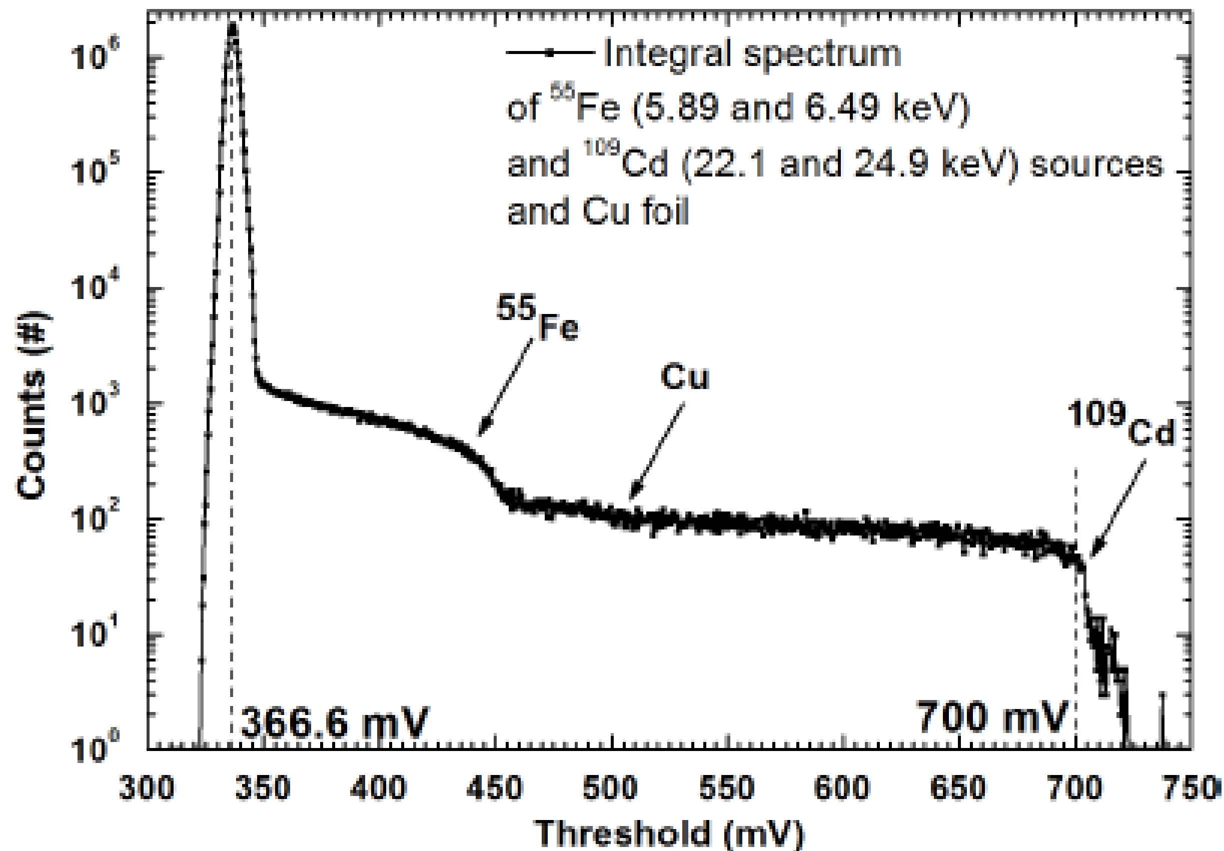
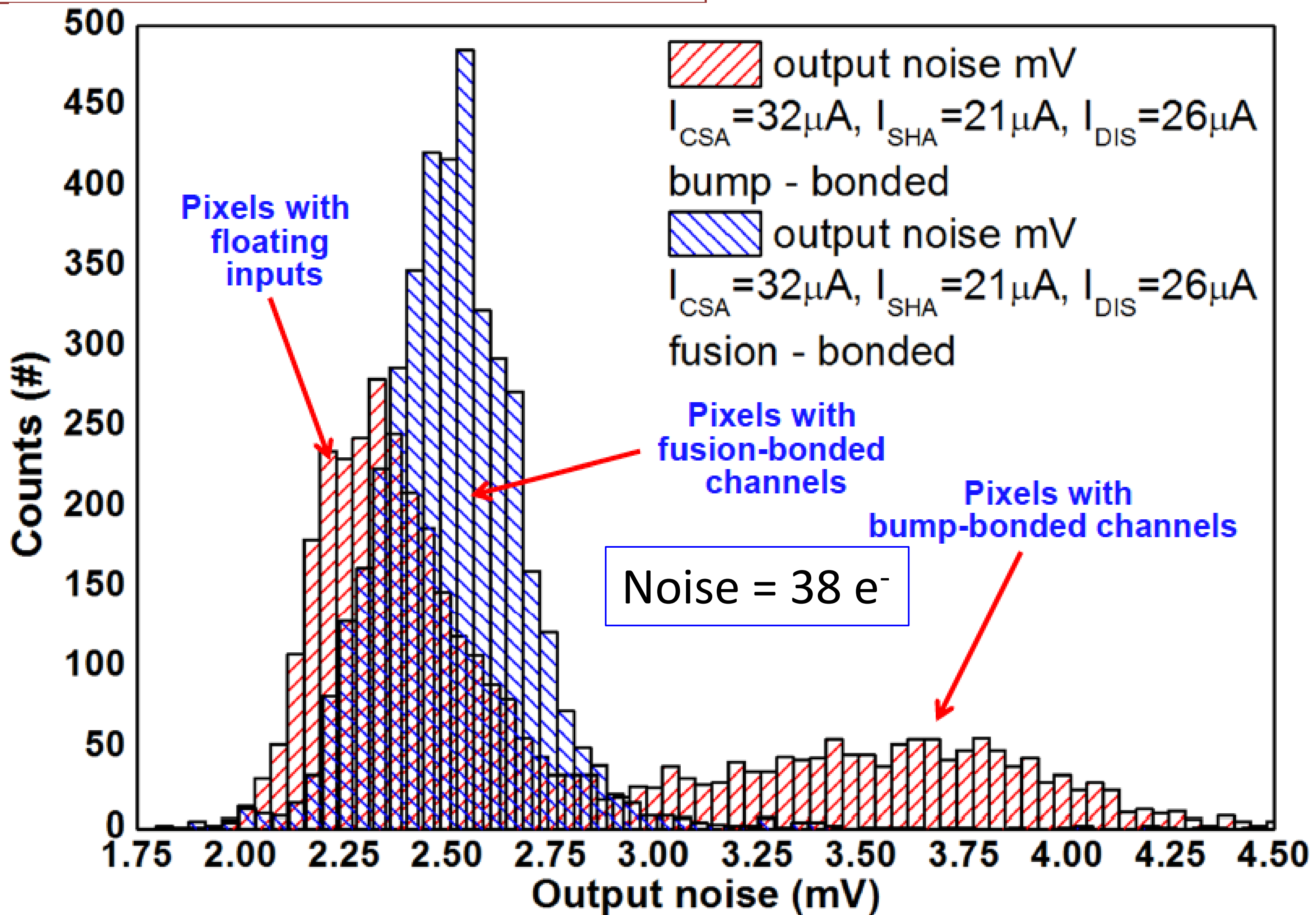


Fig. 5: An integral spectrum registered with simultaneous exposure to ^{55}Fe (back side) and ^{109}Cd (front side) sources.

Because we have both bump-bonded and oxide bonded VIPICs we can compare the performance directly

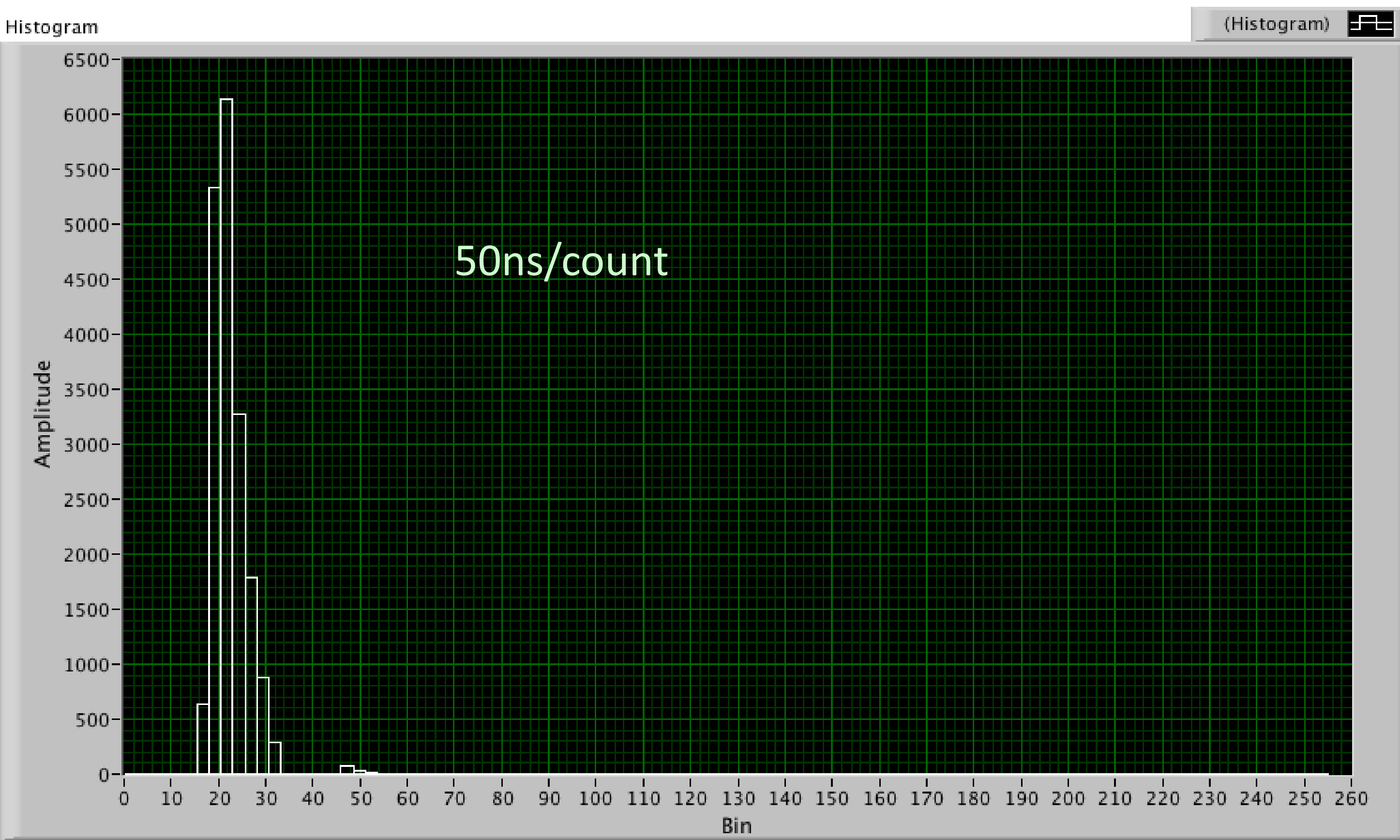
VIPIC Noise



Output noise on oxide bonded devices are close to pixels with no sensors bonded – low interconnect capacitance associated with oxide bond

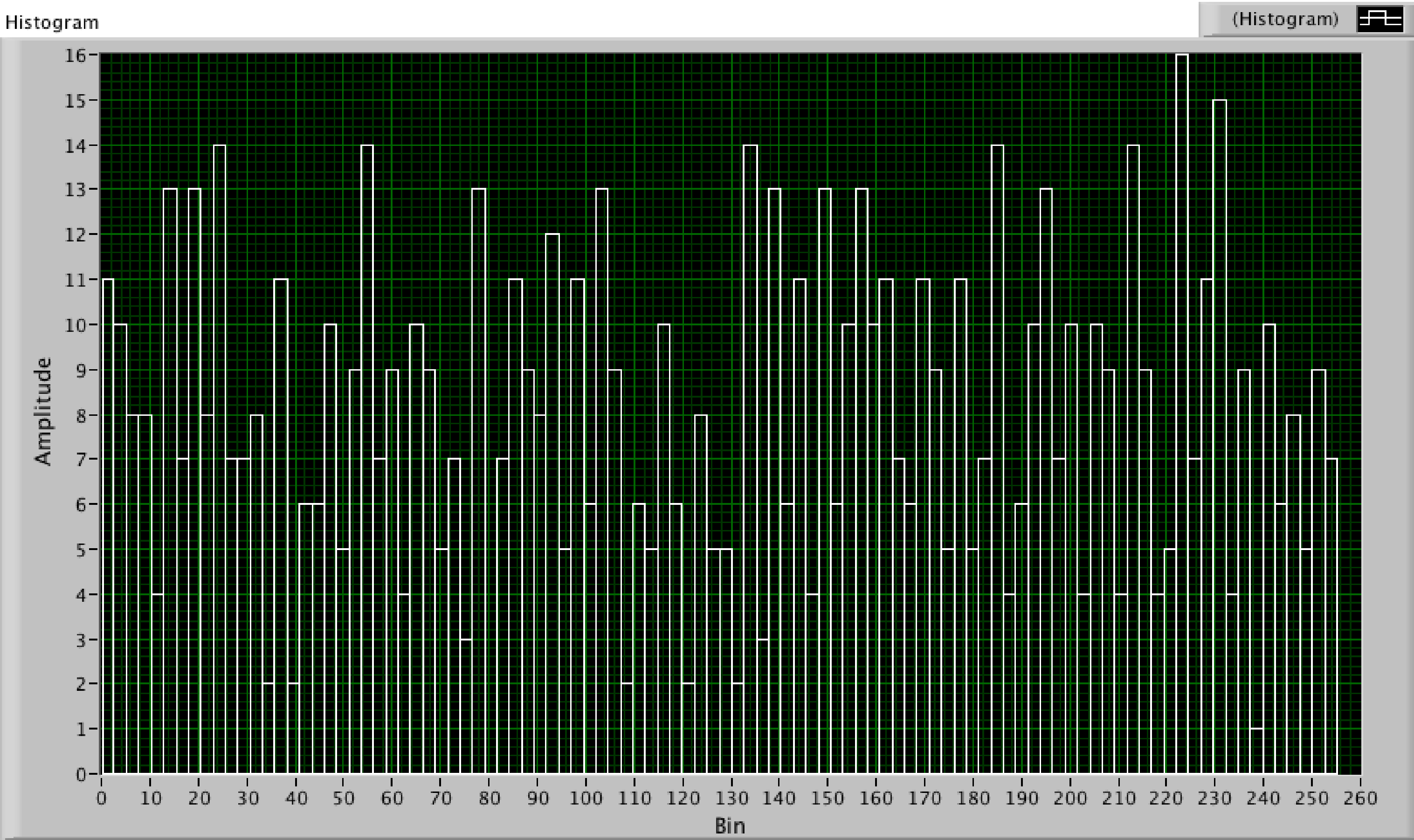
Initial Timing Study

The time distribution of hit channels with Vth= 0.45 and 0.1 V test pulse injection. The distribution moves with test injection timing as expected. For lower thresholds the time distribution also shows a odd/even split due to the differing odd/even thresholds.



Initial Timing Study

The time distribution of hit channels with Vth= 0.2 with the Fe-55 source showing a ~uniform distribution within the time window.



Mounted detectors