

Calice ECAL Status

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Outline

- 1 The Calice Project
- 2 The CALICE ECAL prototype
 - Description
 - Status
 - The Silicon Matrices.
- 3 Outlook

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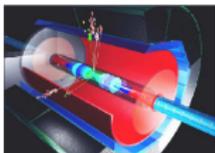
The Calice Project

Final Goal: Calorimeter Design for ILC

Intermediate Goals:

- 1 Proof of principle of the technologies.
- 2 Verification of Geant 4
(tuned Geant 4 required for detector optimisation)
- 3 Full scale prototype module.
- 4 optimised calorimeter design.

1. & 2. → Testbeam program



The collaboration



*CALICE is an open - and growing - collaboration:
Recently new groups from Canada, France, Korea, the UK, the USA*

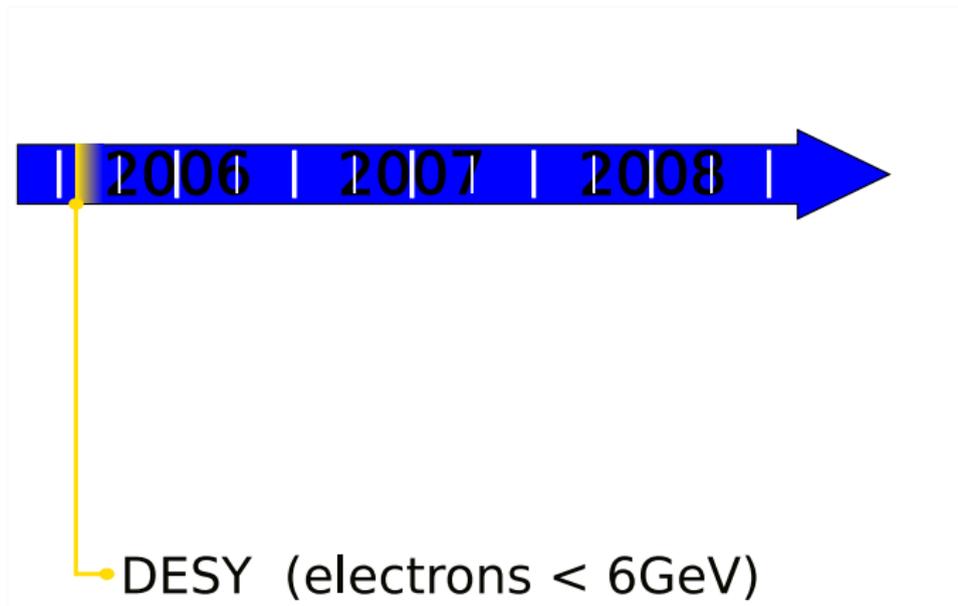
- Sharing of tasks and resources
- Organizational structure and procedures defined in a "Memorandum of Agreement"
- Regular internal reviews to monitor the progress

Considered Calorimeter Options

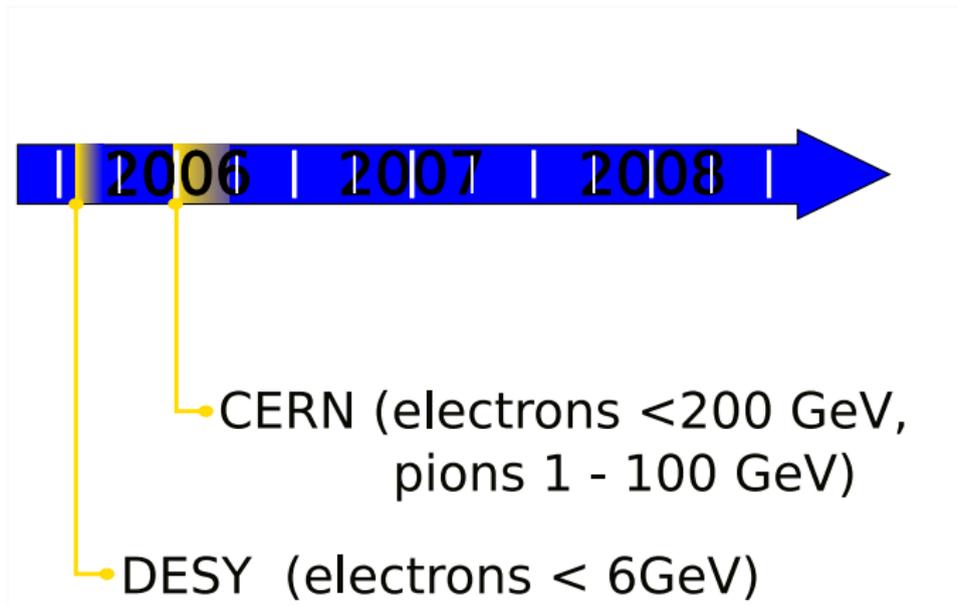
Currently considered calorimeter options:

- ECAL options: Si/W
- HCAL options:
 - tungsten/stainless steel
 - analog scintillator
 - digital gas (rpc/gem)
- Tail catcher:
scintillator/stainless steel

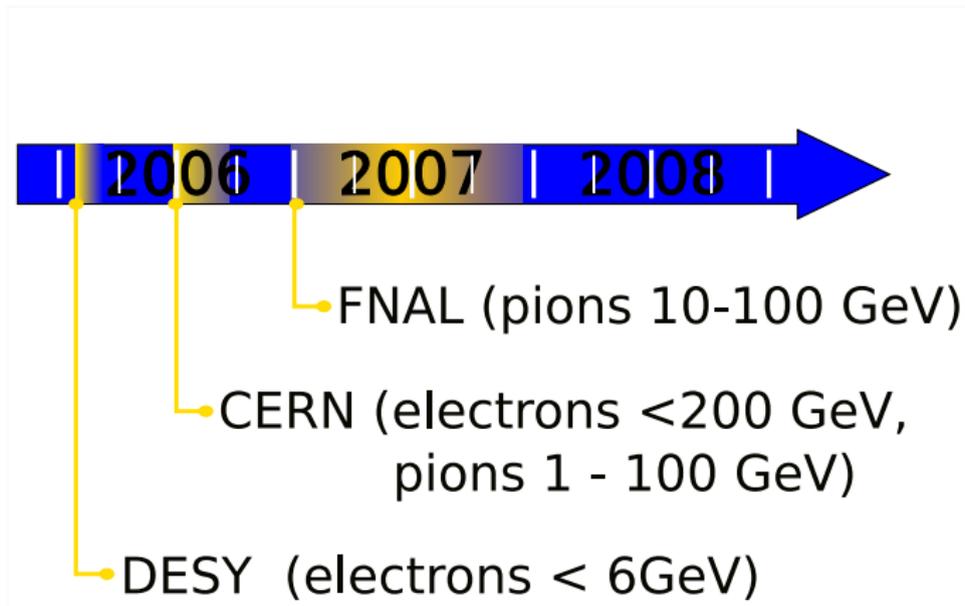
Test beam program



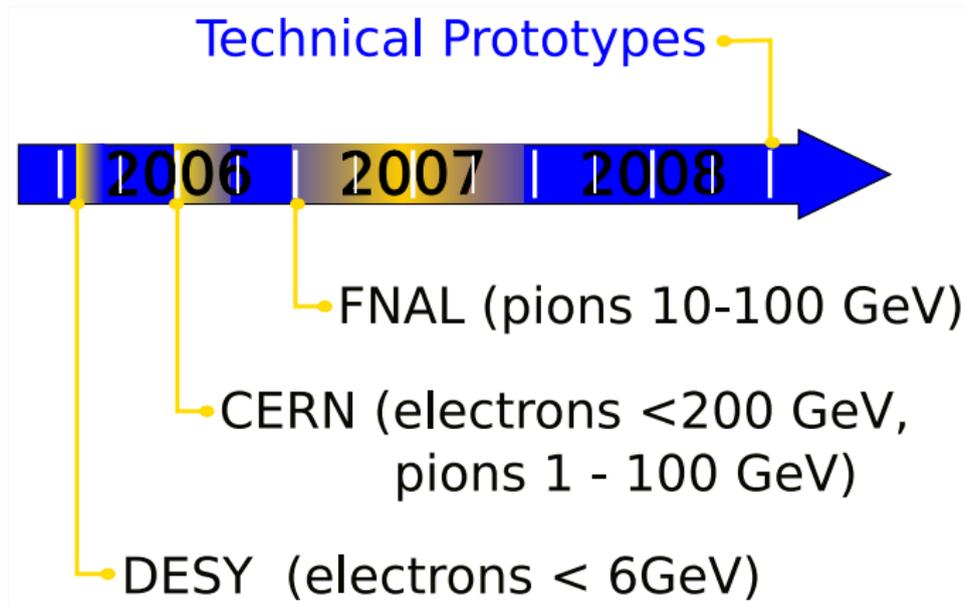
Test beam program



Test beam program



Test beam program



The Calice ECAL Prototype

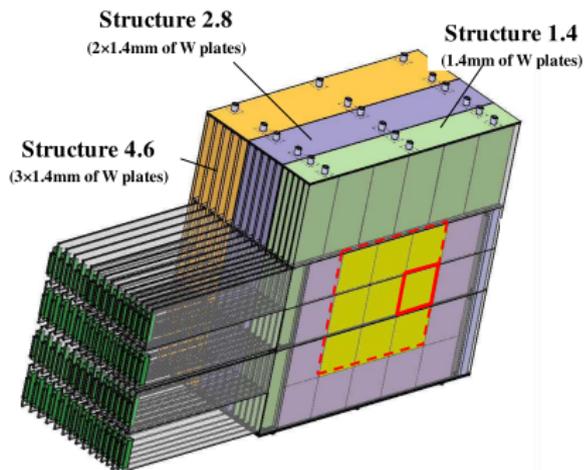
The Calice ECAL Prototype

Specifications

- Si/W Sandwich
- $24 X_0$
- high granularity:
 - $1 \times 1 \text{ cm}^2$ cell size.
 - 30 sensitive layers.
 - 3×3 Si wafer with 6×6 pads.

→ 10k Channels

*Design, Production and Integration
at LLR - Polytechnique*



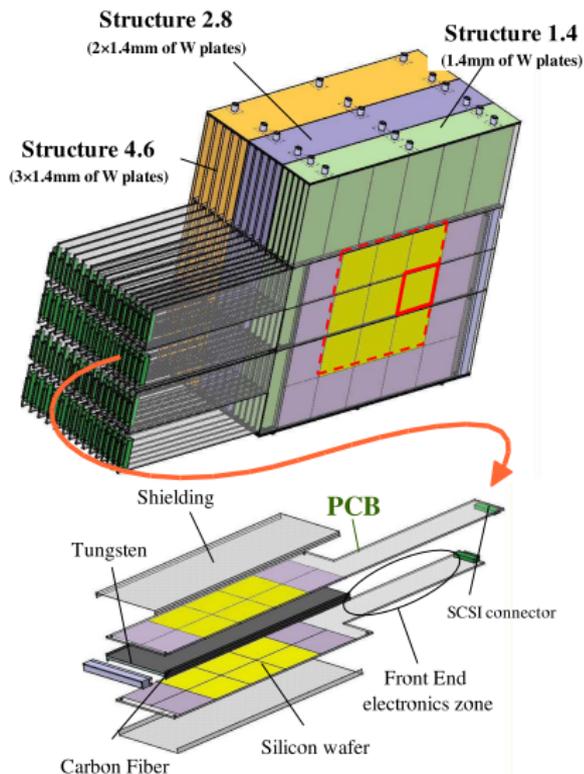
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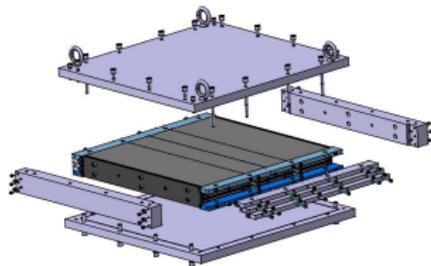
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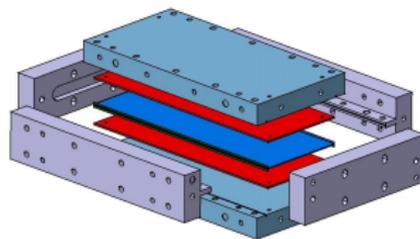


Fabrication of Composite Structures

Alveolar Structure



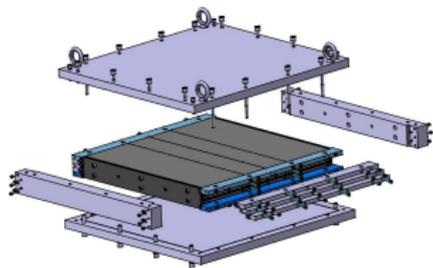
H-Structure



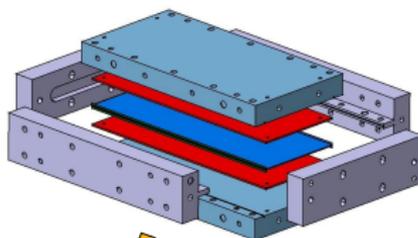
(Here: 1.4 mm of Tungsten)

Fabrication of Composite Structures

Alveolar Structure



H-Structure



(Here: 1.4 mm of Tungsten)

Design criteria for the Silicon Wafers

Keep design as simple as possible

(For example: minimise the required processing steps.)

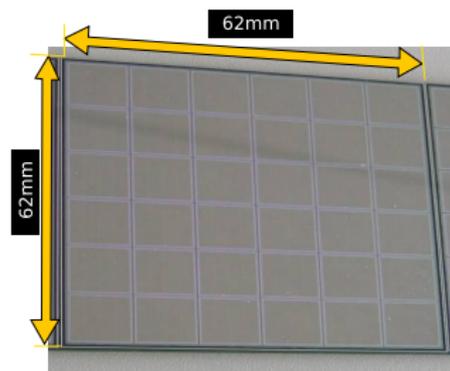
- increases number of potential producers.
- increases yield of good wafers
(reliability and robustness).

→ keeps down cost of full scale detector

The Silicon Wafers

Properties:

- 4" high resistive wafer : $5 \text{ k}\Omega \text{ cm}$
- Thickness : $525 \mu\text{m} \pm 3\%$
- Matrix dimension : $62.0^{+0.0}_{-0.1} \text{ mm}$
- Guard ring
- In silicon: $\sim 80 \text{ eh} / \mu\text{m}$
 $\rightarrow 42000\text{e}^- / \text{ mip.}$
- Capacitance : $\sim 21 \text{ pF}$ (one pixel)



6×6 sensitive pads of $1 \times 1 \text{ cm}^2$

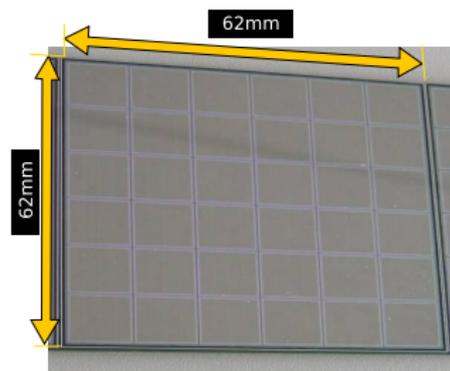
Demanded quality:

- Leakage current @ 200 V : $< 300 \text{ nA}$ (Full matrix)
- Full depletion bias : $\sim 150 \text{ V}$
- Nominal operating bias : 200 V
- Break down voltage : $> 400 \text{ V}$

The Silicon Wafers

Properties:

- 4" high resistive wafer : $5 \text{ k}\Omega \text{ cm}$
- Thickness : $525 \mu\text{m} \pm 3\%$
- Matrix dimension : $62.0^{+0.0}_{-0.1} \text{ mm}$
- Guard ring
- In silicon: $\sim 80 \text{ eh} / \mu\text{m}$
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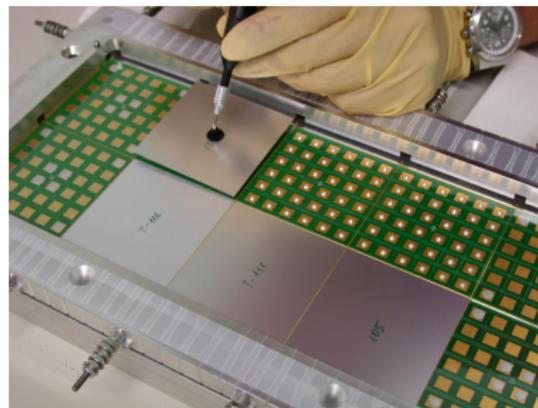
6 × 6 sensitive pads of 1 × 1 cm²

Demanded quality:

- Leakage current @ 200 V : $< 300 \text{ nA}$ (Full matrix)
- Full depletion bias : $\sim 150 \text{ V}$
- Nominal operating bias : 200 V
- Break down voltage : $> 400 \text{ V}$

Gluing the Wafers

- Validation of each step
 - Glue : EPO-TEK E4110 - OK
 - Dispensing system - OK
 - Placing manually wafers - OK
 - Aluminium foil process - OK
 - Polymerisation : 8h at 40 °C - OK
- 2 days / PCB



Front-End PCB

6 active wafers

- 36 silicon PIN diodes each
→ 216 channels per board.
- Diode size: $1 \times 1 \text{ cm}^2$.

Front-End chip

12 FLC.PHY3 front-end chip

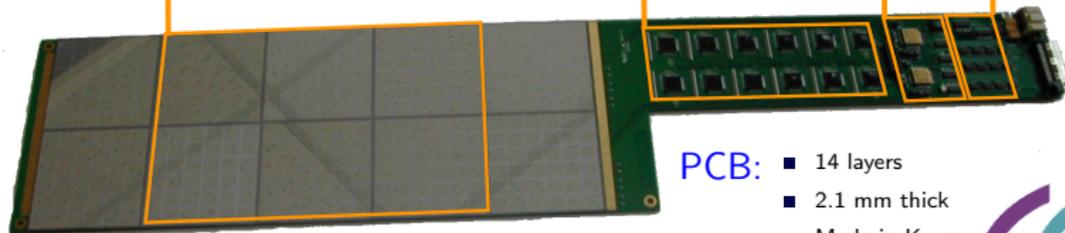
- 18 channels / chip
- 13 bit dynamic range

Calibration chips

- 2 calibration switches chips.
- 6 calibration channels per chip.
- 18 diodes per calibration channel.

Line buffers

- To DAQ part
- Differential.



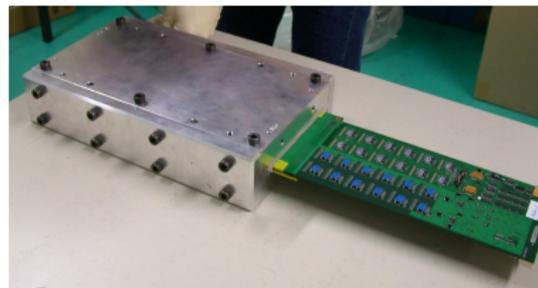
PCB:

- 14 layers
- 2.1 mm thick
- Made in Korea



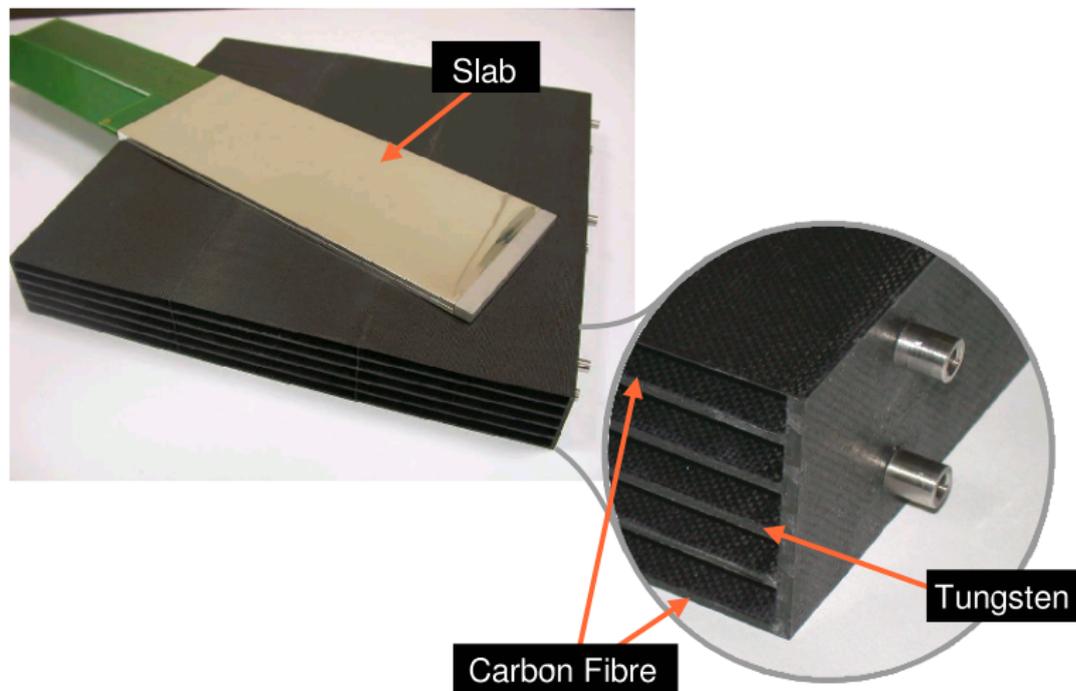
Slab Assembly

- Validation of assembly process :
 - Bending tool of shielding - OK
 - Assembly mould - OK
 - Polymerisation : 8h at 40 °C - OK
- 1 day / slab



Gluing + assembly: 2 days / slab

The Calice ECAL Prototype



The Alveolar Structure (1.4 mm Tungsten)

ECAL Prototype Status

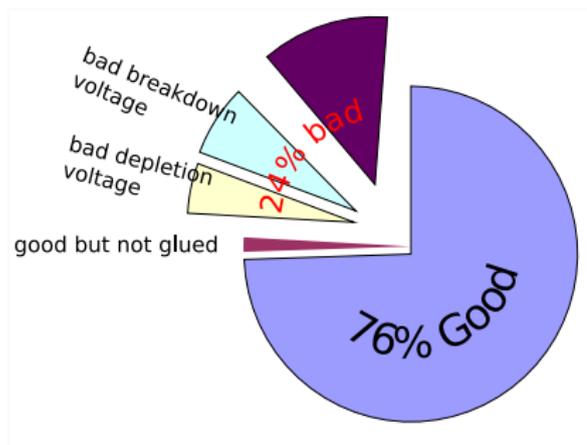
- alveolar structures: 3 of 3 OK
- H-structures: 30 of 30 OK
- fully equipped PCB:
 - central PCB: 4+30 / 30 OK
(10 additional spares soon)
 - bottom left PCB : 3+15 / 15 OK
(5 additional spares soon)
 - bottom right PCB : 3+15 / 15 OK
(5 additional spares soon)
- Silicon Matrices: 96 / 270 Problem!
→ Currently 14 Layers (soon: +2) → $\simeq 7.5X_0$

Currently, two independent productions:

- Russian: 145 wafers (+24 +76).
- Czech: 30 wafers (+10).

Wafers of Russian Production

1. Batch: 145 Wafers

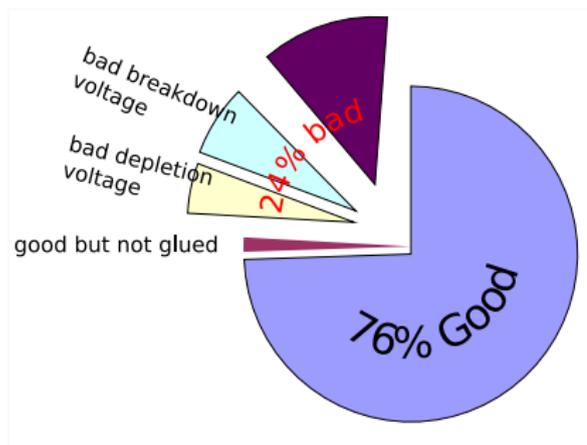


Maybe problem at the end of the production of the 2. batch ?

Wafers of Russian Production

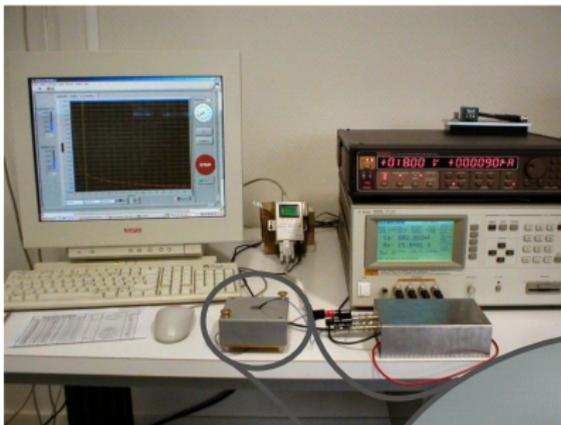
1. Batch: 145 Wafers

2. Batch: 24 Wafers
(of 100 ordered)



Maybe problem at the end of the production of the 2. batch ?

Silicon Matrix Test Bench



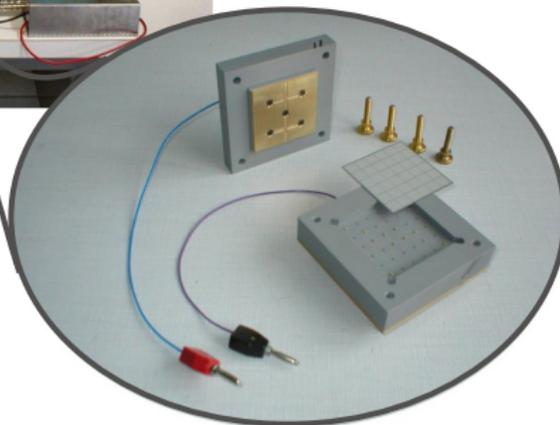
6×6 spring mounter
point contacts.

Measurements:

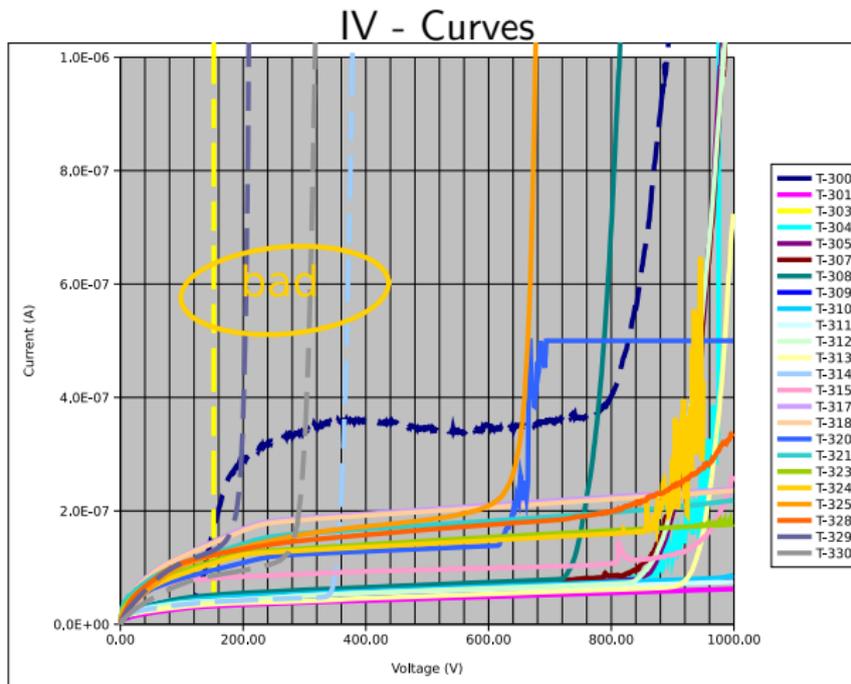
- C-V curve.
- I-V curve

New Test bench

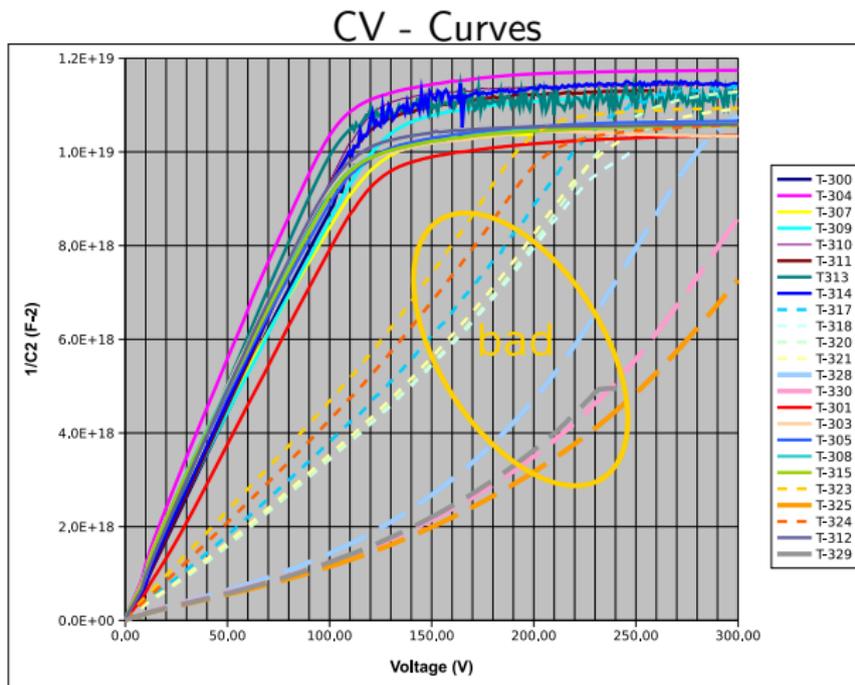
- C-V meter
- pico Ampère meter
- temperature monitoring
- humidity monitoring



Wafers of 2. Russian Production

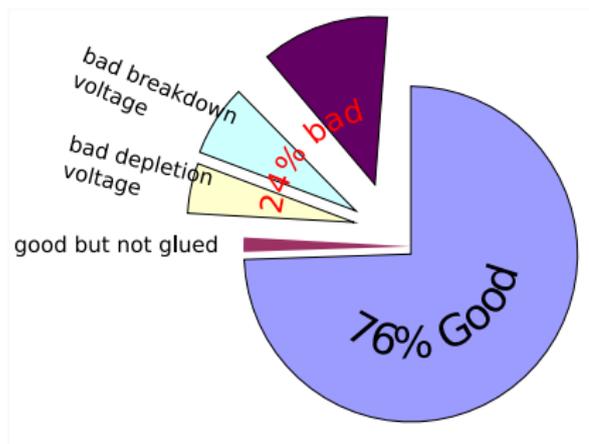


Wafers of 2. Russian Production

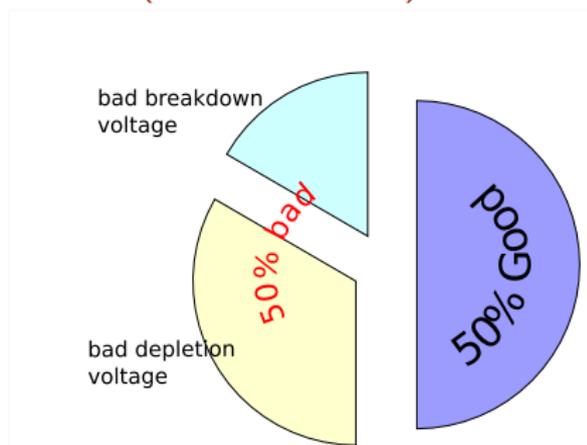


Wafers of Russian Production

1. Batch: 145 Wafers



2. Batch: 24 Wafers
(of 100 ordered)



Maybe problem at the end of the production of the 2. batch ?

Wafers of Czech Production

Q1 2005:

- Wafers are of excellent quality.
(Very low leakage currents before gluing)
- Gluing procedure attacks passivation.
(Leakage currents increase by orders of magnitude after gluing, Breakdown voltage drops.)

Problem was not solved by Chemical surface treatment or different gluing protocols (time, temperature).

Wafers of Czech Production

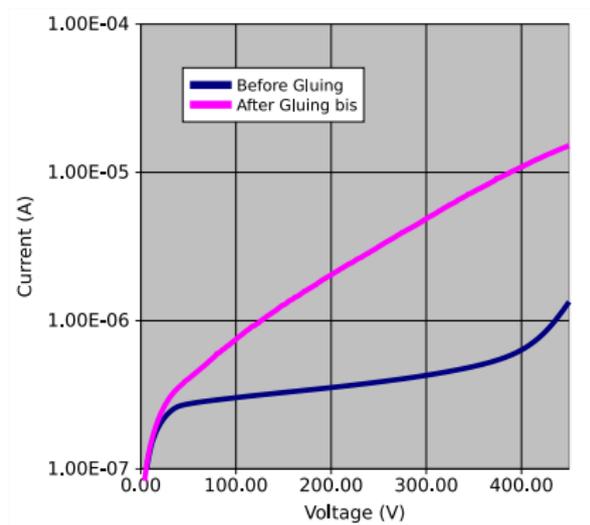
Q3 2005: 10 newly processed Wafers. (ONsemi)

before gluing:

- low leakage current
- stable breakdown voltage

after gluing:

- leakage current $\times 10$.
- But breakdown voltage stable.



Recently, manufactures have reported success. Needs verification!

Wafers for the Calice ECAL

- Unavailability of good wafers delays completion of Calice ECAL prototype.
- Looking for additional producers:
 - 50 wafers will be produced in Korea (December).
 - close contact to other producers (including Hamamatsu).
 - 500 high resistivity raw wafers are ordered.

Future Directions

Can the pad size be shrunk to e.g. $3 \times 3 \text{ mm}^2$?

Problems:

- Mechanical tests with glue drops of 1 mm diameter were successful.
- Electrical properties will be tested soon.
- Is the heat of the additional readout channels tolerable?

Results With the Calice ECAL Prototype

- 1 2 weeks cosmics (December 2004)
- 2 2 weeks (+ commissioning) e^- test beam at DESY (February 2005)

Some Results will be presented by:

- G. Mavromanolakis (this session)
- D. Ward Simulation & Reconstruction

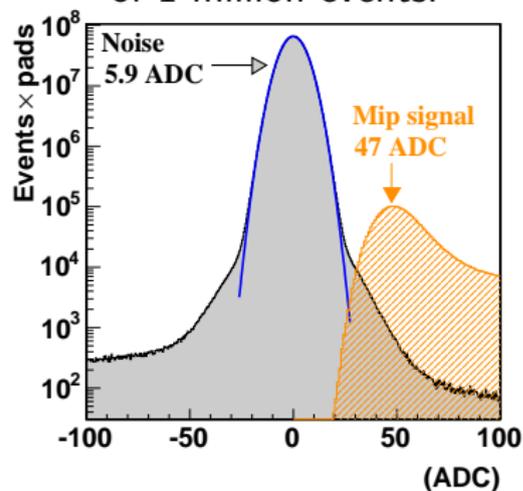
Signal and Noise of all channels
of 1 million events:

- 15 days of continuous data taking
- 10 layers (central part)
($\sim 2k$ channels)
- 1 million events recorded \rightarrow
1% calibration
- Will be repeated with 16
layers in December.

Cosmics Test

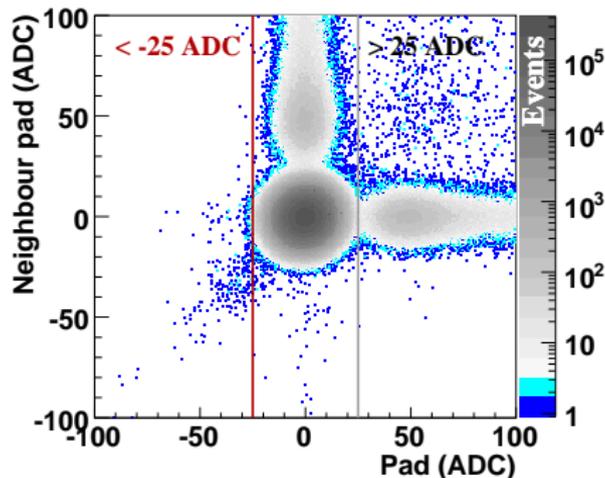
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Signal and Noise of all channels of 1 million events:



\rightarrow signal/noise $\simeq 8$

Correlation between Neighbour Pads

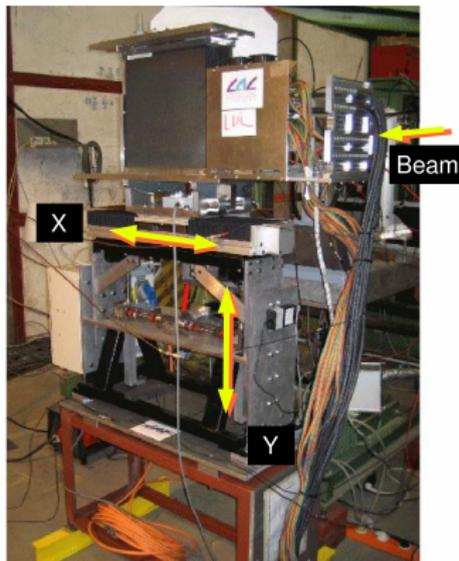


Similar correlation between pads of different half wafers / wafers.

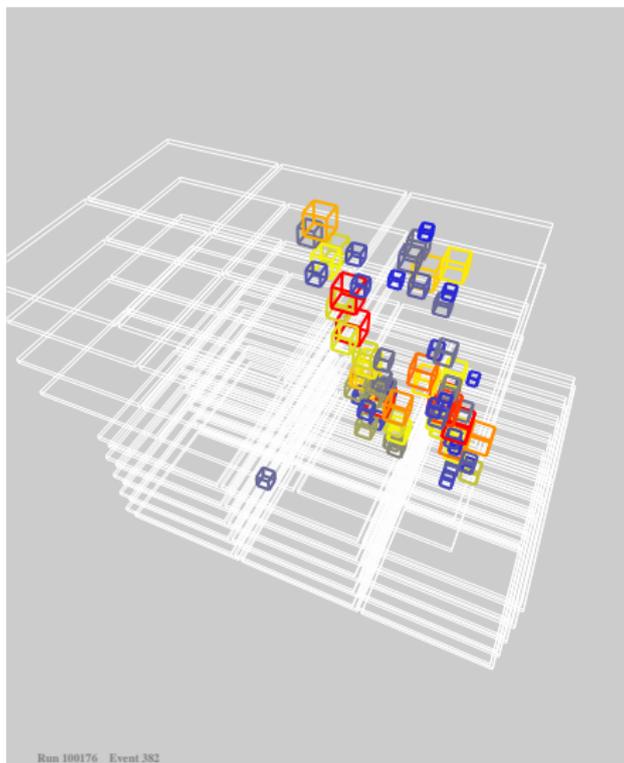
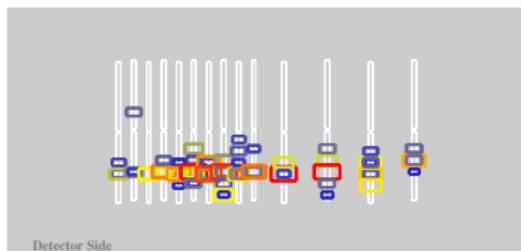
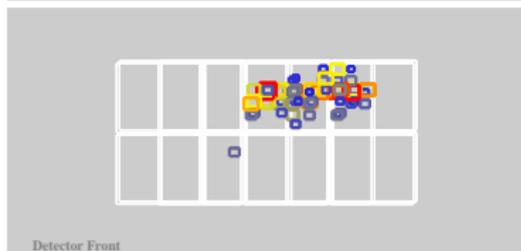
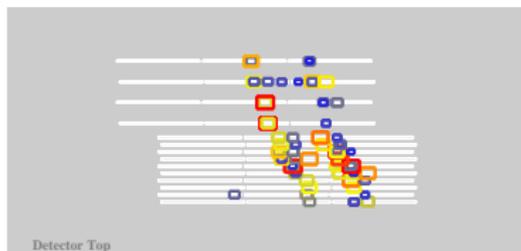
Electron Test Beam at DESY

- Electrons 1 ... 6 GeV
- Angles 0° , 10° , 20° , 30°
- Various x/y impact positions.
(Wafer border/centre, ...)

→ 25 Mevents (230 GB)
in 2 weeks (→ ~ 30 Hz)



Event display - Two Electrons 2 GeV, 30°



Summary and Outlook

- The partially completed Calice ECAL has operated in the test beam and the cosmics test as expected.
 - little coherent noise.
 - signal over noise ~ 8 .
- An exciting test beam program is awaiting us.
- But for the test beams, additional wafers are needed:
 - e^- : complete central part is crucial: \rightarrow 84 wafers!
 - hadrons: complete central and bottom parts are crucial: \rightarrow 174 wafers!

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FIN

ECAL Concept

