

Linear Collider Flavour Identification

LCFI Collaboration Report

P Allport³, D Bailey¹, C Buttar², D Cussans¹, C J S Damerell³, N De Groot⁴, J Fopma⁵,
B Foster⁵, S Galagedera⁶, A R Gillman⁶, J Goldstein⁶, T J Greenshaw³, R Halsall⁶, B Hawes⁵,
K Hayrapetyan³, H Heath¹, S Hillert⁵, D Jackson^{5,6}, E L Johnson⁶, A J Lintern⁶, P Murray⁶,
A Nichols⁶, A Nomerotski⁵, V O'Shea², C Parkes², C Perry⁵, K D Stefanov⁶, P Sutcliffe³,
S L Thomas⁶, R Turchetta⁶, M Tyndel⁶, J Velthuis³, G Villani⁶, T Wijnen⁴, S Worm⁶, S Yang⁵

1. Bristol University
2. Glasgow University
3. Liverpool University
4. Nijmegen University
5. Oxford University
6. Rutherford Appleton Laboratory



UNIVERSITY
of
GLASGOW



THE UNIVERSITY
of LIVERPOOL

Linear Collider Flavour Identification: Activities

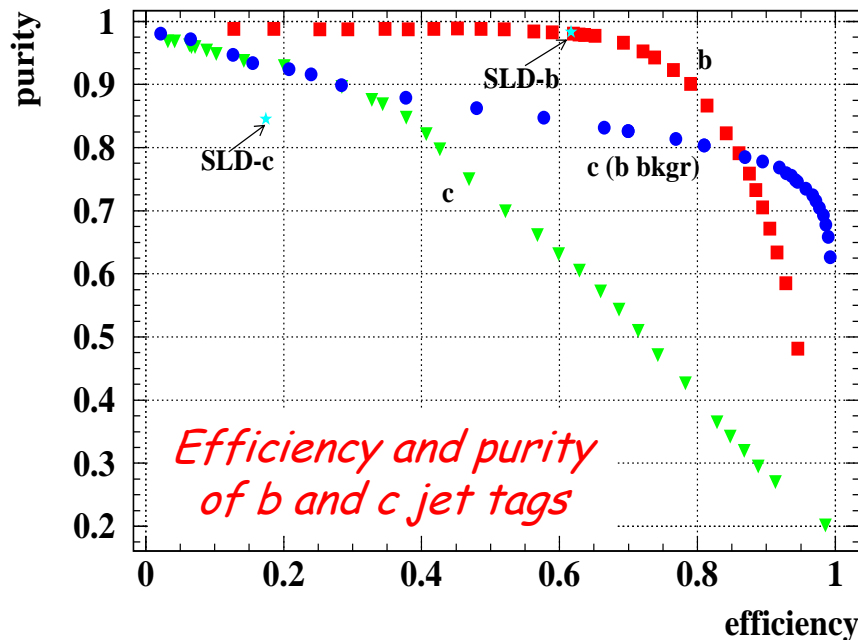
- o LCFI Outline
 - Simulation and Physics Studies
 - Sensor Development
 - Readout and Drive Electronics
 - External Electronics
 - Integration and Testing
 - Vertex Detector Mechanical Studies
 - Test-beam Studies

→ LCFI is active in all aspects of vertex detector development

LCFI Physics Studies

o Identification of b/c quarks

- ZVTOP algorithm plus neural net
- Modest improvement in b tagging over that achieved at SLD.
- Improvement by factor 2 to 3 in charm tagging efficiency.
- Charm tag interesting e.g. for Higgs BR measurements.

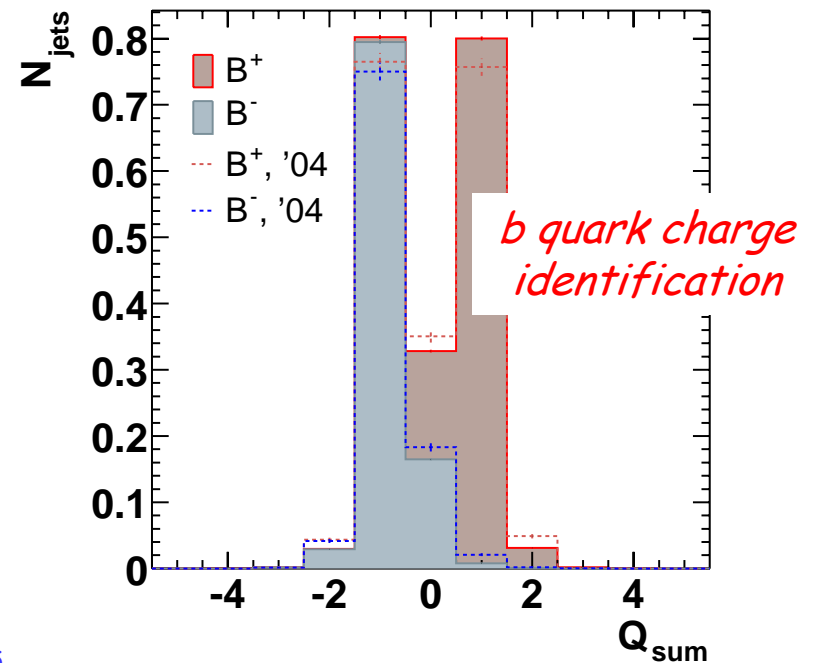


Steve Worm - LCFI

December 16, 2005

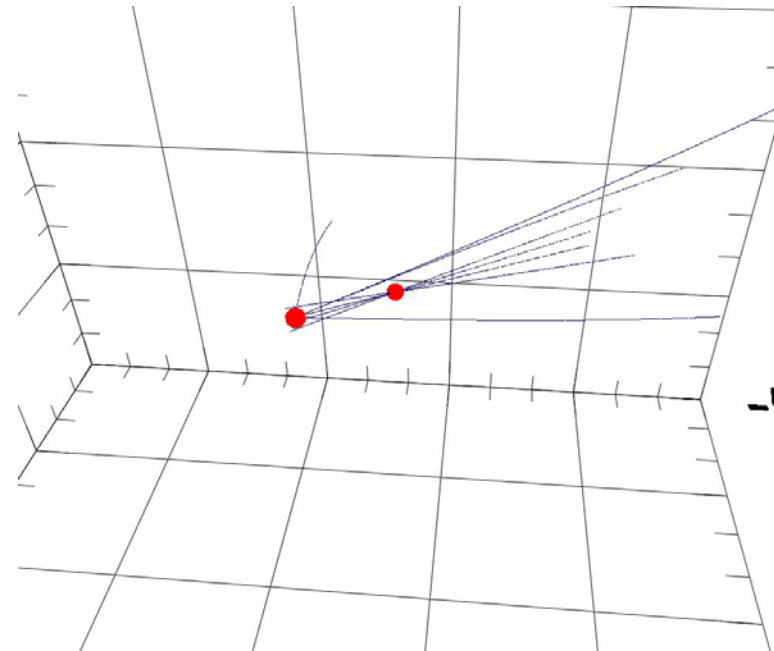
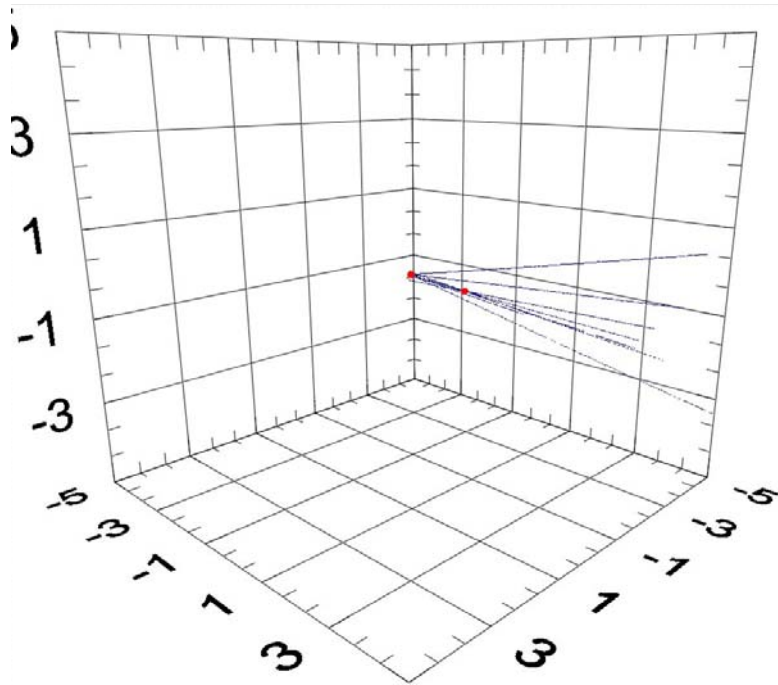
o Identification of quark charge

- Must assign all charged tracks to correct vertex.
- Multiple scattering critical, lowest track momenta ~ 1 GeV.
- Sum charges associated with b vertex:



C++ ZVTOP

The complete original ZVTOP algorithm (also called ZVRES), vertex finding and fitting is now in place and has been used to find vertices in simulated SGV events



Testing and optimisation of the code is in progress

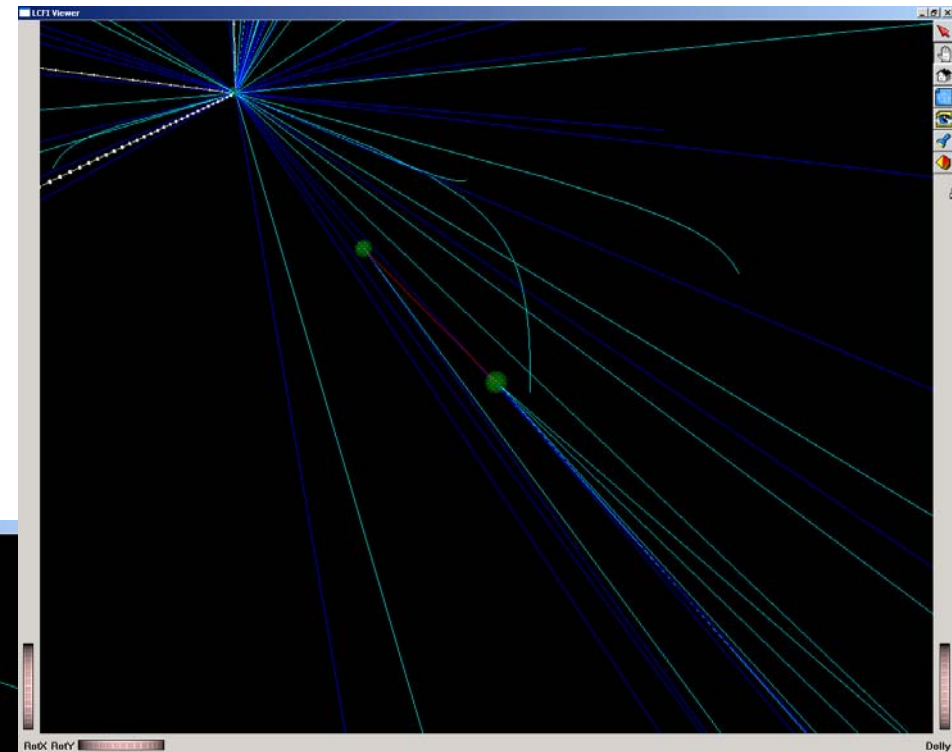
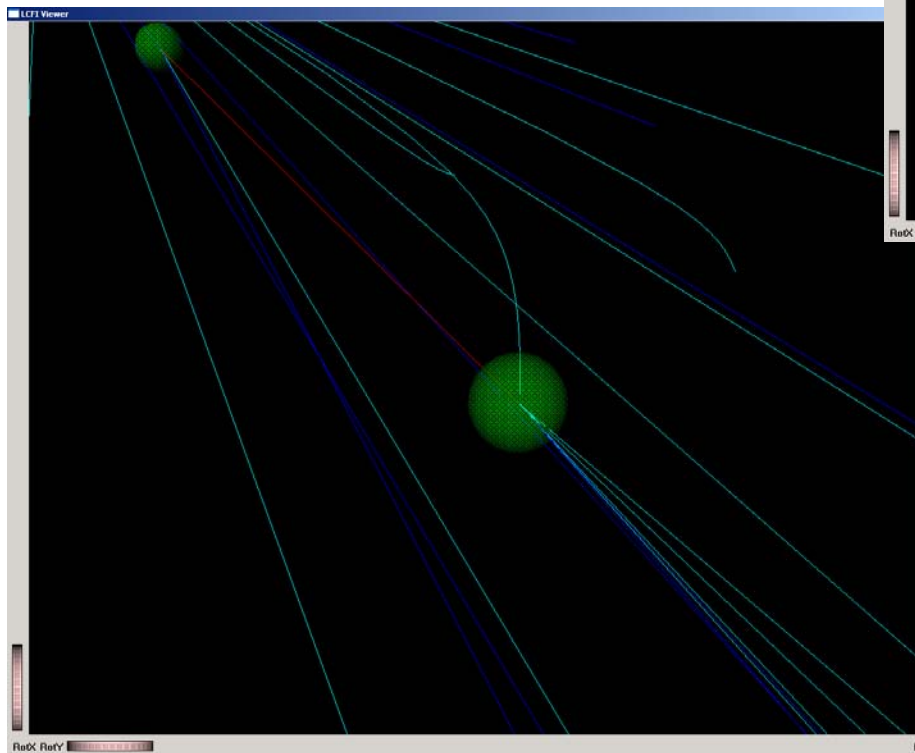
In parallel with this work we are collaborating with colleagues at SLAC developing a Java version of ZVTOP for use with the JAS3 framework

Visualisation Tool

Original tool from Vienna group
not portable

LCFI - independent
implementation still using Coin3D

SGV events and ZVTOP vertices
imported via XML data files

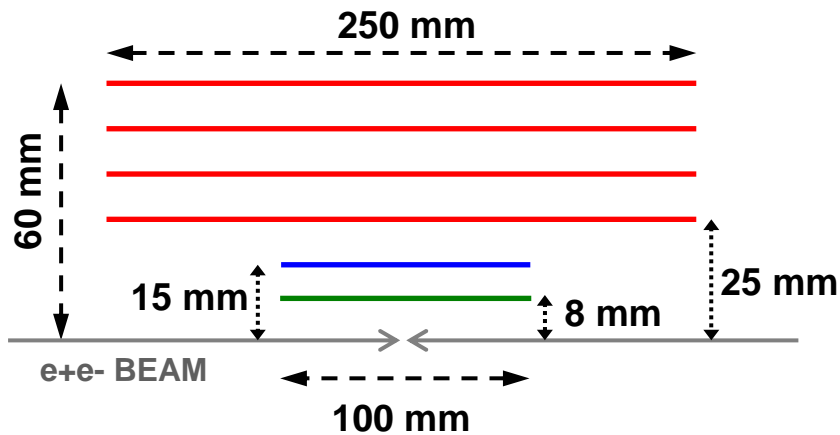


Full 3D perspective display

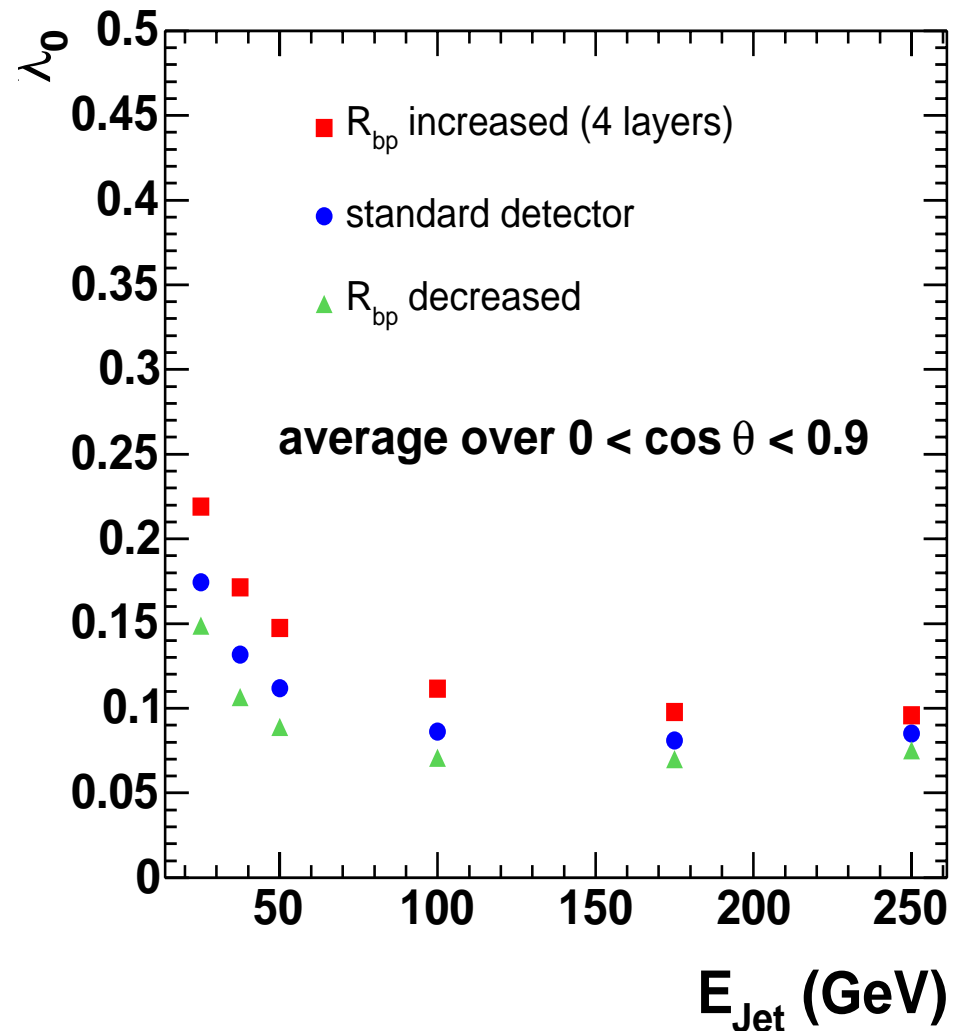
Monte Carlo level as well as
Reconstructed Particles and
Vertices

User defined colour coding of
tracks for diagnostic purposes

Comparing detectors with different beam pipe radius



- Layer thickness $0.1\% X_0$ for all cases.
- However, the beam pipe has to be made thicker as the radius is increased, range 0.4 - 1.0 mm
- The radius of the innermost layer affects the performance over entire jet energy range
- Differences most pronounced at lower jet energies



- Significant input to ILC MDI
'urgent question' on beam pipe radius

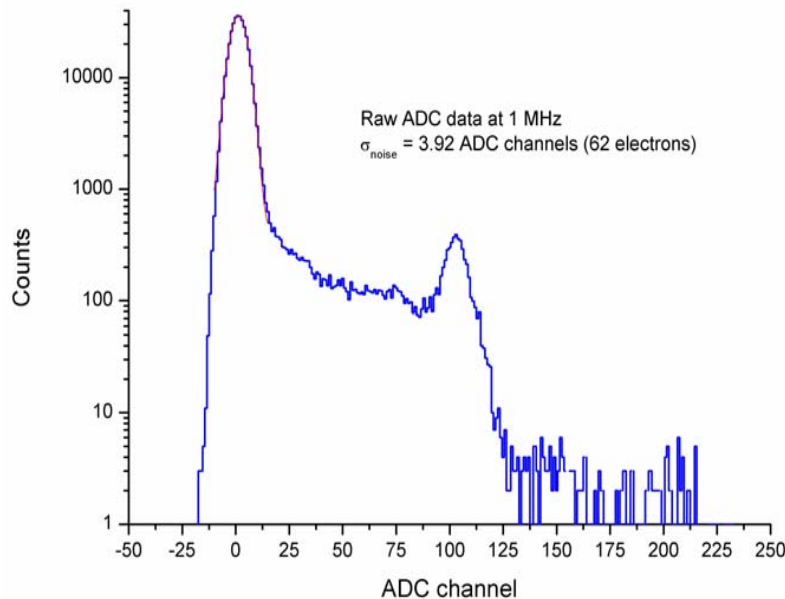
Column-Parallel CCDs: Recent Results

o First-generation tests (CPC1):

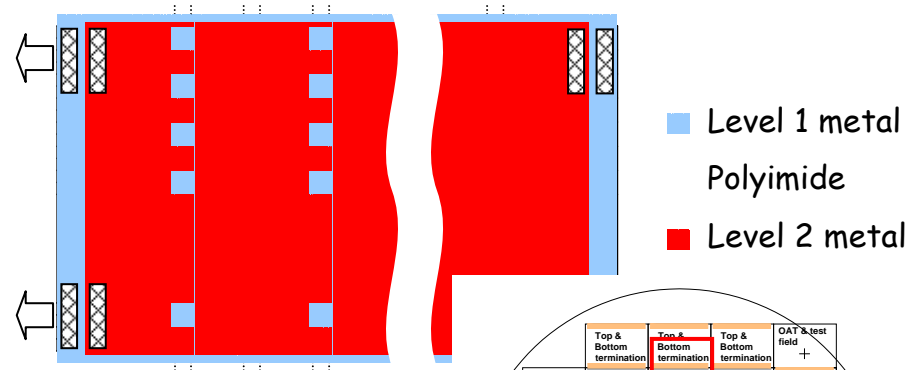
- Noise $\sim 100 e^-$ ($60 e^-$ after filter).
- Minimum clock potential ~ 1.9 V.
- Max clock frequency above 25 MHz (design 1 MHz).
- Limitation caused by clock skew

o Next generation in production (CPC2):

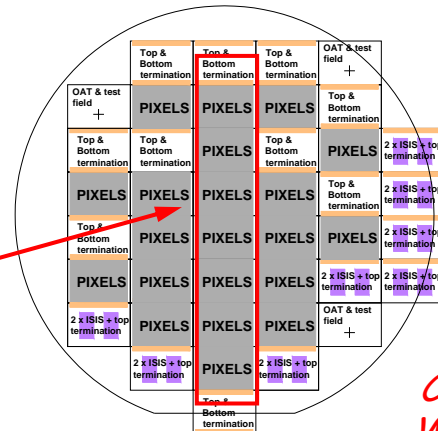
- Busline free design (two-level metal)
- Large area 'stitched' sensor, choice of epi layers for varying depletion depth
- Range of device sizes for test of clock propagation (up to 50 MHz)
- Large chips are nearly the right size



Steve Worm - LCFI



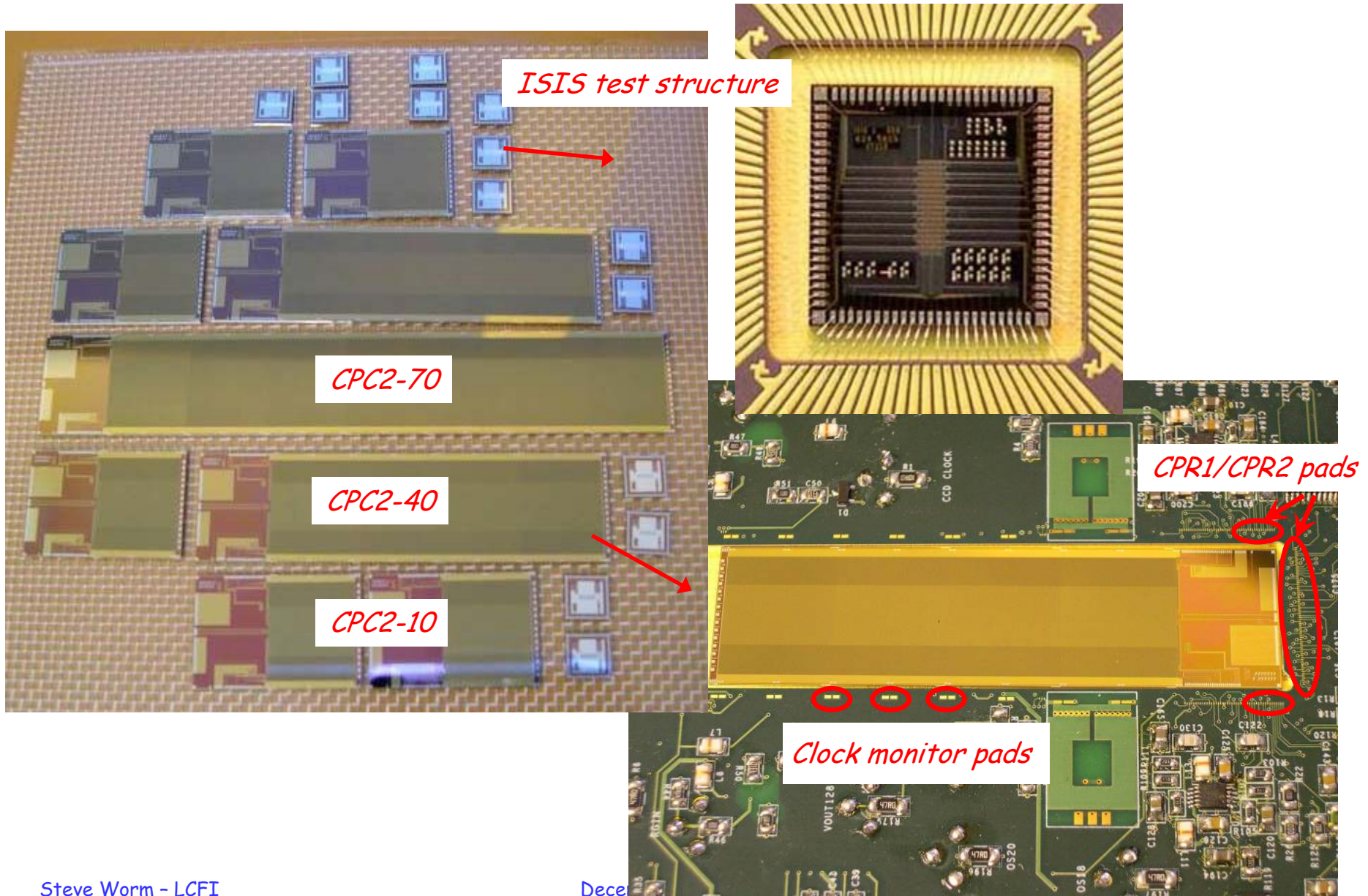
CPC2-70
 9.2 cm



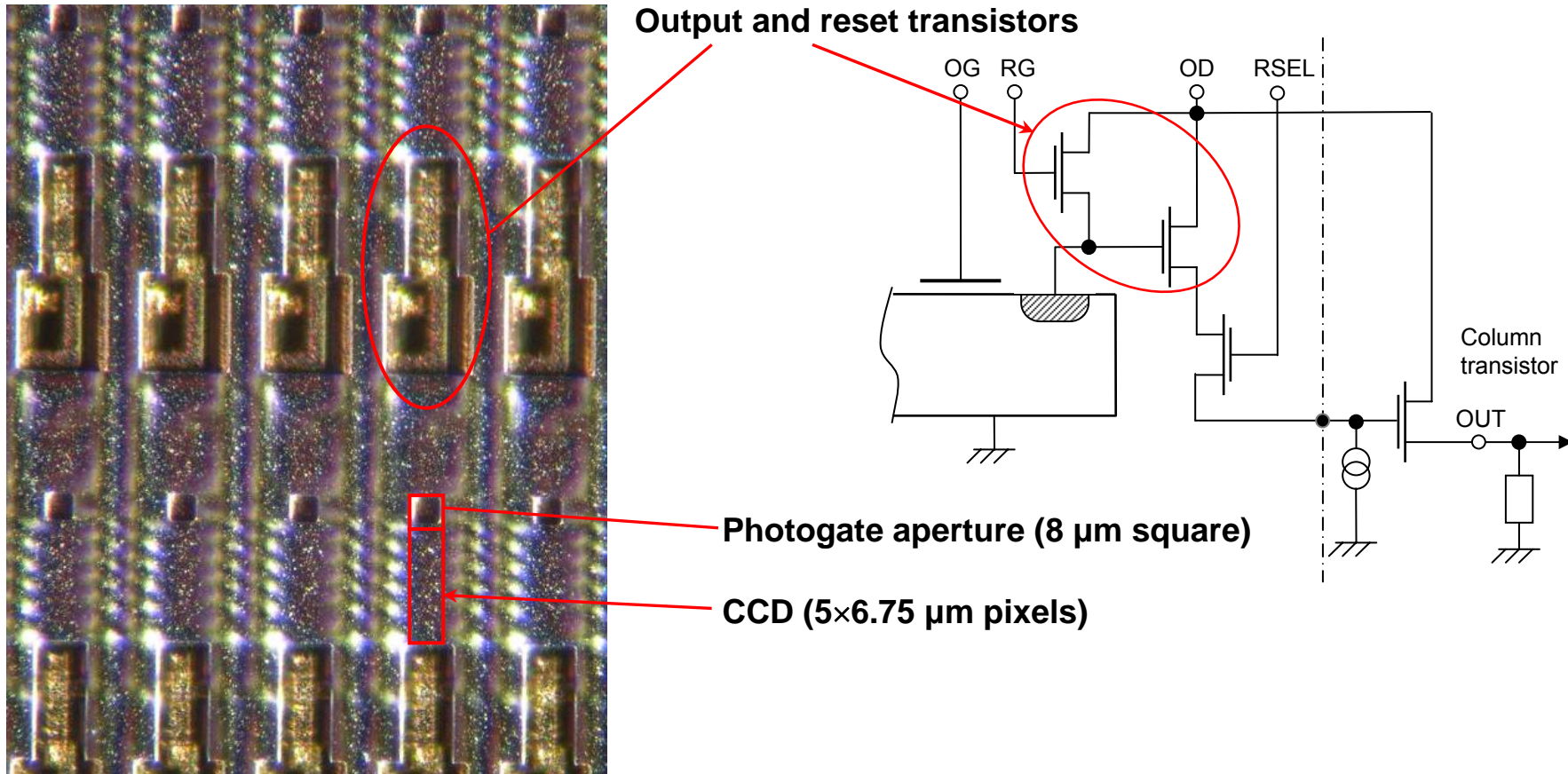
CPC2
 Wafer

December 16, 2005

CPC2/ISIS1 Wafer

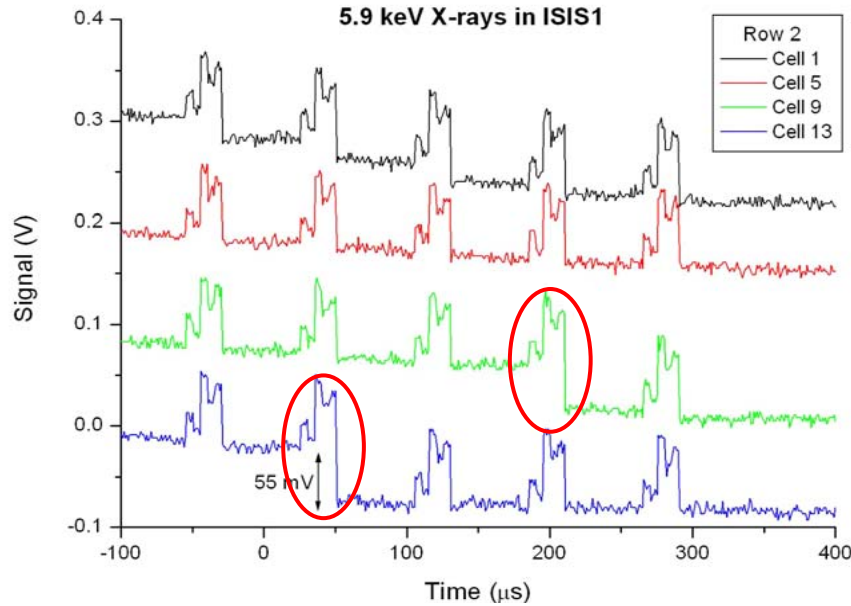


WP5 : ISIS1 Tests



- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm

ISIS Test Results

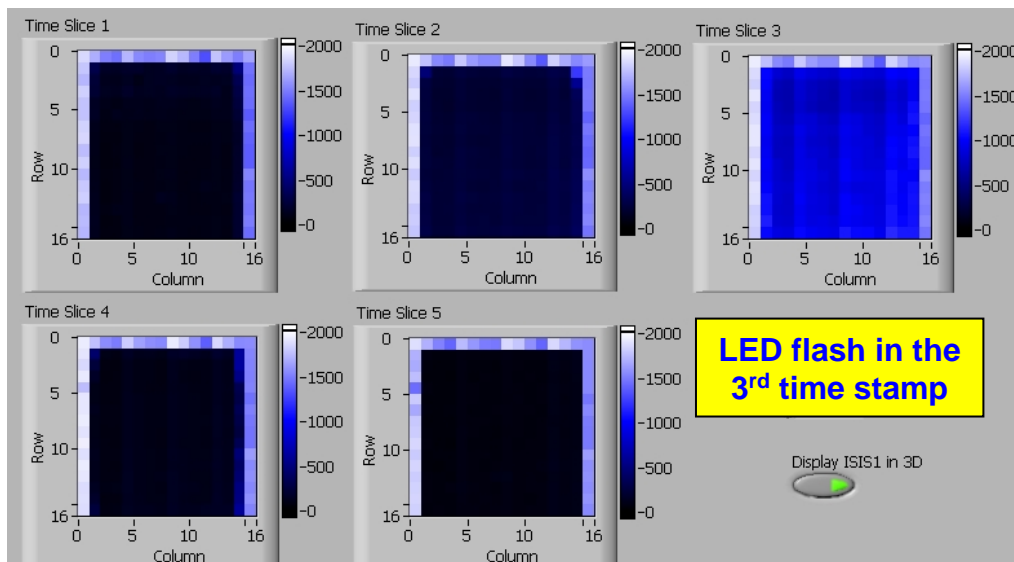


- o X-Ray source

- signal "steps" with the correct amplitude: $3 \mu\text{V}/e^- \times 1620 e^- \times \text{Gain}(10) = 49\text{mV}$

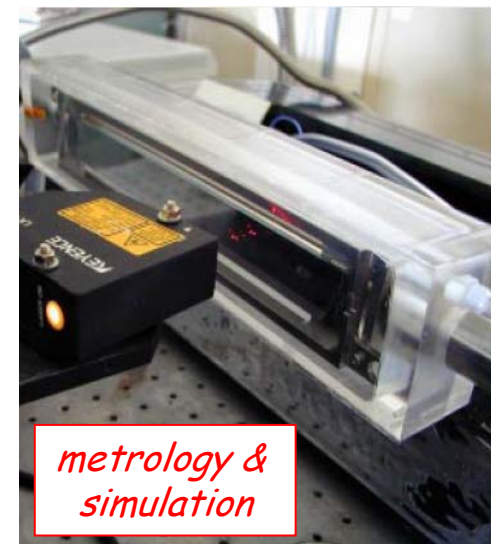
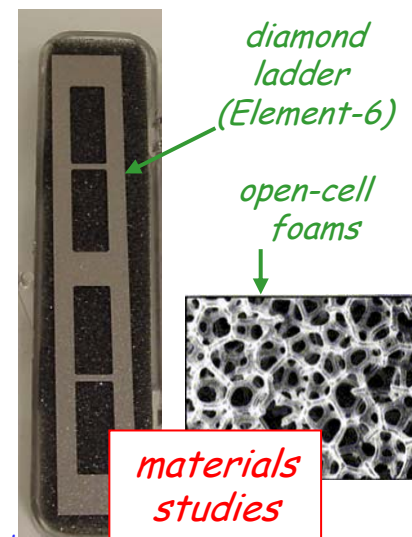
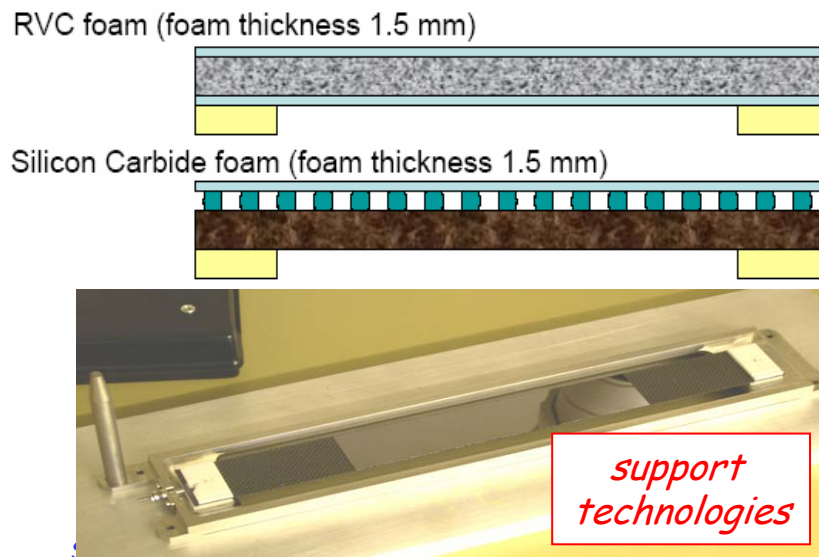
- o LED Light Pulse

- LED pulse appears in 3rd time stamp
- Correlated double sampling implemented
- The top row and 2 side columns are unprotected from parasitic charge collection
- Bottom row protected by circuitry



Vertex Detector Mechanical Studies

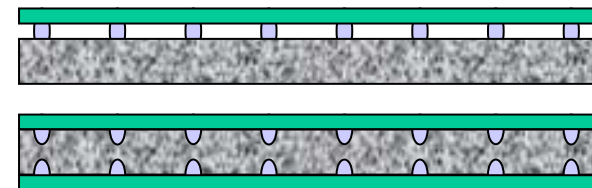
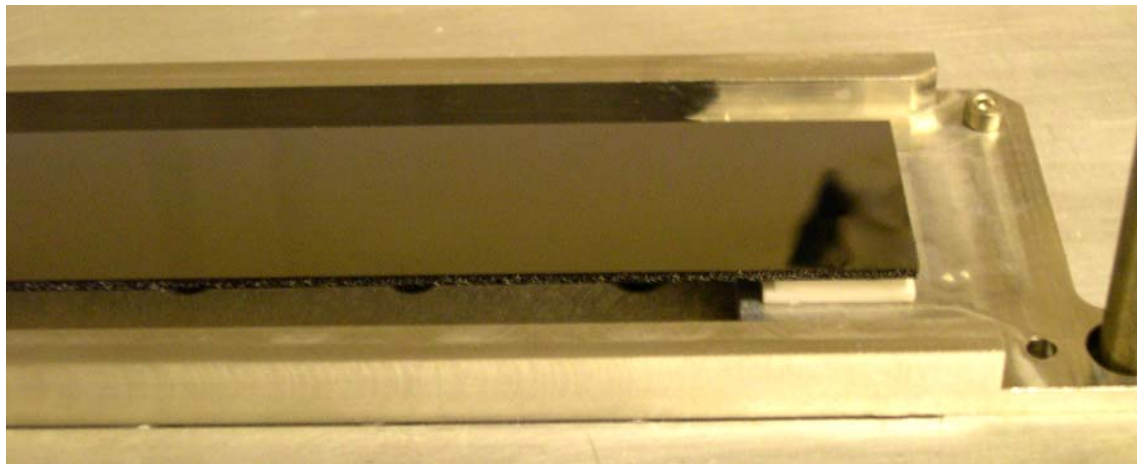
- o Thin Ladder (module) construction Goals are ambitious;
 - $0.1\% X/X_0 \rightarrow$ Thinned silicon sensor, ultra-light support
 - Uniformity over active area
 - Wire or Bump bondable, robust under thermal cycling
- o Mechanical development timeline
 - Develop support technologies, fixturing, production techniques (mid 2007)
 - In parallel, global design and cooling studies, mounting, power, etc
 - Natural evolution into baseline detector design



Thin Ladders

- o Two promising ladders under study
 - Silicon on silicon carbide foam
 - Silicon-carbon foam (Reticulated Vitreous Carbon, RVC) sandwich

Ladder	Material	X/X ₀
Silicon on SiC foam (~ 8% density)	Silicon (25 μm), SiC foam (1.5mm); silicone adhesive (~ 300 μm)	0.16% (~ 0.26% at glue pad)
Silicon on low density SiC foam (~ 5%, not yet made)	Silicon (25 μm), SiC foam (1.5mm), silicone adhesive (~ 300 μm)	0.09% (~0.19% at glue pad)
Silicon-RVC foam sandwich (~ 3% density)	Silicon (25 μm) ×2; RVC foam (1.5mm); silicone adhesive (~100 μm) ×2	0.08% (0.14% at glue pad)



Linear Collider Flavour Identification

- o Energetic programme, with activities including:
 - Simulation and Physics Studies
 - Sensor Development
 - Readout and Drive Electronics
 - External Electronics
 - Integration and Testing
 - Vertex Detector Mechanical Studies
 - Test-beams

→ *LCFI is active in developing the full vertex detector*

