New developments on Si-sensors and common ideas with Paris group

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SiLC common interests

LPNHE

- Very active in developing new sensor readout chips and control electronics
- Interested in thin sensors and novel wiring tech
  chip/Si-module

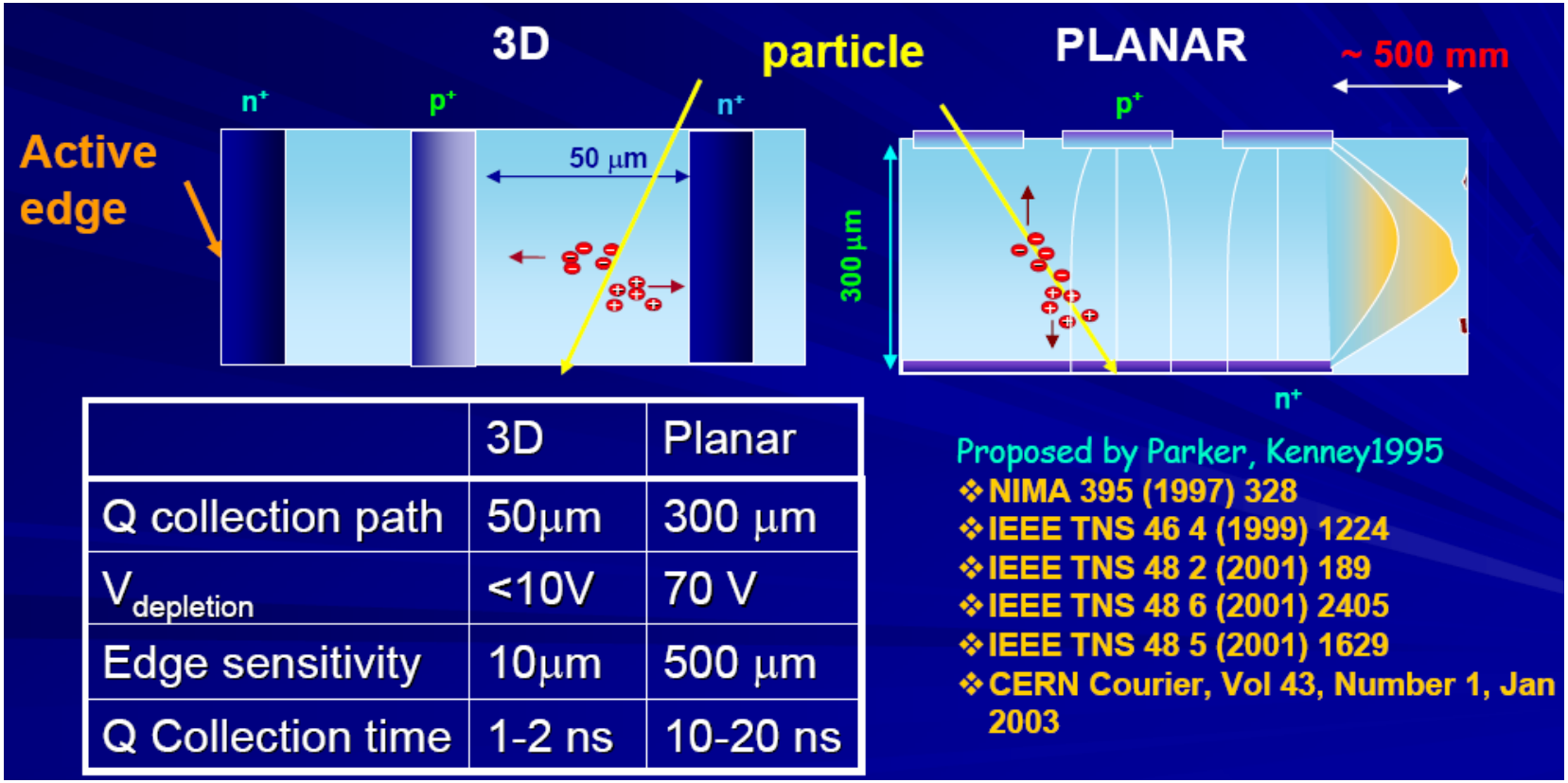
UH/HIP

- Is sensor developer, interested in new 3D technology
- Has access to one of the largest microelectronics centers in Europe (VTT)

• Main objectives of SiLC are to develop new readout and new sensor types
• Helsinki & Paris want to combine their expertise & technology to produce and test new sensor design in next year's EUDET/SilC test beam
• Both groups will benefit a lot from training with this year's (23.10-05.1) silicon test beam

3D sensor technology

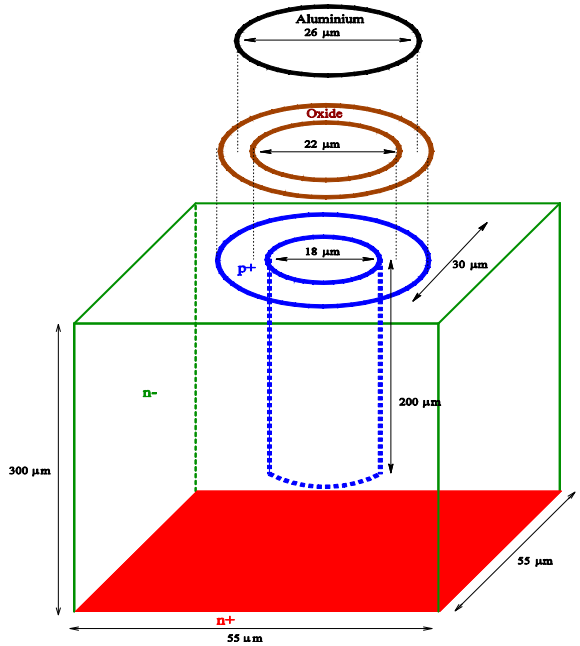
- 3D structures within a silicon detector offer a large amount of advantages: very radiation hard, fast response, small operating voltages and sensitive up to the edge
- Some of these are very attractive to ILC designs:
  - when bonding 2 or 3 sensors you reduce the insensitive area between sensors.
  - These sensors can be made very thin, since charge collection happens along the length of the sensor, rather than the vertical thickness of the sensor.



	3D	Planar
Q collection path	50μm	300 μm
$V_{depletion}$	<10V	70 V
Edge sensitivity	10μm	500 μm
Q Collection time	1-2 ns	10-20 ns

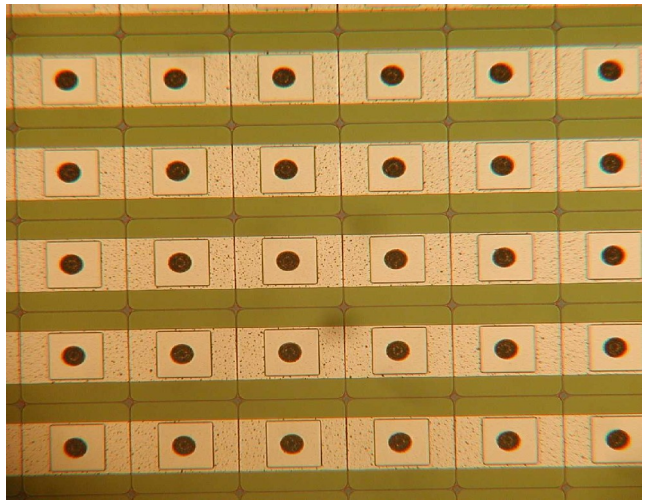
Some existing designs and characterized sensors

Layout of semi 3D
MEDIPIX2 pixel detector



- **Pixel pitch: P=18 µm**
- **vertical pilar: D=18 µm, depth=200 µm**
- **p-type implant: D=30 µm**
- **contact window: D=22 µm, metal: D= 26 µm**
- **300 µm wafer, n-type resistivity > 6 kΩcm**

Fabricated full scale semi 3D
strip detector, 4 cm^2

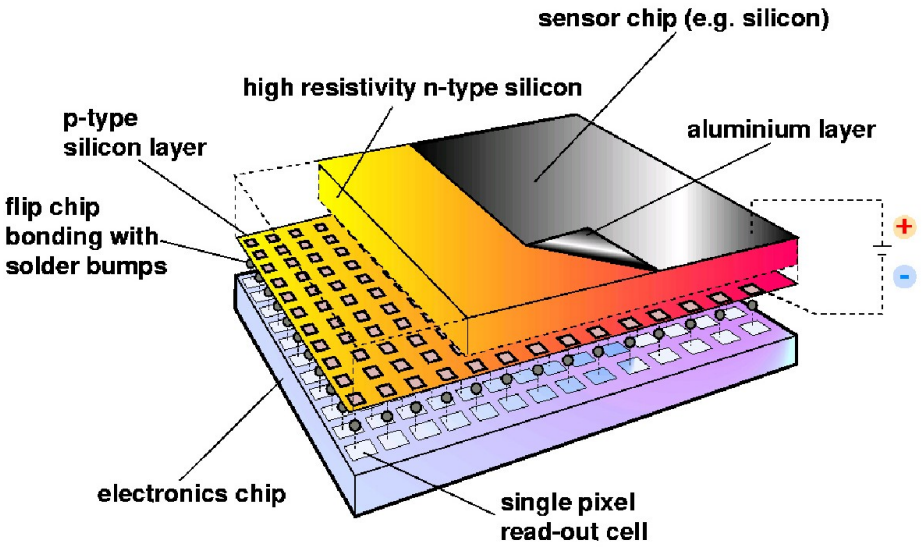


Characterization

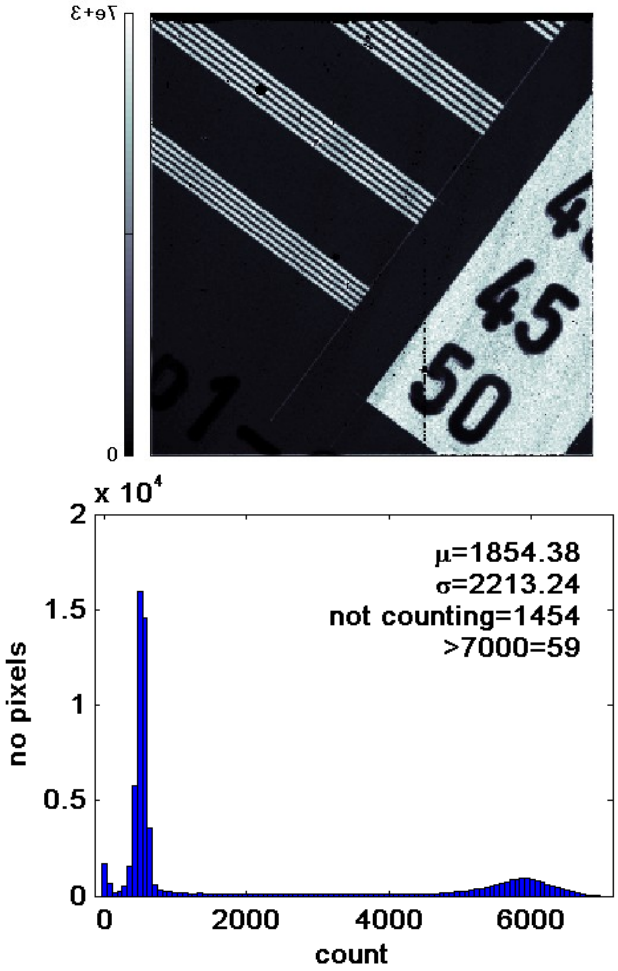
- Leakage currents from 250 to 300 fA/pixel at 80 V.
- Detector fully depleted at 30 V.
- Full depletion capacitances from 3 to 4 fF/pixel.
- Radiation hardness demonstrated (24 GeV/c protons at CERN): depletion voltage below 100 V at fluencies $6 \cdot 10^{15}$ cm^{-2}.

Coupling the semi 3D chip into readout system

MEDIPIX2 readout chip



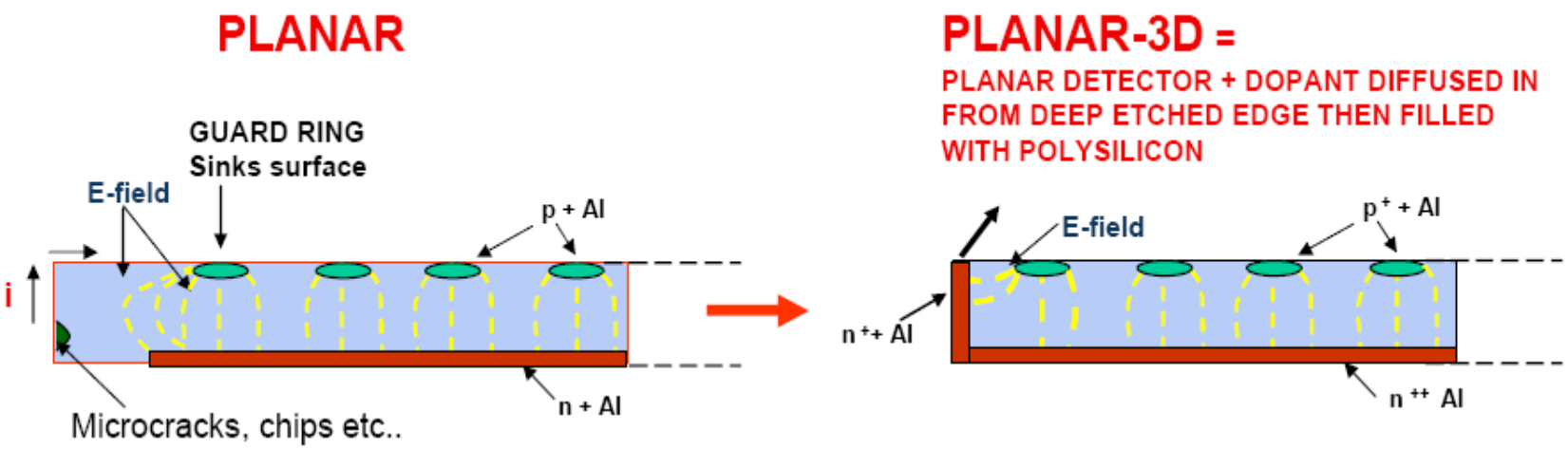
X-ray image of semi 3D detector with W-tube, 35 kV



- 256 x 256 pixel, 55 µm pixel pitch
- sensitive area ~2 cm^2
- fabricated in 0.25 µm technology
- double-threshold energy window discriminator
- 13-bit counter with max count rate of 1 MHz

New design: Planar-3D

- Full 3D sensors are not always easy to produce and handle:
  - Uniform filling of holes with polysilicon is problematic
  - Sensors can become brittle and difficult to dice (cut)
- Planar-3D sensors can be a new successful solution satisfying most of the good qualities from true 3D designs
  - **In planar-3D detectors the n-doped active edge is done by using ICP-etching (trench that surrounds the sensor) and poly-silicon filling.**
  - **Active edge avoid inhomogeneous electric fields and surface leakage currents and permit large active/inactive area ratio (tiled sensors).**



Proposal for EUDET/SiLC

- To process and test a batch of sensors with this new design concept, using LPNHE readout chip and steering electronics
- Match our geometry and electrical specs as early as possible in the design to avoid major design and/or readout modifications
- To make a thorough evaluation and characterization of this new sensor type and publish this in scientific community

Basic design specifications

• Detector material: n-type, resistivity > 7 kΩcm

→ Planar depletion voltage **3.9 V @ 100 μm thickness (underlined agreed thicknesses)**

8.8 V @ 150

15.6 V @ 200

24.4 V @ 250

35.1 V @ 300

Comment: Depletion voltage can be further lowered with the 3D/Semi-3D structures, but so far it has been agreed on strips

• Strips: p-type, pitch 50 μm, DC-coupling

• Device size: 9x9 cm^2 – fabrication on 150 mm silicon on insulator (SOI) wafers

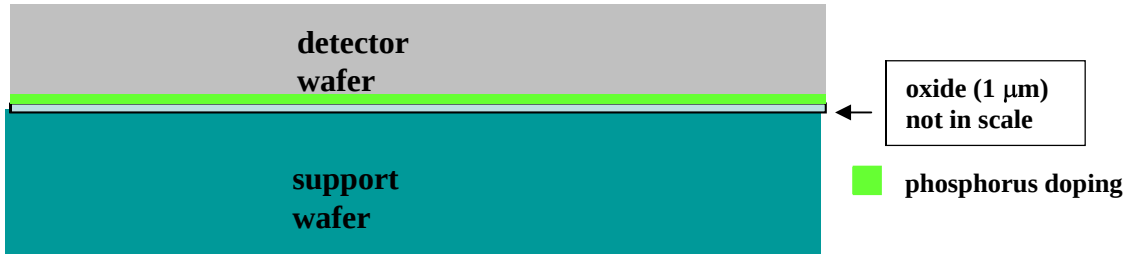
• Radiation hardness enters through reduced thickness dimension – no extra tricks like CZ-material, p-type substrate or 3D/Semi-3D structures are not applied

• Active edge (dead space ≈ 20 μm) achieved through deep silicon etching & n-type poly fill

• Dicing: the chips are diced using deep Si-ething released from the support substrate

Some details on the processing steps

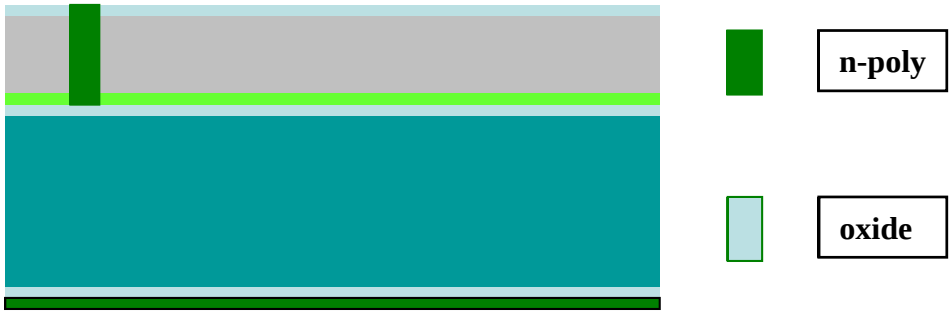
1. Phosphorus implant on detector wafer & bonding to the oxidized support wafer.
Implantation (doping) before bonding



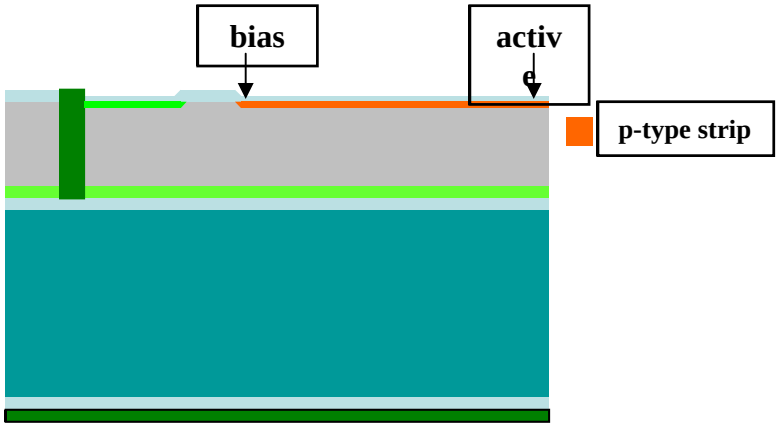
2. Grinding and CMP (polishing) of the detector wafer: detector final thickness achieved

3. Field oxide & active edge formation:

- **Oxidation**
- **Deep silicon etching of edge trench & n-poly fill**

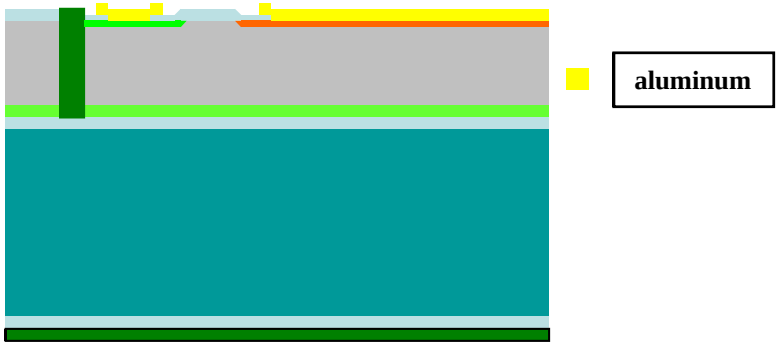


n$^+$-poly encircles the chip



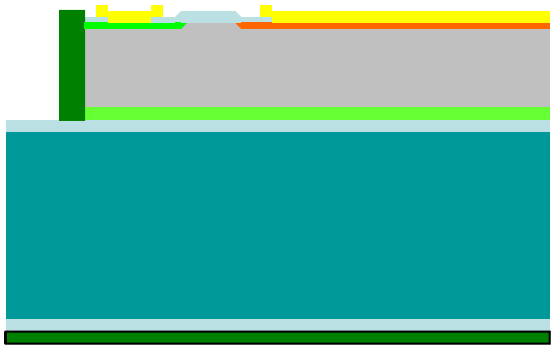
4. Implantations: p-and n-type dopings

- p-type doping forms the active strips
- n- type doping is for bias contact in appropriate location → strip area must be sacrificed (?)



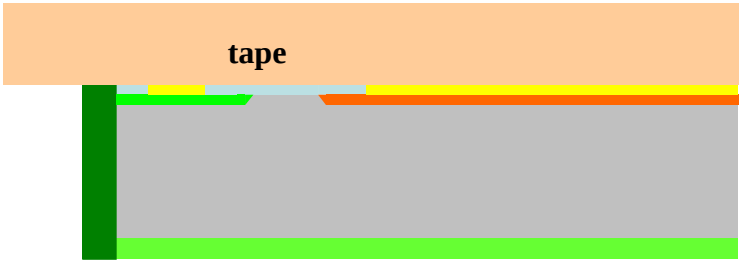
5. Contact windows and metal

- open contact windows to silicon through oxide
- deposite and pattern the aluminum metal



6. Device separation with deep silicon etching

- Detectors are separated using deep silicon etching outside active edge structure



7. Release from support wafer

- attach to tape & grind and etch support wafer away from back

Time Scale & Cost estimate:

- Total cost for a batch of O(20) sensors would be O(40 Keur.)
- VTT has committed themselves 20Keur to this project
- O(20 Keur) to be paid by Helsinki/Paris
- Processing can go fast (masks etc. are available), major time factor depends on substrate material
- If VTT orders material now, we can expect sensors by spring 2007