EUDET Annual meeting, Oct 18-20, 2006
MPI-Munchen

JRA2-Status: SiTRA

A. Savoy-Navarro, LPNHE-IN2P3/CNRS
On behalf of SiTRA Collaboration

EUDET Participants de SiTRA

Members

- HIP, Helsinki (Fi)
- LPNHE, Paris (Fr)
- CU, Prague (CZ)
- IFCA, Santander (Sp)

Associates

- IMB-CNM, Barcelona (Sp)
- IEKP, Karlsruhe (Ge)
- LU, Liverpool (UK)
- MSU, Moscow (Ru)
- OSU, Obninsk (Ru)
- IFIC, Valencia (Sp)

SiTRA is part of the overall SiLC R&D project
therefore includes the SiLC Collaboration
+ CERN, FNAL, SLAC (close contacts) & collab with DESY (t.b.)
and collaboration contacts with Industry

Topics

- ► R&D on new silicon sensors
- ► Towards the fabrication of new modules
- ► R&D on the electronics front
- ► 2006 beam test
- ► Prospects for 2007
  - ● Preparation of new beamtests
  - ● Developing Alignment
  - ● Developing Cooling

SiLC R&D collaboration meetings

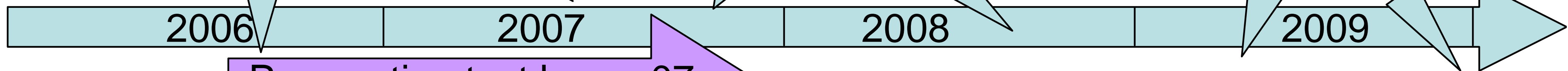
The SiLC collaboration has started to have regular meetings since the last ECFA ILC Workshop in Vienna, November'05.
proven to be quite fruitful so far.

SiTRA Roadmap & Scientific Objectives

23/10/06 -5/11/06 (Eventually more) DESY 5 GeV e- beam, S/N with: 180nm vs VA1, 30cm strips (2modules) &1 long strip module

-Juin 07: CERN 2 mod. 8'' VA1-130nm
-Nov. 07: FNAL (CERN)
-2008: Full size Si detector pro.; combined tests(small calo, F.C. +TPC), B field with various Si prototypes and 128 ch chips

Spring'09: FNAL(CERN) Combined test with final protos of Si tracker, calo and TPC, within B field new foundry FE chips, cooling and alignment protos



Preparation test beam 07: 128ch chips & detector protos

Prepa test beam 09:new chips & new detector protos, cooling & alignment

SiTRA deliverables: VDM FE readout chips to equip test beam prototypes

Large area SIlicon tracking structure prototypes
Cooling & Alignment systems
Series of testbeams Si alone or combined (see Roadmap)

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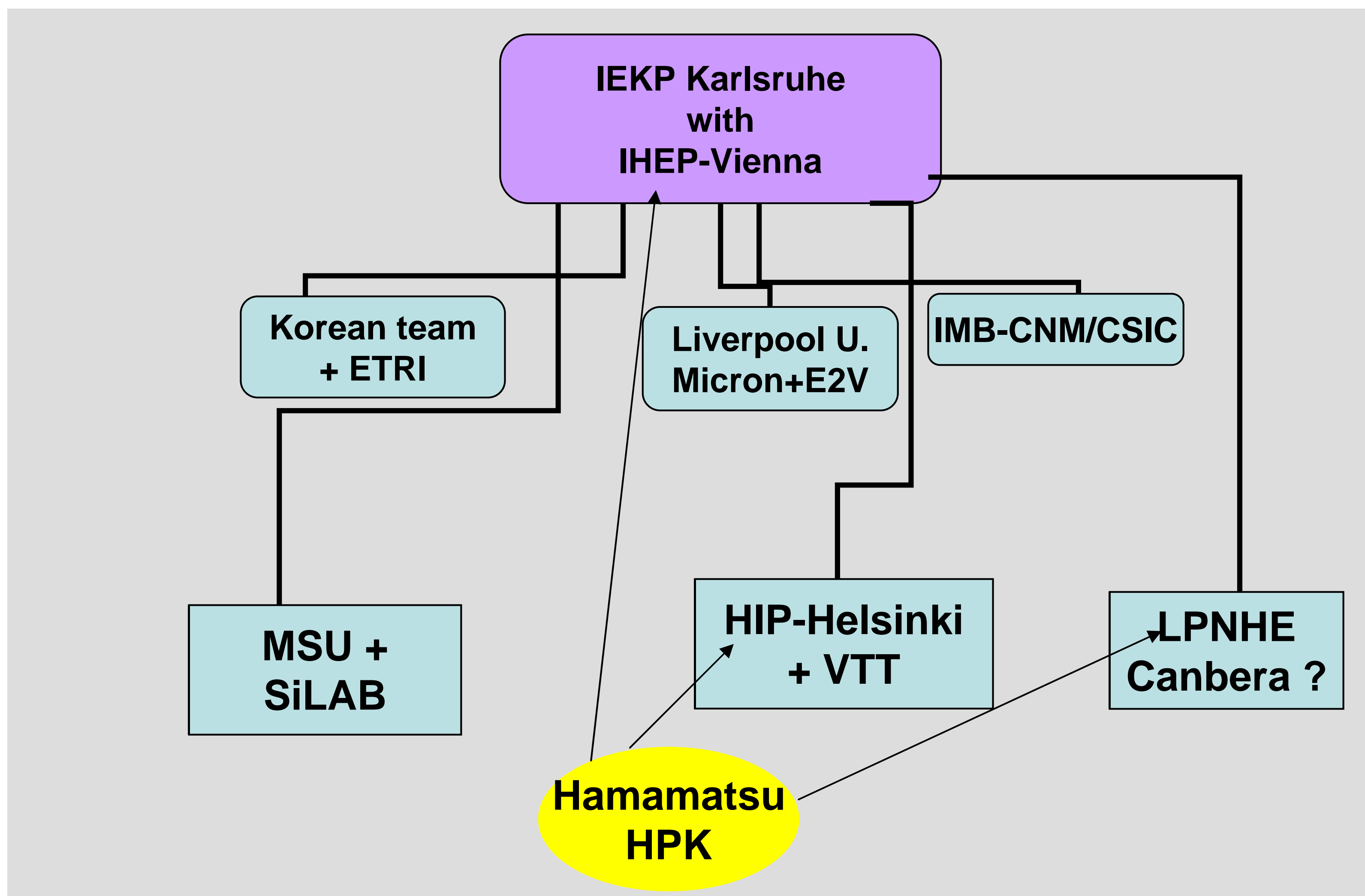
Immediate goals (prototypes in 07):

- Larger single-sided wafer **(8'')** microstrips
- Larger double-sided wafer **(6'')** microstrips
- Eventually thinned (1/2 or 3)
- Starting to develop new tech prototypes:
  - -> see VTT
  - -> see novel wiring

R&D on Si sensors: organisation



Helsinki-Paris proposal for new sensors

(N. Van Remortel (HIP-Helsinki) and VTT)

Helsinki (sensor devel.) & Paris (readout chip & electronics) want to combine their expertise & technology to produce and test new sensor design in next year's EUDET/SilC test beam

Planar 3D concept by Helsinki

3D structures within a silicon detector offer a large amount of advantages:

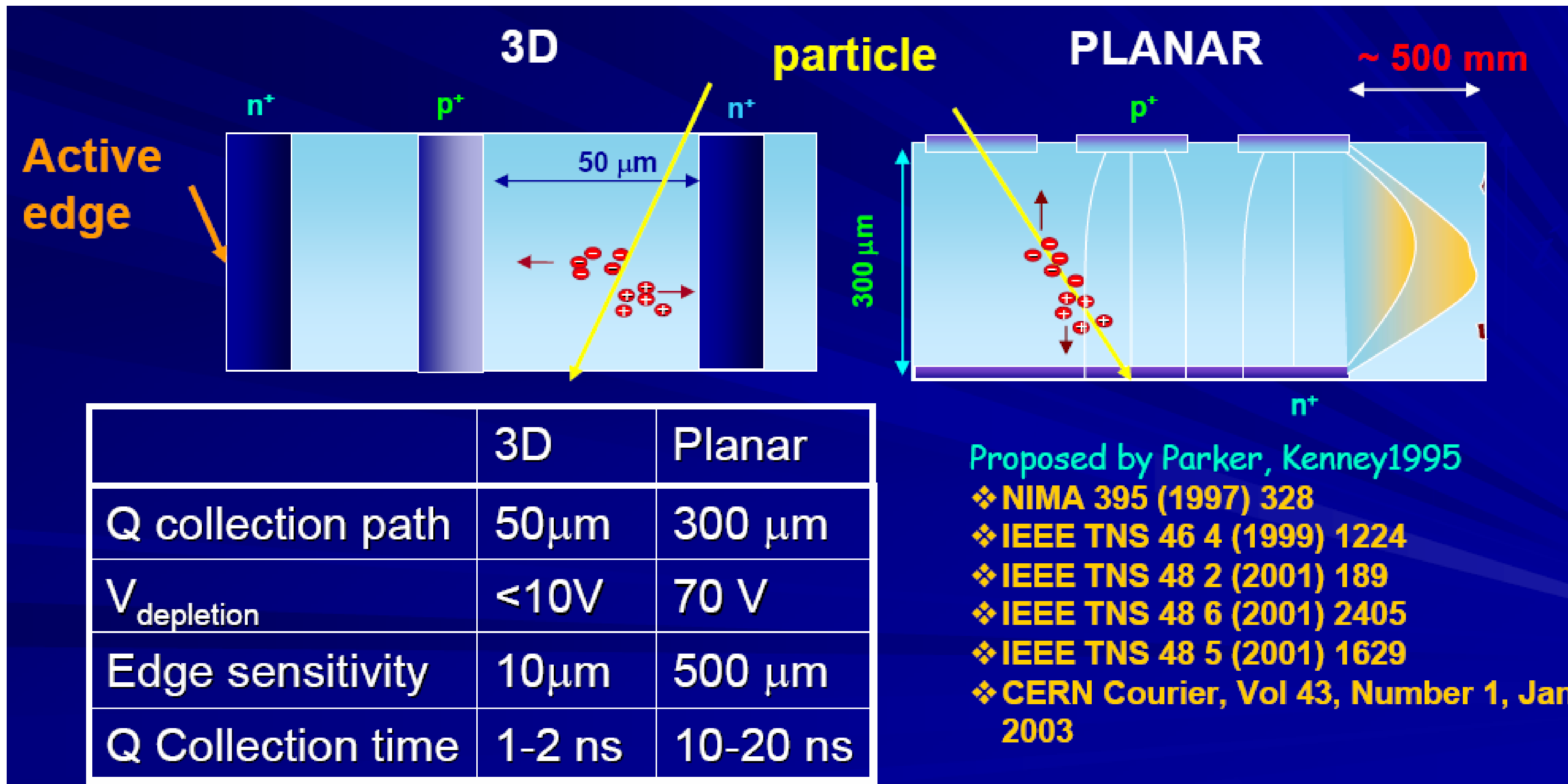
- very radiation hard
- fast response
- small operating voltages
- sensitive up to the edge

Some of these are very attractive to ILC designs:

- when bonding several sensors you reduce the insensitive area between sensors.
- sensors can be made very thin, since charge collection happens along the length of the sensor, rather than the vertical thickness of the sensor.

Benefits of 3D technology

Prepared by N. van Remortel (HIP-Helsinki) and VTT



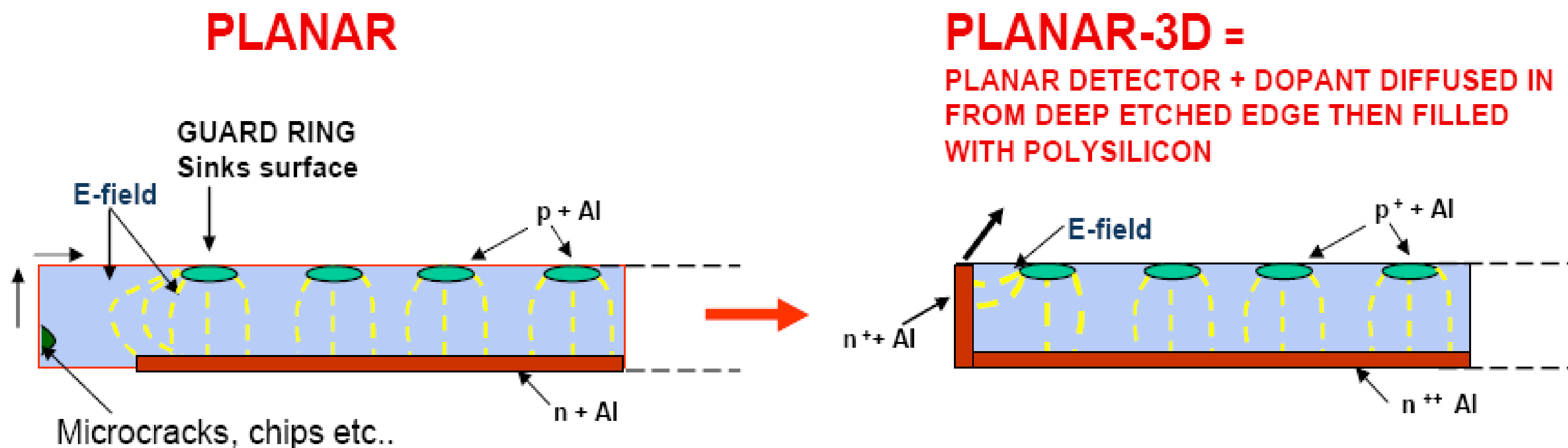
	3D	Planar
Q collection path	50µm	300 µm
$V_{depletion}$	<10V	70 V
Edge sensitivity	10µm	500 µm
Q Collection time	1-2 ns	10-20 ns

BUT:

- Full 3D sensors are not always easy to produce and handle:
  - **Uniform filling of holes with polysilicon is problematic**
  - **Sensors can become brittle and difficult to dice (cut)**

Planar-3D sensors

- Planar-3D sensors can be a new successful solution satisfying most of the good qualities from true 3D designs
  - In planar-3D detectors the n-doped active edge is done by using ICP-etching (trench that surrounds the sensor) and poly-silicon filling.
  - Active edge avoid inhomogeneous electric fields and surface leakage currents and permit large active/inactive area ratio (tiled sensors).



- Total cost for a batch of O(20) sensors would be O(40 Keur.)
- VTT has committed themselves 20Keur to this project
- O(20 Keur) to be paid by Helsinki/Paris
- Processing can go fast (masks etc. are available), major time factor depends on substrate material
- If VTT orders material now, we can expect sensors by spring 2007

Pepared by N. van Remortel (HIP-Helsinki) and VTT

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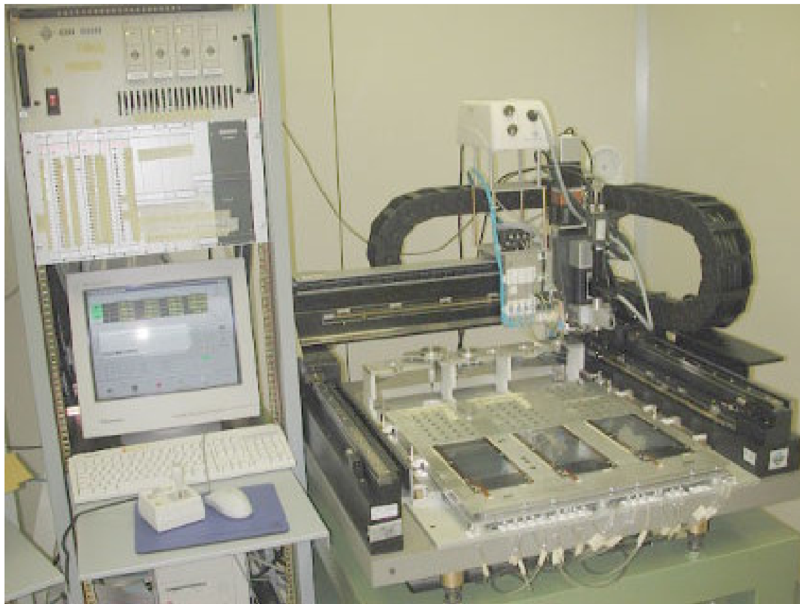
The elementary module: tile of the overall architecture

Based on present experience (LHC) must be light, precise, robust, easy to build & assemble:

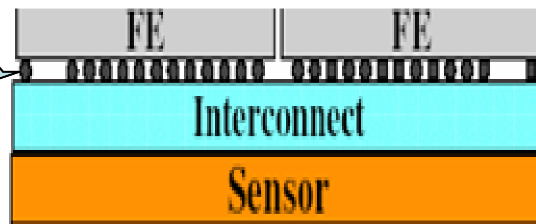


Robotic assembly (CMS)

- **New sensors (next generation)**
- **Support: new material &design**
- **VDSM FE electronics & wiring**
- **Precise positioning on the module & the support structure**
- **Easy to build (robotisation ?)**
- **Industry transfer: big number**
- **Favouring a ''universal tile'' (instead of different shapes)**

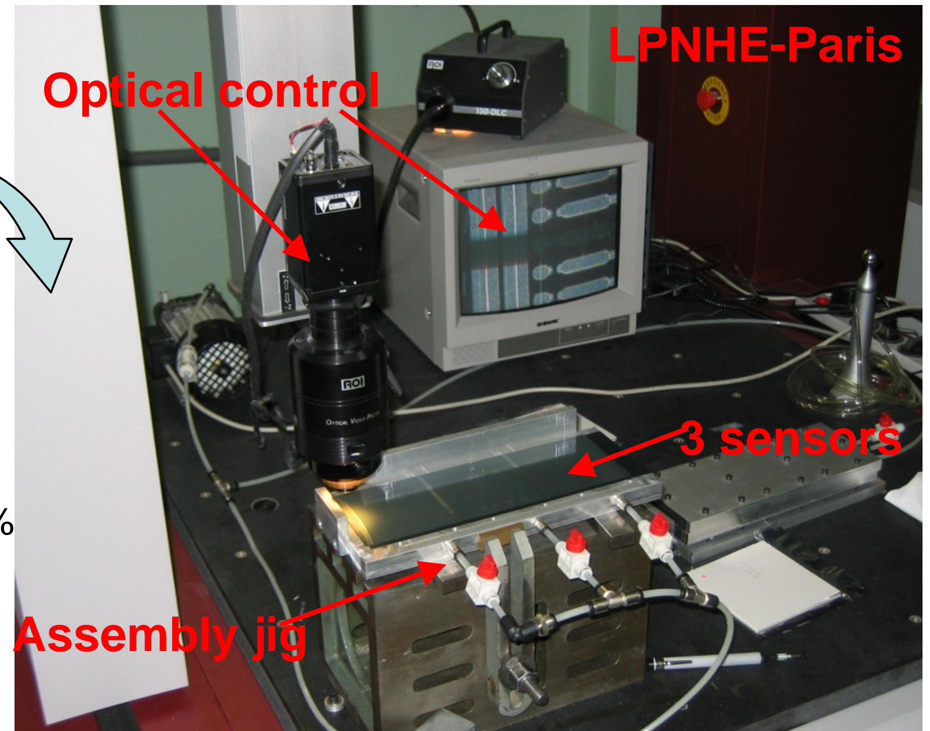
R&D on the new elementary module concept

LPNHE-Paris, IMB-CSIC, and others in SiLC



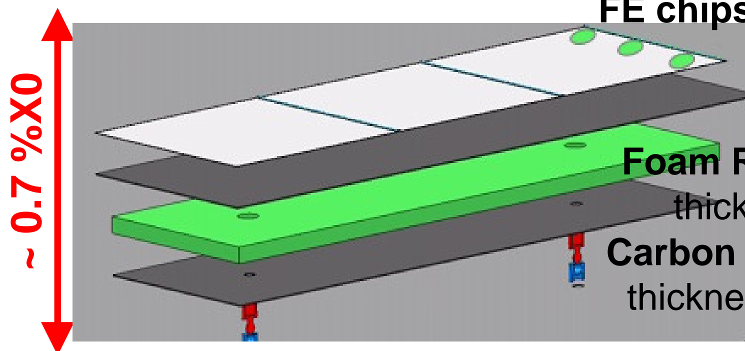
New wiring of FE chips onto the detector: under investigation

LPNHE-Mechanics& Electronics, Paris/CNRS-IN2P3



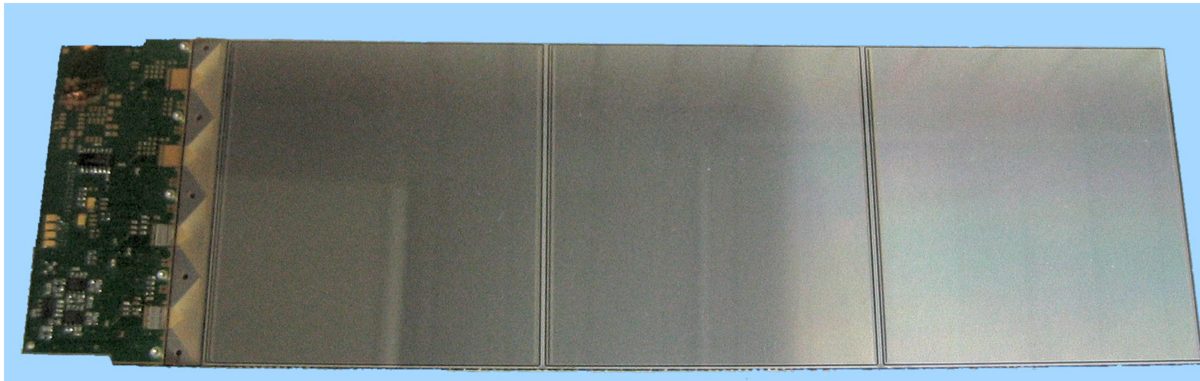
Si sensors: 0.3%X0

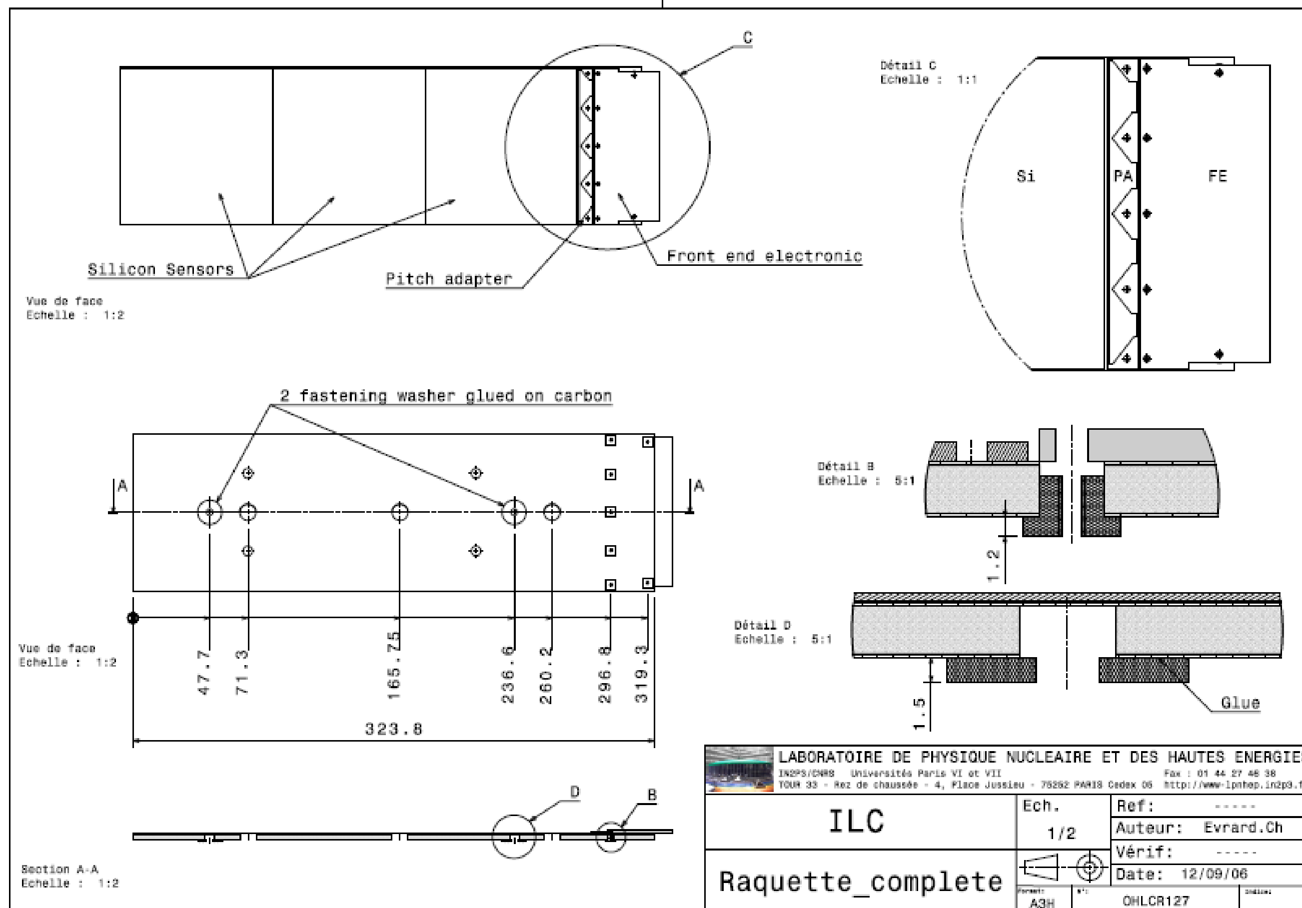
FE chips: ~0.1%X0+?

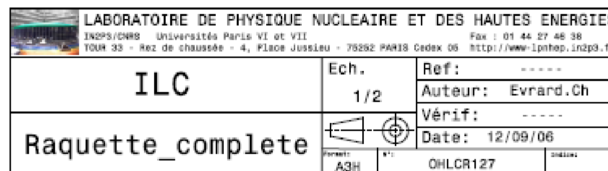


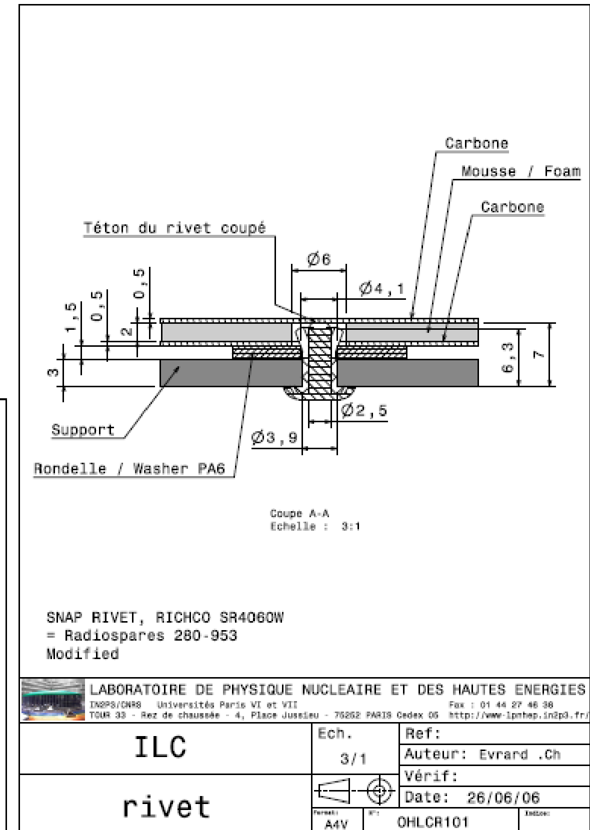
Foam Rohacell 0.05%
thickness ~ 4mm

Carbon f. 0.15% X0
thickness ~ 0.4mm









LPNHE: construction of module-3CMS:
First attempts to gain expertise, thanks to . the collaboration with A. Honma et col. CERN

New sensors, new modules

- **New sensors**: organization with IEKP Karlsruhe as coordinator helped by IEHP Vienna.

  Need closer contacts with Industry (in progress)

  Automated fabrication line, starting to be experienced with A. Honma et al. at CERN, on very first new modules built at LPNHE.
- **New modules**: under R&D very dependent of the technology used for wiring the electronics on detector. Collaboration with industry (sensor fabs and chip foundry) is starting including teams from SiLC.

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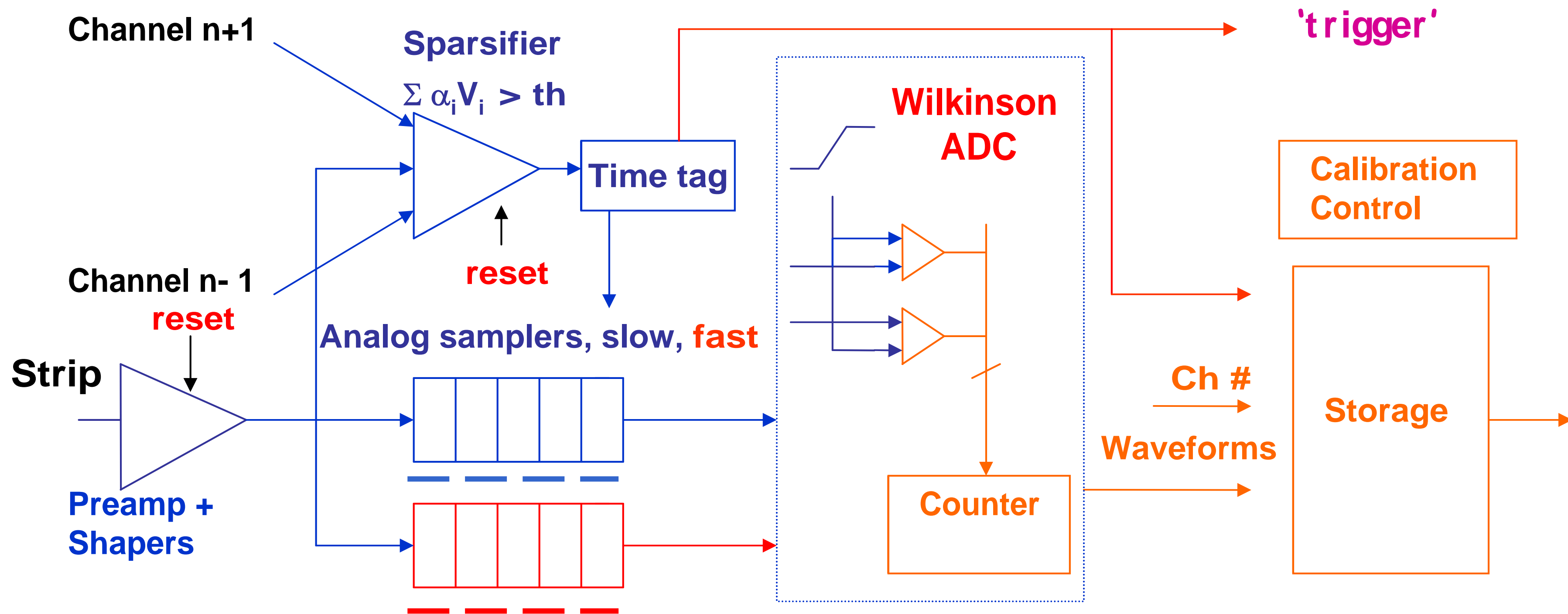
Foreseen Front-end architecture

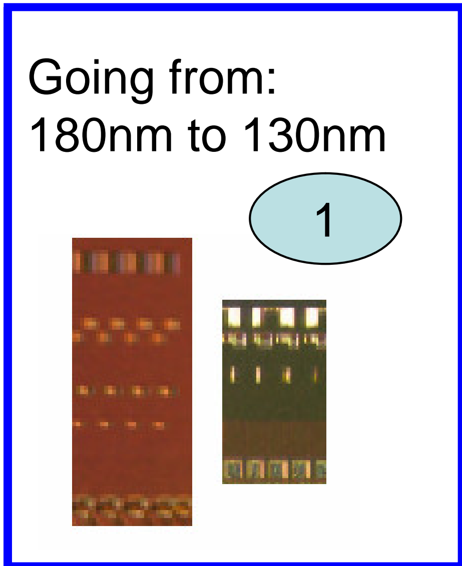


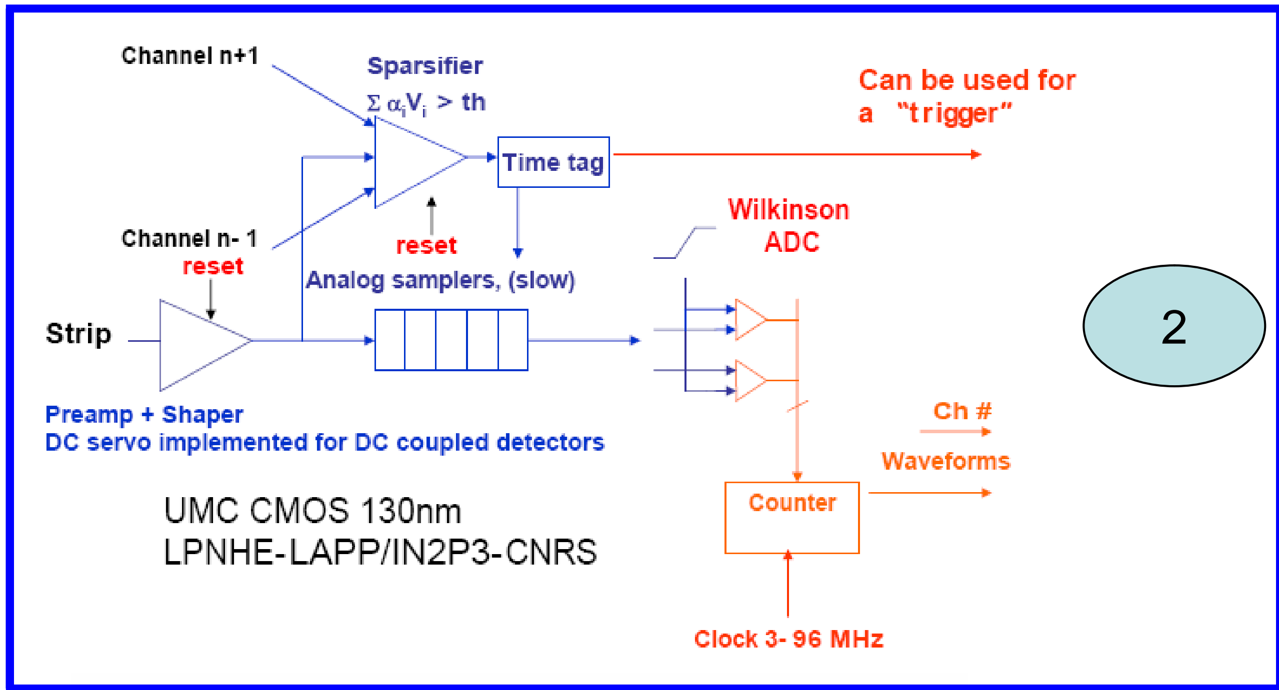
Charge 1-40 MIP, Time resolution: BC tagging 150-300ns, fine: ~ 1ns

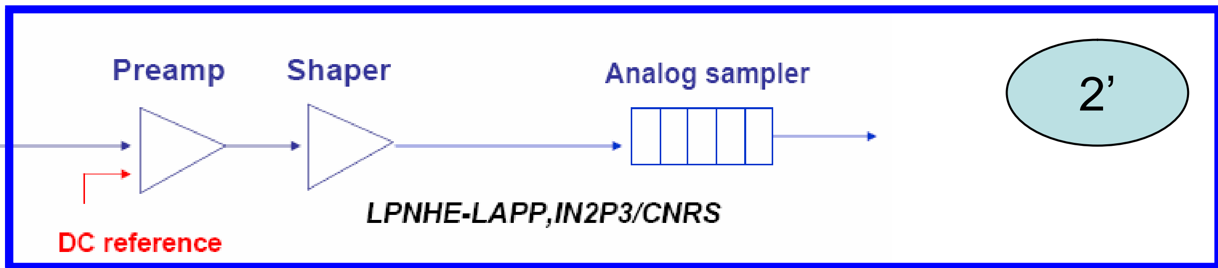
Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

FE readout Electronics main achievements in 2006

Going from:
180nm to 130nm







Starting now: 3
Test of the first chips UMC-180nm and later UMC-130nm connected to a Si module at the Lab test bench and then at the DESY beam test; ***from chip to demonstrator***

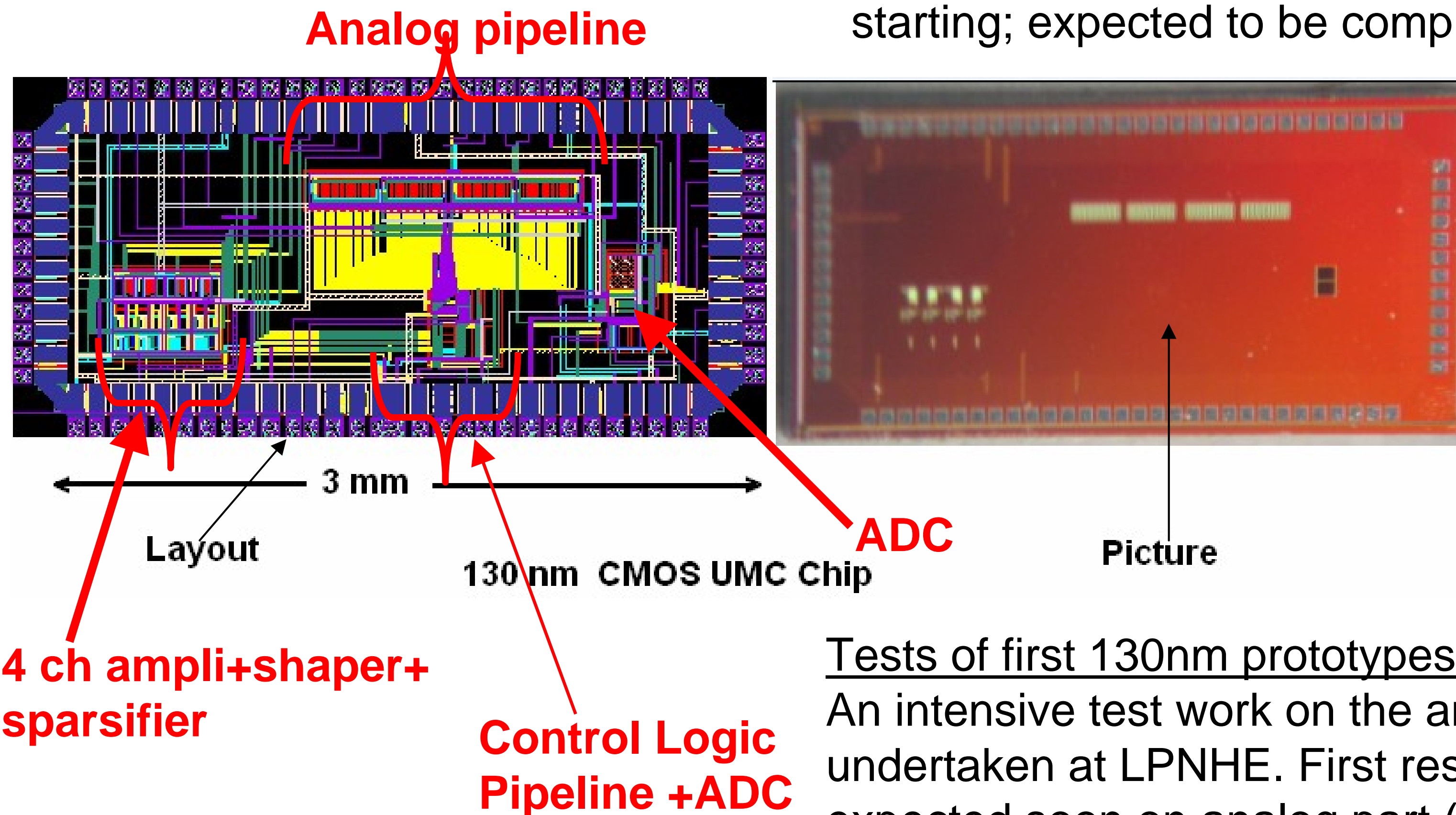
Development of the VDMS FE and r.o. chip to equip EUDET beam tests

- **First prototype in 130nm UMC techno and with full FE+ RO chain:**

LPNHE+LAPP+IMEC

submitted April 19 2006

received August 15 2006, the tests are starting; expected to be completed end 06.



<u>Tests of first 130nm prototypes:</u>
An intensive test work on the analog part is undertaken at LPNHE. First results are expected soon on analog part (noise?). Followed by tests on digital part.

VDMS FE+r.o. chip to equip EUDET t.b. (cont'd)

- ❖2nd prototype in 130nm UMC: F.E. only (improved) + DC servo+calib (LPNHE-LAPP-IMEC), sent to foundry October 4th.

- ❖3rd prototype in 130nm IBM, analog part only: CERN+LPNHE Meeting/Decision on the technology for 1st production (128 ch)

- ❖Full Prototype with 32/64 channels, before production of 128 channels. To be sent next (or go right away with 128 ch?)

- ❖Packaging, detector wiring and r.o. cards (HIP+VTT, IMB-CNM Barcelona + LPNHE + Industrial firms): starting…

Actions are conducted in parallel

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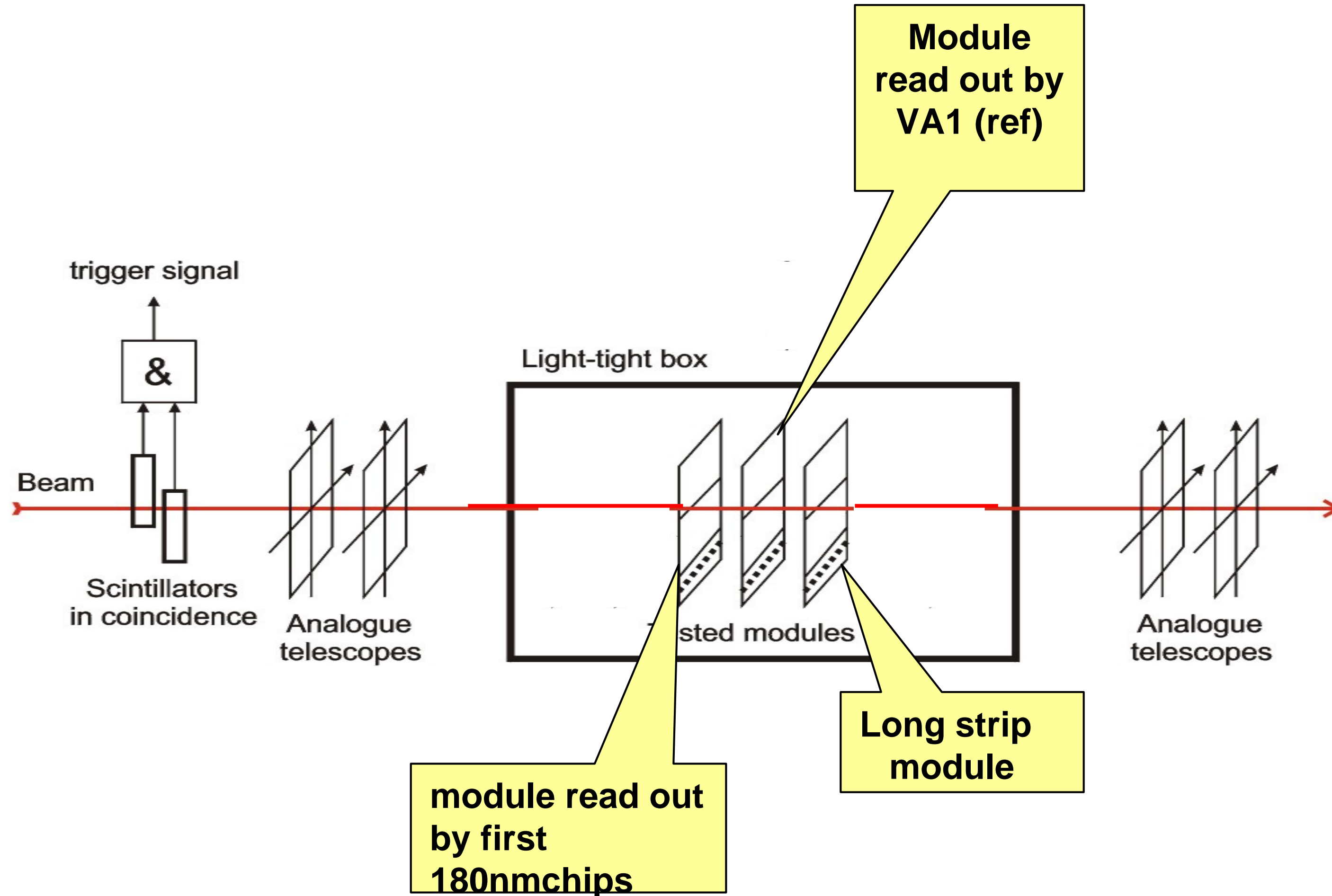
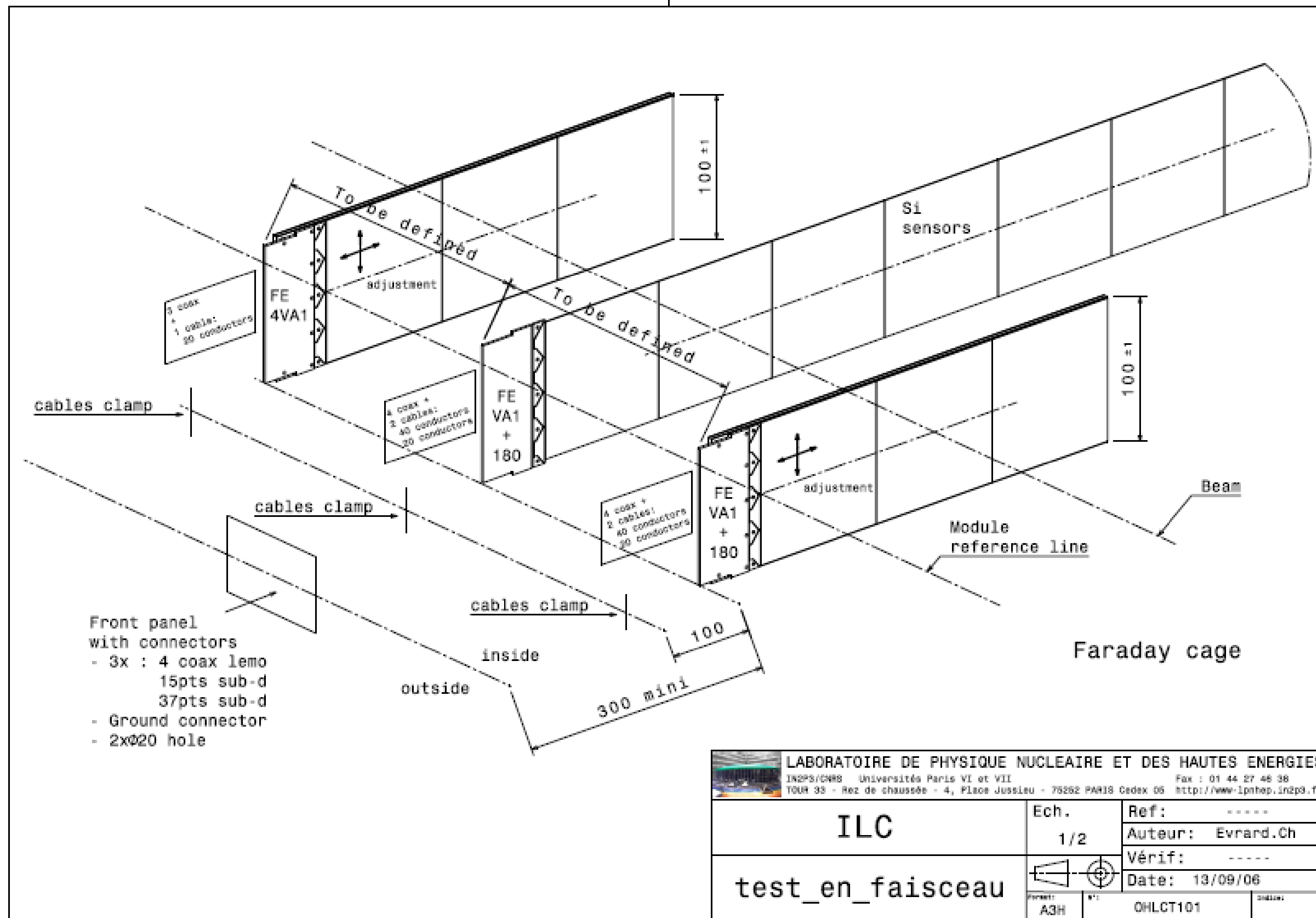
EUDET Test beams @DESY in 2006

First series of tests starting 23/10/2006 at DESY e- test beam, no magnetic field:

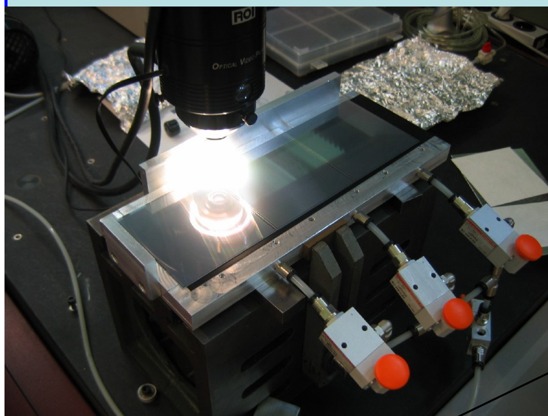
- Test new FE chip prototype (first 180 prototypes)
- Measure S/N



CAD design of the 3 modules in test set-up



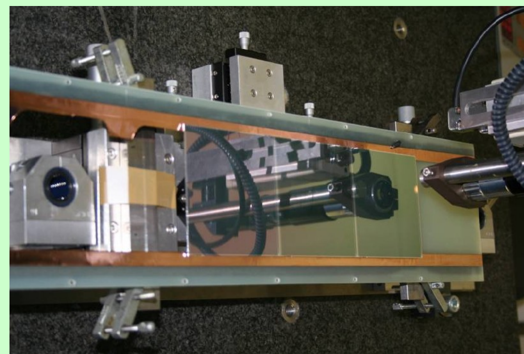
Detector prototypes:CERN (A. Honma et al.), IEKP-Karlsruhe, LPNHE-Paris, IEHP-Vienna, Hamamatsu



Assembly

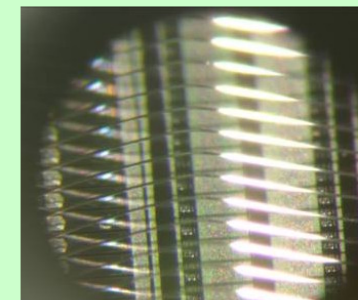
3 CMS sensors 28 cm strip long
Read out:
VA1+180UMC r.o
and all VA1 r.o.

2 modules fabricated in Paris,
bonding CERN on automated CMS system
(Collab CERN-LPNHE)
Ready by September 25th



Assembly:
Module = 10 GLAST sensors
90 cm strip long

Bonding

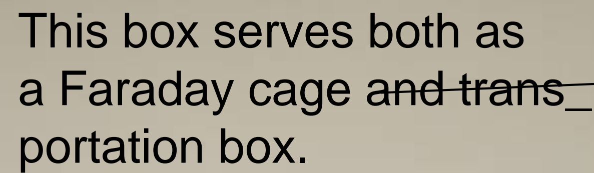


The full construction done at IEKP

R.O.
Pitch adapter +
VA1 + 180UMC
provided by Paris
Ready by September 25th

Long ladder in box

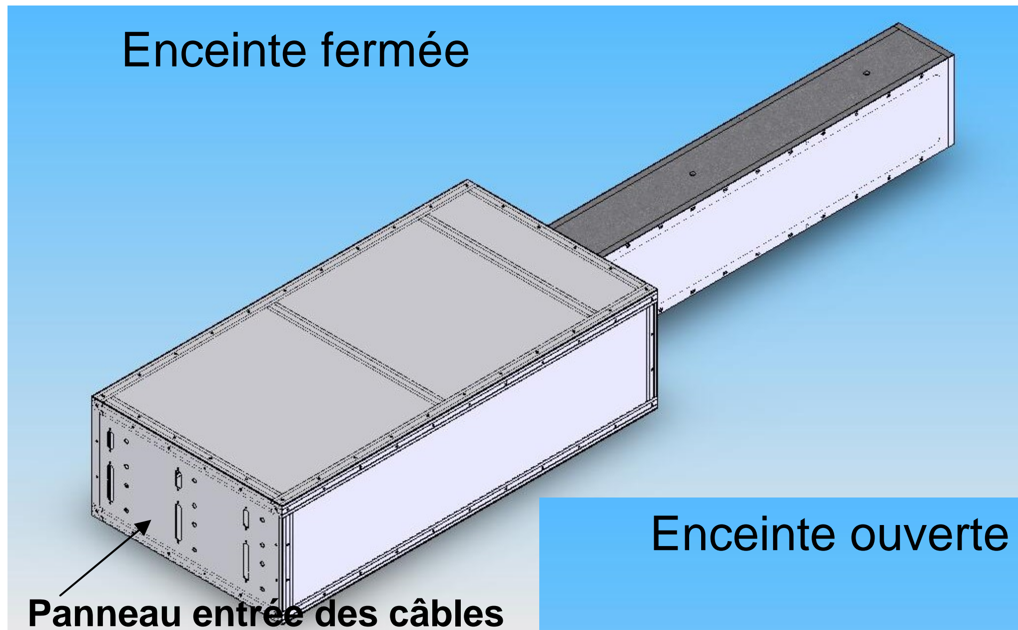
IEKP Karlsruhe

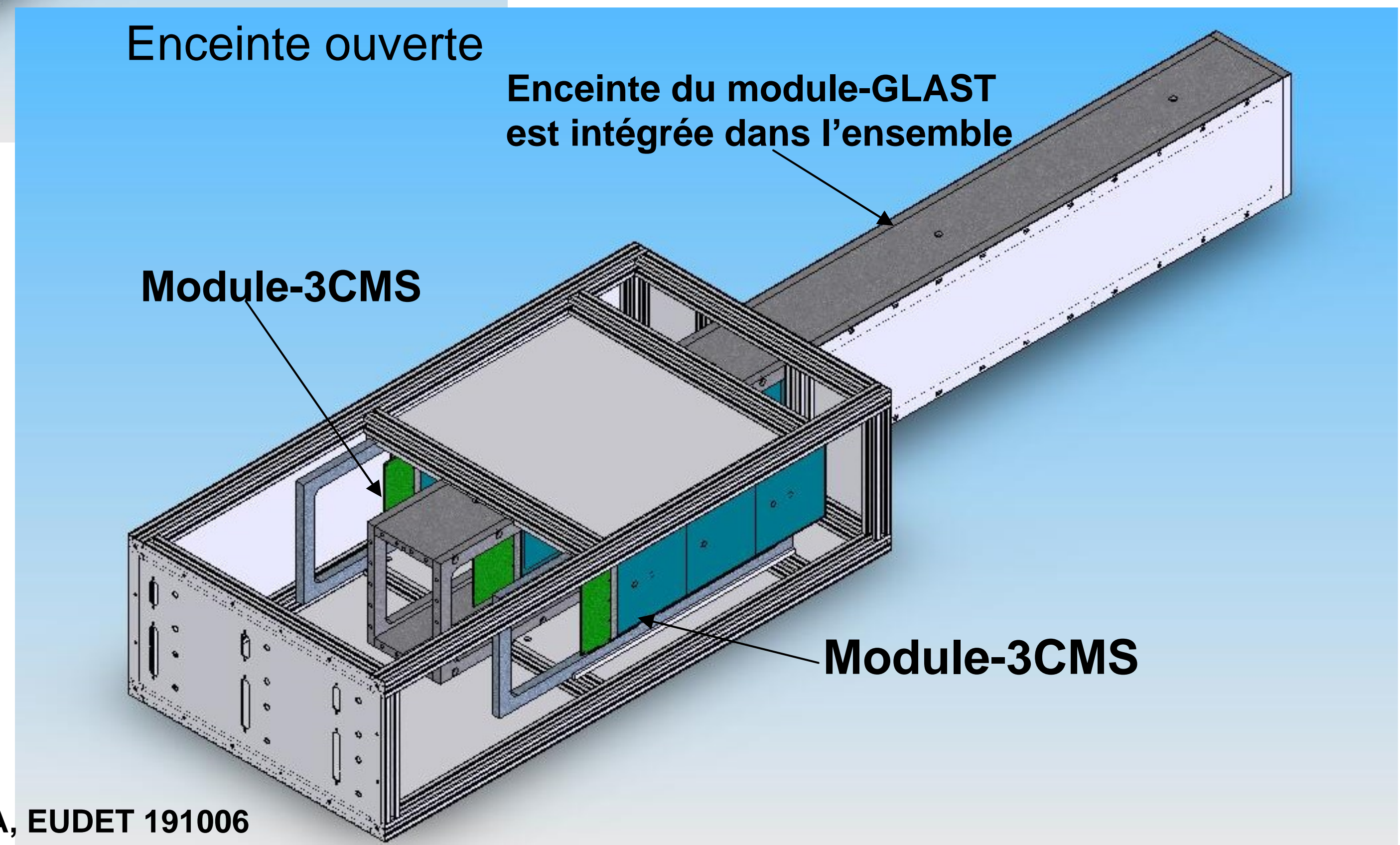


Enceinte isolante pour 2 modules-3CMS et module-10GLAST

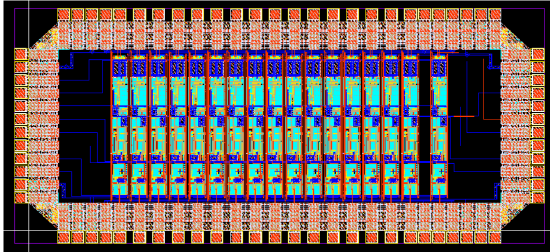
P. Modesto (IFIC-Valencia)

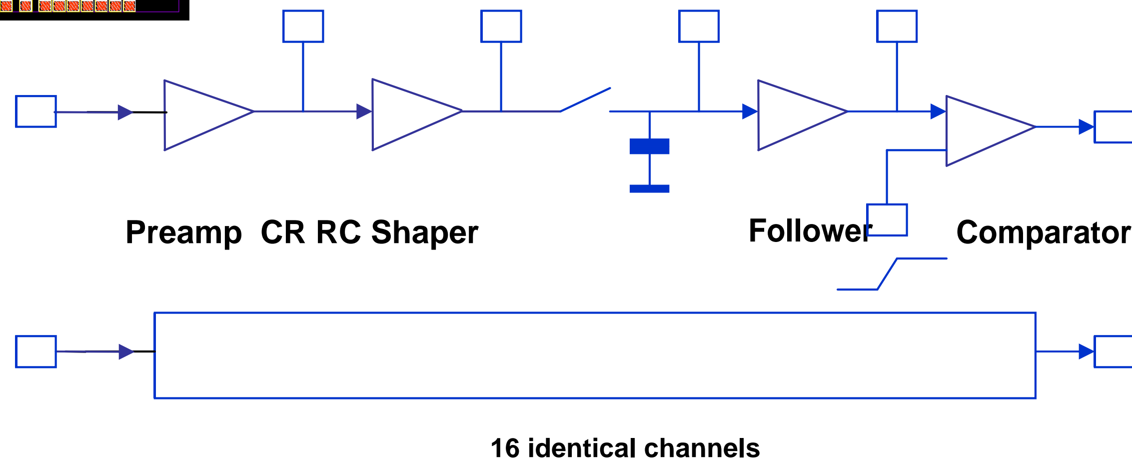
N.B. Cette enceinte est recyclable (autres modules courts)

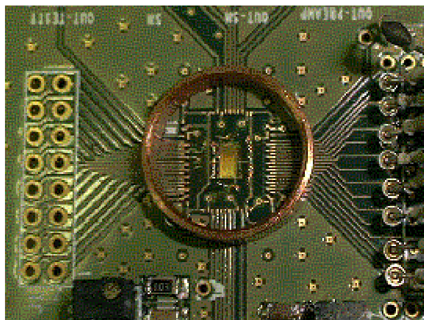




Front-end test chip in CMOS 180nm







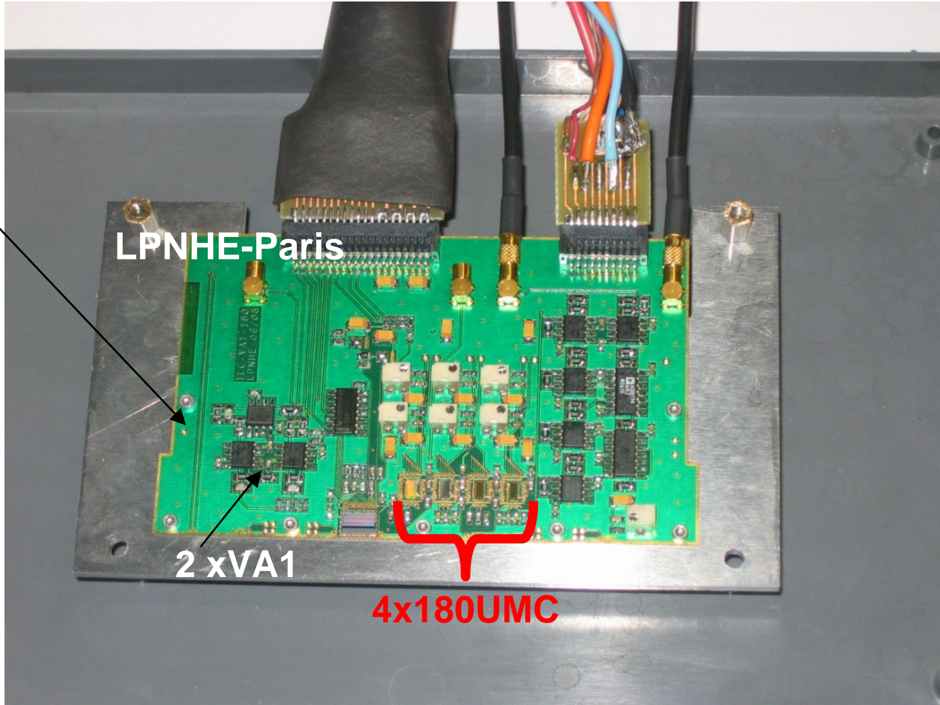
- Low noise amplif icat ion + pulse shaping
- Sample & hold
- Comparator

Readout Electronics: LPNHE Paris

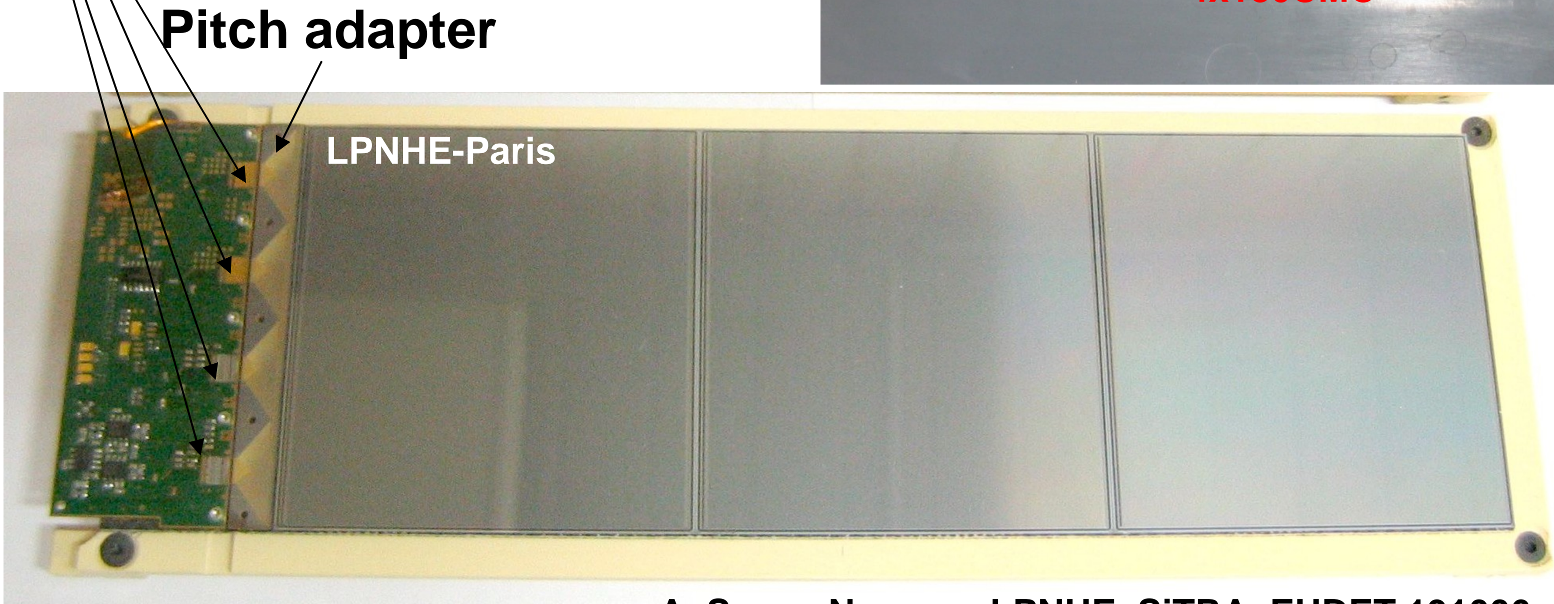
2 VA1 + 4x 180UMC channels: hybrid R.O. card under test

- VA1 r.o. card ready
- 2 hybrid r.o. cards: VA1+180UMC ready Both being tested at Paris Lab test bench

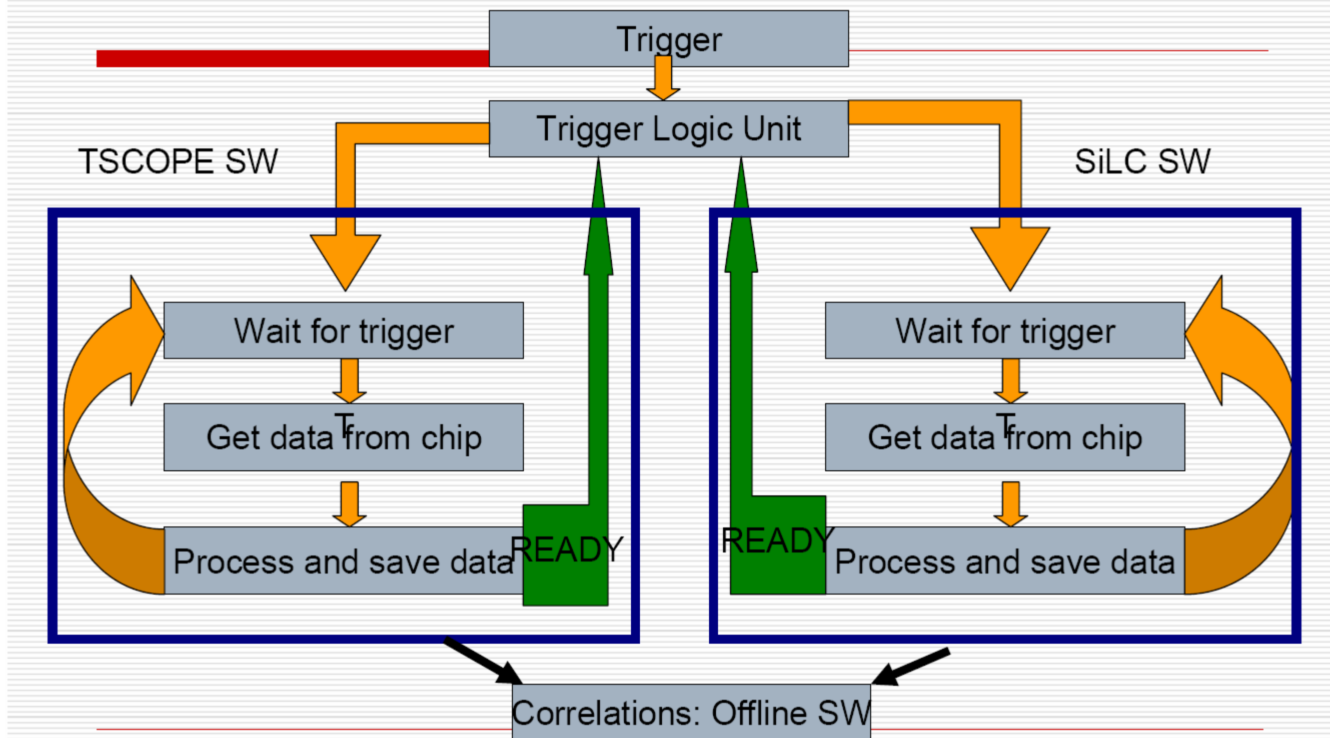
4 VA1 r.o card



Pitch adapter



DAQ: hardware & software



LPNHE-Paris:
Rebuilt its DAQ test bench
To be used both for

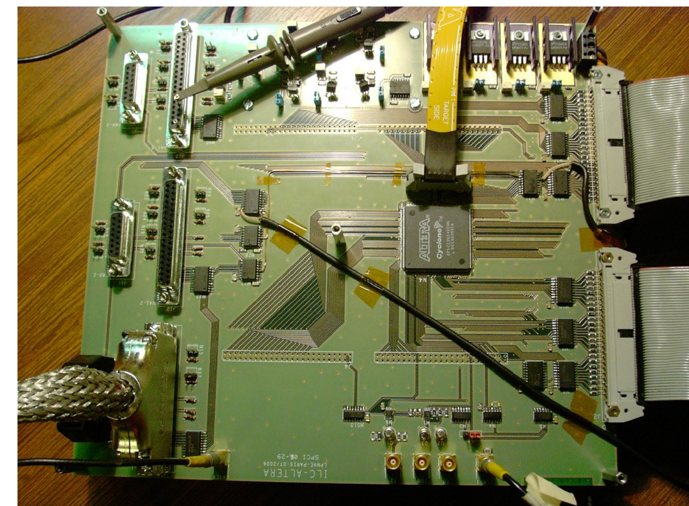
- Tests @ Lab t.b. before
- Tests @DESY t.b.

Adapted to

- new R.O. electronics
- and to link with DAQ

of the beam telescopes (mostly done, now under test).

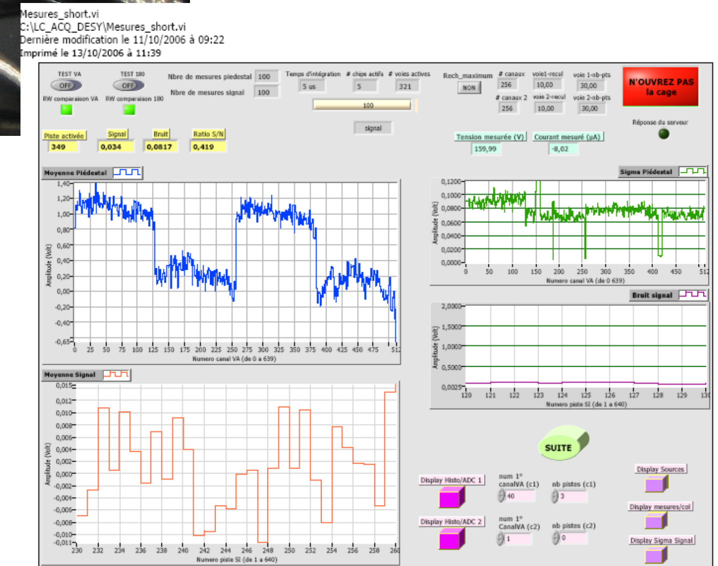
DESY and CU-Prague:
Use of the existing hardware and software developed by DESY for the beam telescopes implementing a very basic trigger logic for connecting the two DAQ systems.



Tests at the Lab Test bench before DESY

- Complete upgrade of the Paris Lab test bench
- Characterization of the new readout chips (VA1 and 180UMC)
- Characterization of the new Si modules:
  - → 2 x 3CMSmodule
  - → One long strip module
- Test of the functioning of the new DAQ hardware
  - → New command card
  - → New Altera card
  - → Effect of 15 m long cable between Altera & detector R.O.
- Test 2 DAQ's running in parallel (beam telescope and Si detector R.O.)
- Test analysis packages with Lab test bench runs

All these tests are going on at Paris Lab test bench since end of September till October 20.



Ongoing tests at the Lab test bench in Paris, before going to DESY. Karlsruhe module on the Lab test bench.

A. Savoy-Navarro, LPNHE, SiTRA, EUDET 191006

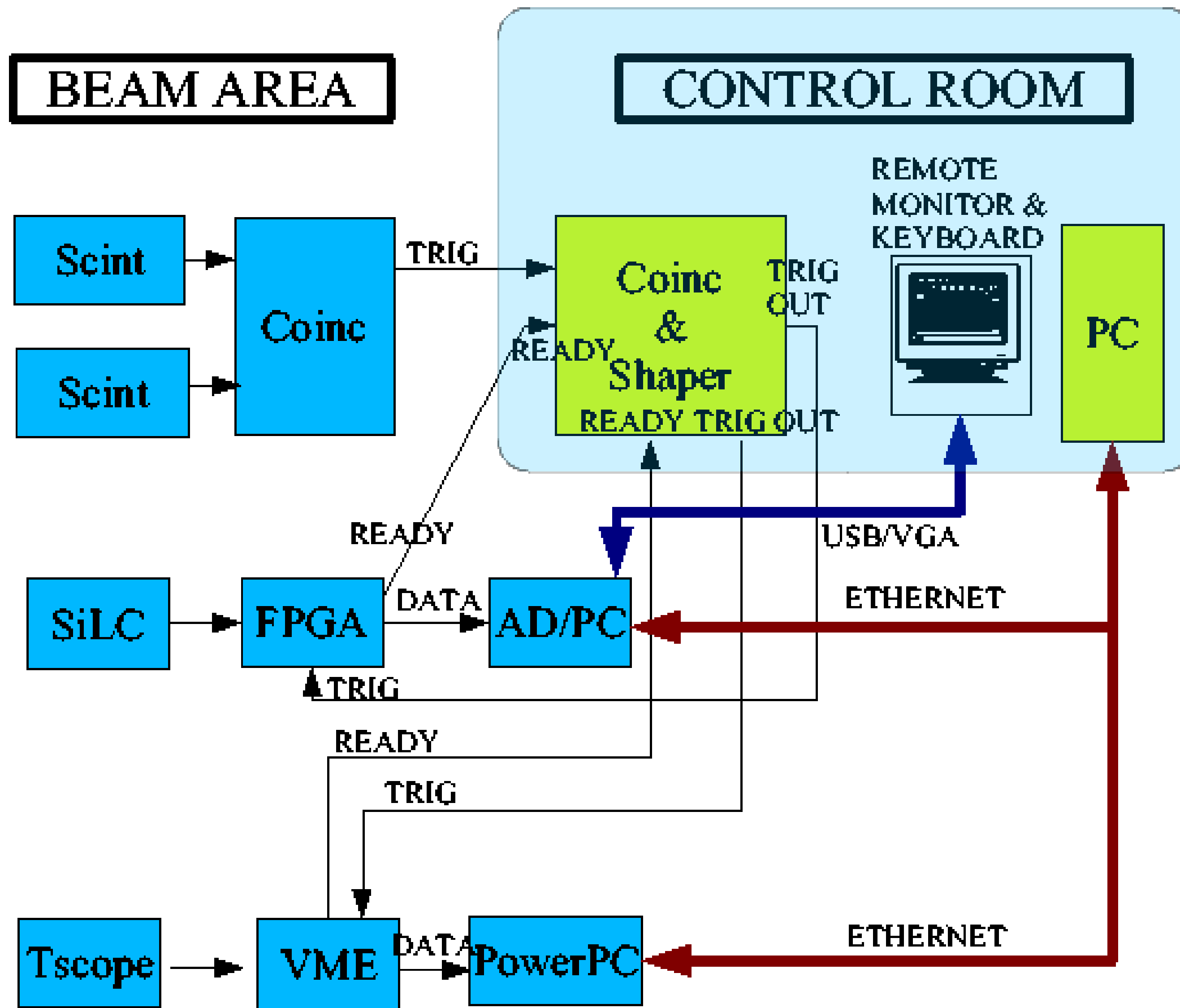
Preparation for the DESY test beam

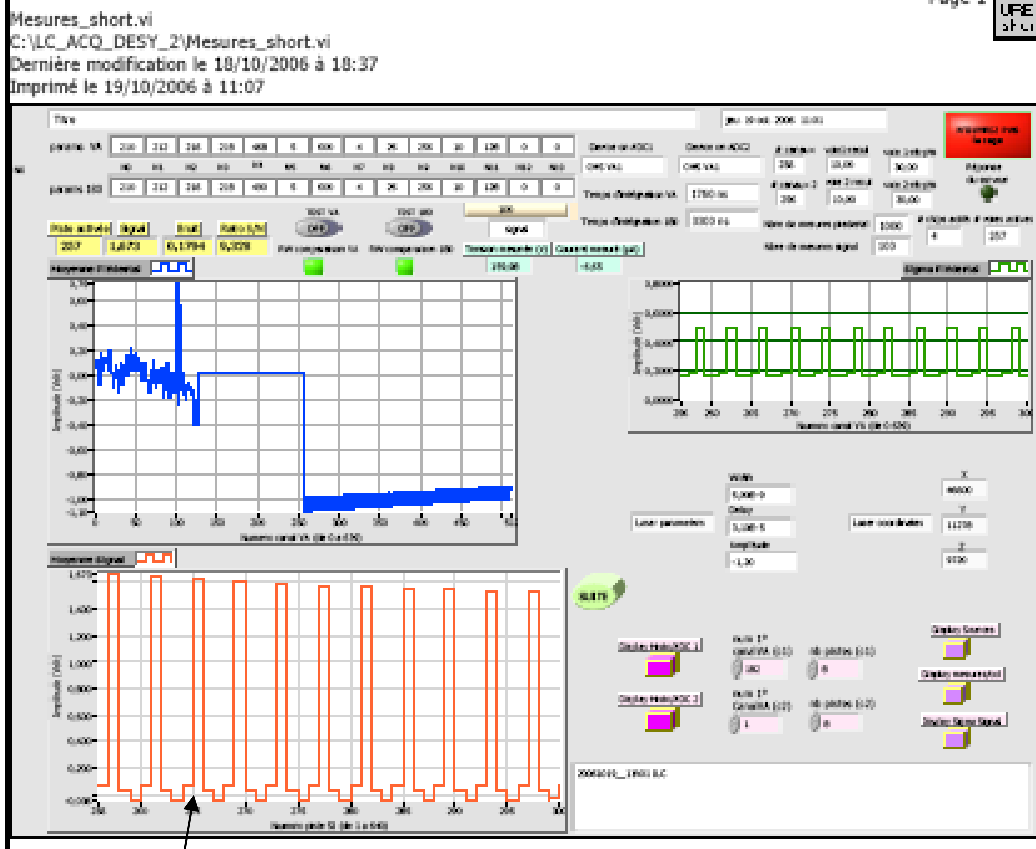
October 23 to Nov 5, 2006

Sharing of tasks

- Construction of the detector prototypes: **CERN, IEKP-Karlsruhe, LPNHE-Paris &** IHEP Vienna, Hamamatsu providing the sensors)
- Mechanics: DESY,LPNHE Paris, **IFIC Valencia**
- FE and readout electronics: **LPNHE-Paris**
- DAQ hardware: **DESY for beam telescopes, LPNHE-Paris for SiLC**
- DAQ software: **DESY, LPNHE-Paris, CU Prague**
- Test in test bench prior to go to test beam: **LPNHE-Paris,** IEKP Karlsruhe, CU Prague,
- Beam Telescopes and Beam infrastructures: DESY, OSU Obninsk, **CU Prague**,
- Analysis tools: **CU Prague**, OSU Obninsk, LPNHE Paris
- Participation to the run: HIP Helsinki, IEKP Karlsruhe, OSU Obninsk, LPNHE Paris, CU Prague, IFIC Santander and contribution of DESY (beam & telescopes)

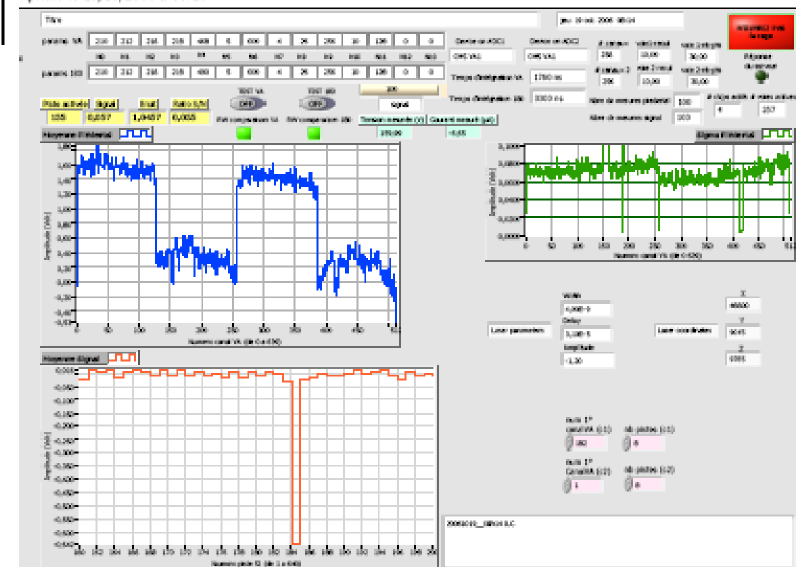
SiTRA test beam DAQ system in DESY





Latest news from Lab test bench: Both VA1 eadout cards and 180UMC+VA1 cards are working fine when reading out LD1060 signal

180nm UMC channel attached to 3 CMS Sensor module: response to LD1060 sinal



Still two crucial challenges ahead of us before the end of the year:

- Beam test at DESY
- Test of the new chip 130nm

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2007 Workpackages for SiLC/EUDET

WKP 0: Beam test in DESY (January-February 2007)
Pursuing the forthcoming test with 130nm 4ch-preproto

WKP 1: Beam tests at CERN (June 2007)
« Repetition » for the November run:
- 2 modules made of 2 **new** 8'' single-sided sensors
  readout: VA1(ref)+ **130nm-32ou64v (preproto128v)**
  wiring chip-on-detector, new insulating box (related to cooling issue)
- 3D-planar module test

WKP2: Beam test at CERN or FNAL (?) (Nov. 2007)
- Prototype 60x60cm2, 8'' single-sided sensors
  lecture VA1+130nm-128v, connectique chip/détecteur

- *Other SiLC collaborators SiLC will join these beam tests and foresee to bring other detector prototypes. The hosting labs: CERN and FNAL (providing beam test 'infrastructure': DAQ, beam telescopes, mechanics…)*

- *December SiLC meeting in Barcelona: decisions on the baseline for 2007*

Work on all mechanical aspects including alignment, cooling,on developing further the FE-readout electronics and on addressing the associated DAQ will go on in //.

Workpackage 2, in 2007 is

Going from demonstrator to mini series for performing beam tests…

- Big step forward, new issues to be addressed on all the aspects of the project:
  Electronics, Mechanics, On-line & DAQ, data analyses.

- Strategy for tasks dispatching between collaborators (to be defined for 2007)

- Collaborations with Industrial firms (fabrication => quality tests)

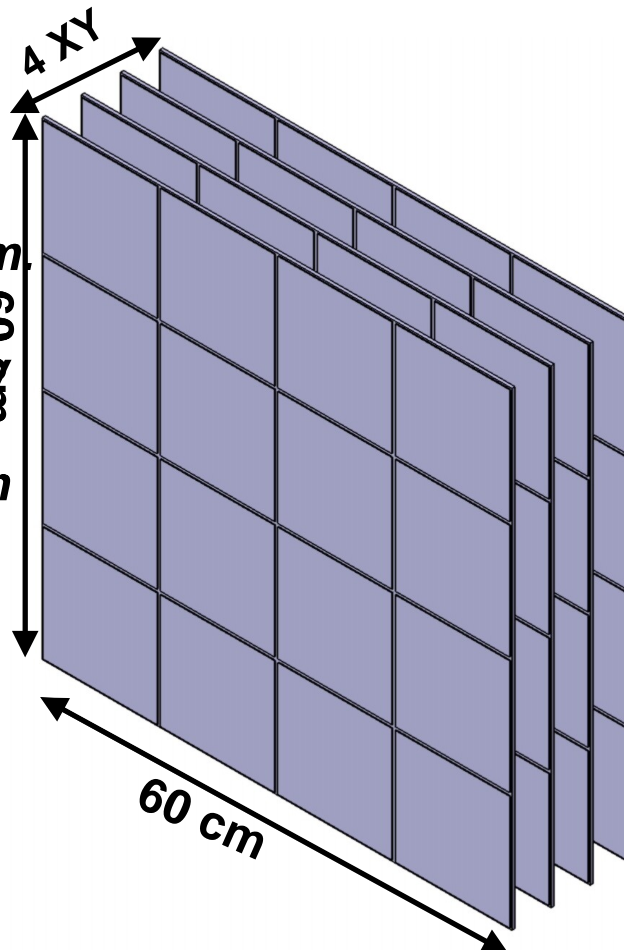
- Importance of estimating the related risks (tasks dispatching, quality tests on Silicon sensors, chips, wiring or readout cards, industrial transfers, realistic cost evaluation)

EUDET test beams with Silicon tracking

Series of tests from 2007 to 2009, combined test beams with other subdetectors & high magnetic field:

- ➢ Test new FE chip prototype (130 nm prototype-128)
- ➢ Various detector prototypes with new sensors and new FE chips (baseline defined at the 3rd SiLC meeting in Liverpool)

8'' sensors proto for 2007 test beam. Other prototypes with different new sensors. Interest of Korean and US teams to participate.



Example:
4 '' telescope layers '' made of 15 x15 cm sensors (≥ 8''), false double sided, thinned, equipped with new chips.

Total: 128 sensors
60000 channels
(~150µm r.o.pitch)
About 250 FE chips

Topics

- ► R&D on new silicon sensors
- ► Towards the fabrication of new modules
- ► R&D on the electronics forefront
- ► 2006 beam test
- ► Prospects for 2007
  - Preparation of new beamtests
  - Developing Alignment
  - Developing Cooling

ALIGNMENT SYSTEM (IFCA)

Usage of collimated laser beams (IR spectrum) going through silicon detector modules. The laser beams would be detected directly in the Si-modules. This requires:

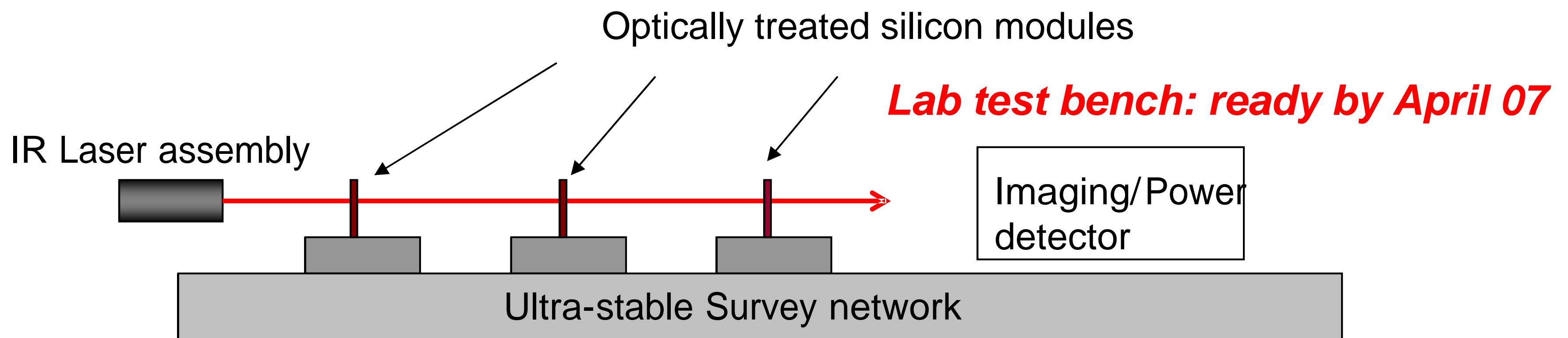
- Silicon module surface requires special treatement to improved its optical quality/transmitance
- Dedicated ultra-stable test stand for “optical” characterization of the modified silicon modules: reflectivity, transmitance, absorption, polarization sensitivity, wedge effect, response uniformity...

Main advantages:

Particle tracks and laser beam share the same sensors removing the need of any mechanical transfer.

Minimum interference with Silicon support structures

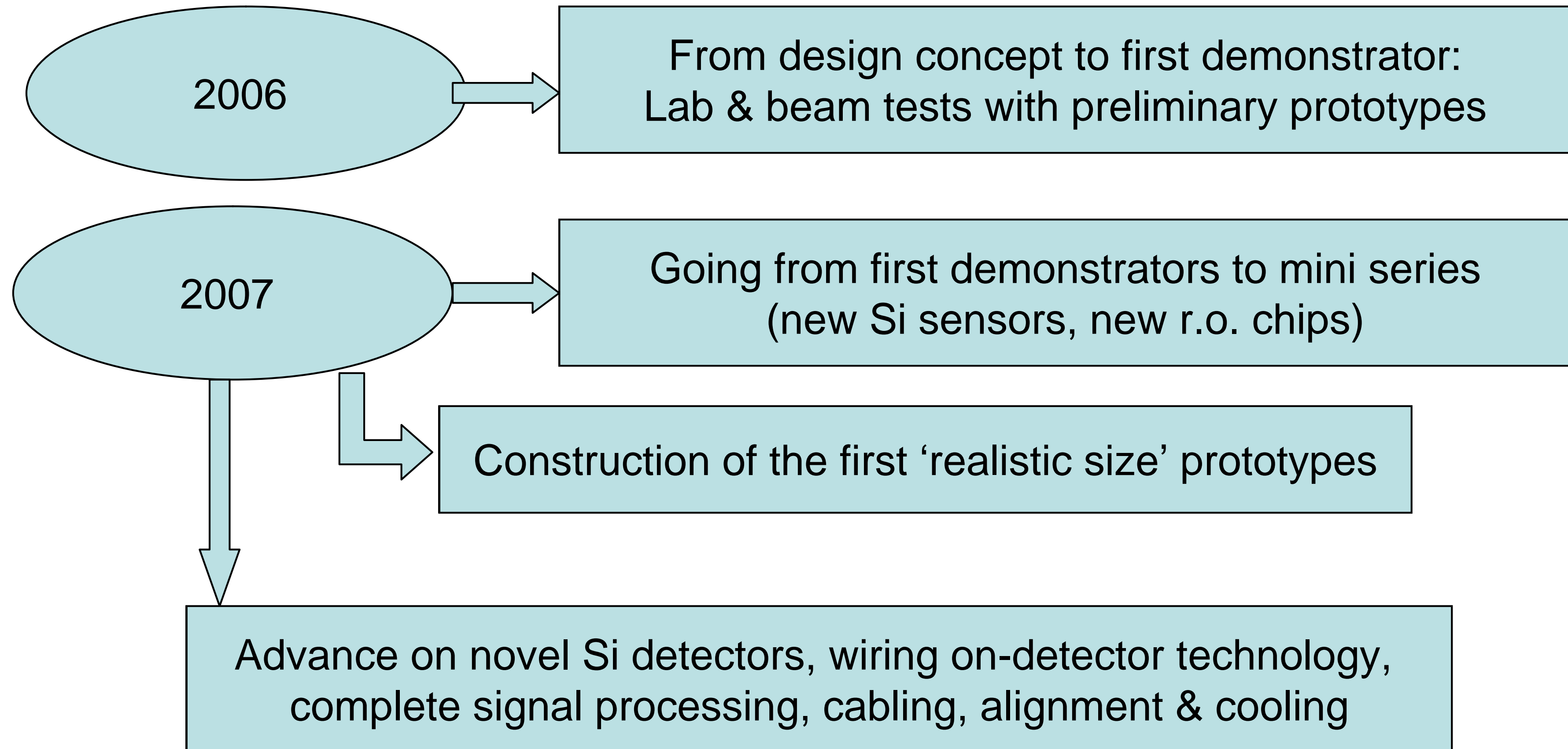
No precise positioning of the aiming of the collimators. The number of measurements has to be redundant enough



Lab test bench: ready by April 07

Prepared by Celso Martinez Rivero –IFCA-Santander

Transitions of phase:



Goal is to fit with the deliverables we have to provide in this project

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