Accessing 130 nm CMOS Tech for ILC (Public Version)

Oct 2006, Munich

A. Marchioro

CERN, Div. PH

1211 Geneva 23, Switzerland

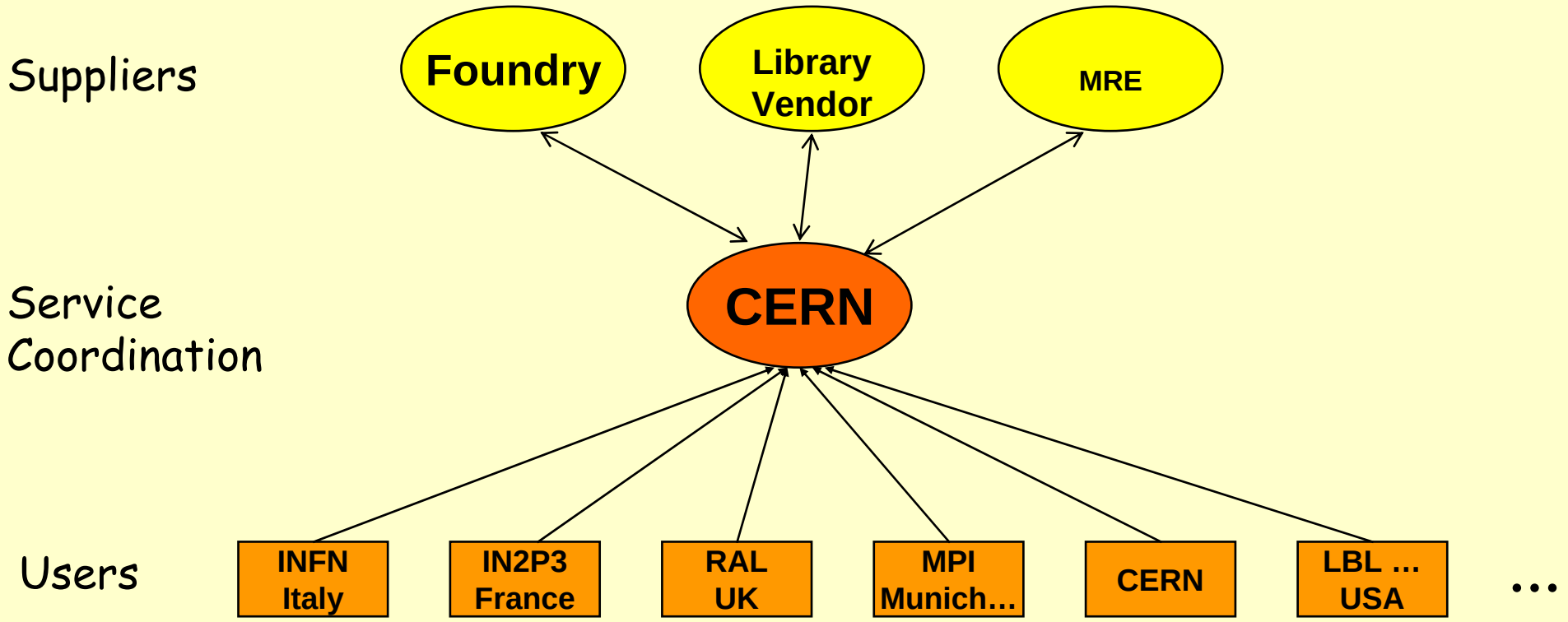
Components

- Technology
- Tools: Design Assistance Package
- Services:
  - Design Services
  - Prototyping and Production Services

Technology access

- CERN foundry contract
  - Done! Final prices are fixed, conditions are very interesting and well suited for HEP
    - » Excellent engineering support still in place
- Conditions are same or better than those we obtained in 2000 for accessing the ¼ micron generation
- Community can globally gain if good coordination will be maintained for the SLHC, ILC and any other future ASIC activity

Organizational model

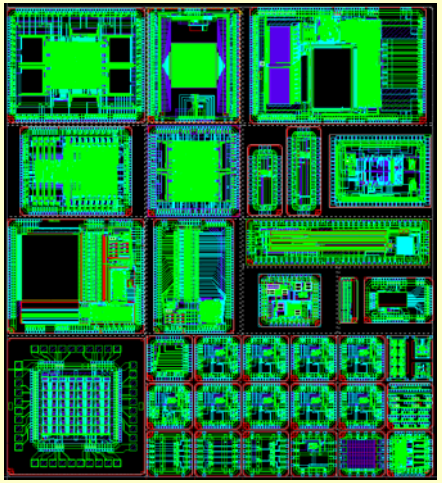


Technology

- For LHC, SLHC, ILC and others
  - 130 nm CMOS, 90 nm later
  - 130 nm BiCMOS
    - » 2 flavors available:
      - Very high Performance
      - High performance, cost effective
    - » Radiation tolerance to be studied, but large body of work already available.

MPW Runs

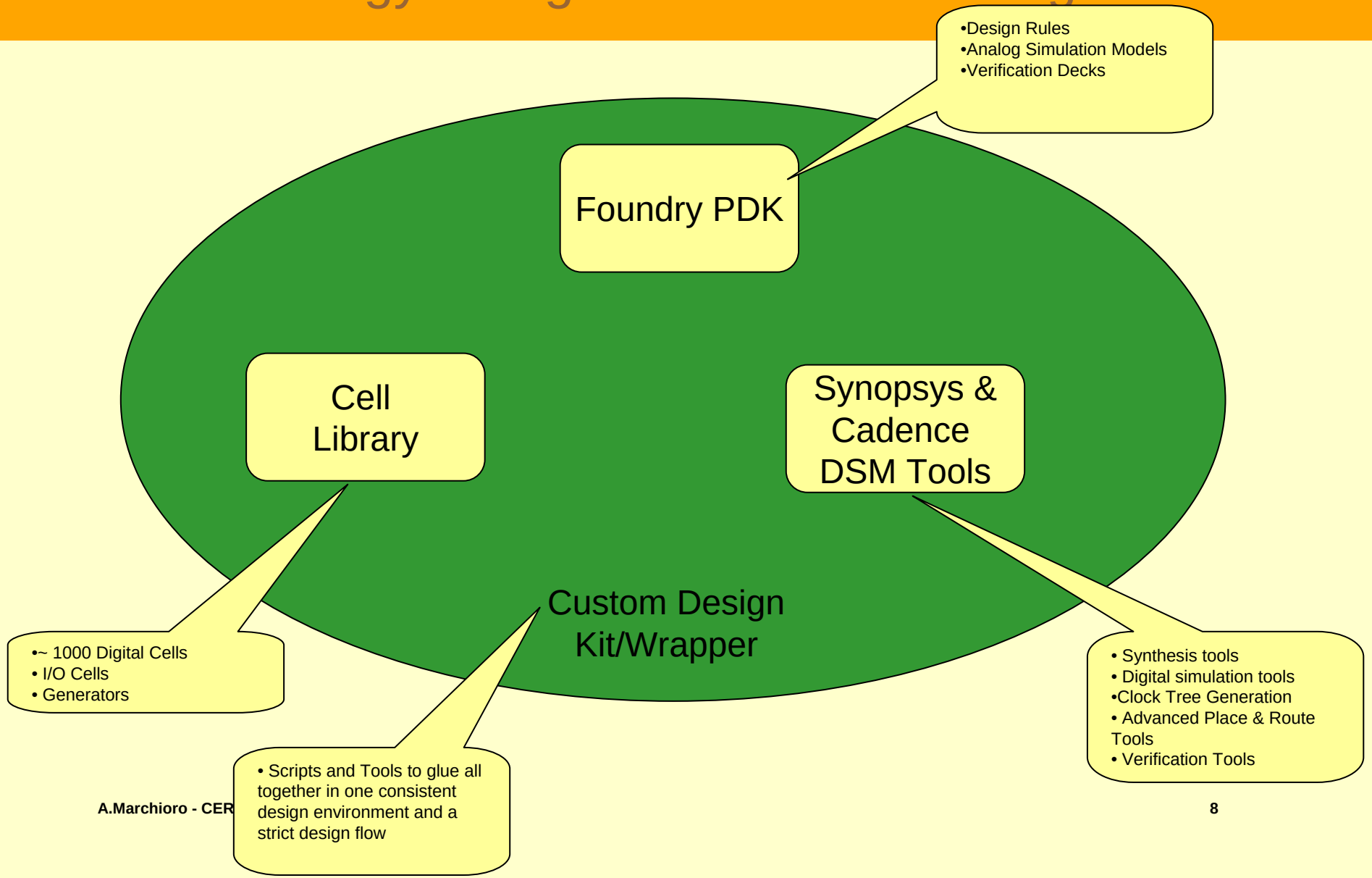
- CERN MIC group has organized 16 MPW runs since 2000 in ¼ micron
  - Each run had up to 20 participants
  - Easily delivered several hundred chips/run
    - Smooth transition to production runs
    - Encourage and support the organization of shared production runs for modest volumes



130 nm MPW run details

- RF process including:
  - poly and diff resistors
  - triple well
  - Low-Vt N and PMOS
  - Zero-Vt NMOS
  - e-fuses
  - Thick (5.2 nm) transistors for IO @ 2.5 V
- 6 metals with LM upper stack, all Cu
  - Vertical metal to metal cap: 1.3 fF/um^2
  - 8 metals possible for private runs (+ 64 K$)
- Variety of metal capacitors
- Bump-bonding if desired (run split possible)
  - Low cost
- Hundreds (or thousands!) of chips from proto run
- Preferred chips sizes: multiple of 2x2 mm^2
- Cost below MOSIS at about 70-80 mm^2.

Technology Design Assistance Package



Tools

- 130 nm “wrapper” available through CERN contract to every HEP Institutes for 2,000 €/year
  - We expect that “normal” Cadence licenses are available in each Institute
  - Commercial Digital Library from vendor available for free for download (library is paid by submitted wafers at production time)
  - A service for advanced P&R and design verification (DRC) can be organized at CERN if enough demand present

Tools Distribution

- The 130 nm Distribution Kit will contain:
  - Foundry PDK
  - Digital library
  - MRE tools
  - Europractice software will have to be obtained through the normal EU channels
- You need to provide to CERN
  - Copy of NDA with Foundry
  - Copy of EULA with Library Vendor

Do NOT download any private version from the vendors, as they may be out of sync with the CERN version

Contacts

- Organizational issues, contract etc.:
  Alessandro.Marchioro@cern.ch
- CMOS Technology:
  Federico.Faccio@cern.ch
- Tools Utilization:
  Kostas.Kloukinas@cern.ch
- Tools installation issues:
  Bert.van.Koningsveld@cern.ch
- Purchase of MRE Wrapper:
  ekenberg@mri-se.com

Future runs

- 130 nm:
  - Shared MOSIS run on Nov 25, 2006
  - 2 MPW runs in 2007 (~ Q2 & Q4)
  - Tech. details of run from F. Faccio
- ¼ micron (as in the past)
  - 1 MPW run in Q2/Q3