CMOS Sensors for the Nominal Beam Telescope

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on behalf of DAPNIA-Saclay, LPSC-Grenoble, LPC-Clermont, IPHC-Strasbourg

OUTLINE

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  - Basic improvements provided by final sensors
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- Status of the development :
  - Column // r.o. architecture
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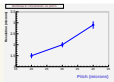
  - $\emptyset$ micro-cicuits
- Refining the requirements :
  - Spatial resolution
  - Dimensions
  - Read-out frequency
  - Availability
- Summary

Introductory Remarks

  -

Essential Improvements Provided by Final Sensors

⇛ **Improvements focus on sensors equipping the arms (not DUT surface) :**

- **Increase of read-out speed by one order of magnitude :**
  - **Demonstrator provides frame read-out time of 1.6 ms (possibly 800 μs)**
  - **Final sensors will provide frame read-out time $\sim$ 100 μs (possibly $\sim$ 50 μs)**

- **Extension of sensitive area by factor 3.5 :**
  - **Demonstrator sensitive area : 7.68 x 7.68 mm^2**
  - **Final sensor sensitive area : 20.48 x 10.24 mm^2**
    $\rightarrowtail$ encompasses width of ILC-VD sensors

- **Integrate several other improvements resulting from R&D progress**
  ($\rightarrowtail$ signal amplification, data compression, etc.)

Development Strategy

- **3 micro-circuit components developed in parallel :**
  - **column // architecture with binary output**
  - **ADCs to be integrated at end of each column**
  - **∅ micro-circuits to be integrated downstream of each ADC**

- **Sharing of tasks :**
  - **Col. // architecture design : DAPNIA & IPHC**
  - **ADC designs : LPC-Clermont, LPSC-Grenoble, DAPNIA, IPHC**
  - **∅ micro-circuit design : IPHC (or nearly so ...)**
  - **chips characterisation : IN2P3 (several labs), DAPNIA, DESY et al., INFN (several labs)**
    - ★ **likely to be a bottle neck ...**

- **2 design options under consideration :**
  - **Sensors with binary encoding of signal charge : most straightforward**
  - **Sensors with 4- or 5-bit ADC encoding : will provide twice better spatial resolution**

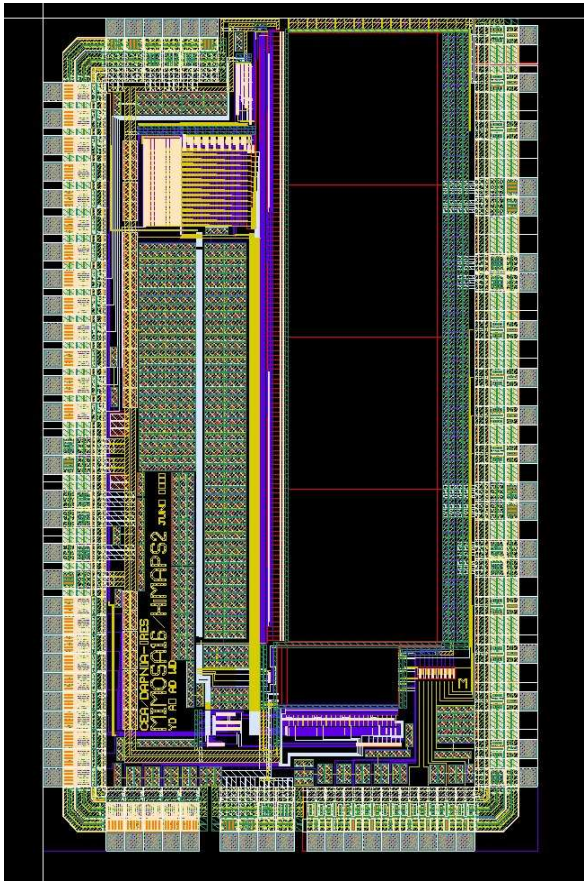
⇛ **Discussion needed to refine sensor requirements**

Status of the Development

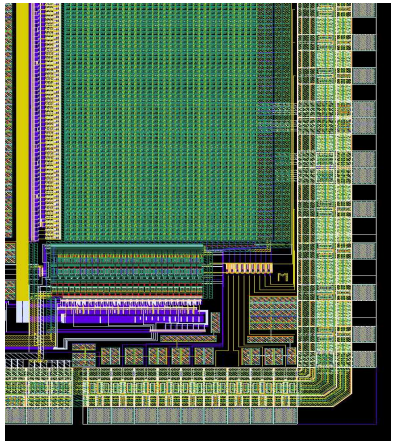
High Read-Out Speed Architecture

MIMOSA-16 design features :

- Fab. via STAR engin. run (Summer '06)
- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–16 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (repeated at end of each column)
- discriminator at end of each column
- 4 sub-arrays :
  - ⁂ 2 alike MIMOSA-8 (2 different pitches)
  - ⁂ 1 with ionising radiation tol. pixels
  - ⁂ 1 with enhanced in-pixel amplification
    (against noise of read-out chain)



$\Rightarrow$



24 col. with discri.

Next steps :

- back from foundry $<$ end Oct. '06 $\longmapsto$ lab tests $\gtrsim$ Nov. '06 $\longmapsto$ beam tests $\gtrsim$ Summer 2007
- next generations :
  - ⁂ "large" prototype (320 columns of 256 pixels, 16 μm pitch, integrated $\varnothing$ micro-circuits) ???
  - ⁂ small prototypes with ADCs replacing discriminators

- **Several different ADC architectures under development at IN2P3 and DAPNIA (most for ILC)**
  - **LPCC (Clermont) : flash 4+1.5-bit ADC $\mapsto$ 1st proto tested, 2nd proto back from foundry**
  - **LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5-bit ADC $\mapsto$ 1st proto tested, 2nd proto under test**
  - **DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC $\mapsto$ 1st proto under test**
  - **IPHC (Strasbourg) : SAR 4-bit and Wilkinson 5-bit ADCs: 1st proto to be submitted end Octobre '06**

    ►►► **Present outcome of development :**
    - **Typical differences between architectures is $\sim$ factor 2 in power & speed (also dimensions)**
    - **Modest differences expected on single point resolution**
    - **observed pbs: loss of 1–2 bits (e.g. due to offset dispersion between columns)**

      $\Rightarrow$ **solutions under study include enhanced signal amplification before ADC**

- **Next steps :**
  - **Final ADC designs expected to come out in 2007**
  - **Submission of 1st col. // pixel array proto equipped with ADCs & $\varnothing \gtrsim$ end 2007**

⇛ **No design started yet !!!!!** ⇛ **Need to hurry up ...**

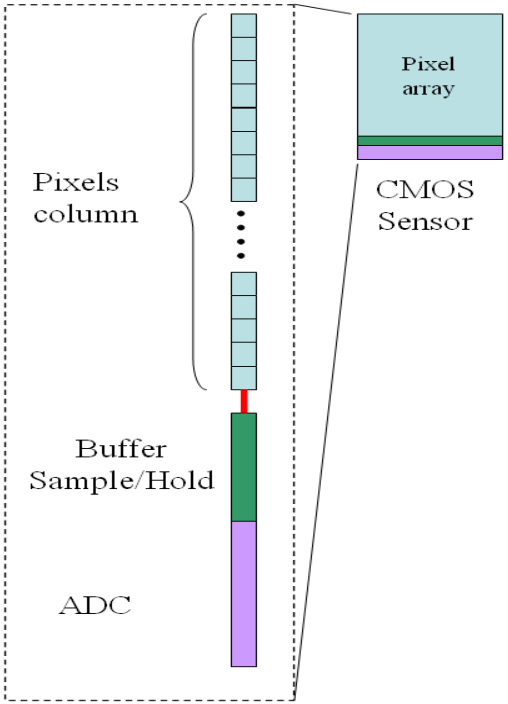
⇛ **IPHC will start next month :**

- **1st prototype < Summer 2007**
- **final prototype in 2008**

Prospect on Development of Final Sensors

Baseline Architecture with Integrated ADCs

- **Geometry :**
  - 1024 columns of 512 pixels
  - 20 μm pitch ($\longrightarrow \sigma_{sp} < 2.5\ \mu m$)
  - Sensitive area = 20.48 x 10.24 mm^2



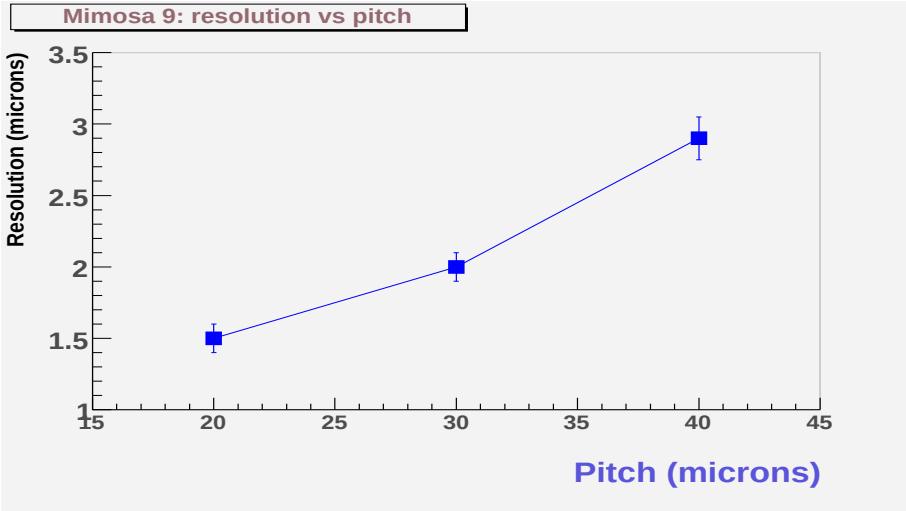
- **Functionnalities :**
  - pixels with integrated CDS (possibly repeated at end of column)
  - sensor with integrated 4-/5-bit ADC
    - ▷ ADC possibly preceded by discri. $\longrightarrow$ 1 ADC for 8 - 16 col. ?
  - $\emptyset$ micro-circuit integrated downstream (?) of ADCs

- **Read-out speed (adapted to DESY beam) :**
  - default $\mathbf{t_{r.o.}}$ = 512 lines / 5 MHz $\sim$ 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\longrightarrow$ $\mathbf{t_{r.o.}} \sim$ 500 – 50 μs

Spatial Resolution

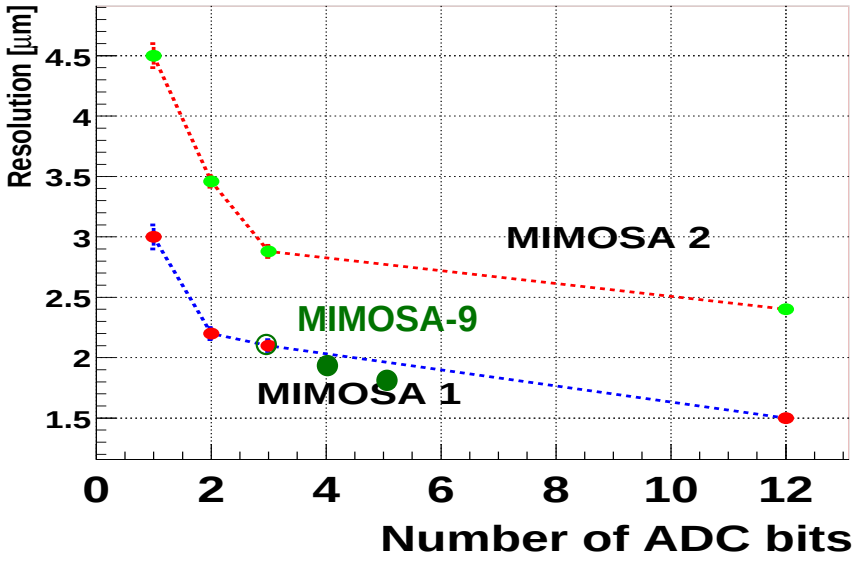
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
  $\longmapsto \sigma_{sp} \lesssim 2\ \mu m$ (30 μm pitch)
- obtained with signal charge encoded on 12 bits



σ_{sp} dependence on ADC granularity:

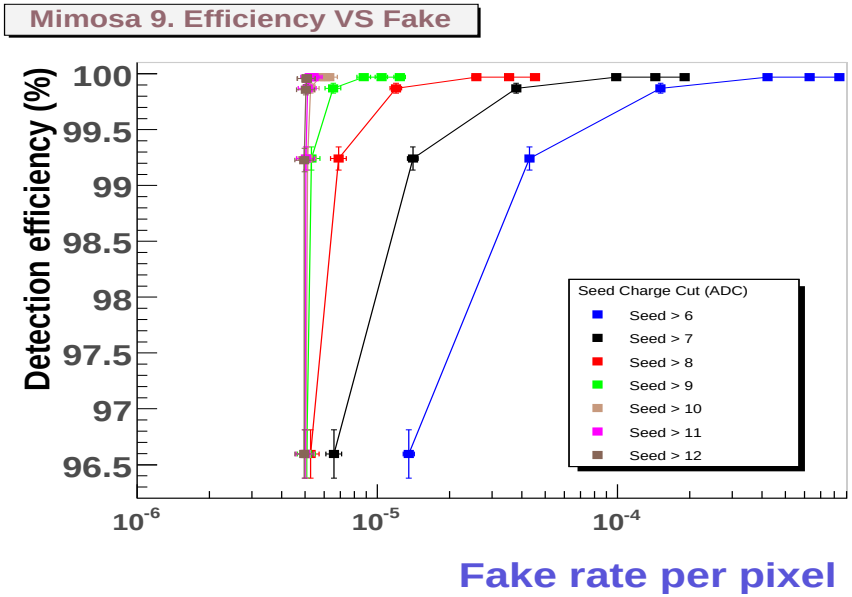
- minimise number of ADC bits
  $\longmapsto$ minimise dimensions, $t_{r.o.}$ & P_{diss}
- effect simulated on real MIMOSA data
  (20 μm pitch ; 120 GeV/c π^- beam)



▷▷ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\longmapsto$ 1.7–1.6 μm (5 bits)
(MIMOSA-9 : 20 μm pitch; T= + 20 °C)

- Warning : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

- **Baseline assumptions :**
  - sensor made of 1024 col. of 512 pixels $\longmapsto \sim 5{\cdot}10^5$ pixels / frame
  - $t_{r.o.}$ = 100 μs $\longmapsto$ 10 kfps (can be twice more or twice less)
  - $\lesssim$ 5 hits / frame
  - noisy pixel rate $>$ threshold $\lesssim 10^{-4}$ $\longmapsto$
  - pixel data size = 2 Bytes
    (10 bits of address & 5 bits for charge)



- **Data rate from pixel noise :**
  - 50 pixels / frame $\longmapsto$ 1 MB/s

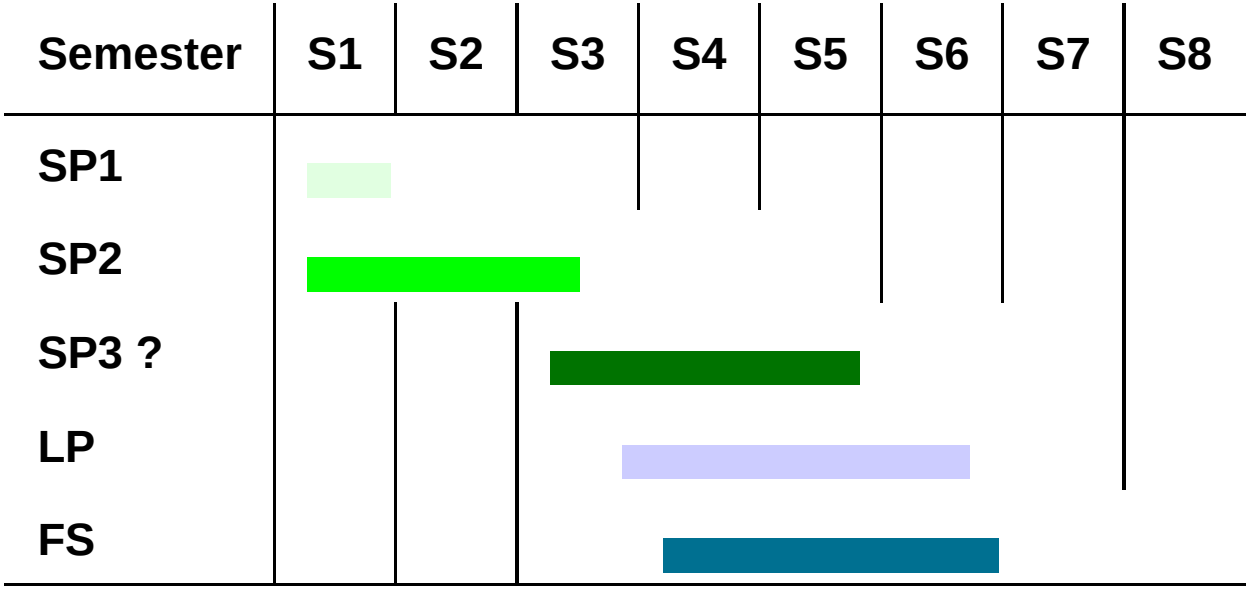
- **Data rate from beam particle hits :**
  - 5 hits of 9 pixels / frame $\longmapsto$ 1 MB/s

$\Rightarrow$ **Total $<$ 1 kB/frame $\longmapsto$ few MB/s only**

- **Geometry :**
  - 1280 columns of 640 pixels
  - 16 μm pitch ($\longrightarrow$ $\sigma_{sp} < 5\ \mu m$)
  - Sensitive area = 20.48 x 10.24 mm^2
- **Functionnalities :**
  - pixels with integrated CDS (possibly repeated at end of column)
  - column ended with integrated discriminator $\longrightarrow$ binary encoding of charge
  - $\emptyset$ micro-circuit integrated downstream of discriminators
- **Read-out speed (adapted to DESY beams):**
  - default $t_{r.o.}$ = 640 lines / 6.4 MHz = 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\longrightarrow$ $t_{r.o.}$ = 640 – 64 μs

$\Rightarrow$ **Less development needed to finalise sensor than with integ. ADC $\Rightarrow$ available earlier**

Provisionnal Schedule of Sensor Delivery



- **Sensor production based on 5 steps (perhaps only 4, i.e. SP3 included in LP) :**
  - **MIMOSA-8 $\equiv$ SP-1 : 25 μm pitch, epi $<$ 7 μm**
  - **MIMOSA-16 $\equiv$ SP-2 : 25 μm pitch, epi $\sim$ 11 or 16 μm, rad. tol.**
  - **M16+ $\equiv$ SP-3 : like SP-2 but integ. $\emptyset$, 20 μm pitch (ADC) or 16 μm pitch (binary)**
  - **M16++ $\equiv$ LP : like SP-3 but 320 col. of 256 pixels**
  - **M16+++ $\equiv$ FS : like LP but 1024 x 512 pixels (ADC) or 1280 x 640 pixels (binary)**

- **Which single point resolution over which area ?**
  - **Arms : $< 2.5\ \mu m$ or $< 5\ \mu m$ over 2 x 1 cm^2 ?**
  - **DUT surface : $\sim 1\ \mu m$ over 5 x 5 mm^2 ?**
- **How much surface should the sensor planes cover ?**
- **Is t$_{r.o.}$ $\sim 100\ \mu s$ all right ? with how much flexibility ?**
- **When should the sensors be delivered ?**
- **How do we organise ourselves w.r.t. sensor characterisation ?**

Summary

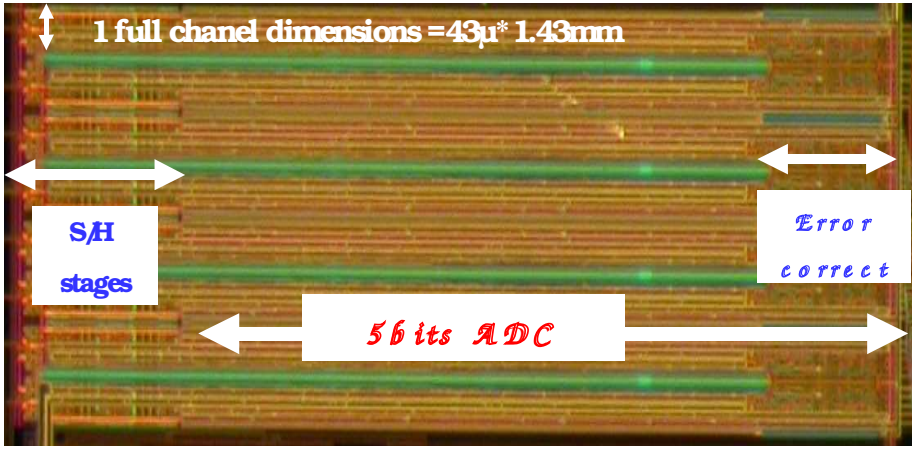
- **Development of final sensors for BT arm is progressing :**
  - **Column // archi.**
  - **Compact & fast ADCs**
  - **$\varnothing$ micro-circuits (just starting !)**

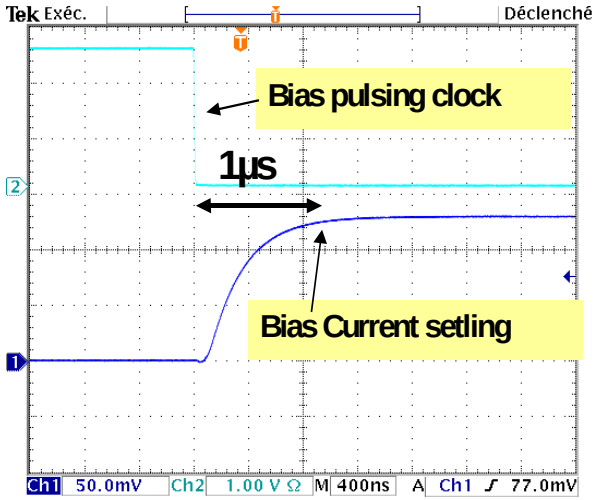
  $\Rightarrow$ **should increase demonstrator r.o. speed by one order of magniture and sensitive area by factor 3.5**

- **Need to decide on :**
  - **σ_{sp}**
  - **Surface**
  - **Frame r.o. speed**
  - **Delivery date**

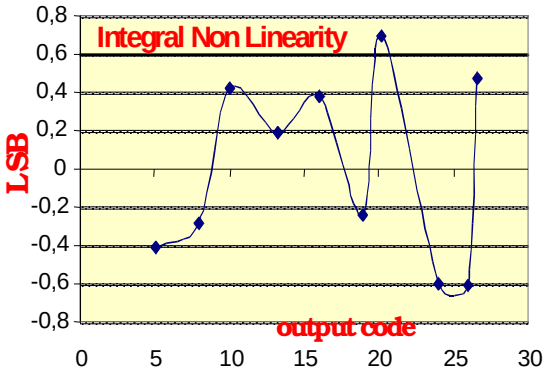
  $\Rightarrow$ **In particular : integrated ADC ($\sigma_{sp} <$ 2.5 μm) vs integrated discri. alone ($\sigma_{sp} <$ 5 μm)**

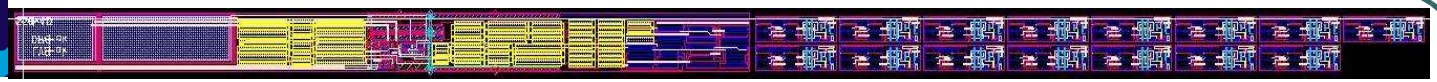
S/H & 5 bits Pipe line ADC =>(LPSC)





	Sample & Hold	5 bits ADC
Frequency	25Mhz	25Mhz
Dimensions	43µ * 250µ	43µ * 1200µ
Power@ 3.3V	0.413 mW	1.287 mW
Power@ 2.5V	0.313 mW	0.975 mW

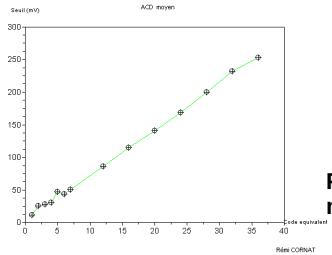




VADC juin 06 1100x45 µm²

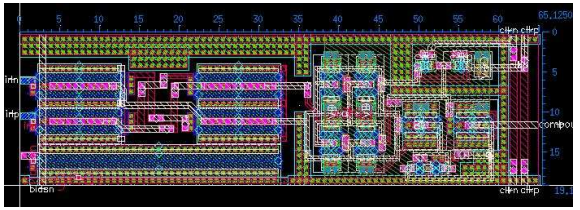
Flash ADC 20 Mhz, 2 mW, 4 bits/300 mV pour ILC VDET (collaboration LPC-IRES)

- Septembre 05
  - Version 3.3 V
  - Consommation x20 !
  - Offsets comparateurs > lsb (= 15 mV)

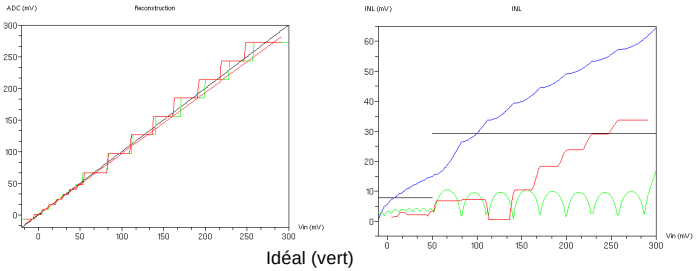


Fonction de transfert moyenne non monotone

- Juin 06
  - Version **2.5 V**
  - Fonderie le 26 juin
  - Nouveau comparateur d'offset réduit
  - Double étage d'entrée (gain x3)
  - Répartition non linéaire des points de basculement
  - 20 MHz (taille et consommation double, 1 pour 2 voies)
  - Echelle résistive compensée pour une charge de 1 pF



Nouveau Comparateur 65x19 µm²

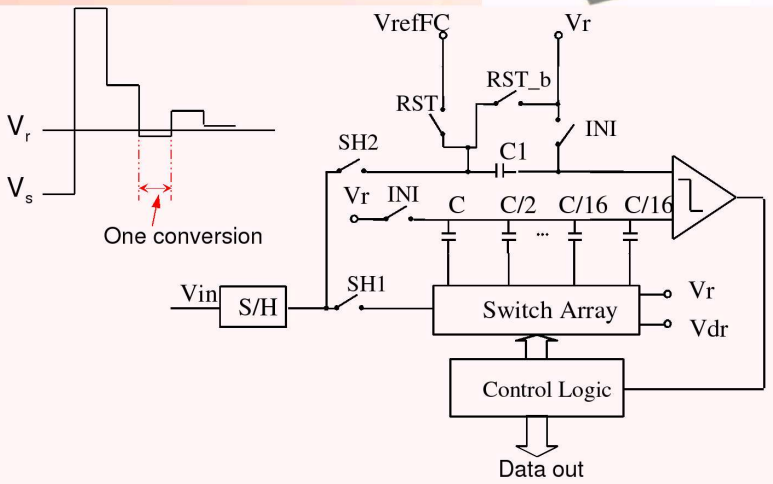


Fonction de transfert — Idéal (vert) Simulé (rouge) — INL

Status of ADC Devt at DAPNIA

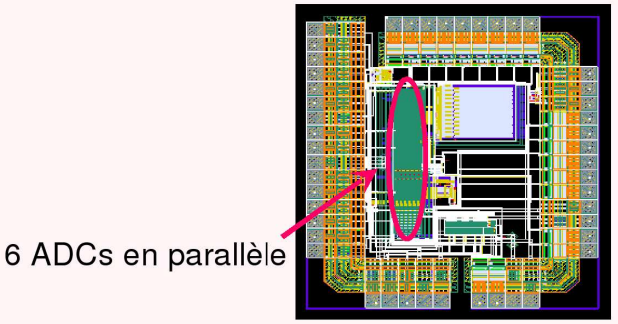
ADC à approximation successive (DAPNIA)

- Type : Approximation successive
- Discrimination intégrée pour limiter la puissance dissipée
- Dimensions: 25 µm x 1 mm (comprenant le S&H et le sérialiseur)
- Deux versions : 5-bit et 4-bit
- Temps de conversion : ~250 ns
- Puissance dissipée :
  Vin < VrefFC → ~350µW (diss. statique)
  Vin > VrefFC → >350µW (statique+dynamique)



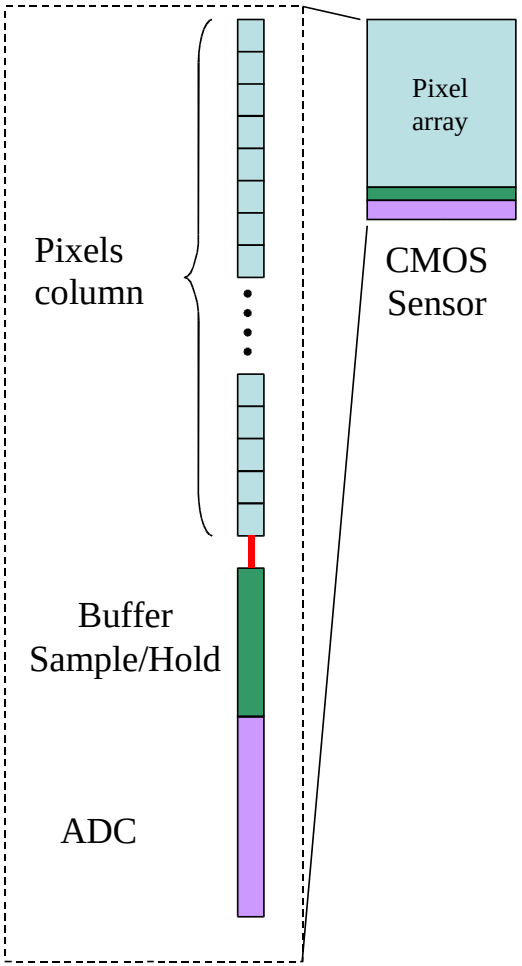
➢ Tests en cours

- Fonctionnel mais bits manquants (pour les faibles dynamiques) à cause des couplages dus au layout
- Refaire le layout & intégrer un amplificateur entre le pixel et l'ADC?



Layout du prototype soumis en mars 2006
(Techno : AMS CMOS 0.35µm Opto)

Development of ADC at IPHC



Successive Approximation ADC

- Process : 0.35 µm AMS , Hi-Res Substrate
- 4 bits ADC (LSB = 7,8 mV)
- Analog input dynamic : 125 mV
- Core area : 25 µm × 920 µm.
- Conversion speed : 7.1 MS/s and 6.25 MS/s
- Static power dissipation : 330µW

Double Scale Wilkinson ADC

- Process : 0.35µm AMS , Hi-Res substrate.
- 4 bits ADC (LSB = 7,8 mV)
- Analog input dynamic : 125 mV
- Core area : 25 µm × 840 µm.
- Conversion speed : 10 MS/s and 6.67 MS/s
- Static power dissipation : 250µW

Submission of 2 chips : 24 October 2006