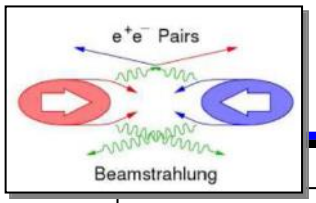
VXD and intermediate tracking Integration Status

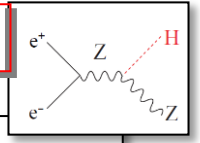
A. Ishikawa, M. Vos, A. Besson

- News from R&D groups
- Beam background updates
- Costing
- Power consumption
- Cabling
- SIT
- Conclusion

Reminder: ILC VXD requirements

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$



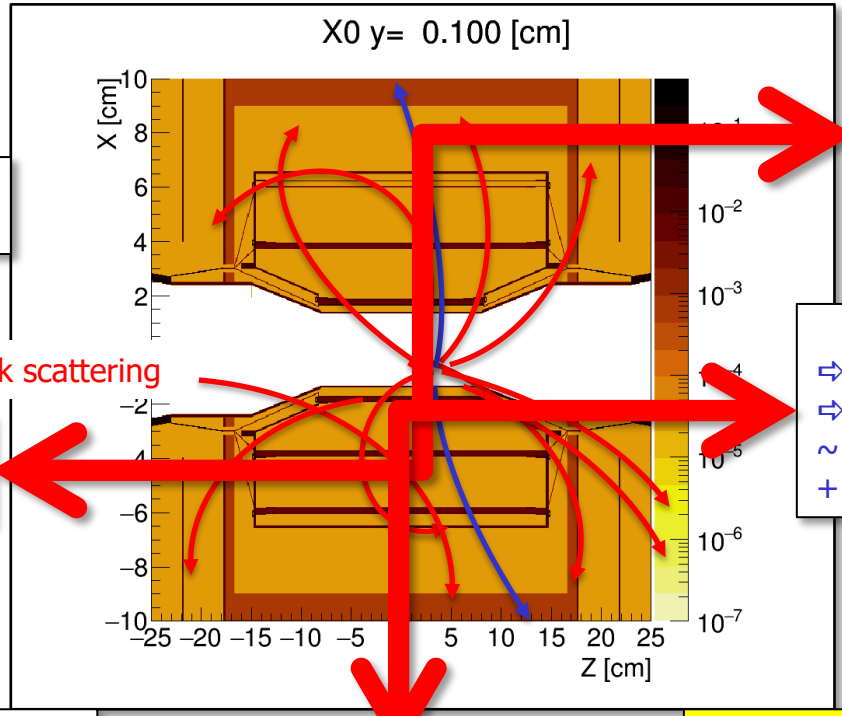


Physics
⇨ Flavour tagging
⇨ Low pT tracks

Beam background

Physics (<Hz/cm²)

Beam background (~ 5 hits/BX/cm² on layer 0)



Vertex reconstruction
⇨ granularity
⇨ Pitch ~17 um
⇨ (σ_{sp} ~3 um)

Radiation hardness
O(100kRad/an) & O(10^{11})neq/an

Rad.Tol. devices

Back scattering

Material Budget
⇨ ~ 0.15% X_0 / layer
⇨ < 1% X_0 for the whole VTX
~ 900 μm Si
+ ~0.14% X_0 for the beam pipe

Read-out speed
O(1-10 μs)

Power consumption
~< 50mW/cm²

Fast read-out & low Power architectures

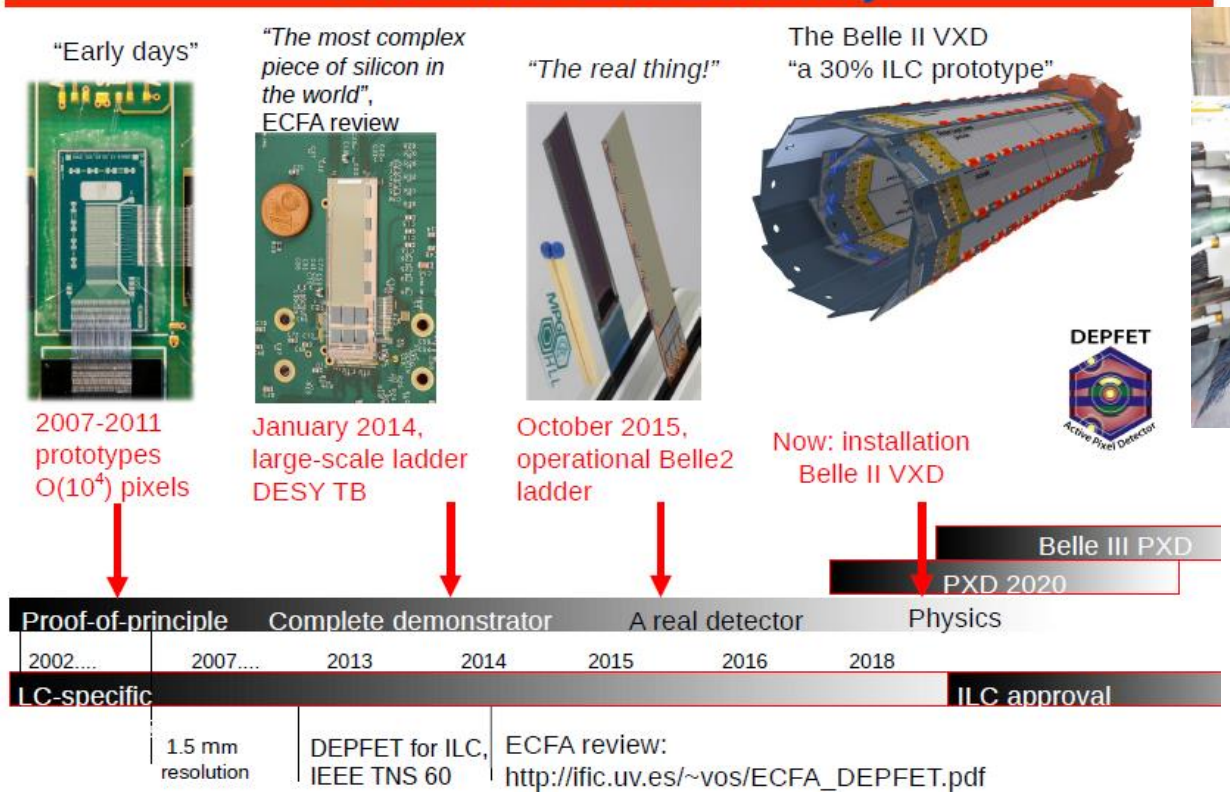
Cooling
Stiffness / Alignment

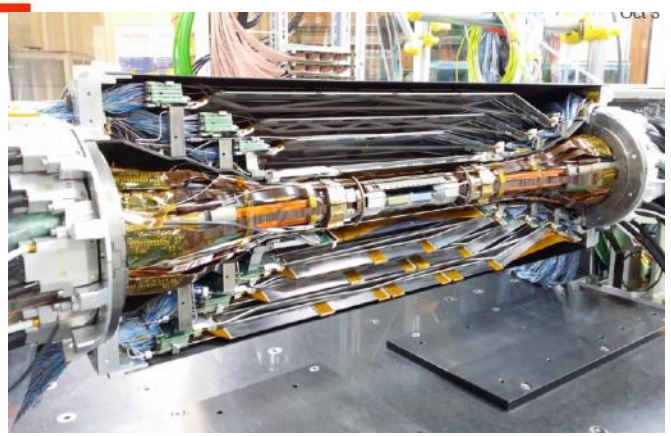
Low material detectors & supports structures

Challenge : meet the requirements all together

News from DEPFET

One-slide DEPFET history





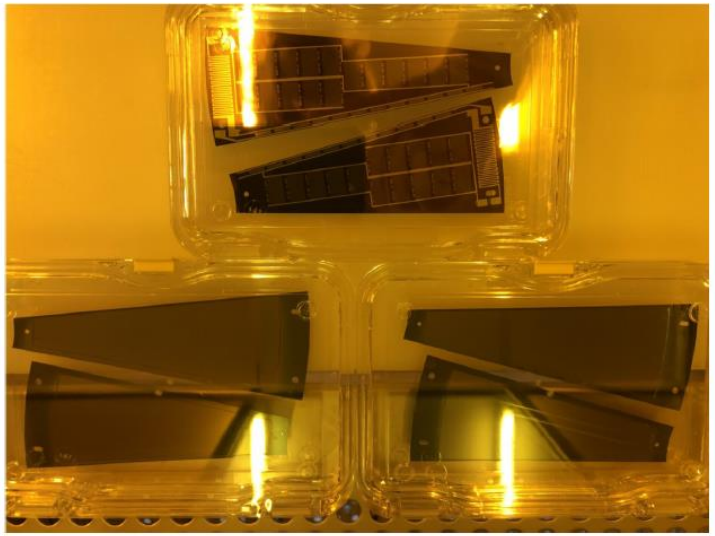
- Real experience gained for Belle II
  - Installation of vertex detector and preparation of PXD2020
- ILC-specific activity has been 2nd priority
  - Approval required to for signficant renewed interest
- Thinking about Belle III has started
  - Advanced DEPFET and CMOS options pursued by the collaboration

News from Forward disks

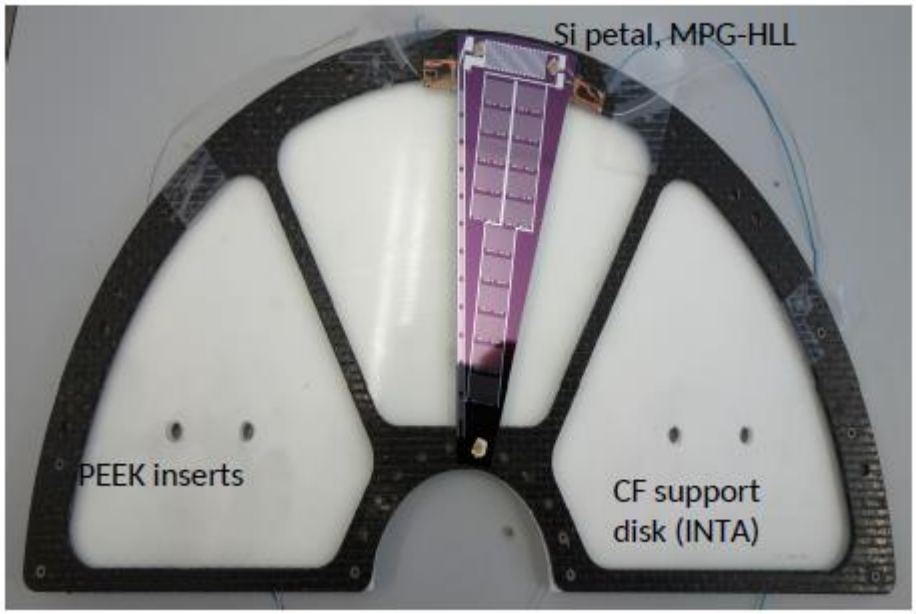
- A new mock up is being built (FTD1 & 2)
  - Thermo-mechanical properties
  - Planarity

New production at silicon lab of the Max Planck society in Munich

Petals arrived at IFIC in September 2018 and are currently being mounted on mock-up structure



Mock-up for FTD1 and 2 is being assembled at IFIC

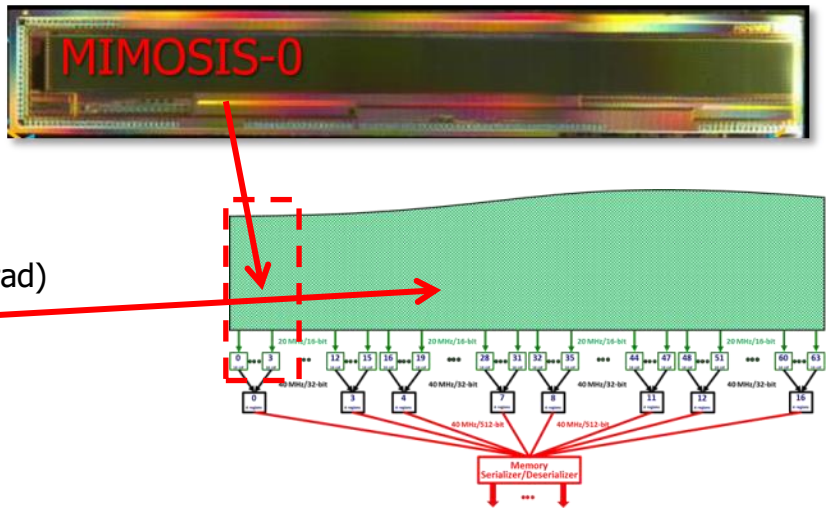


AIDA 2020

First measurements look promising:
- kinematic mount absorb thermal expansion as expected
- deformations under power load and air-flow are O(5 μm)
- mechanical stability in stable conditions is much better

News from CMOS Pixel Sensors

- MIMOSIS-0 prototype (2018)
  - 1st prototype for CBM experiment @ FAIR
  - Design adaptable to ILD
  - Ongoing tests
    - Pixel dispersion, architecture
    - Radiation hardness tests ongoing (10^{14} n_{eq}/cm^2 & 20 Mrad)
- MIMOSIS-1 (2019)
  - Full scale
  - Ongoing design



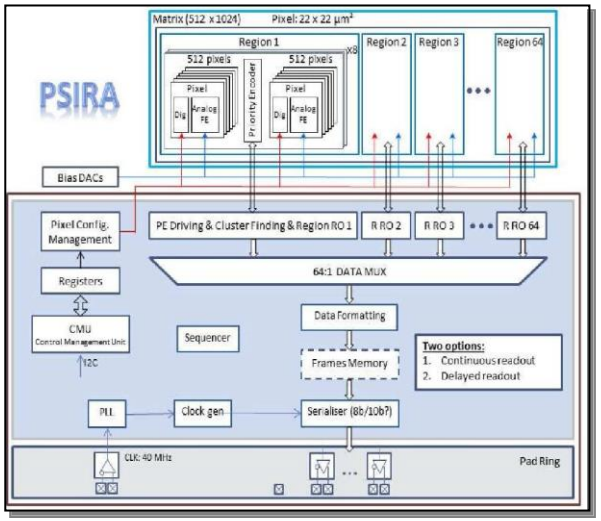
- CREMLINplus program (EU + Russia)
  - with DESY, CERN, JINR, FAIR, BINP, KINR, Frankfurt & IPHC
  - Telescope with MIMOSIS 1 or 2
    - Double sided ladders & faster read-out time 100 μs -> 5 μs. w.r.t to Mimosa 26 (EUDET)
    - Slightly degraded resolution compensated by double sided
- Long term R&D (with CERN)
  - Stitching -> reduce ladder overlap / reduce space between sensors
    - ~150 μm to ~<50 μm
  - Synergy with ALICE plans
  - 65 nm technology exploration
    - Mixed CMOS processes

Extension of MIMOSIS to ILC vertexing and tracking

- Conservative approach
  - Minimize changes w.r.t. MIMOSIS
    - Keep TJ 0.18 μm technology & a similar architecture
  - 2 sub-systems targeted
    - Vertex detector & Silicon inner trackers (SIT @ ILD)

⇨ PSIRA

⇨ Finalize CPS ~2025



- Expected Performances
  - σ_{sp} ~4 μm ⇨Use double sided ⇨ σ_{sp} ~2.8 μm
    - 22x22 μm² ~ 20% better spatial resolution % ALPIDE (vertexing)
    - Faster = higher Power consumption
  - Read-out time: 2-4 μs (ILD-VXD) and 1 μs (ILD-SIT)
  - Single pixel address read-out = 50 ns
    - (with 20 MHz clock)
  - Sustainable occupancy (~5 pixels/hits)
    - ~ 4 hits/region/μs ~ 100 hits/cm²/μs

- Can one reach : Pitch ~ 18 x 18 μm (σ_{sp} ~ 3 μm) & r.o.time ~ 2-4 μs ?
  - Doable with smaller feature sizes

⇨ PSIRA architecture already reaching 4-8 BX read-out time
⇨ Power vs read-out speed compromise
⇨ Avoiding power pulsing possible ?

Beam background

Beam background updates effects

- D. Jeans and Akiya beam background studies:

Large, 250 new params, anti-DID
[I believe: (mean #hits/BX +/- bunch-by-bunch variation)

```
----------------------------------------
Subsystem : VXD
  Layer 1: 7292 hits.  hitsperBX = (810.2 +- 339.) hits/BX.  (5.89 +- 2.471) hits/cm^2/BX.
  Layer 2: 4215 hits.  hitsperBX = (468.3 +- 204.) hits/BX.  (3.40 +- 1.488) hits/cm^2/BX.
  Layer 3: 906 hits.   hitsperBX = (100.6 +- 57.4) hits/BX.  (0.16 +- 0.094) hits/cm^2/BX.
  Layer 4: 746 hits.   hitsperBX = (82.88 +- 47.2) hits/BX.  (0.13 +- 0.078) hits/cm^2/BX.
  Layer 5: 279 hits.   hitsperBX = (31    +- 17.1) hits/BX.  (0.03 +- 0.018) hits/cm^2/BX.
  Layer 6: 266 hits.   hitsperBX = (29.56 +- 16.6) hits/BX.  (0.03 +- 0.017) hits/cm^2/BX.
```

~ 6 hits/ cm^2/BX on layer 1

Total VXD hits/BX	L12 EARLY	L12 LATE
DBD		
01m250_DBD_fieldX02	662.80	34.00
02m500_DBD_fieldX02	1276.50	126.50
NEW SIMULATIONS with new 250 GeV beam params		
LARGE, no anti-DID		
71_BEAMLIMITS_l5v03_250A	1040.11	1233.44
LARGE, anti-DID		
72_BEAMLIMITS_l5v05_250A	1050.50	339.70
LARGE, anti-DID, lower momentum threshold		
73_BEAMLIMITS3_l5v05_250A	970.11	308.44
SMALL, no anti-DID, smaller maximum step length		
74_BEAMLIMITS2_s5v03_250A	827.67	1386.00
SMALL, anti-DID, smaller maximum step length		
75_BEAMLIMITS_s5v05_250A	738.40	401.20
SMALL, anti-DID, new 250 GeV params		
76_BEAMLIMITS2_s5v05_250A	713.89	420.00
√s = 500 GeV:		
LARGE, anti-DID, intermediate result, for illustration,		
43_akiya_l5_500TDR	1344.70	579.50

- Now backscattered particles ~ 50-55% of total background (without antiDID)
- Anti-DID effect
  - Reduces only backscattered particles rate
  - ~ -35% reduction on total background
- Small geometry: small B field effect
- The safety margin for data flow/band width/power estimates: ~ 3-5
- Percent level occupancy can be reached
  - E.g.: safety factor of 5, BX ~500 ns, pitch ~22um, read-out time ~ 4 us, cluster multiplicity ~5

⇨ Background (DBD@500GeV) ~ Background(@250GeV with new L*, new lumi, with A-DID, bug corrected)
⇨Anti-DID effect significant now but moderate.
⇨Large uncertainties remains (+bunch-by-bunch variations)

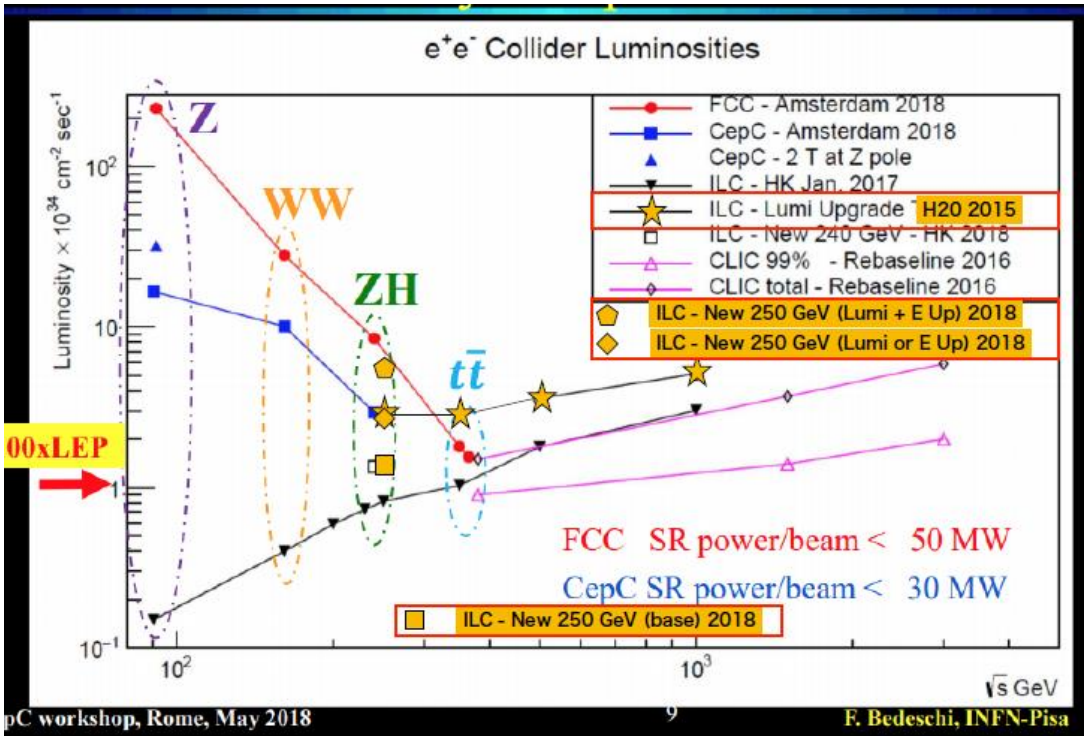
Luminosity options and beam background

arXiv:1711.00568

Lumi ($cm^{-1}.s^{-1}$)	TDR	New (2018)	2625 bunches 5 Hz	2625 bunches 10 Hz
$\sqrt{s}$ = 250 GeV	0.82 x 10^{34}	1.35 x 10^{34}	2.7 x 10^{34}	5.4 x 10^{34}

- Luminosity $\propto (\delta_{bs})^{1/2}$
  - affordable @ 250 GeV

⇨ significant effect on #hits/BX



- 2 other options
  - # bunches: 1312 ⇨ 2625
  - Repetition rate: 5 ⇨ 10 trains

⇨ no effect on #hits/BX
⇨ no effect on #hits/read-out if bunch time spacing remains the same (~ 500 ns)
⇨ significant effect (x4) on data flow per second.

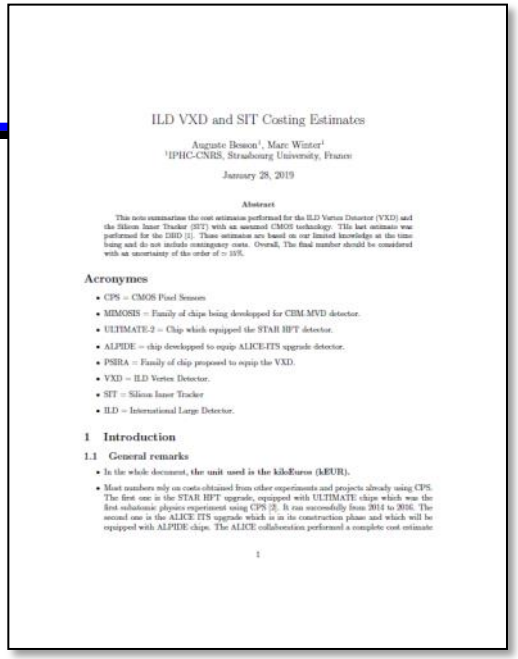
Data flux (New Background estimates @√s= 250 GeV)

Layer	DBD occupancy (hits/cm²/BX)	Detector surface (mm²)	#hits/BX	#hits/read out	#hits/train	# hits/s	Data rate (Mbits/train)	Data rate (Mbits/s)	Data rate (Mbits/train) With safety factor of 3	Data rate (Mbits/s) With safety factor of 3
	@ √s = 250 GeV	Length x width x # ladders		assuming 4 μs i.e. 8 BX	Assuming 1312 bunches per train	Assuming 5 trains / s	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit
0	5.89± 2.47	125 x 11 x 10 = 13 750	810	6480	1062 K	5 314 K	106	530	318	1590
1	3.40± 1.49	125 x 11 x 10 = 13 750	470	3760	616 K	3 083 K	62	310	186	930
2	0.16± 0.09	125 x 2 x 2.2 x 11 =60 500	97	776	127 K	636 K	13	65	39	195
3	0.13± 0.08	125 x 2 x 2.2 x 11 =60 500	79	632	104 K	518 K	10	50	30	150
4	0.03 ± 0.02	125 x 2 x 2.2 x 17 =99 000	30	240	39 K	197 K	4	20	12	60
5	0.03 ± 0.02	125 x 2 x 2.2 x 17 =99 000	30	240	39 K	197 K	4	20	12	60
TOTAL		346 100 mm² ~ 0.35 m²	1516	12128	1 989 K	9 945 K	200	1 000	600	3 000

- average raw data size per BX, event or train. (with or without safety factor on beam background included)
  - Average size per BX : ~0.15 Mbits / BX ⇨ 0.45 Mbits / BX (with safety factor of 3)
  - Average size per event (~8 BX) : ~1.2 Mbits/ readout ⇨ 3.6 Mbits / readout (with safety factor of 3)
  - Average size per train : ~200 Mbits / train ⇨ 600 Mbits / train (with safety factor of 3)
  - Average size per second: ~1000 Mbits / train ⇨ 3000 Mbits / second (with safety factor of 3)

Costing

Cost estimates and integration



ILD VXD and SIT Costing Estimates

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January 28, 2019

Abstract

This note summarizes the cost estimates performed for the ILD Vertex Detector (VXD) and the Silicon Inner Tracker (SIT) with an assumed CMOS technology. This last estimate was performed for the DBD [3]. Those estimates are based on our limited knowledge at the time being and do not include contingency costs. Overall, The final number should be considered with an uncertainty of the order of ± 15%.

Acronymes

- CPS = CMOS Pixel Sensors
- MIMOSIS = Family of chips being developped for CBM-MVD detector.
- ULTIMATE-2 = Chip which equipped the STAR HFT detector.
- ALPIDE = chip developped to equip ALICE-ITS upgrade detector.
- PSIRA = Family of chip proposed to equip the VXD.
- VXD = ILD Vertex Detector.
- SIT = Silicon Inner Tracker
- ILD = International Large Detector.

1 Introduction

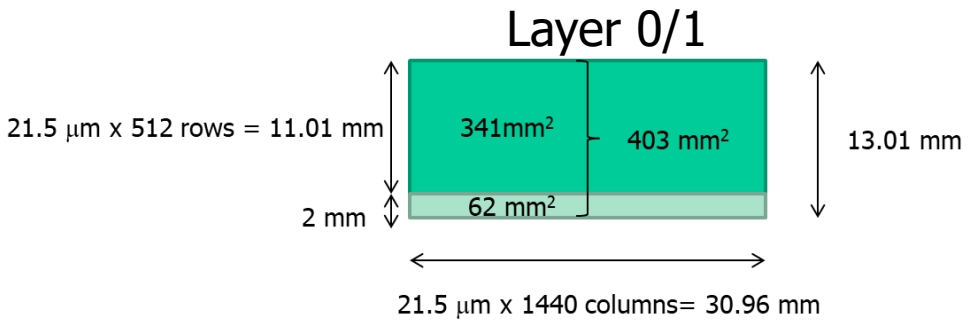
1.1 General remarks

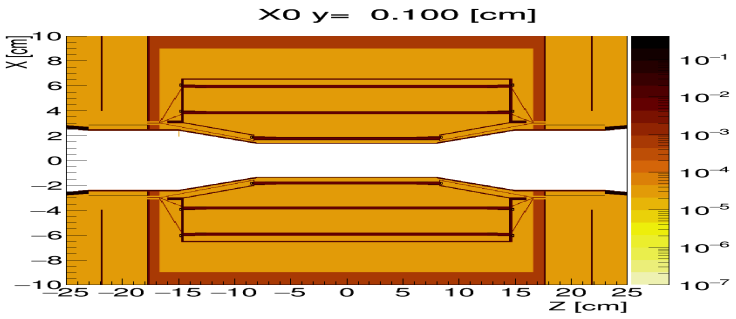
- In the whole document, the unit used is the kiloEuros (kEUR).
- Most numbers rely on costs obtained from other experiments and projects already using CPS. The first one is the STAR HFT upgrade, equipped with ULTIMATE chips which was the first subatomic physics experiment using CPS [2]. It ran successfully from 2014 to 2016. The second one is the ALICE ITS upgrade which is in its construction phase and which will be equipped with ALPIDE chips. The ALICE collaboration performed a complete cost estimate

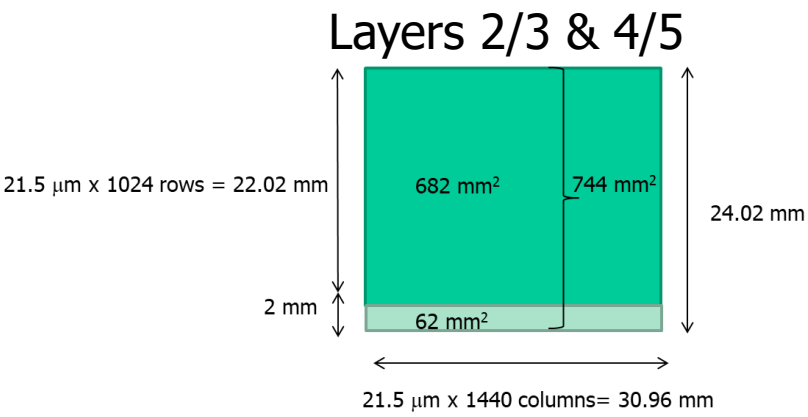
1

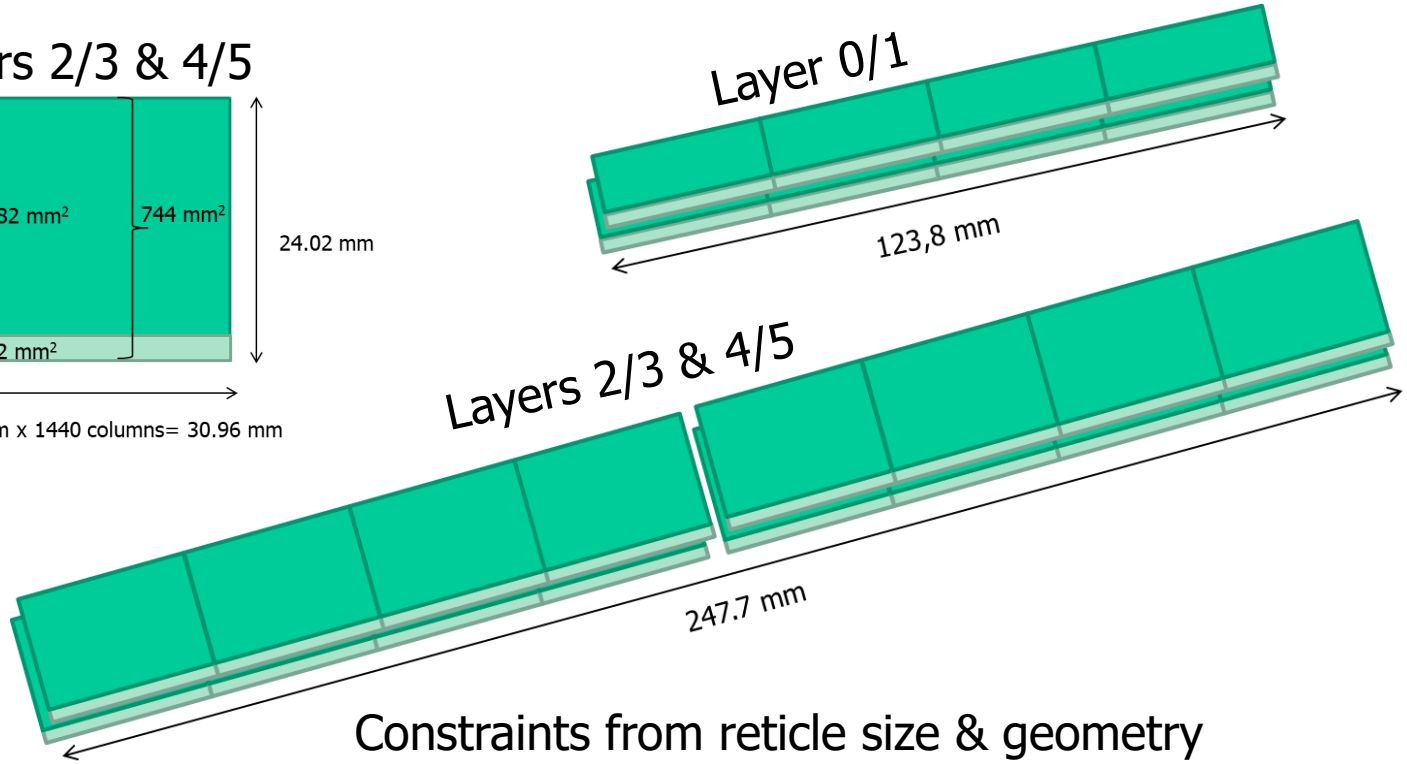
- Added value:
  - Opportunity to identify issues and to revisit the design
- Sources:
  - STAR HFT, ALICE ITS upgrade and discussions with experts
- Assumptions
  - No contingency added
  - No R & D costs included
    - Preproduction runs included
  - Beam background and data flux staying below the estimated value x 5
  - Assumed:
    - 1 chip design for SIT
    - 2 chip designs for the VXD (might be 1 or 3)
  - Chip Production yield (50%), Spares (20%)
  - Some topics needs more detailed studies
    - (Faraday cage, installation, etc.)
- Uncertainties ~ 15 % (1σ)
  - Evolution of the technology
  - Beam background background

Chip dimensions & ladders









Constraints from reticle size & geometry
Minimize overlaps and dead space between chips

VXD dimensions

Figures per layers						
Layer	0	1	2	3	4	5
Layer Radius (mm)	16	18	37	39	58	60
Layer $\|z\|max$ (mm)	61.9	61.9	123.8	123.8	123.8	123.8
Chip Pixel Number in X	1440	1440	1440	1440	1440	1440
Chip Pixel Number in Y	512	512	1024	1024	1024	1024
Chip Pixel PitchX (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Pixel PitchY (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Dimension X (mm) (sensitive area)	30.96	30.96	30.96	30.96	30.96	30.96
Chip Dimension Y (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
Chip Dimension Y (mm) (non sensitive area)	2.0	2.0	2.0	2.0	2.0	2.0
Chip Surface (mm^2) (sensitive area)	341	341	682	682	682	682
Chip Surface (mm^2) (non sensitive area)	62	62	62	62	62	62
Chip Surface (mm^2) (total)	403	403	744	744	744	744
Ladder Length (mm) (sensitive area)	123.8	123.8	123.8	123.8	123.8	123.8
Ladder Width (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
N chip per ladder on each side	4	4	4	4	4	4
Layer Surface (cm^2) (sensitive area)	136.3	136.3	599.7	599.7	926.9	926.9
N Chips Per Layer	40	40	88	88	136	136
Total surface (cm^2) (sensitive area)	3484					

Figures per double layers			
	Layer 0/1	Layer 2/3	Layer 4/5
N Chips in z	4	$4 + 4 = 8$	$4 + 4 = 8$
N Ladders	10	$2 \times 11 = 22$	$2 \times 17 = 34$
N Chips Per double Layer	80	176	272
N Chips (per architecture)	80	448	
N Total Chips	528		

Costs Estimates (VXD)

More details
in the costing document

PRELIMINARY

Domain	Item	Material Unit Cost	Material Cost	Manpower Costs	Total Costs	Notes
Sensors			1152	100	1252	
Sensors	Masks	300	600	0	600	a
	blank wafers	0.1	30	0	30	
	Quality Assurance	2.4	30	0	30	
	Wafer production	3.2	192	0	192	b
	Thining	0.5	30	0	30	c
	Dicing	0.5	30	0	30	c
Tests	Probe station	200	200	0	200	d
	Others		40	100	140	e
Mechanics			452	500	952	
Ladders	Mechanical support	0.5	34	0	34	f
	Gluing	1	68	0	68	f
	Others		0	100	100	
Mechanics	Be support and others		200	100	300	g
	Assembling		50	200	250	h
Faraday cage			100	100	200	g
Electronics			486	400	886	
Flex cable	Construction	0.7	140	100	240	j
	Gluing		100	50	150	cf
	Bonding		80	20	100	cf
	Tests		0	30	30	
Read-out	Optical cables	0.3	24	0	24	i
			0	0	20	
			0	0	20	
				100	100	
			2	100	182	i
			0	0	20	
			0	250	1020	
			0	20	100	i
			5	25	50	
			5	5	20	
			0	50	350	
			0	0	50	
			0	0	150	
			0	50	100	
			0	100	200	
			0	200	300	
			0	200	250	
			0	0	50	
			50	1450	4410	

[a] Assumed 2 engineering runs
[b] 12 (inner) + 48 (outer) wafers assumed
[c] High unit costs due to small production

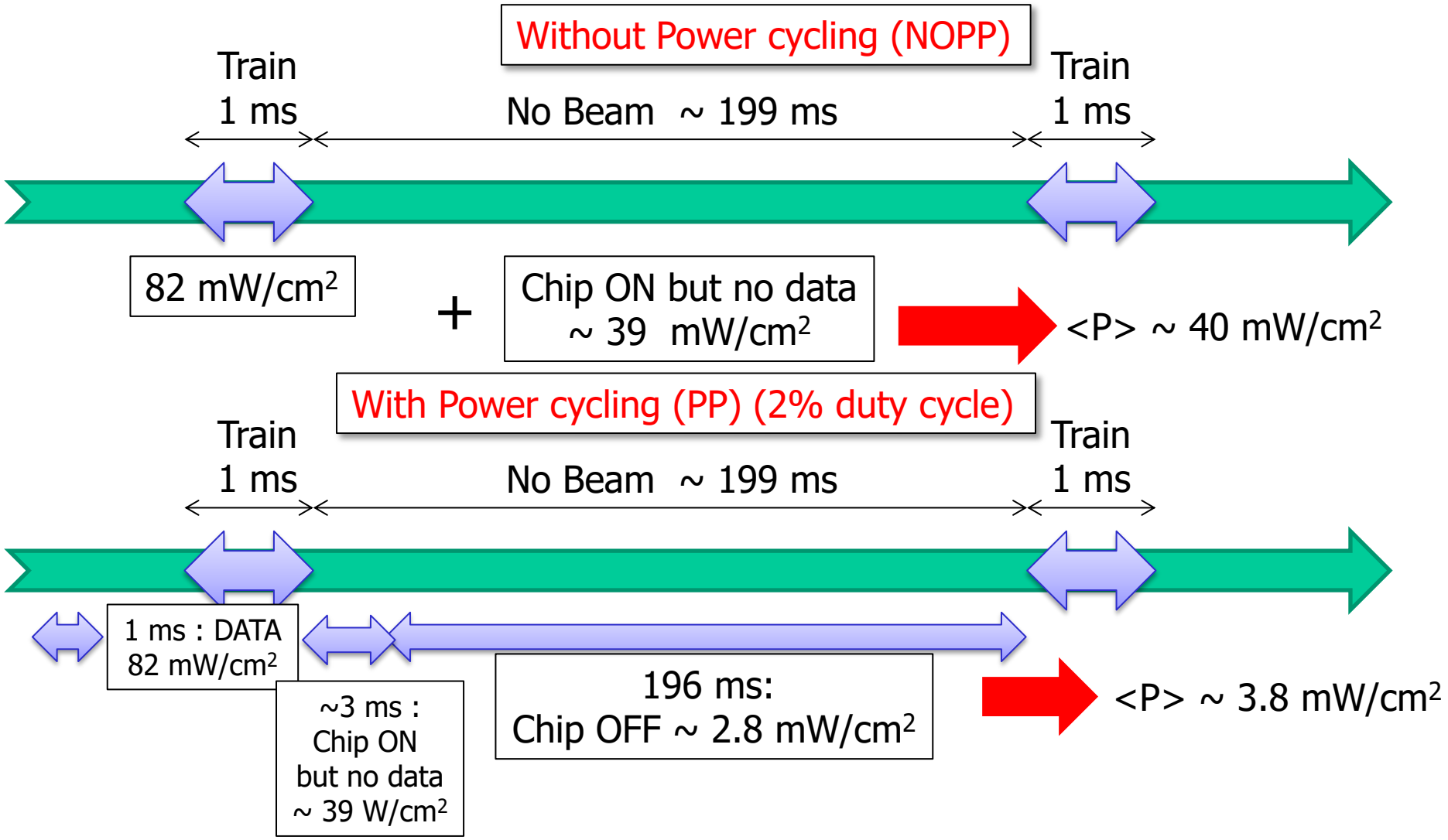
9

	ILD VXD L0-L1	ILD VXD L2-L5	ILD VXD total	ILD SIT	ALICE ITS	STAR HFT	ITS/VXD ratio	ITS/SIT ratio	note
Detector surface (m^2)	$\simeq 0.03$	$\simeq 0.3$	$\simeq 0.35$	7	10	0.16	30	1.5	
Chip surface (mm^2)	403	744	-	735	450	459	$\simeq 1$	$\simeq 1$	
# Chips mounted	80	448	528	9000	24500	400	45	2.5	a
# Chips to produce	192	1075	1267	21600	58800	1920	45	2.5	b
# Chips per wafer	45	22	-	22	45	$\simeq 50$			
# Wafers produced	12	48	60	1000	1300	$\simeq >75$			cd
# Chips produced	540	1056	1596	22000	58800	3600			
# Pixels	$60M$	$660M$	$720M$	$8.2G$	$13G$	$360M$			
# Ladders	10	56	66	280 ?	192	40			
# Layers	2	4	6	4	7	2			
# Chips per ladder	8	8	-	24/42	e	10			f

Detector	Cost	Sensors	Mechanics	Eletronics	Services	Installation	Total
VXD	Material	1152	452	486	770	100	2960
	Manpower	100	500	400	250	200	1450
	TOTAL (kEUR)	1252	952	886	1020	300	4410

Power estimates

Power scheme for VTX-ILD (inner layer)



Hypothesis: 3 double sided layers (3483 cm²), PSIRA architecture (4 μs / 4 μm), DBD background @ √s = 500 GeV, no safety factor

Power: Results

- Chip read-out speed
  - 2 ms - 4 ms
- Power pulsing
  - Power ON, no beam during 1-3 ms
    - Leading parameter With NO P.P.
  - Power OFF: 10-30 mW/chip
    - Leading parameter with P.P.
- Outer layers
  - Lower occupancy
  - Power is dominated by outer layers
- Beam background rate
  - DBD – DBD x 2

Power Analog ($mW/chip$)	49.22
Power Bias ($mW/chip$)	4.5
Power PriorityEncoder ($mW/chip$)	4.219
Power DigitalPeriphery ($mW/chip$)	64.27
Power PLL ($mW/chip$)	18.5
Power Serializer With Data ($mW/chip$)	86.06
Power Serializer With No Data ($mW/chip$)	0
Power LVDS ($mW/chip$)	56.4

Period	Relative Energy
E during train	225 mJ ~ 4 %
E between train (Power ON)	380 mJ ~ 6 %
E between train (Power OFF)	5740 mJ ~ 90 %

Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

Beam background rate	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
	(μs)	(W)	Conservative	Ambitious
DBD	4 μs	102 W	~31 W	~12 W
DBD	2 μs	122 W		
DBD x 2	4 μs	107 W		
DBD x 2	2 μs	127 W		

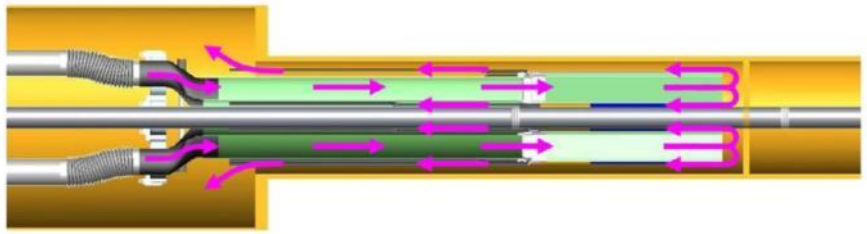
Power consumption

- Power estimates:

  Relatively robust when playing with different parameters

  - 100-130 W range with NOPP, 10-30 W range with PP (uncertainties to be reduced with MIMOSIS)
  - Valid for this architecture only.
- Air Cooling:
  - STAR HFT demonstrated that 23°C air flow cooling @ ~ 10 m/s could extract up to ~ 150 mW / cm^2 (~350 W in total)

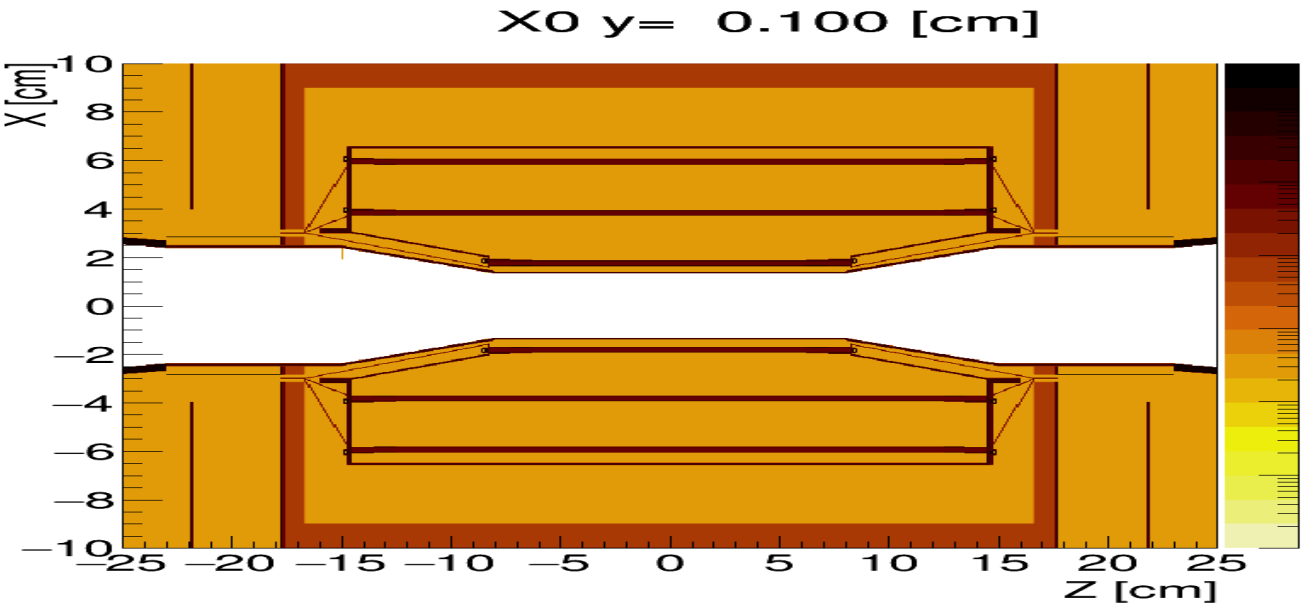
    The STAR MAPS-based PiXeL Detector NIM, A 907 (2018) 60-80
    - Caveat: 15 cm diameter flexible ducts was used (not possible for ILD)

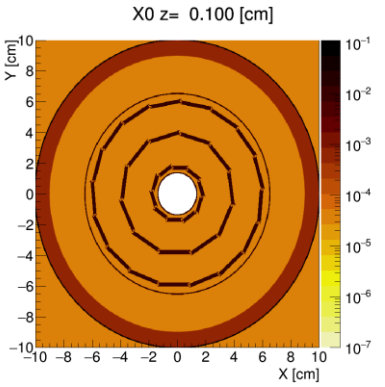


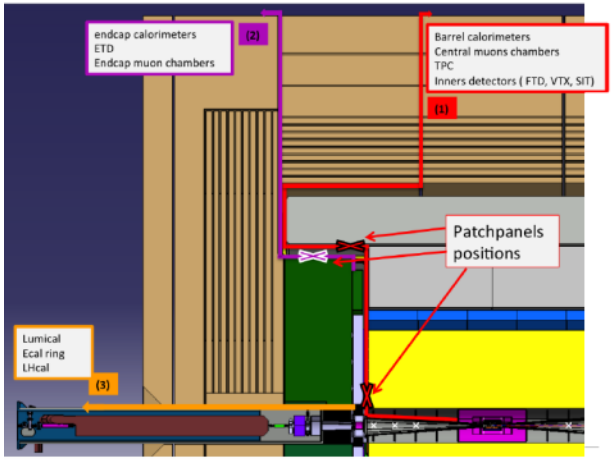
- Margin of improvement:
  - Optimize each layer ?
  - Smaller feature size ⇨ lower digital Power

Cabling discussion

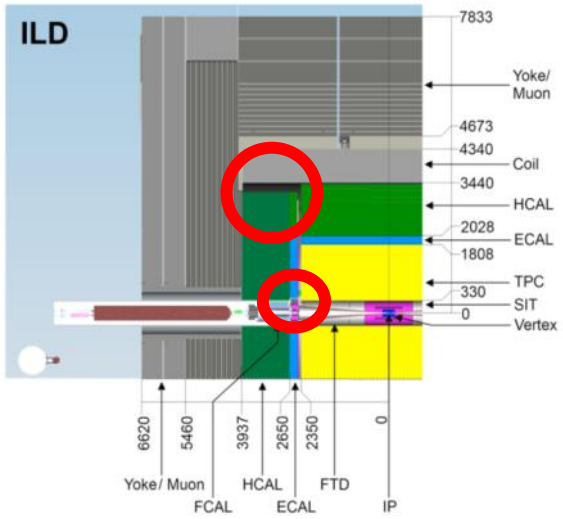
Read-out scheme: connectors/patchpanels

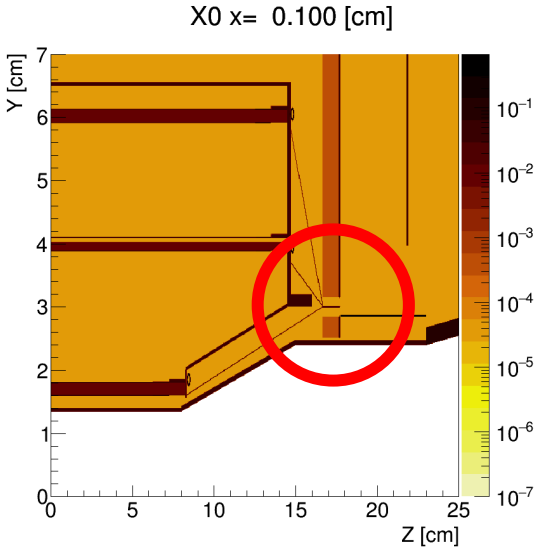


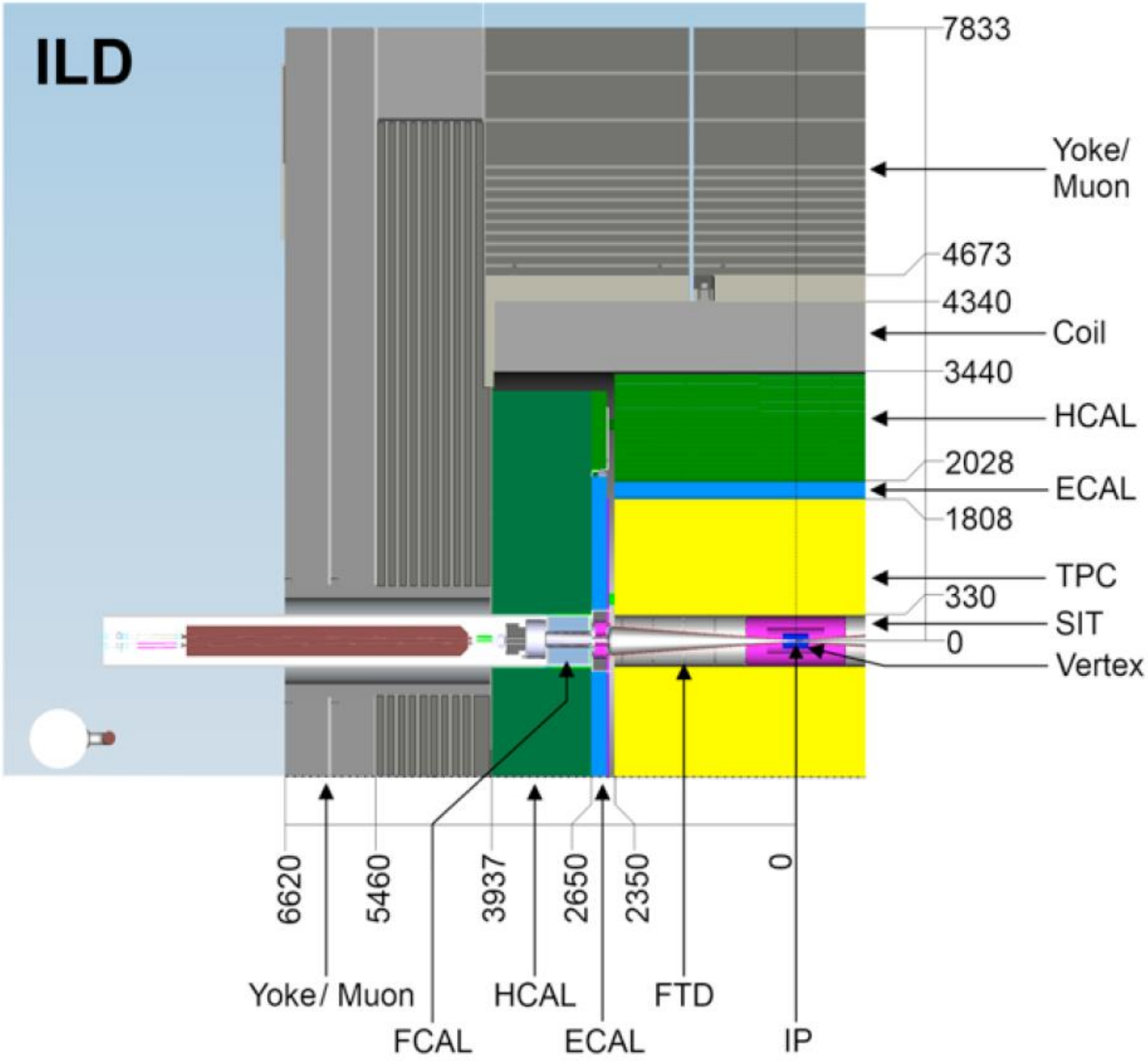




C. Clerc et al. (2009)






ILD
7833
Yoke/
Muon
4673
4340
Coil
3440
HCAL
2028
ECAL
1808
TPC
330
SIT
0
Vertex
6620
5460
3937
2650
2350
0
Yoke/ Muon
FCAL
HCAL
ECAL
FTD
IP

Architecture assumed

- Direct translation of MIMOSIS (for CBM) design adapted to ILD

- What will/may change in the future
  - R & D towards faster read-out
  - Feature size technology
  - Stitching capabilities
  - Material budget optimization

- What still needs to be studied more extensively
  - Cooling
  - Mechanics
  - DAQ

Data encoding & rates (assuming 4 μs read-out time)

- Beam background hits (new lumi @ √s = 250 GeV); no safety factor.
- Total number of hits/read-out
  - Layer 0+1: ~ 12 000 hits
  - Layer 2+3: ~ 1400 hits
  - Layer 4+5: ~ 500 hits
  - Total hits (in 4 us) ~15 000 hits

- Data encoding:
  - 16 bits/pixel x 5 pixels/cluster + trailers/headers ~ 100 bits/hit

- Instantaneous data flux (No safety factor !)
  - Flux = 15 000 hits x 100 bits/hit / 4×10^{-6} s ~ 375 Gbits/s

- Optical fibers (assuming ~8 Gbits/s as a standard)
  - Ladders 0/1 -> 40 fibers
  - Ladders 2-3-4-5 (1 fiber/ladder) -> 28 fibers
  - ⇨ ~35 fibers on each side
  - Diameter: ~ 1 mm ⇨ 28 mm^2 ~ Section

- Surfaces:
  - L0: ladders: 1.1 x 12.5 x 10 = 137.5 cm^2
  - L1: ladders: 1.1 x 12.5 x 10 = 137.5 cm^2
  - L2: ladders: 2.2 x 12.5 x 2 x 11 = 605 cm^2
  - L3: ladders: 2.2 x 12.5 x 2 x 11 = 605 cm^2
  - L4: ladders: 2.2 x 12.5 x 2 x 17 = 990 cm^2
  - L5: ladders: 2.2 x 12.5 x 2 x 17 = 990 cm^2
  - TOTAL : ladder surfaces = 3461 cm^2

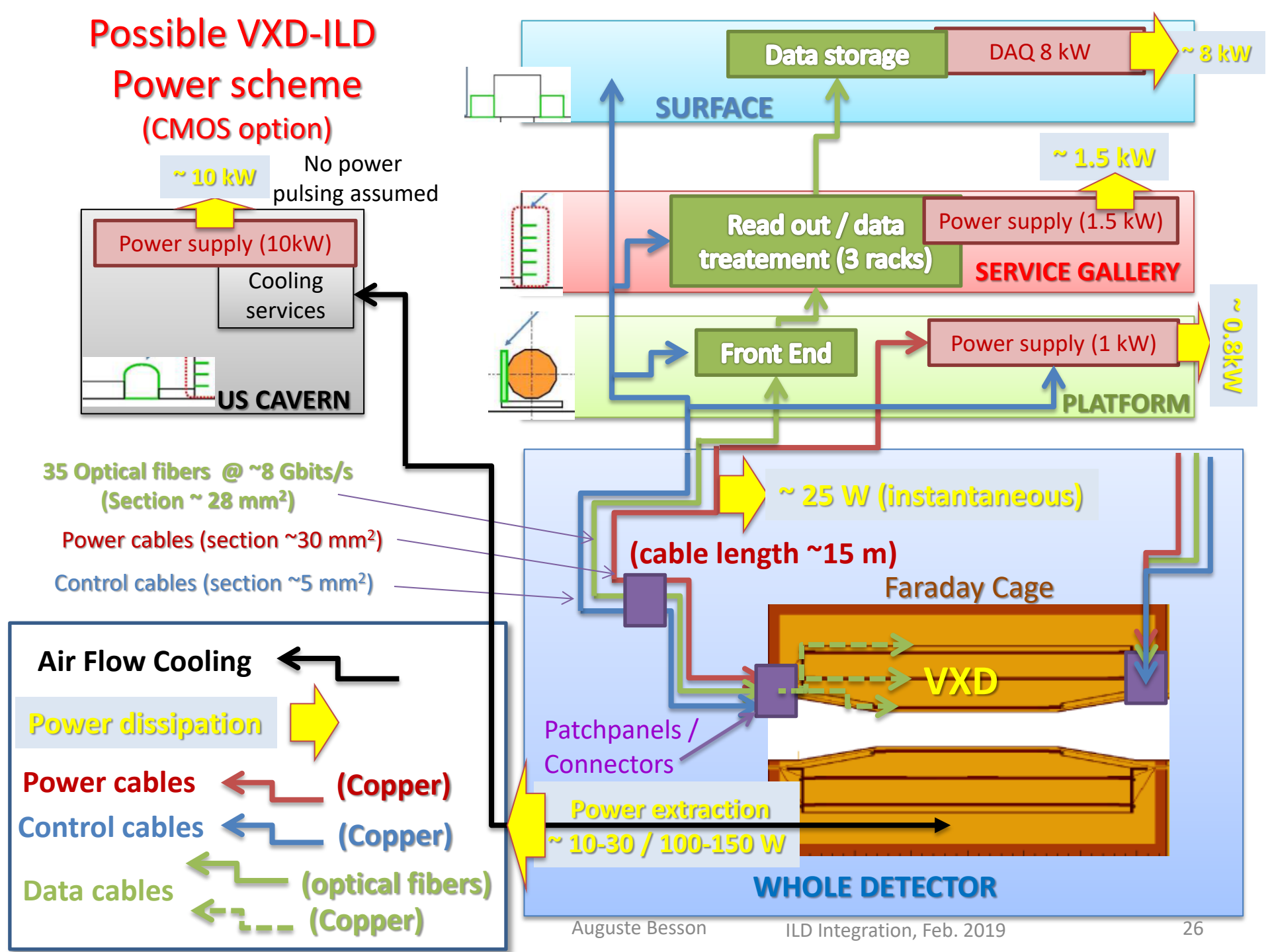
Cables (no shielding included)

- Power consumption VXD (instantaneous)

INSTANTANEOUS POWER						
Power ON During Train per chip $(mW/chip)$	293.4	293.4	178.1	178.1	171.1	171.1
Power ON Between Train per chip $(mW/chip)$	138.8	138.8	101.2	101.2	101.2	101.2
Power OFF Between Train per chip $(mW/chip)$	10	10	10	10	10	10
Power ON During Train per cm^2 (mW/cm^2)	82.21	82.21	49.92	49.92	47.95	47.95
Power ON Between Train per cm^2 (mW/cm^2)	38.9	38.9	28.37	28.37	28.37	28.37
Power OFF Between Train per cm^2 (mW/cm^2)	2.802	2.802	2.802	2.802	2.802	2.802
Power ON During Train per layer $(W/layer)$	11.73	11.73	31.35	31.35	46.54	46.54
Power ON Between Train per layer $(W/layer)$	5.553	5.553	17.81	17.81	27.53	27.53
Power OFF Between Train per layer $(W/layer)$	0.4	0.4	1.76	1.76	2.72	2.72
TOTAL : Surface=3483 cm^2 ; Total Peak Power = 179.3 W						

  - P_{tot} ~ 200 W ; @ 1.8 V ⇨ I_{tot} ~ 100 A ⇨ I_{1side} = 50 A per end caps
- Power cables
  - Assuming copper (Aluminium doesn't change the picture)
    - Cable length L ~15 m
    - P_{diss}(cables) ~ 25 W ⇨ $\Delta V = P_{diss}(cables) / I_{1side}$ = 0.5 V
    - $R = \rho L / S = \Delta V / I_{1side}$ ⇨ $S = \rho L I_{1side} / \Delta V$ ~ 30 mm^2 ~ Section
- Control cables (copper)
  - Section ~ 5 mm^2

Possible VXD-ILD Power scheme (CMOS option)



SIT

Geometry		
R[mm]	Z[mm]	$\cos\theta$
153	368	0.910
300	644	0.902

SIT

Geometry		
R[mm]	Z[mm]	$\cos\theta$
153	368	0.910
300	644	0.902

- Costing done in parallel
  - Much more open integration questions
    - More educated guesses…
  - PLUME ladders have to be revisited
    - Length / double sided ladder thickness / stiffness not the same
    - Larger flex cable
    - Stitching = improved stiffness ?
    - ALICE ITS upgrade:

      Comparable dimensions and surfaces (not double sided though)
  - Cabling / data flow schemes to be done
- Power (raw estimate with MIMOSIS architecture, 2 μs)
  - Distribution in parallel ? (ALICE = 1 cable / ladder)
  - Total surface: ~ 67 000 cm^2
  - Very low occupancy w.r.t to the VXD
    - <P> ~ 30 mW/cm^2 (NO power pulsing) ⇨ 2 kW ☹
    - <P> ~ 3.5 mW/cm^2 (with power pulsing) ⇨ 235 W
  - More space for air flow
  - Faster read-out (0.5 – 1 μs range) would need more power.

SIT costing

Figures per layers				
Layer	0	1	2	3
Layer Radius (mm)	153	155	298	300
Layer $\|z\|max$ (mm)	368	368	644	644
Chip Pixel Number in X	1152	1152	1152	1152
Chip Pixel Number in Y	800	800	800	800
Chip Pixel PitchX (μm)	26.6	26.6	26.6	26.6
Chip Pixel PitchY (μm)	27.5	27.5	27.5	27.5
Chip Dimension X (mm) (sensitive area)	30.64	30.64	30.64	30.64
Chip Dimension Y (mm) (sensitive area)	22.0	22.0	22.0	22.0
Chip Dimension Y (mm) (non sensitive area)	2.0	2.0	2.0	2.0
Chip Surface (mm^2) (sensitive area)	674	674	674	674
Chip Surface (mm^2) (non sensitive area)	61	61	61	61
Chip Surface (mm^2) (total)	735	735	735	735
Ladder Length (mm) (sensitive area)	367.7	367.7	643.4	643.4
Ladder Width (mm) (sensitive area)	22	22	22	22
N chip per ladder on each side	12	12	21	21
Layer Surface (cm^2) (sensitive area)	8089	8089	25500	25500
N Chips Per Layer	1200	1200	3780	3780
Total surface (cm^2) (sensitive area)	$\simeq$ 67 000			

Figures per double layers		
	Layer 0/1	Layer 2/3
N Chips in z	$12 + 12 = 24$	$21 + 21 = 42$
N Ladders	$\simeq 2 \times 50 = 100$	$\simeq 2 \times 90 = 180$
N Chips Per double Layer	1200	7560
N Total Chips	$\simeq$ 9000	

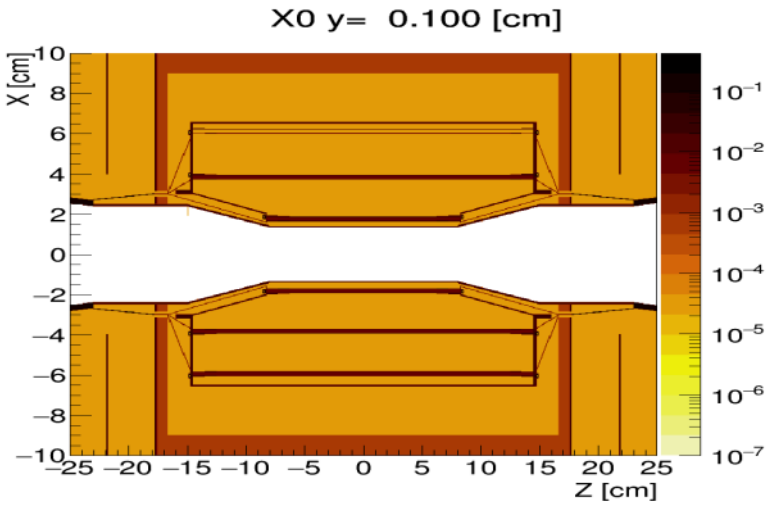
More details
in the costing document

PRELIMINARY

Detector	Cost	Sensors	Mechanics	Eletronics	Services	Installation	Total
VXD	Material	1152	452	486	770	100	2960
	Manpower	100	500	400	250	200	1450
	TOTAL (kEUR)	1252	952	886	1020	300	4410
SIT	Material	3820	760	1275	1580	110	7545
	Manpower	200	500	800	300	200	2000
	TOTAL (kEUR)	4020	1260	2075	1880	310	9545

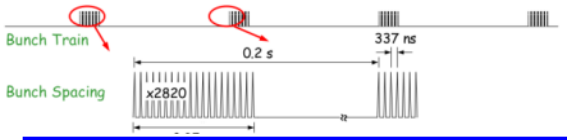
Open questions and conclusion

- Not covered
  - Cooling options
  - DAQ scheme
  - Mechanical support design
- Open questions
  - Cooling the beam pipe ?
  - Shielding cables to be evaluated
  - Faraday cage
  - Patch panels ⇨ detector opening ?
  - Data cable ⇨ Connectors to optical fibers

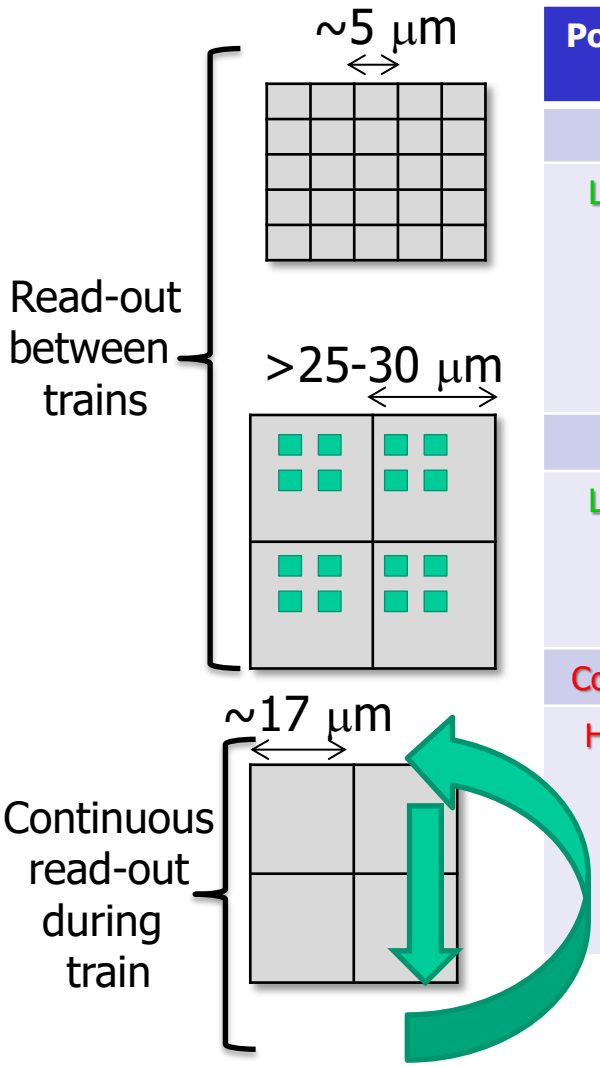


- Integration:
  - A lot to be done ⇨ manpower issue
  - Waiting for March 7th…

Back up



Read-out strategies vs resolution/occupancy



Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^5 grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.
⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

Configuration 0						
N Trains = 5						
InterTrain Duration = 200 ms						
Train Duration = 1 ms; StandBy Duration = 3 ms; Power OFF Duration = 196 ms						
Layer	0	1	2	3	4	5
Chip Pixel Number in X	1440	1440	1440	1440	1440	1440
Chip Pixel Number in Y	512	512	512	512	512	512
Chip Pixel PitchX (μm)	22	22	22	22	22	22
Chip Pixel PitchY (μm)	22	22	22	22	22	22
Chip Dimension X (mm)	31.68	31.68	31.68	31.68	31.68	31.68
Chip Dimension Y (mm)	11.26	11.26	11.26	11.26	11.26	11.26
Chip Surface (mm^2) (active area)	356.8	356.8	356.8	356.8	356.8	356.8
Layer Radius (mm)	16	18	37	39	58	60
Ladder Length (mm) (active area)	126.7	126.7	126.7	126.7	126.7	126.7
Ladder Width (mm) (active area)	11.26	11.26	22.53	22.53	22.53	22.53
Ladder Number	10	10	22	22	34	34
Layer Surface (cm^2)	142.7	142.7	628	628	970.6	970.6
N Chips Per Layer	40	40	176	176	272	272
Read Out Time (μs)	4	4	4	4	4	4
Background Rate ($hits/cm^2/BX$)	6.3	4	0.25	0.21	0.04	0.04
Average Pixels Per Cluster	5	5	5	5	5	5
Power Analog ($mW/chip$)	49.22	49.22	49.22	49.22	49.22	49.22
Power Bias ($mW/chip$)	4.5	4.5	4.5	4.5	4.5	4.5
Power PriorityEncoder ($mW/chip$)	4.219	4.219	4.219	4.219	4.219	4.219
Power DigitalPeriphery ($mW/chip$)	64.27	64.27	64.27	64.27	64.27	64.27
Power PLL ($mW/chip$)	18.5	18.5	18.5	18.5	18.5	18.5
Power Serializer With Data ($mW/chip$)	86.06	86.06	8.438	8.438	1.406	1.406
Power Serializer With No Data ($mW/chip$)	0	0	0	0	0	0
Power LVDS ($mW/chip$)	56.4	56.4	18.8	18.8	18.8	18.8
INSTANTANEOUS POWER						
Power ON During Train per chip ($mW/chip$)	293.4	293.4	178.1	178.1	171.1	171.1
Power ON Between Train per chip ($mW/chip$)	138.8	138.8	101.2	101.2	101.2	101.2
Power OFF Between Train per chip ($mW/chip$)	10	10	10	10	10	10
Power ON During Train per cm^2 (mW/cm^2)	82.21	82.21	49.92	49.92	47.95	47.95
Power ON Between Train per cm^2 (mW/cm^2)	38.9	38.9	28.37	28.37	28.37	28.37
Power OFF Between Train per cm^2 (mW/cm^2)	2.802	2.802	2.802	2.802	2.802	2.802
Power ON During Train per layer ($W/layer$)	11.73	11.73	31.35	31.35	46.54	46.54
Power ON Between Train per layer ($W/layer$)	5.553	5.553	17.81	17.81	27.53	27.53
Power OFF Between Train per layer ($W/layer$)	0.4	0.4	1.76	1.76	2.72	2.72
TOTAL : Surface=3483 cm^2 ; Total Peak Power = 179.3 W						
AVERAGE POWER						
MeanPower per chip NOPP (mW)	139.6	139.6	101.6	101.6	101.6	101.6
MeanPower per cm^2 NOPP (mW/cm^2)	39.12	39.12	28.47	28.47	28.46	28.46
MeanPower per layer NOPP ($W/layer$)	5.584	5.584	17.88	17.88	27.63	27.63
Mean Power total NOPP (W) = 102.2 W						
MeanPower per chip PP (mW)	13.35	13.35	12.21	12.21	12.17	12.17
MeanPower per cm^2 PP (mW/cm^2)	3.741	3.741	3.421	3.421	3.412	3.412
MeanPower per layer PP ($W/layer$)	0.534	0.534	2.149	2.149	3.311	3.311
Mean Power total PP (W) = 11.99 W						
Energy per layer During Train (mJ/layer/train)	11.73	11.73	31.35	31.35	46.54	46.54
Energy per layer DuringStandBy(mJ/layer/train)	16.66	16.66	53.44	53.44	82.59	82.59
Energy per layer BetweenTrain(mJ/layer/train)	78.4	78.4	345	345	533.1	533.1
E During Train (mJ) = 179.3; E DuringStandBy (mJ) = 305.4; E BetweenTrain (mJ) = 1913						
Mean Power total NOPP (W) = 102.2 W ; Mean Power total PP (W) = 11.99 W ;						

Table 1: Power Consumption, configuration 0