SiEcal – Elements of R&D and Design Constraints

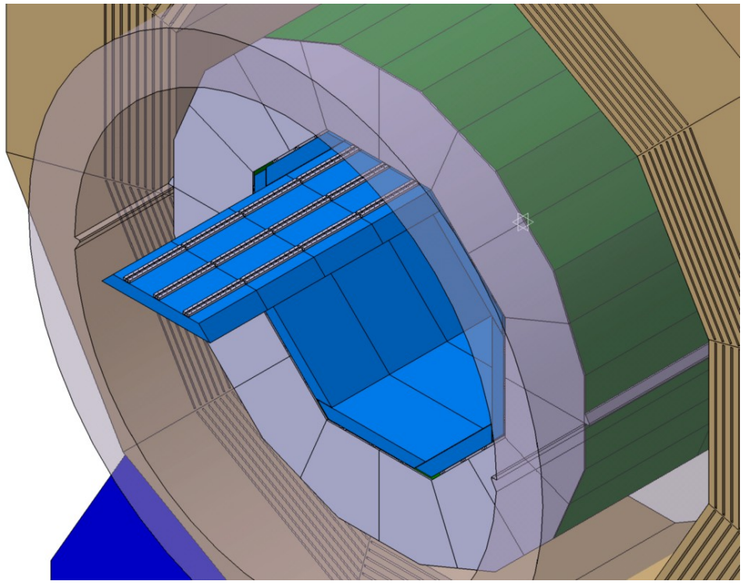
Roman Pöschl,

ILD Integration Meeting, February 2019, DESY/Hamburg, Germany

SiEcal - Introduction

Optimized for Particle Flow Algorithm

Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- O(10^8) cells
- “No space”

=> Large integration effort

Basic Requirements:

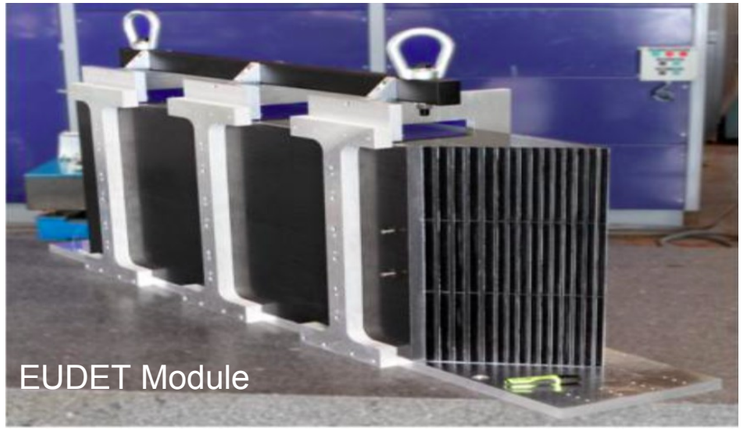
- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

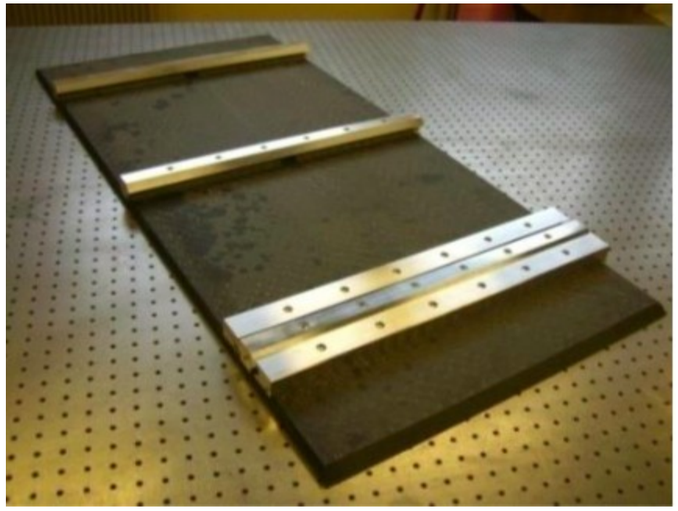
Basic Choices:

- Tungsten as absorber material
- X_0=3.5mm, R_M=9mm, Θ=96mm
- Narrow showers
- Assures compact design

- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 as design value

SiEcal Alveaolar Structure(s)



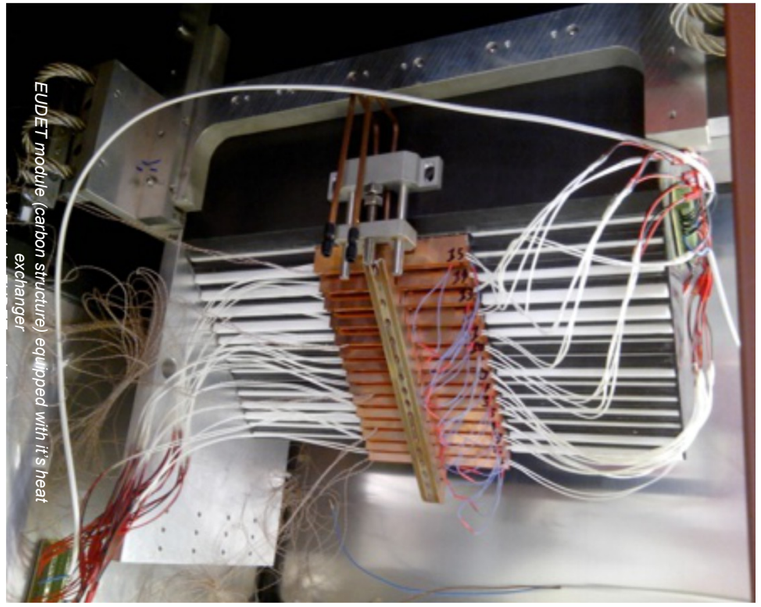


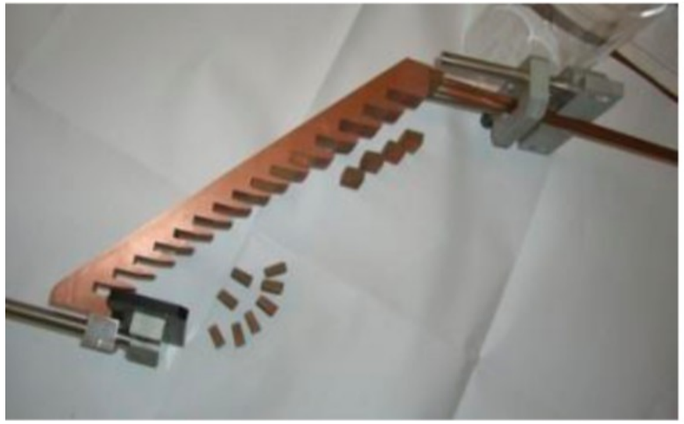
Construction of full size mechanical C/Fibre structures

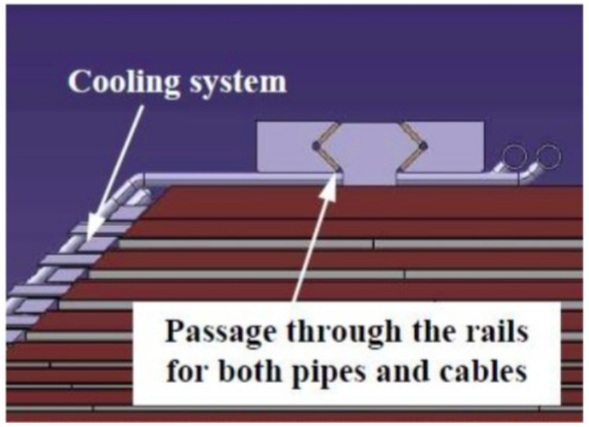
up to 2.5m long alveoli

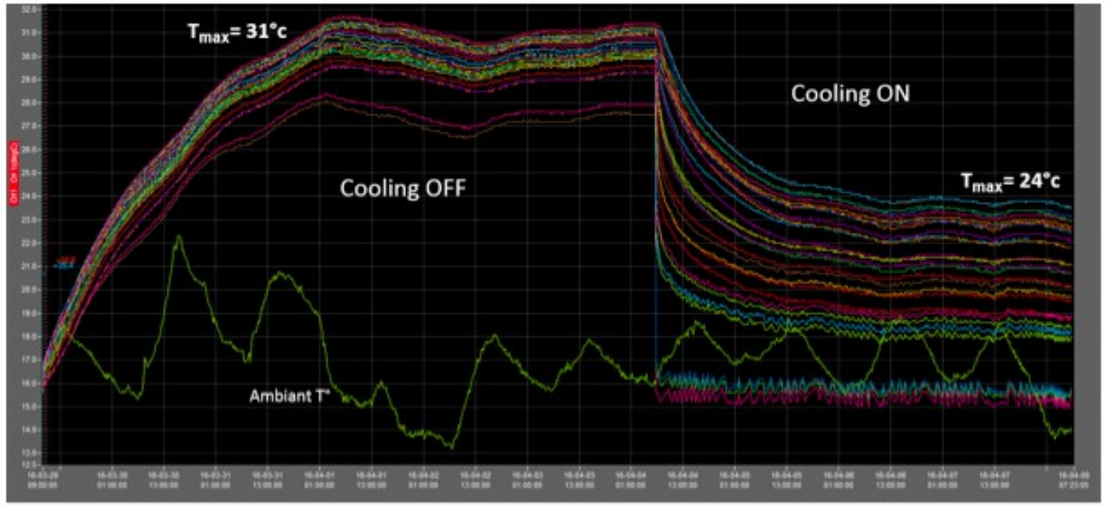
Interface to other detectors
i.e. HCAL in ILD

SiEcal – Thermal tests







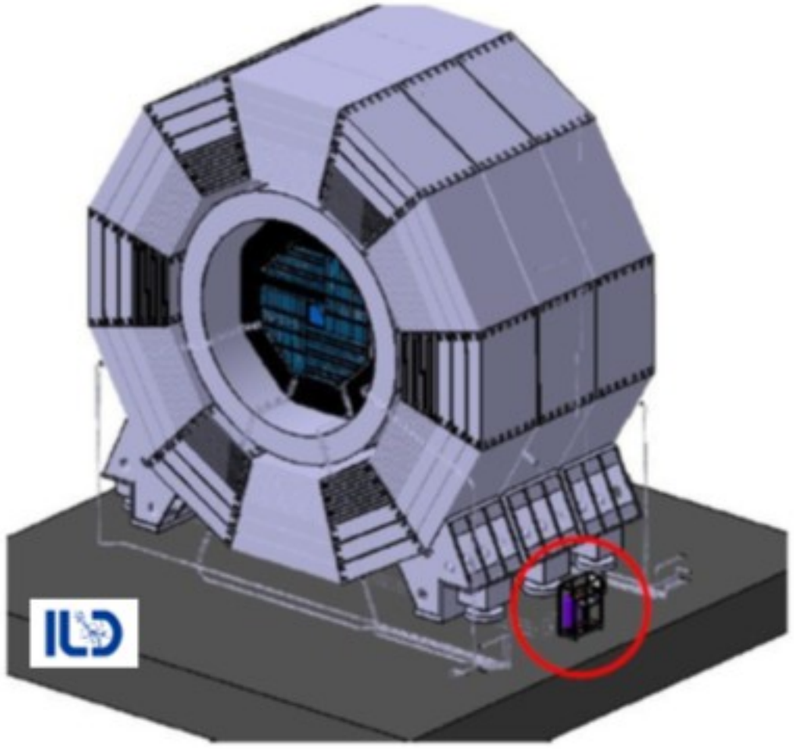


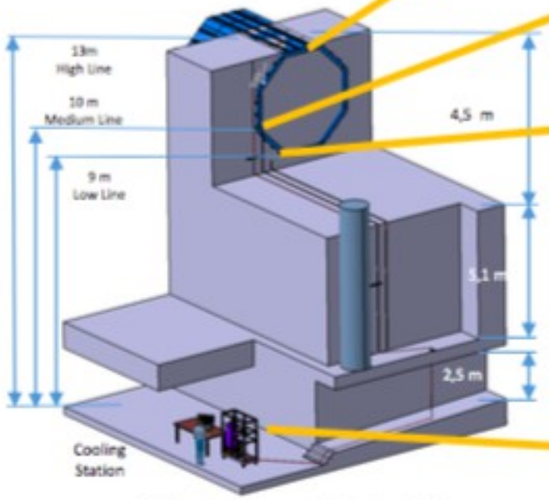
- EUDET Module used as thermal demonstrator
- Real size test of local cooling system

- Maximal Temperature 24˚ at the extremity of slab (~1.5m)

SiEcal – Cooling system: Large leakless loop

- Demonstration and performance of a large leak-less cooling-loop on 3 levels (13m-10m- 9m)





LPSC cooling test area with a drop of 13 m

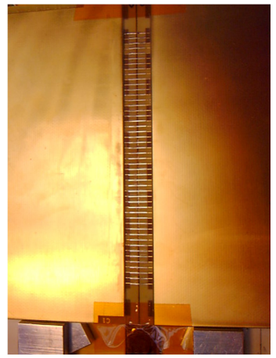
Upper part of the experiment

Julien Giraud

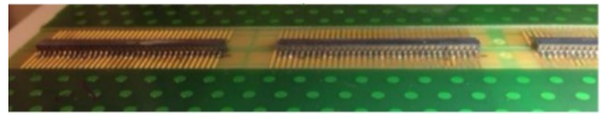
SiEcal – A layer

A layer is composed of several short ASUs:

- A.S.U. : Active Sensors Units

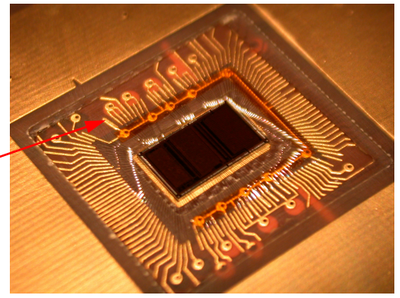


Interconnection
Important for signal integrity

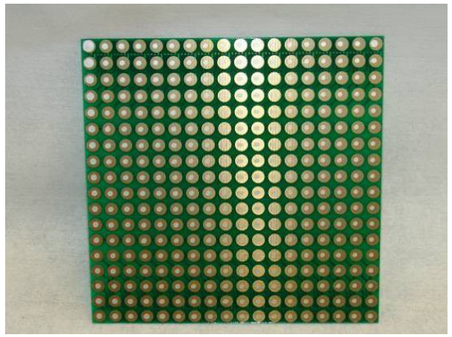


ASIC+PCB+SiWafer =ASU

Wire Bonding or BGA



PCB is glued onto SiWafers using gluing robots



Length of layer:
1.5m for barrel
2.5m for endcaps

Front end electronics readout and DAQ

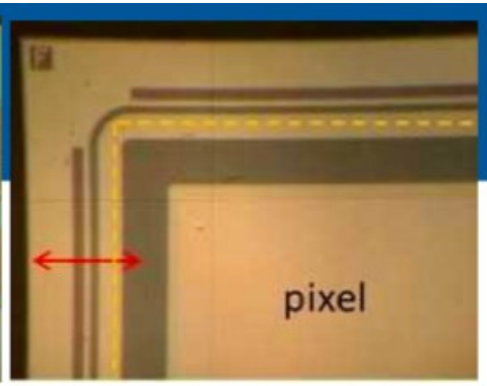
Silicon Sensors

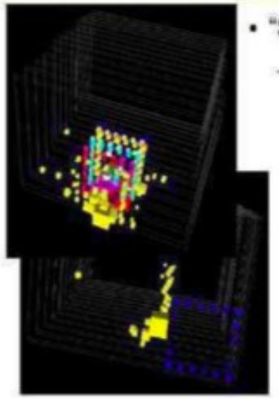
Cost driven

- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction(**CALIIMAX program**)
- Decoupling of Guard Ring (Square Events).
- new design of ILD detector

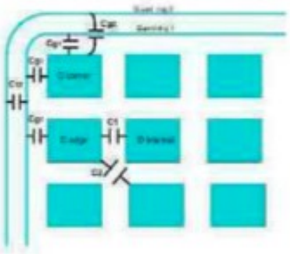
Command Sensors (@ Hamamatsu)

- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8'' in 186mm alveola
  320 → 550, 650 → 725 µm ?

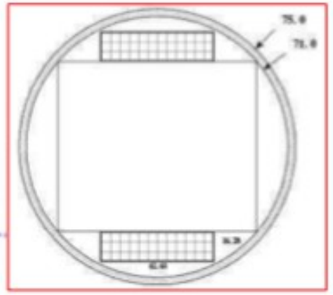


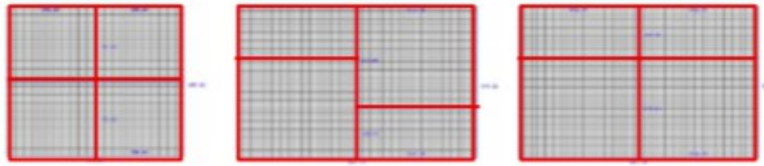


- "Square events"
  - cross talk between guard rings and pixels



'quantum unit' of ILD dimensions (here 6'' wafer)





Front end electronics readout and DAQ

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

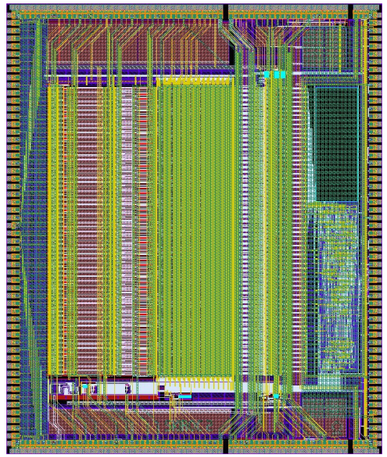
SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels

High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)

Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)

Auto-trigger at ½ MIP, on chip zero suppression

Low Power: (25µW/ch) power pulsing



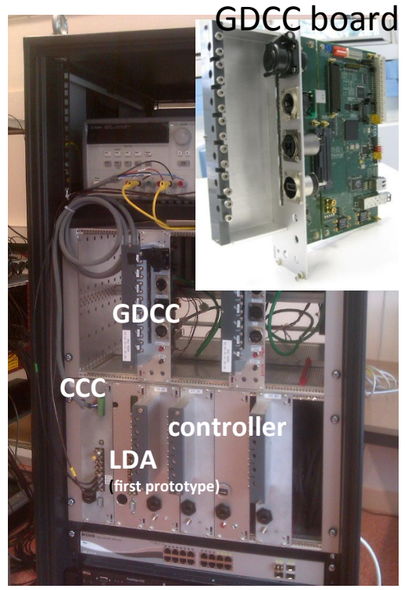
Since 2016:
SKIROC2a

Readout system and DAQ for beam tests

Standard: Giga-ethernet, 8b10b encoded local link, diff. pairs lvds signals over HDMI

Scalable: architecture of a computing network w/o routing, modular software configured using XML, scripted using python.

Compact: one cable for slow control, data acquisition, fast signals and possibly power



PCB R&D

Two options:

BGA packaged chips

Solution for technological prototype

test of chips before soldering ;

Space for external decoupling capacitors

Symmetric stacking will improve flatness,

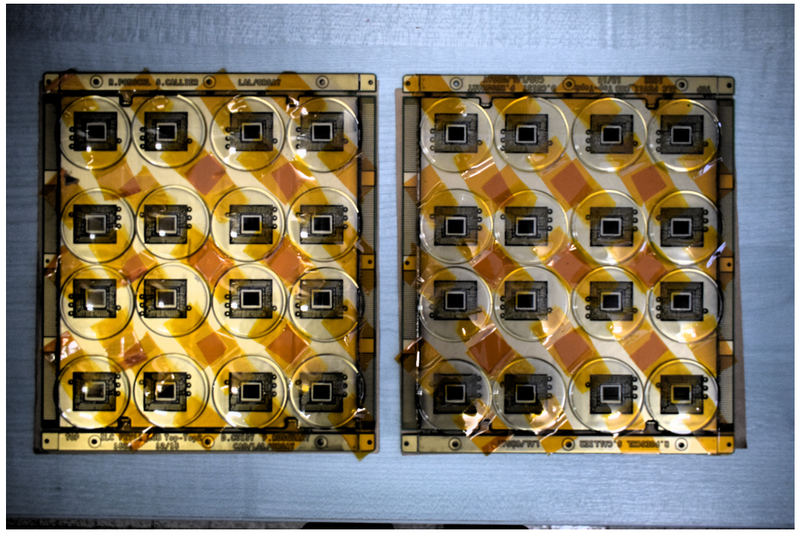
good for wafer gluing

Optimal shielding of signal traces

Test beams with FEV11, FEV12 and FEV13

since 2015

PCB with naked die

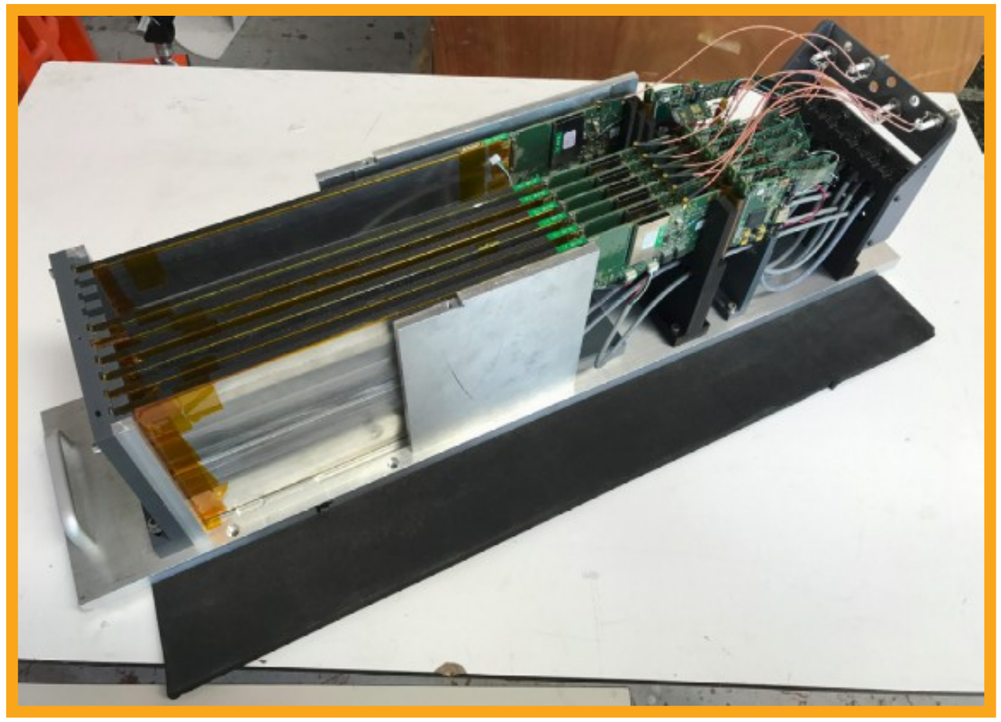


- Thin board (~1.2mm)
=> maximal channel density

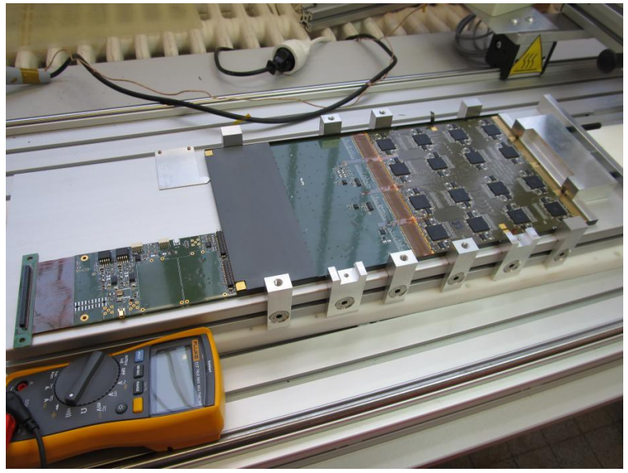
- Tests since 2015
=> Intensive test programme
e.g. Noise and cross talk

- Cosmics since 2018 (see backup)
- Beam test Summer 2019

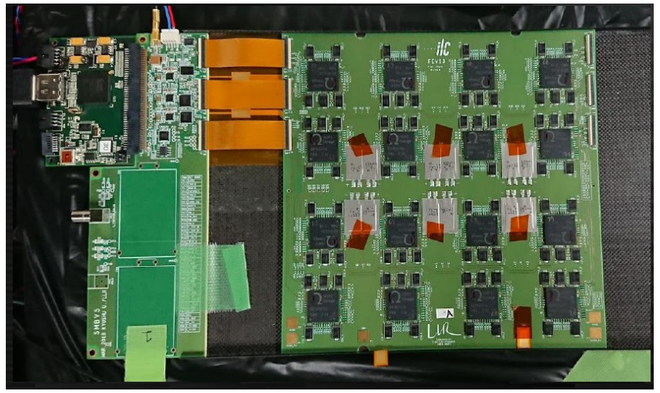
PCBs in beam test



Detector assembly using dedicated assembly chain in Paris region and at Kyushu University

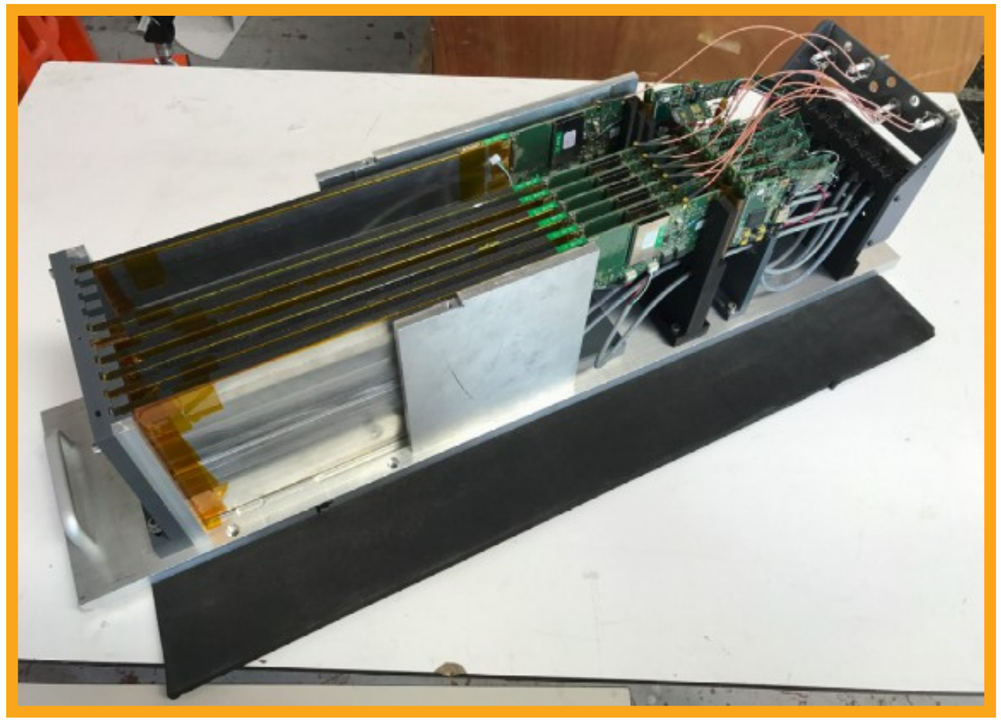


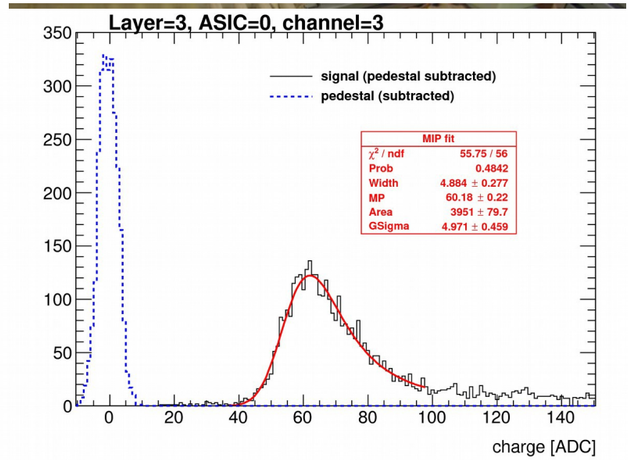
FEV12
With long adapter card



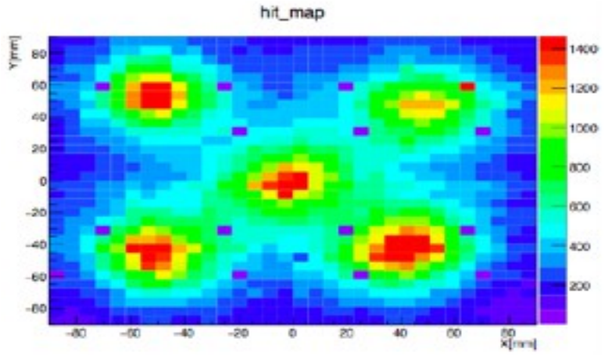
FEV13
With small adapter card

Validation of ASUs





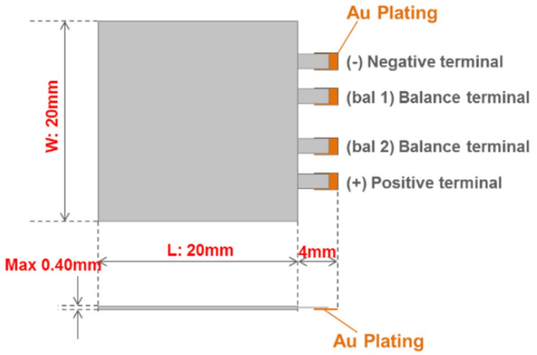
FEV12
With long adapter card

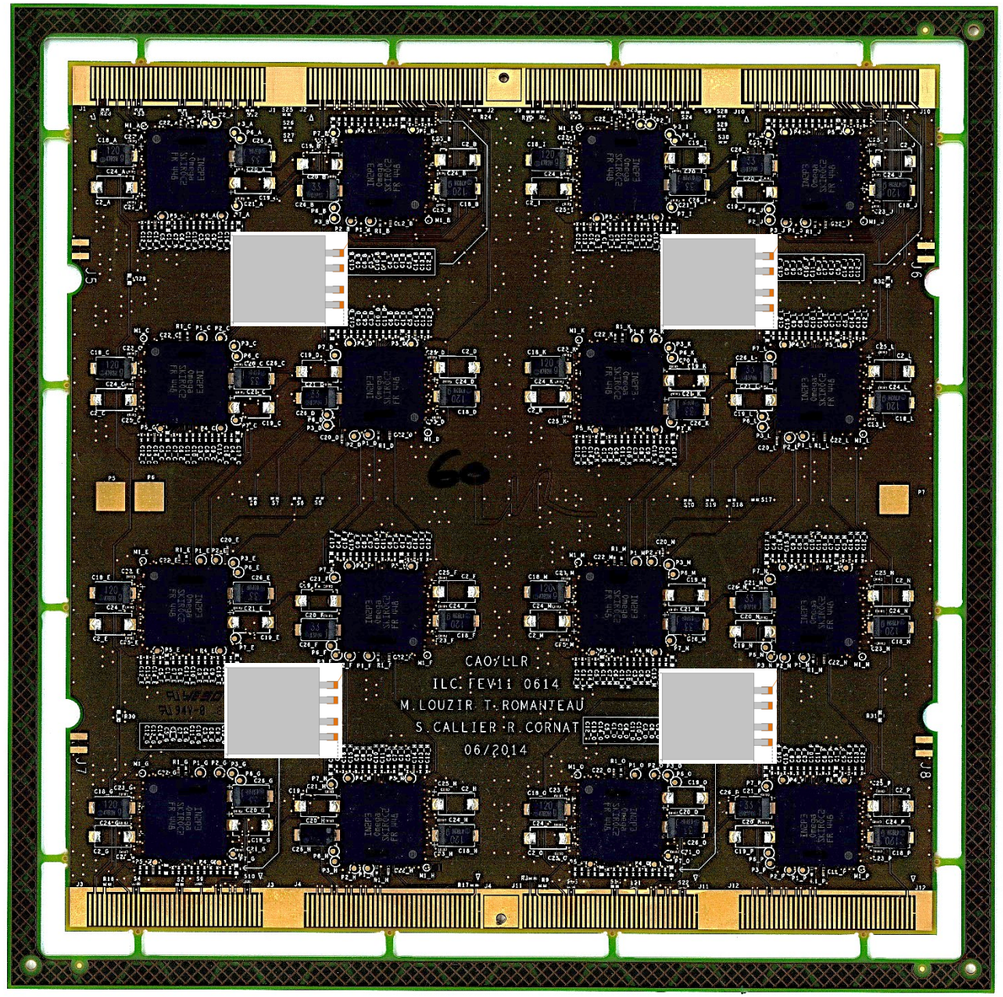


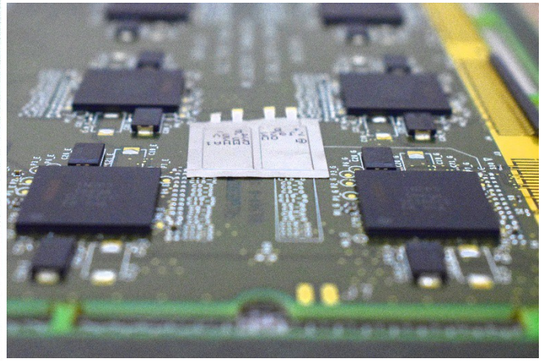
FEV13
With small adapter card

PP – Power stored on chip

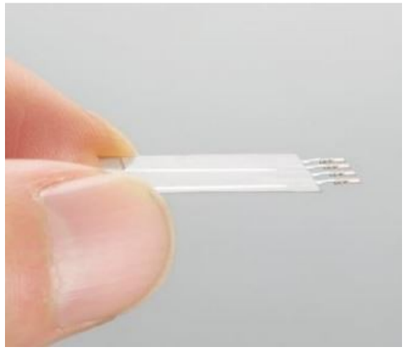
Ultra-Thin Supercapacitor
DMH series
DMHA14R5V353M4ATA0
35 mF / 4.5 V







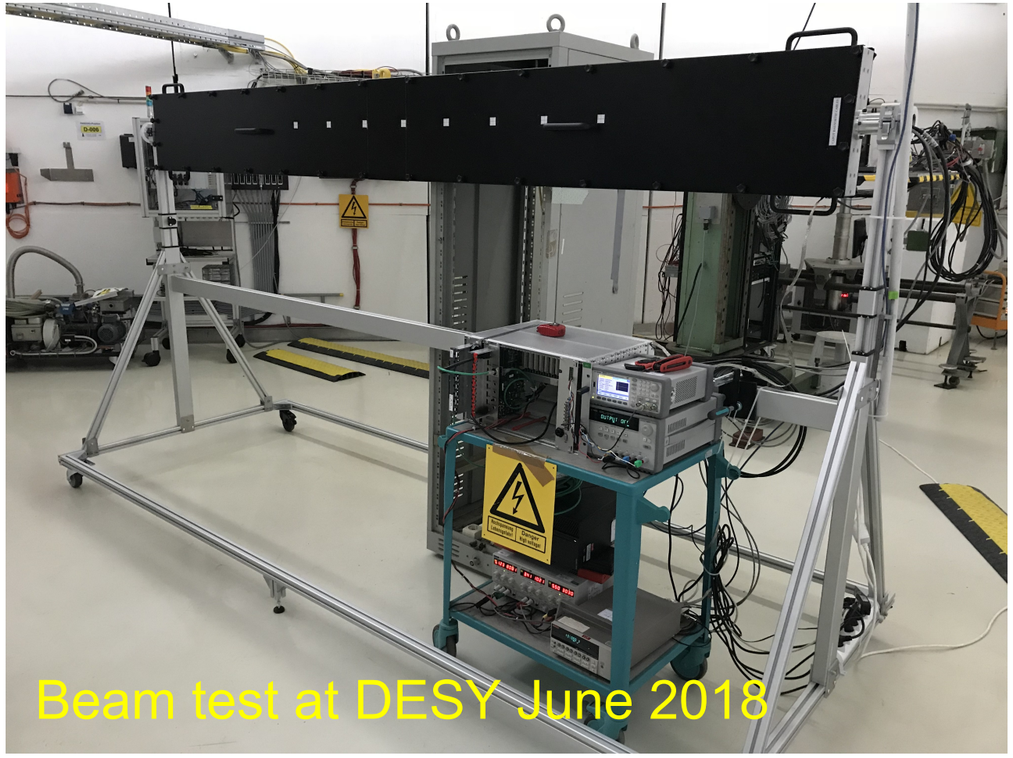
Integrated capacitors permit **the peak current of ~1.5A <u>to be local</u>** during power pulsing => recharge is limited to a total of ~150mA …

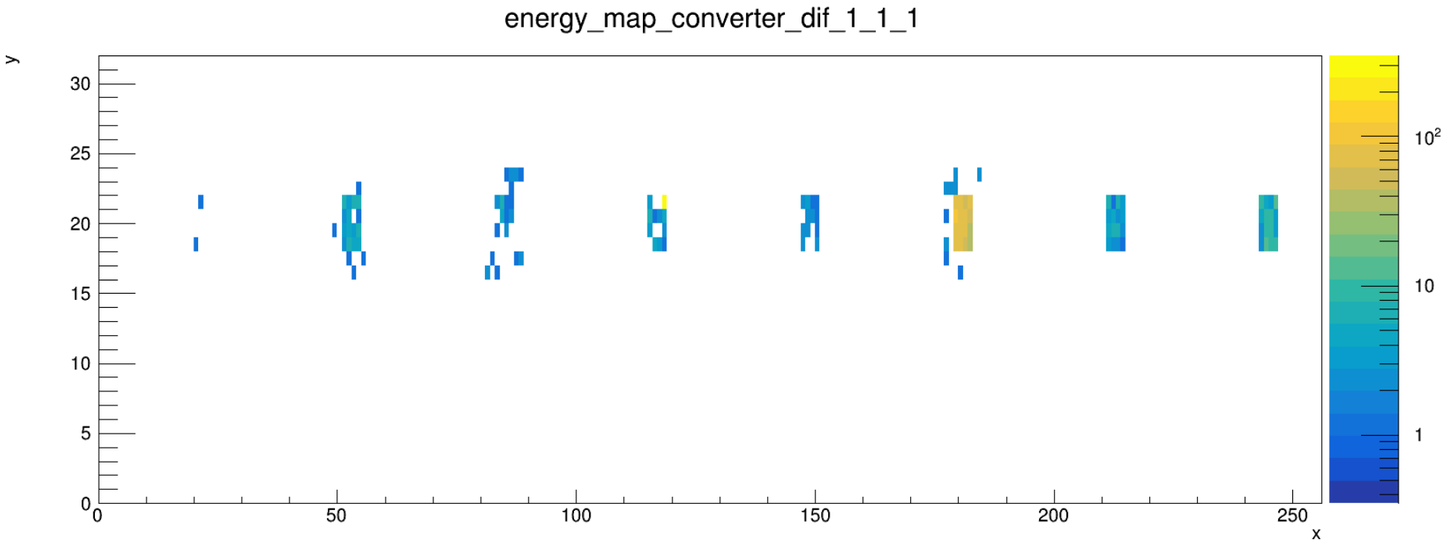


Life time has to be checked, depends on voltage and temperature…

Electrical long slab in beam test

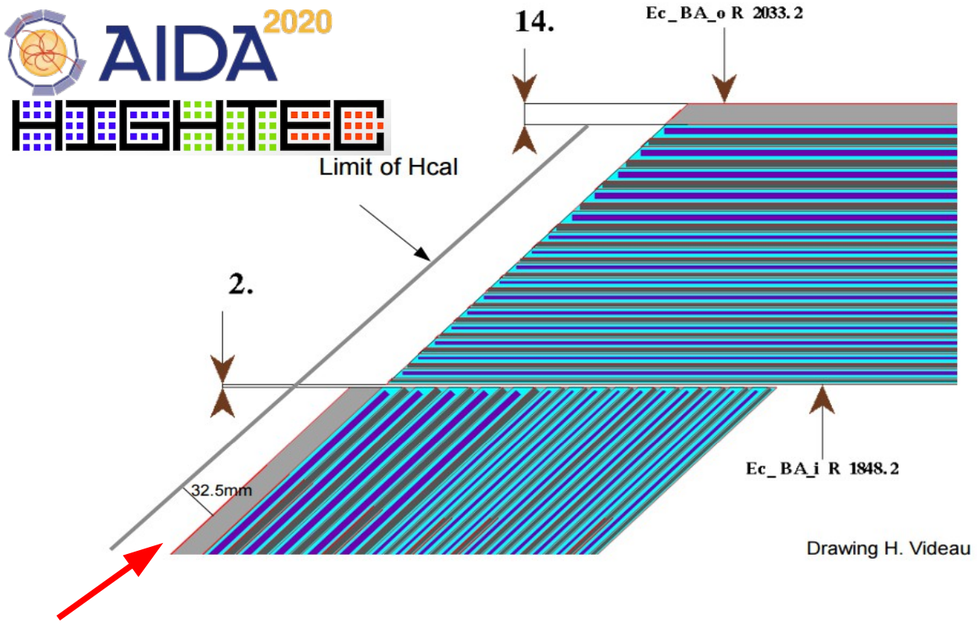
Chain of
8 detection elements
~3m



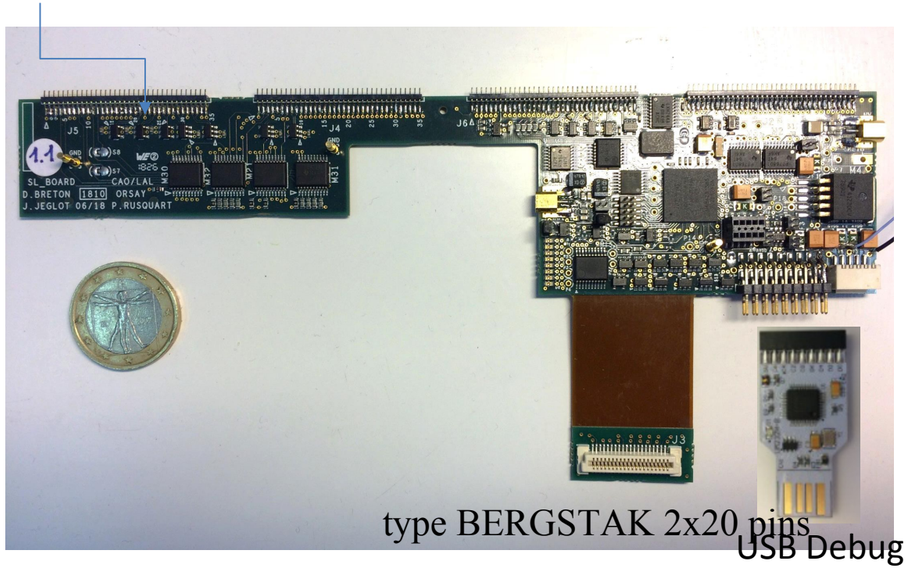


- Very encouraging results
- Credibility for concept as foreseen for e.g. ILD
  - Analysis ongoing
- Issues with signal drop towards extremities about to be remain to be understood

Digital electronics – Getting fit for ILD

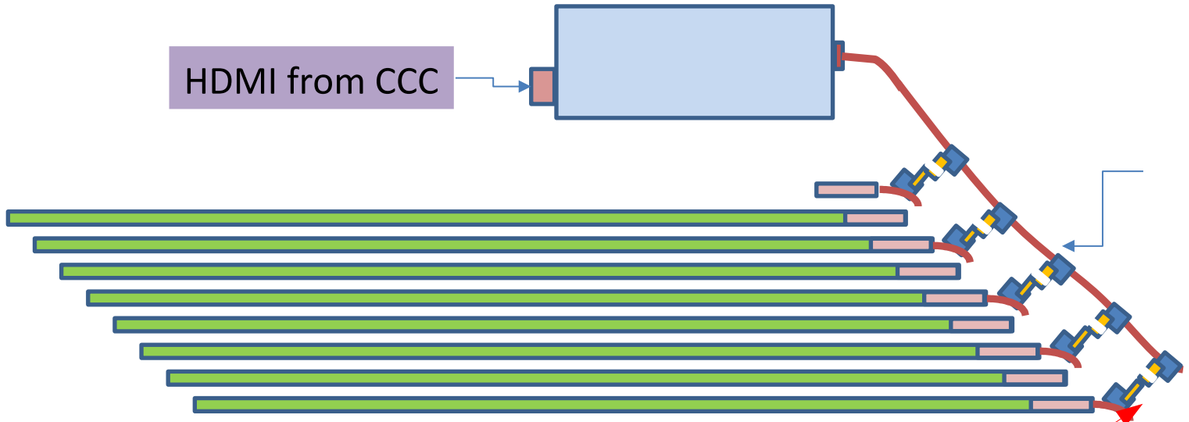


Approximately 6cm between Ecal and Hcal

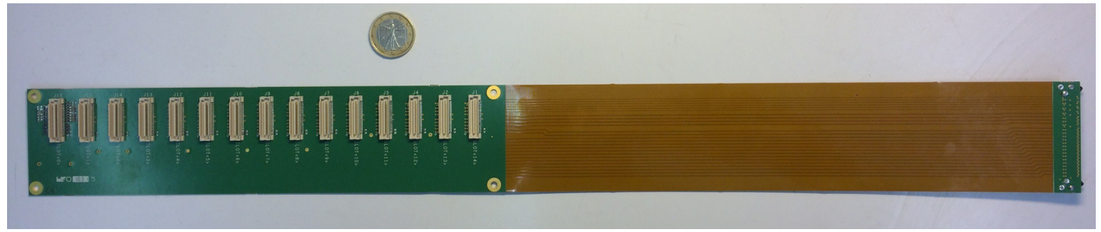


SL Board at the end of layer

CORE Kapton – replaces bulky HDMI cables



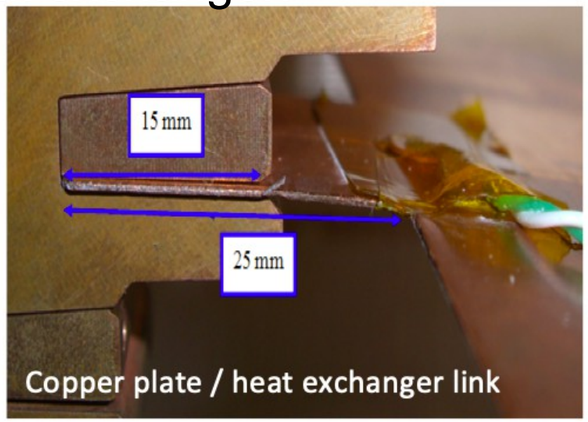
Guiding/receiving signals to/from slabs



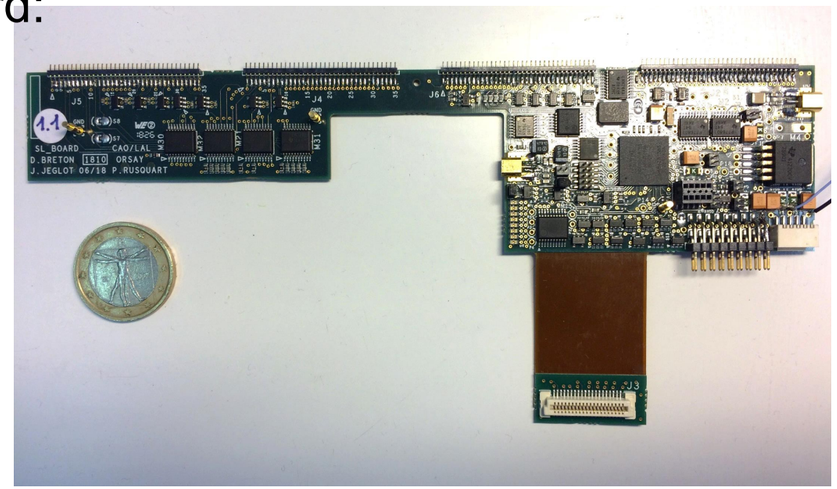
- Hardware exists:
- Firmware for communication with ASICs about to be written
- Expect first conclusive results for Summer 2019

SiEcal - “Local Integration – End of layers” I

Heat exchanger:



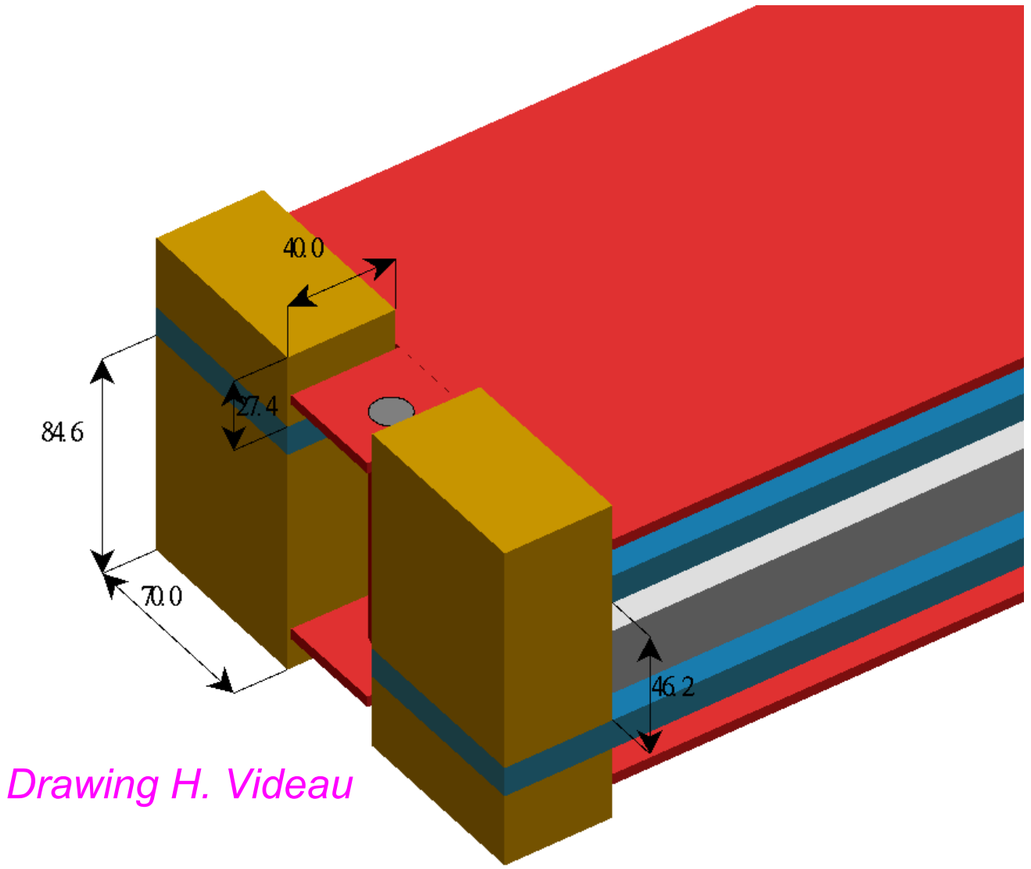
SL-Board:



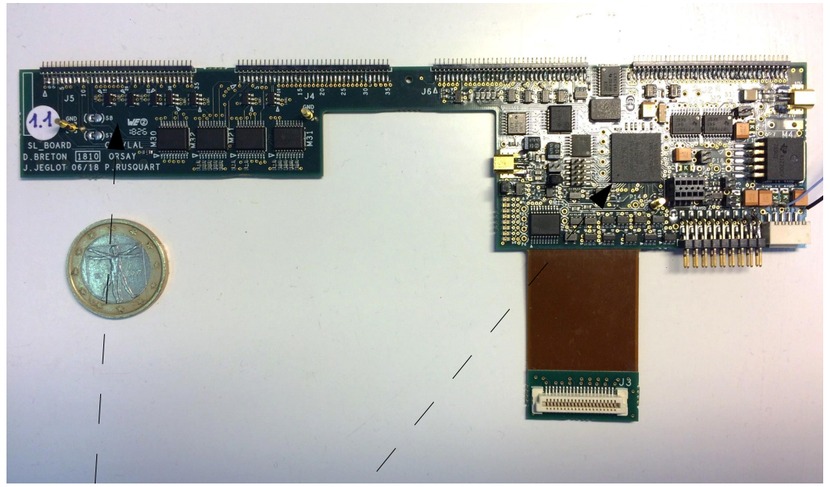
- Need to bring the individual pieces together

- A first meeting between developers of Cooling system and developers of SL-Card revealed no showstopper on integration

SiEcal - “Local Integration – End of layers” II

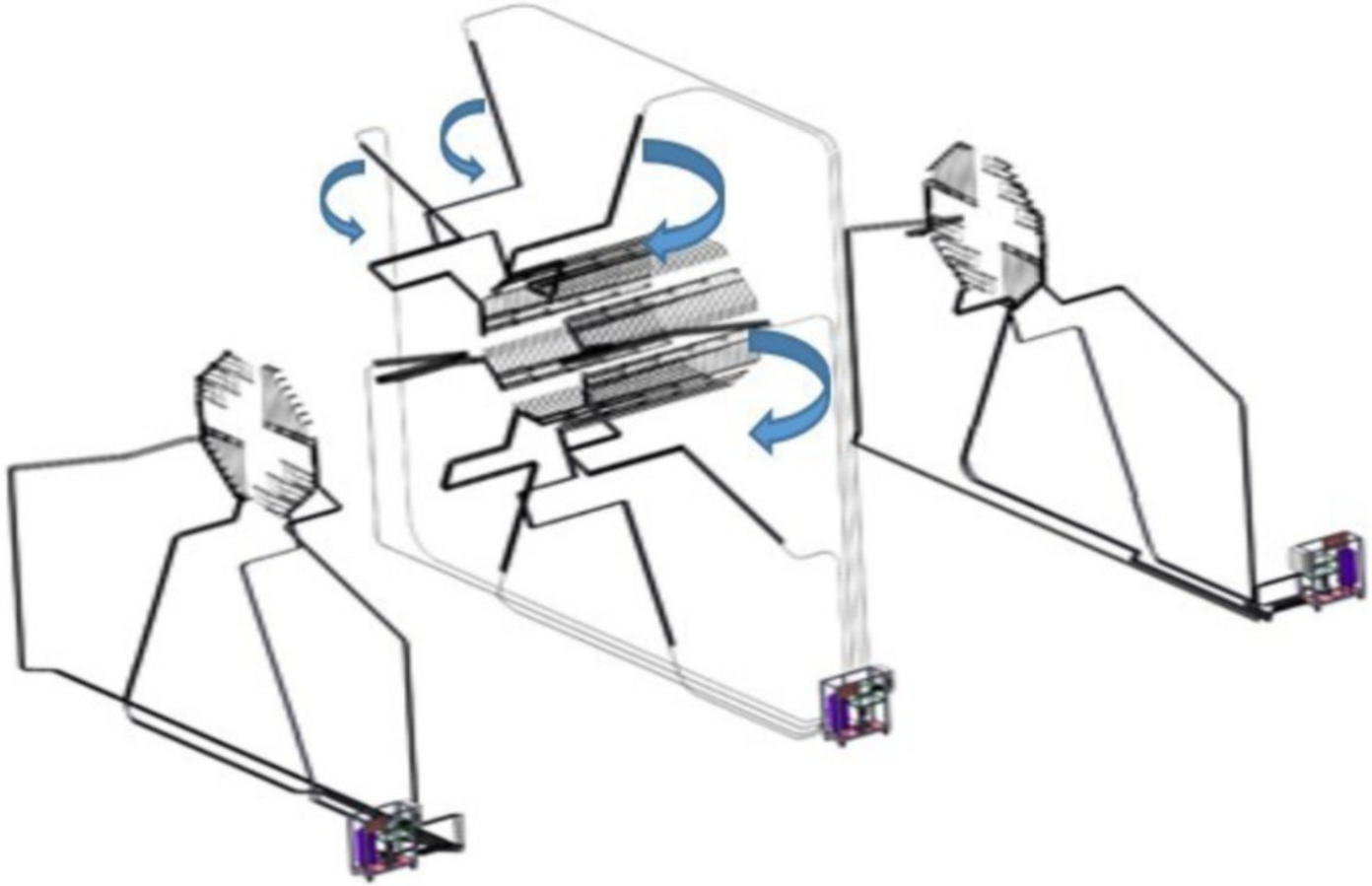


Drawing H. Videau



- Height available for components on Readout board ~46.2mm/2 (space between 2 PCBs
  - Details depend on arrangement
- Components have to be oriented “towards W plates”

SiEcal – Routing of services

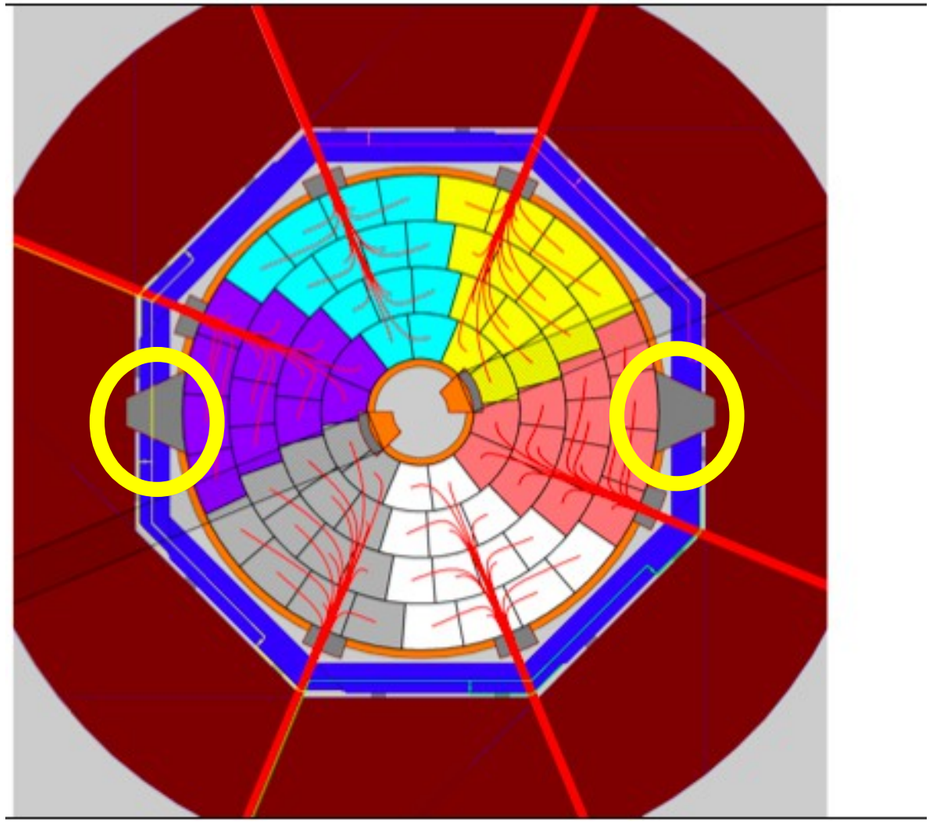


D. Grondin, J. Giraud, LPSC

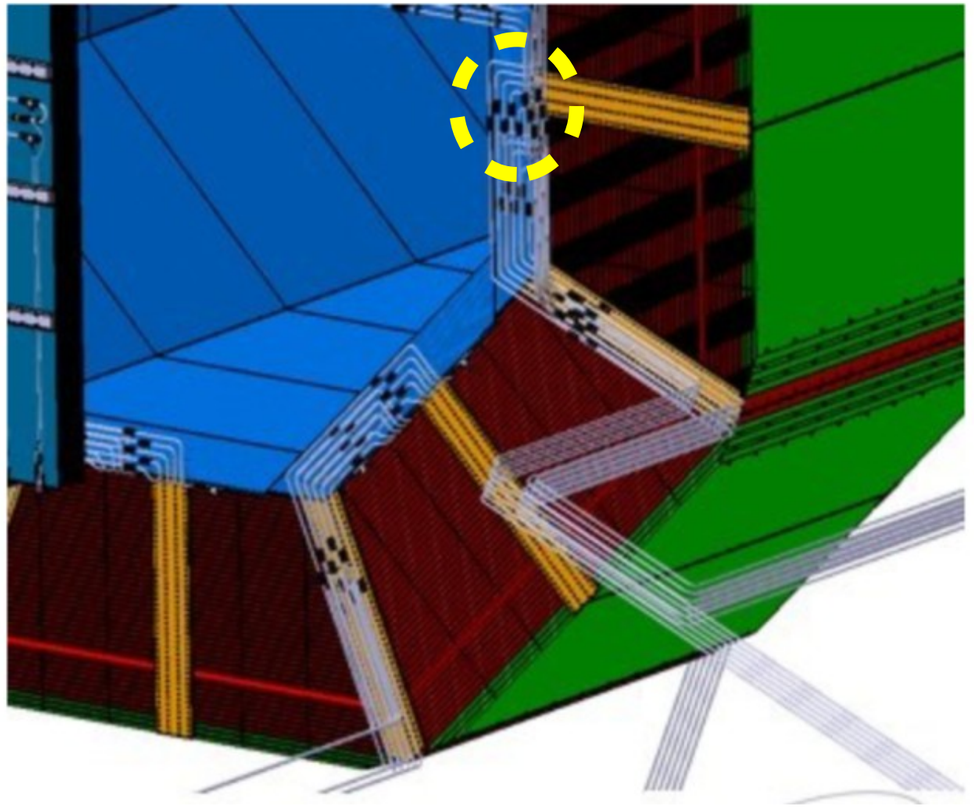
Design principle:

- Cooling (shown here) on one end of barrel
- Cables for electrical services and data transfer on the other end of barrel

SiEcal – Cooling system and TPC fixation



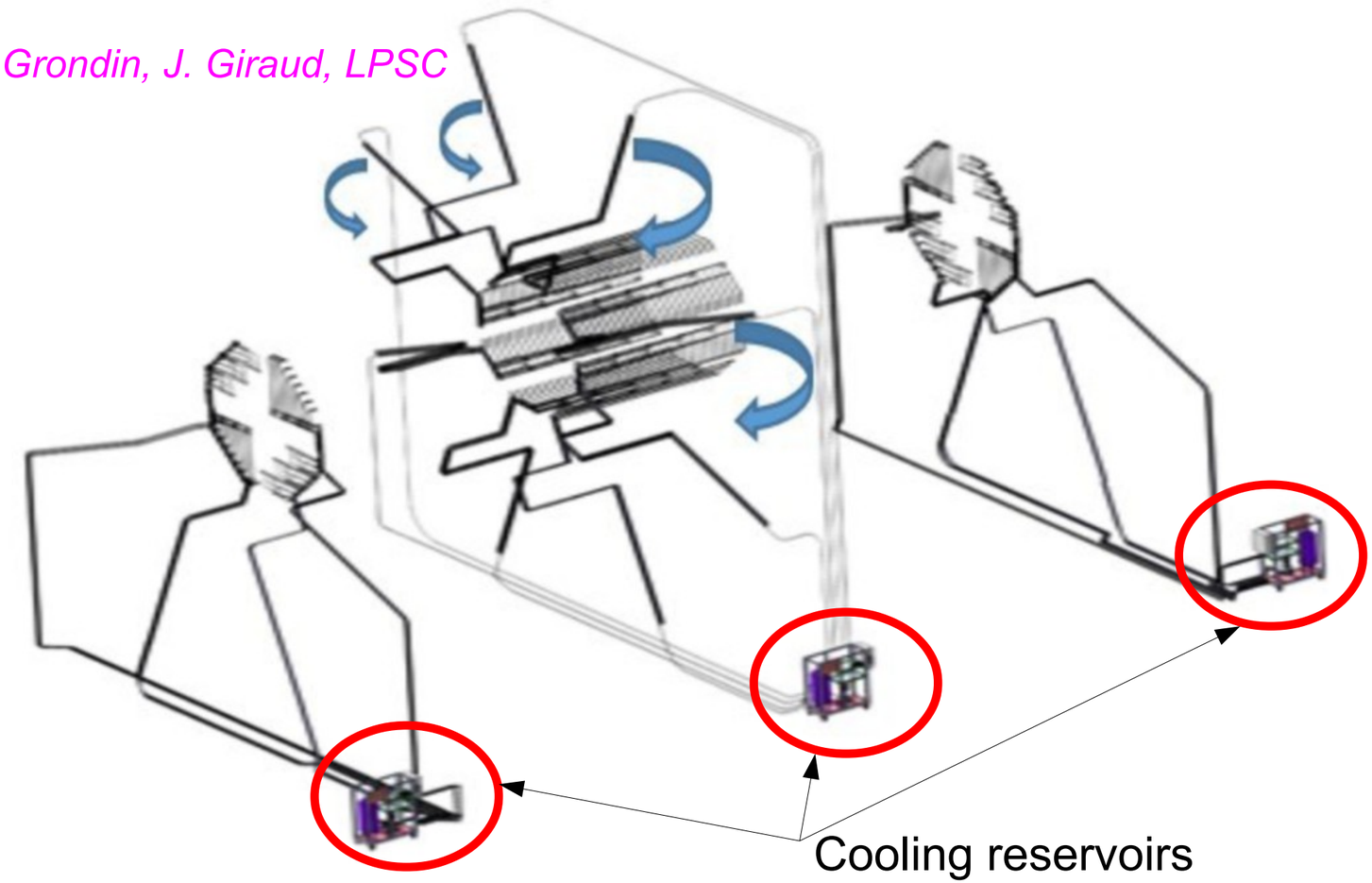
Drawing H. Videau
Presented at LCTPC Meeting(?)

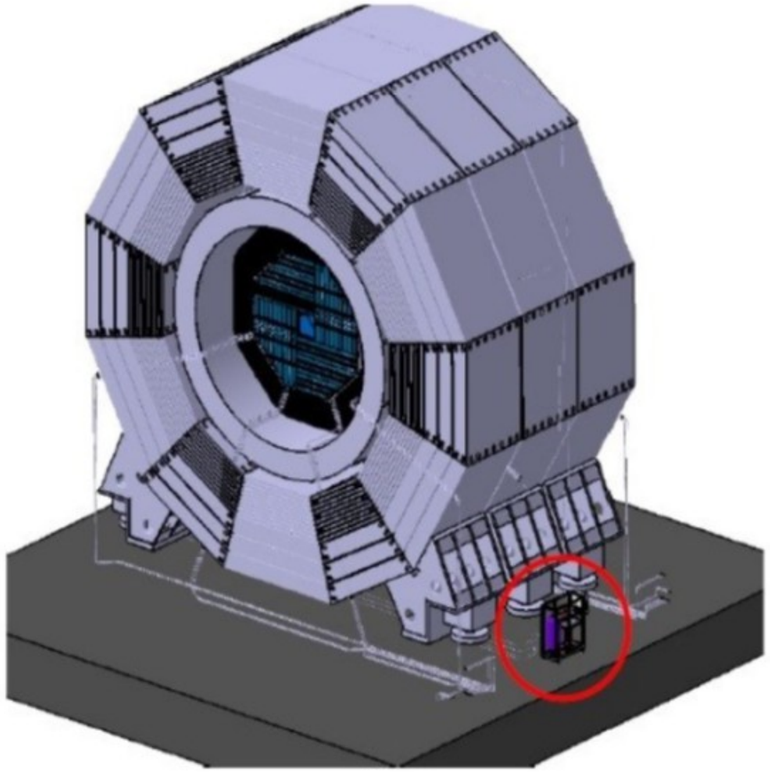


- TPC fixation at “3h” and “9h” in conflict with routing of cooling system
- SiEcal prefers fixation at “4h” and “8h” (or another solution)

SiEcal – Cooling system in detector hall

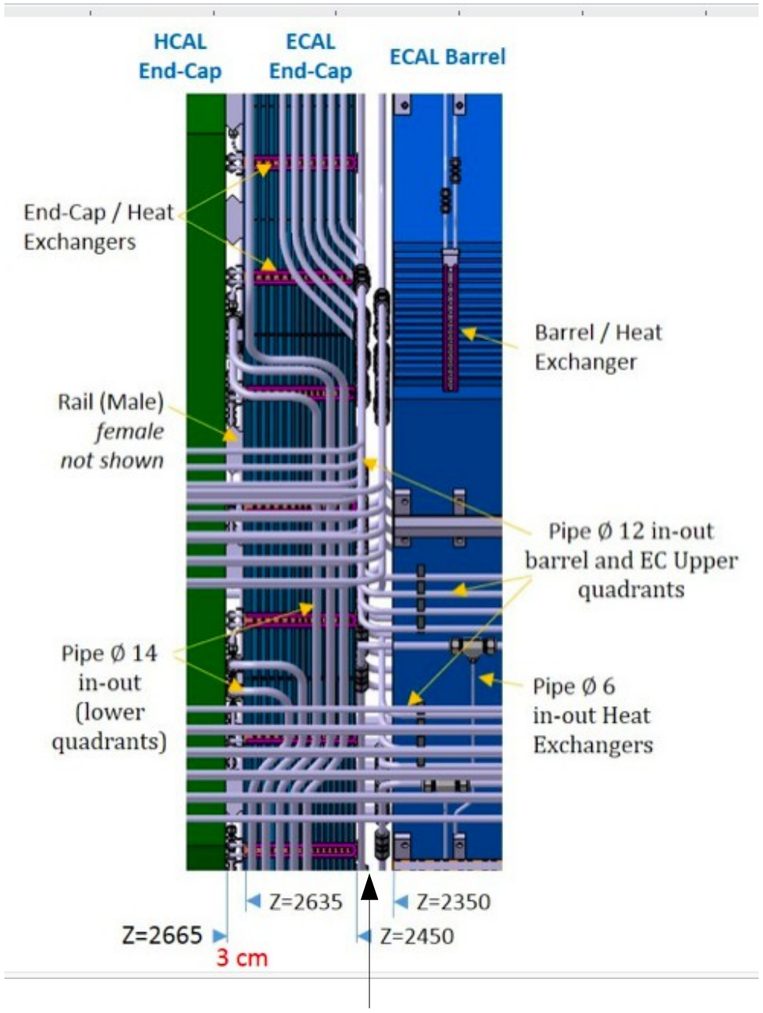
D. Grondin, J. Giraud, LPSC



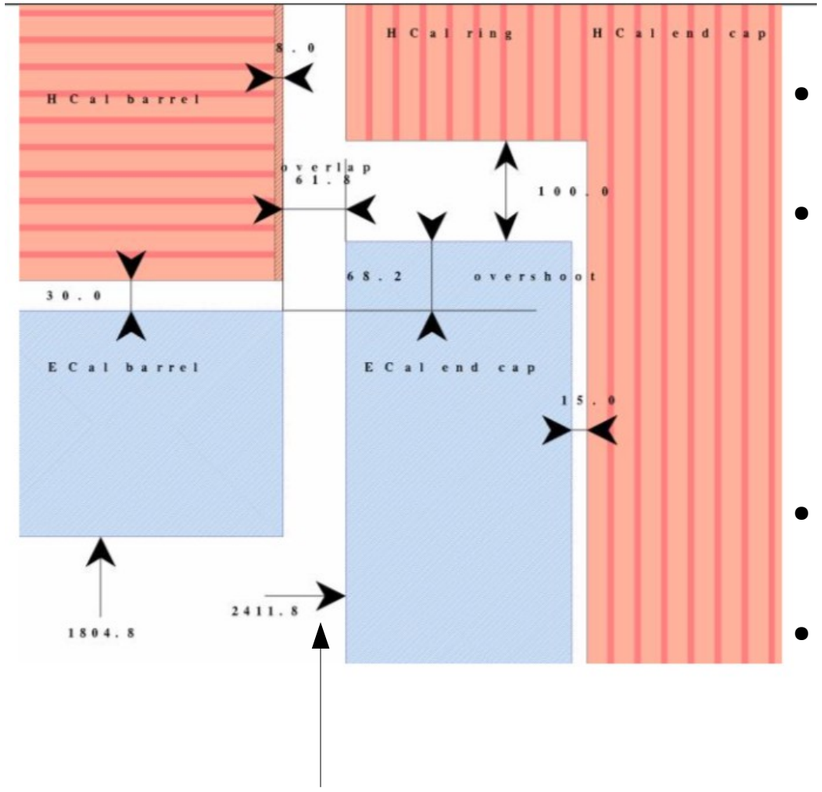


- Cooling reservoir has to be placed at a given height according to leakless design
- Preferable position is on platform, if not at corresponding place in service gallery
  - However, cooling pipes should also remain as short as possible to avoid friction losses
  - Current R&D (see above) supposes placement on platform

SiEcal – Cooling system and Hcal ring



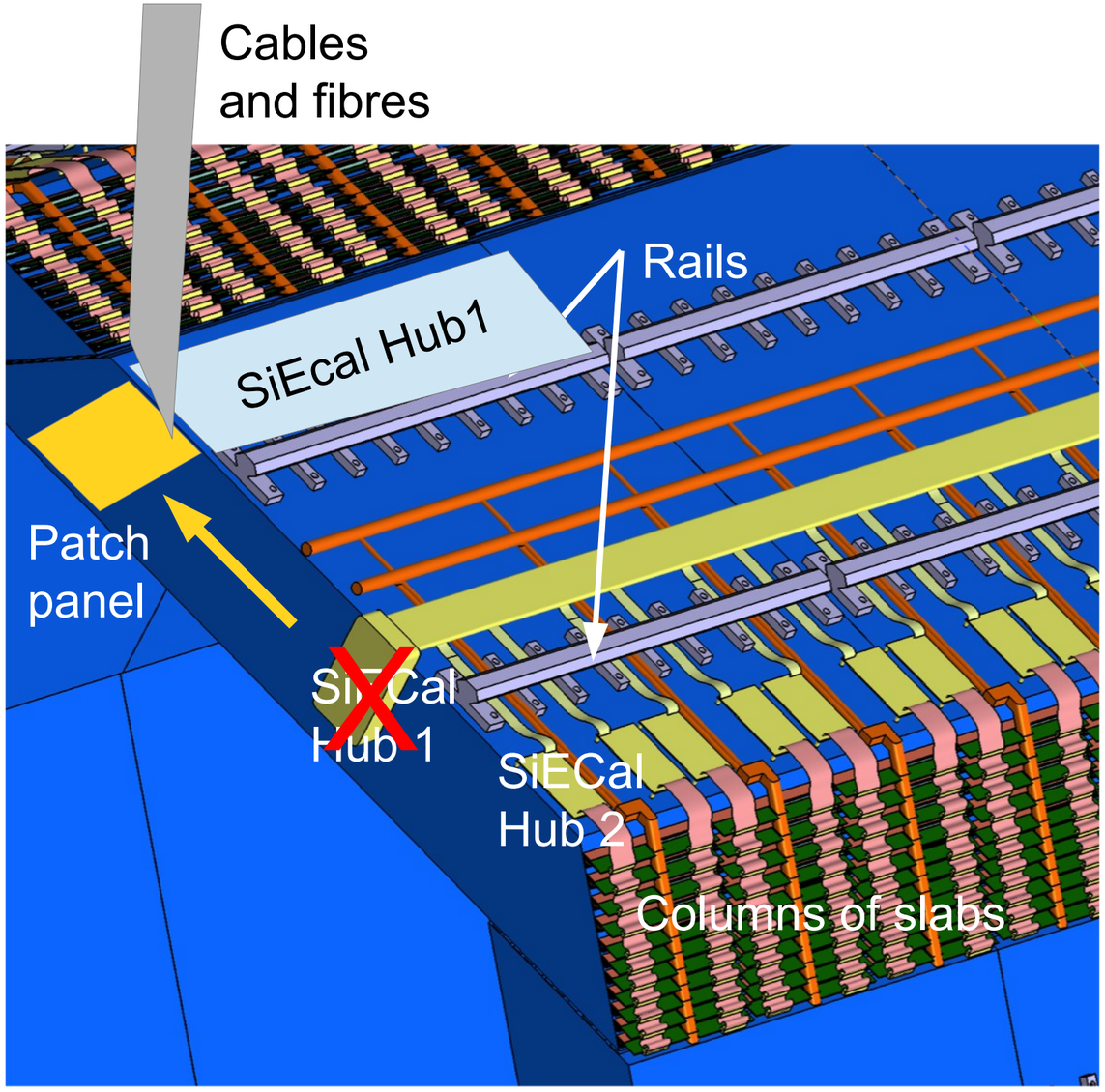
100mm



62.8mm

- So far cooling system has been designed for 100mm between barrel and end cap (i.e. DBD design)
- IDR (large model) foresees only 62.8mm
- Dedicated discussion on 4/2/19 lead to the conclusion that cooling pipes could be accommodated within 62.8mm
- However, circuit-points are rather bulky
- Would prefer to maintain 100mm between Hcal barrel and Hcal ring
- At the expense to remove one layer from Hcal ring
- In general endcaps require many further careful looks

SiEcal Integration Barrel – Between Ecal and Hcal



- Cables will arrive at specific place at alveolar structure
  - Simple patch panel
  - Being close to Hub1
  - Avoid conflict with TPC fixation (see below and tomorrow)

- Note introduction of Hub1 between Ecal and Hcal
  - Potential heat source ~10W/hub
  - 5 hubs in total => 50 W/stave
  - => 400 W In barrel

- Reminder Hub2:
- 10x5 Hub2/stave each consuming 3-5 W
- => ~250 W per stave
- => 2kW for barrel

Summary and conclusion

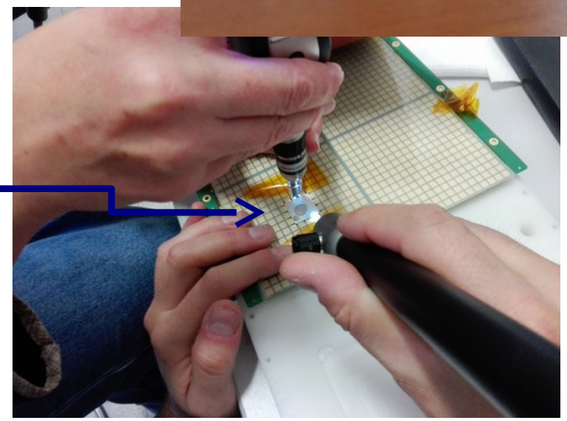
- R&D for SiEcal addresses all elements relevant for an installation into the ILD detector
- Current effort concentrates on space reduction of individual components (i.e. Digital r/o)
- Alltogether we believe that we can build the SiEcal largely as designed
- Design of SiEcal puts several constraints on other detectors
- 5 Hubs of type Hub1/stave between Ecal and Hcal may constitute a heat source (~10 W each)
  - Should not forget the 50 Hub2/stave with ~3-5 W consommation each
- Need a decision on how TPC will be fixed
- Need a decision whether we will be allowed to stay on the platform
  - If not need to find space at corresponding height in service gallery
- Update of ICD in progress

Backup

SiEcal – News from COB

- **LAL/OMEGA collaboration with Corean Group of SKKU (EOS company for the PCB)**
  - FEV11_COB: **10 boards of 1.2mm**, good planarity and good electrical response.
  - SK2a wirebonded at CERN (Study by LPNHE and P2IO Platform CAPTINNOV)

- **Successful debugging w/o sensors:**
  - (~4% of noisy channels, good response to injected signals)



Visual inspection of the result of the gluing

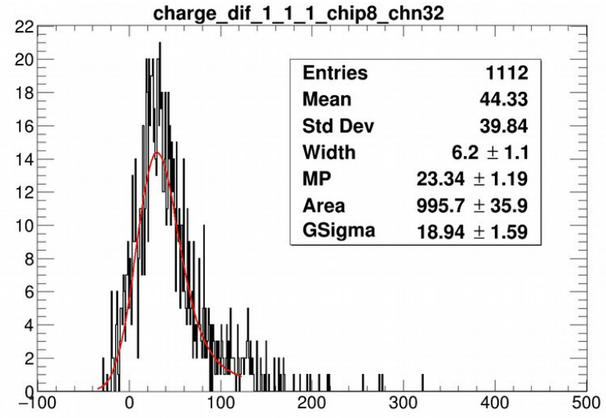
- **Debugging with sensors (baby wafers 3x3 px)**
  - The system was not ready for test at DESY@2018.
  - New wafer testbench setup in LAL borrowed from LPNHE.
  - Duplication ongoing at LAL (using the CAPTINOV platform)

- ● 3 baby wafers characterized, glued and tested with cosmics. Test with radioactive sources are in preparation.

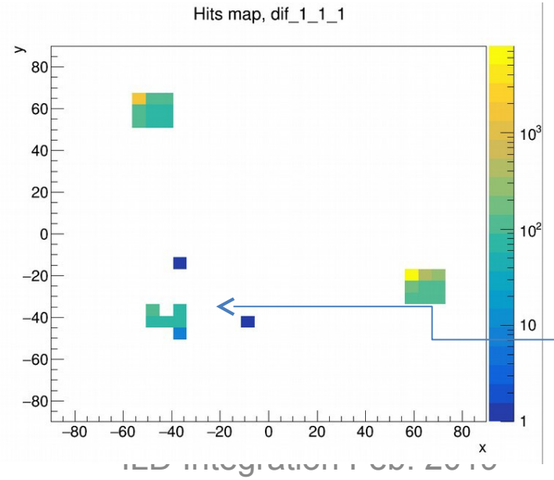
A. Example of MIP spectrum from cosmic rays.

B. 3.6pF

Plot from V. Lohezic



A. Example of MIP spectrum from cosmic rays.



A. Hit map with for cosmic runs.

B. (different mapping to BGA versions)

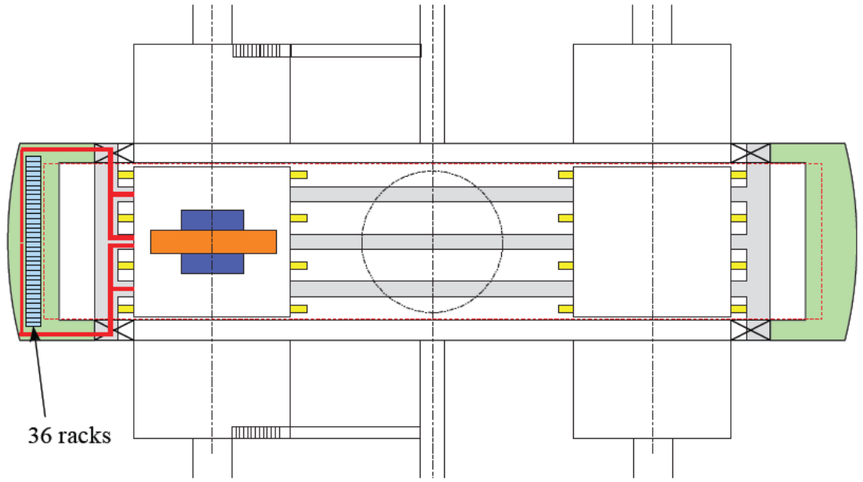
C. Baby wafer tested in DESY. Some glue is spilled.

Reminder on service infrastructure

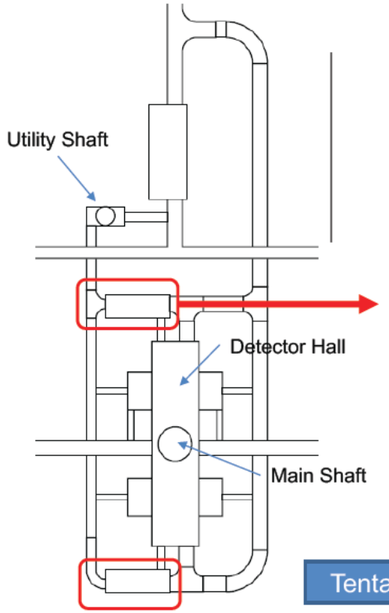
Detector Utilities in Underground Areas

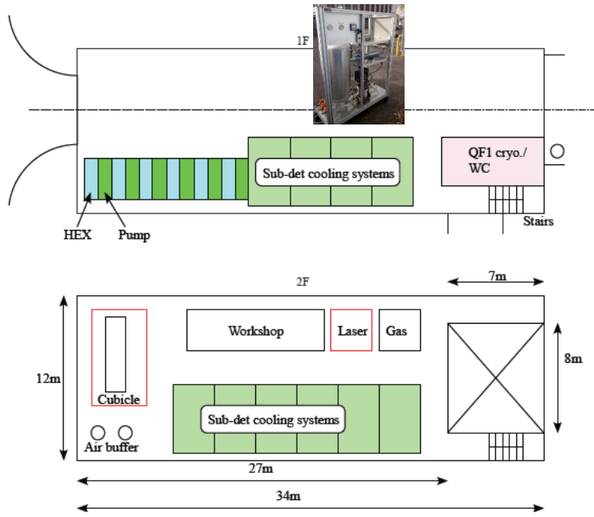
Service gallery

- 3F-5F



Utility/service cavern





Tentative design

Y. Sugimoto

Karsten Buesser - ILD Meeting - 21.02.2018 28