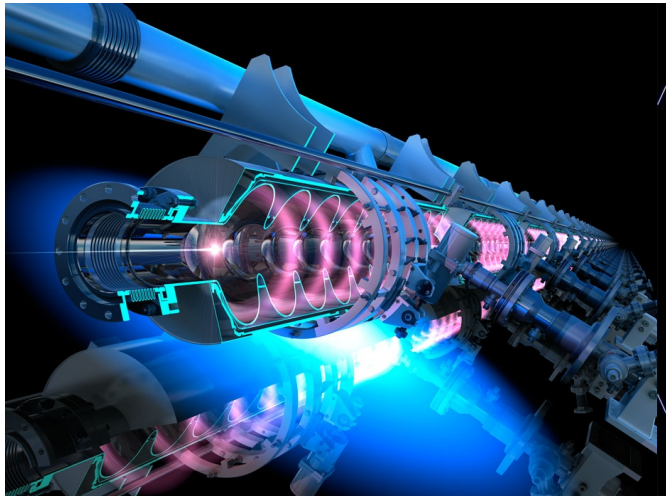
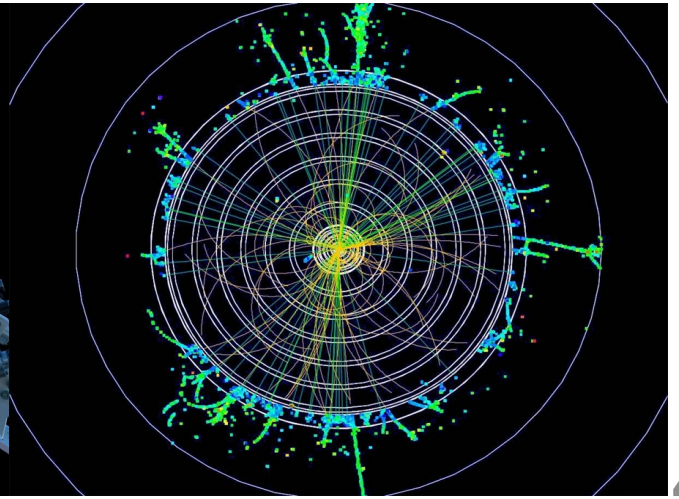
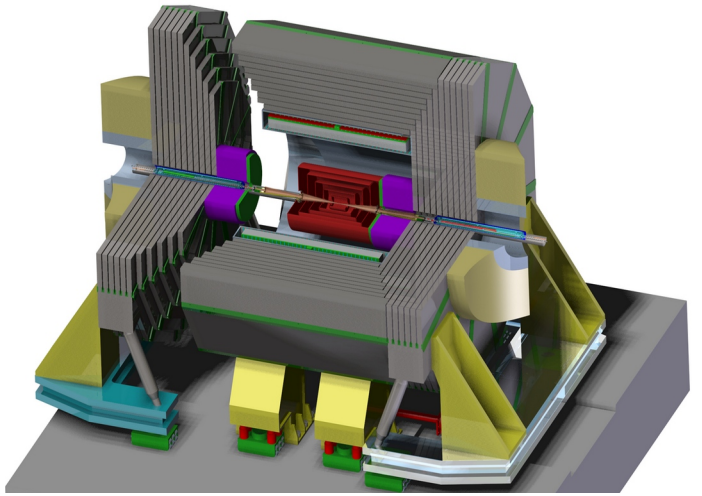
SiD

Plans for the IDT phase

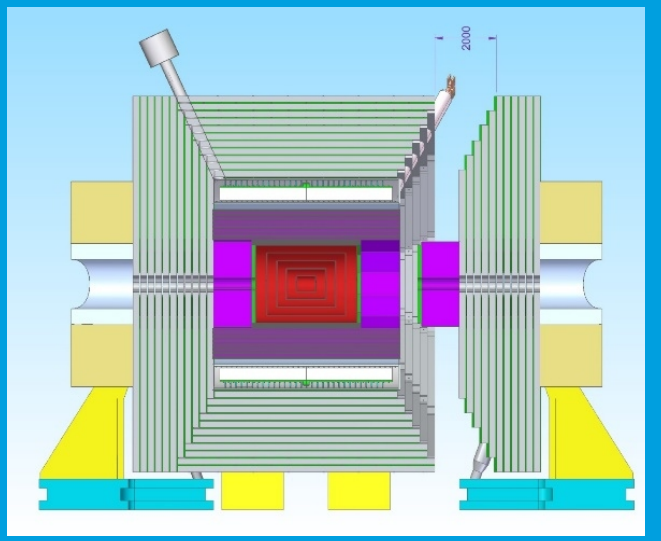




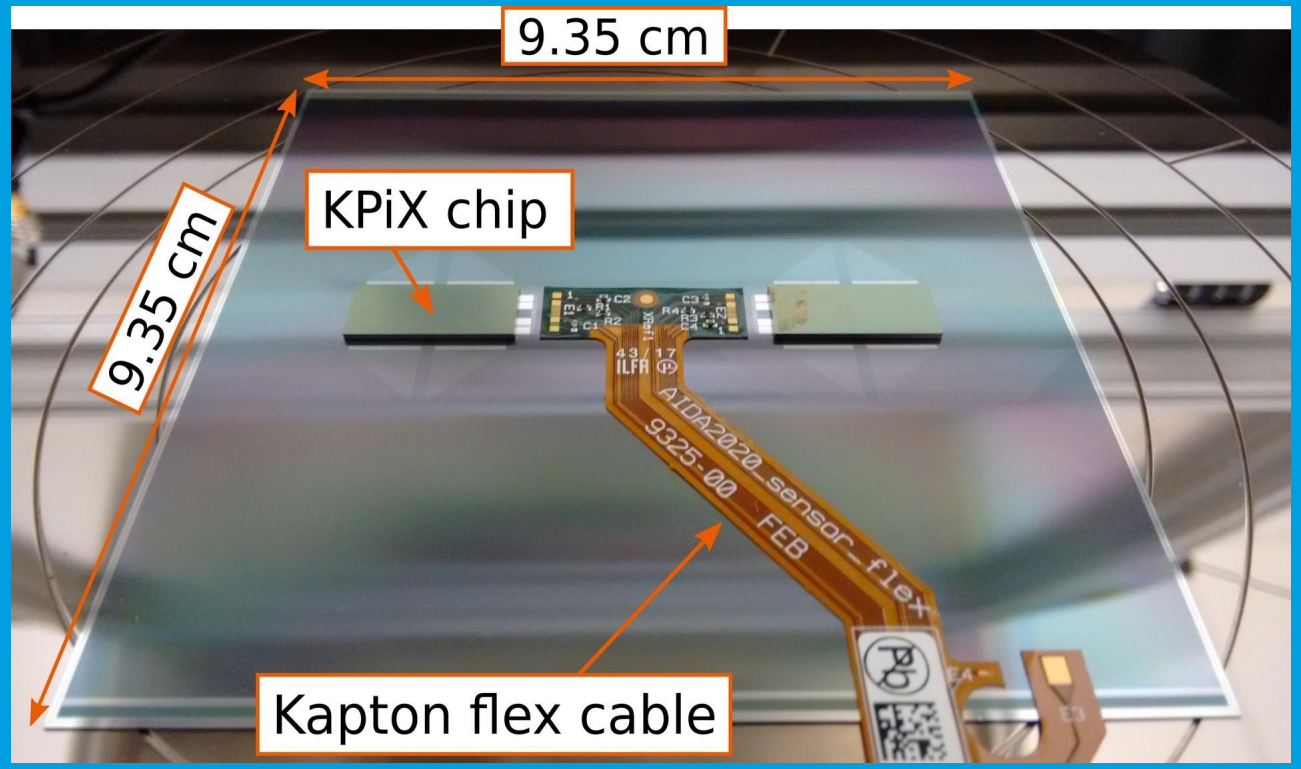
Marcel Stanitzki
16/04/2021

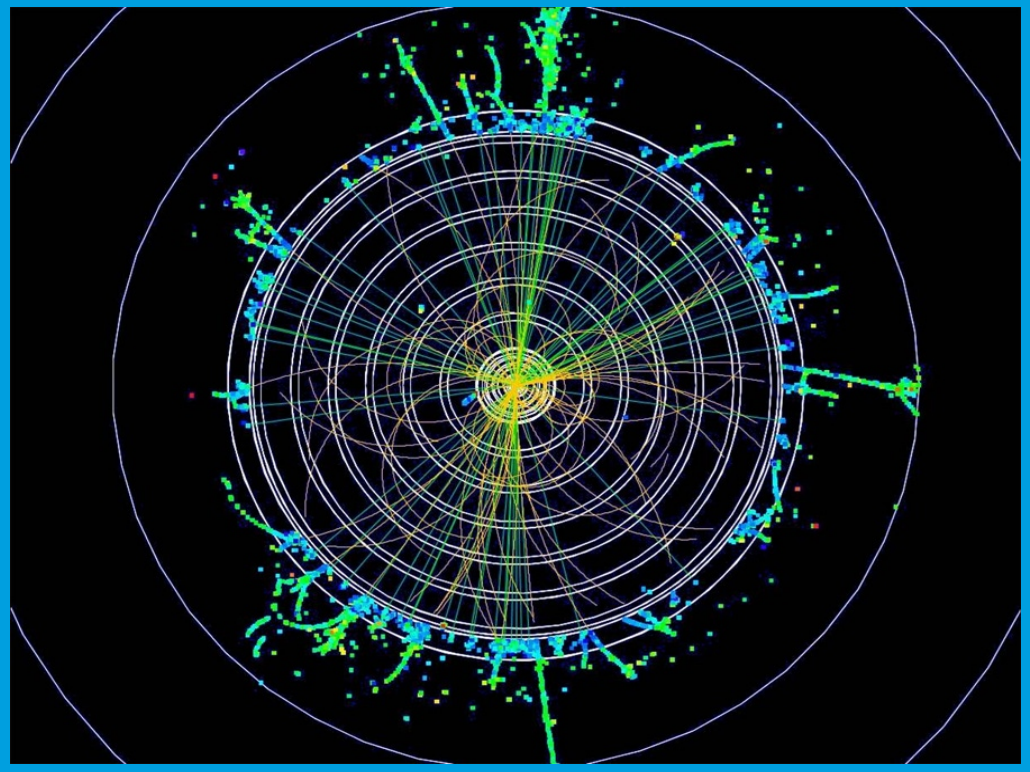
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

SiD Status

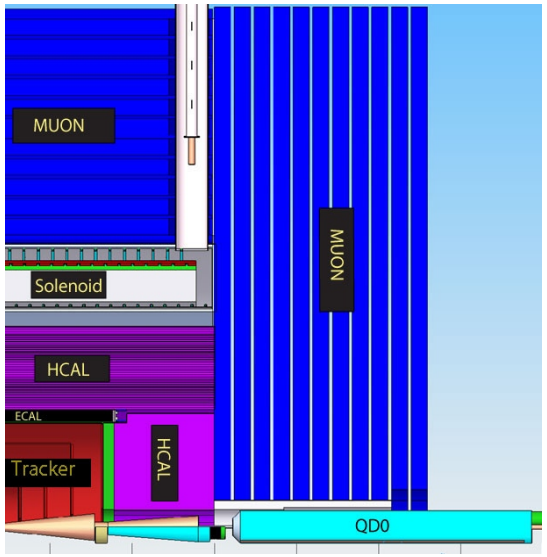



9.35 cm
9.35 cm
KPiX chip
Kapton flex cable
AIDA2020_sensor_flex
9325-00 FEB



SiD – Compact Silicon Detector

The "Post-DBD" Configuration



- Compact high-field design
- All-Silicon tracking
- B Field 5 T, r_{ECAL}=1.25 m
- Robustness against backgrounds
- Integrated Design
- Designed for PFA

SiD BARREL	Technology	Inner radius	Outer radius		z max
Vertex detector	Silicon pixels	1.4	6.0	±	6.25
Tracker	Silicon strips	21.7	122.1	±	152.2
ECAL	Silicon pixels-W	126.5	140.9	±	176.5
HCAL	Scintillator-Steel	141.7	249.3	±	301.8
Solenoid	5 Tesla	259.1	339.2	±	298.3
Flux return	Scintillator/steel	340.2	604.2	±	303.3

SiD ENDCAP	Technology	Inner z	Outer z	Outer radius
Vertex detector	Silicon pixels	7.3	83.4	16.6
Tracker	Silicon strips	77.0	164.3	125.5
ECAL	Silicon pixel-W	165.7	180.0	125.0
HCAL	Scintillator-Steel	180.5	302.8	140.2
Flux return	Scintillator/steel	303.3	567.3	604.2
LumiCal	Silicon-W	155.7	170.0	20.0
BeamCal	Semiconductor-W	277.5	300.7	13.5

SiD – A bit of history

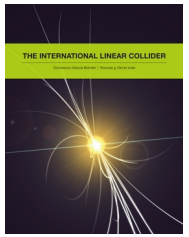
How SiD came into being

2003:SiD first appears at ALCPG.
SiD is aimed at the NLC

2006: Detector Outline Document

2009: SiD Letter Of Intent

2013:
ILC TDR/DBD



2008/9: CLIC_SiD Starts for Multi-TeV machines

2009: SiD validated

2017: ILC Re-baselining To 250 GeV

2004 :WWS starts the detector concept studies at the Victoria meeting :SiD, GLD, LDC Beginning of the Silicon Detector Concept Study

2007: Detector Concept Report
First SiD workshop

2011: CLIC Physics and Detectors Conceptual Design Report

2014: Site studies

202X: Japanese Decision

Concept Phase

LoI Phase

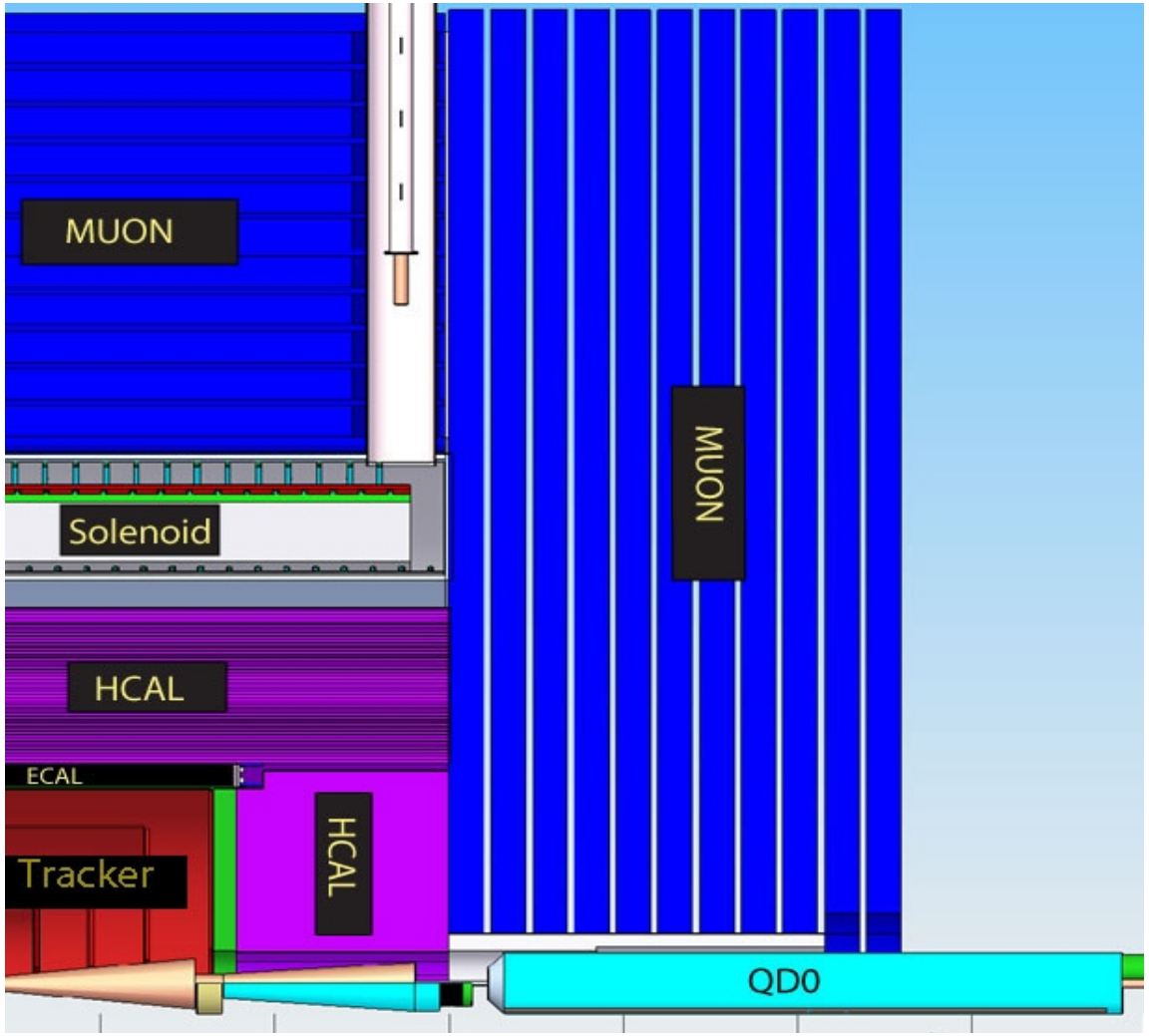
DBD Phase

Japanese Decision Phase

SiD – Baseline choices

Baseline Technologies

- The DBD was finalized **2012/13**
  - Tchnology has made huge progress since then
  - HL-LHC as technology driver
- Overall assessment
  - Basic concept of a compact all-silicon detector is sound
- Decisions already taken
  - Move from DHCAL (RPC-based) to SiPM-AHCAL
- Obvious to take advantage of new technology
- State of conceptual design studies
  - To take it further many studies will now require effort & engineering
- Assumption: IDT will lead to a pre-lab and to **construction**



Past Performance does not indicate future success ...

The ATLAS ITk Strip Tracker

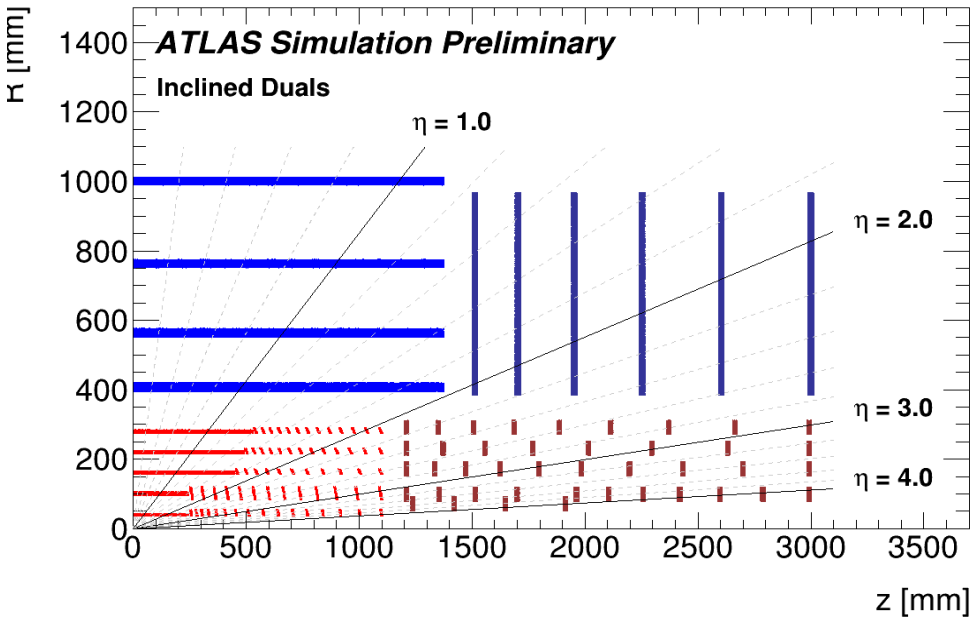
Short Overview

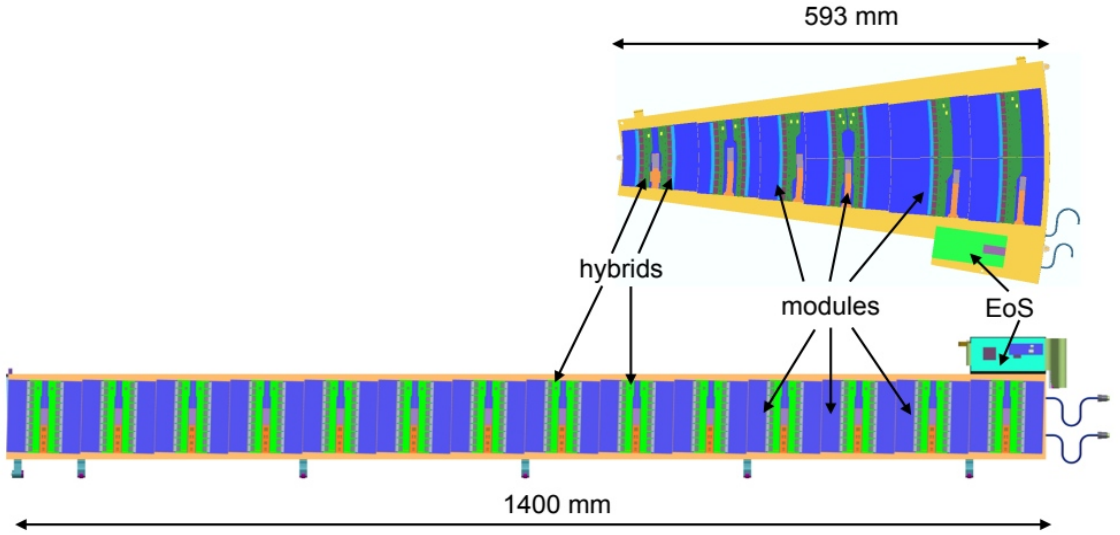
Status

- Currently entering pre-production, Installation in 2026

System Overview

- ITk – Inner Tracker for HL-LHC
  - Pixel System
  - Strip System 4 barrel layers + 6 endcap disks
- The ITk Strip in numbers
  - 50 million channels
  - 17888 modules
  - 776 staves and petals
  - ~166 m^2





The ATLAS ITk Strip Tracker

A short timeline

Pre-face

- All this was done in an existing and fully funded host-lab and an already established Collaboration
- The overall scope of the Phase II Upgrade is 270 MCHF CORE

R&D for HL-LHC (~2005-2012)

- No project, individual R&D efforts

Letter of Intent (Dec 2012)

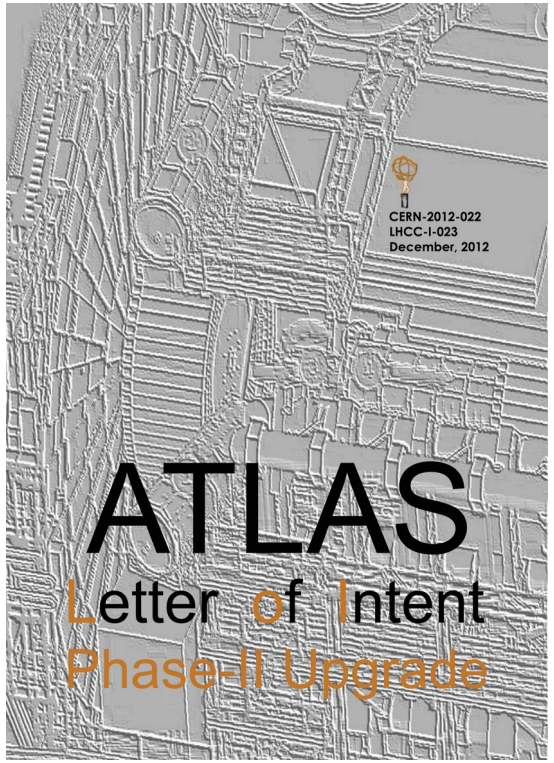
- December 2012 for the entire Phase II Upgrade
- Moving toward a project
- European Strategy identifies **HL-LHC as highest priority**

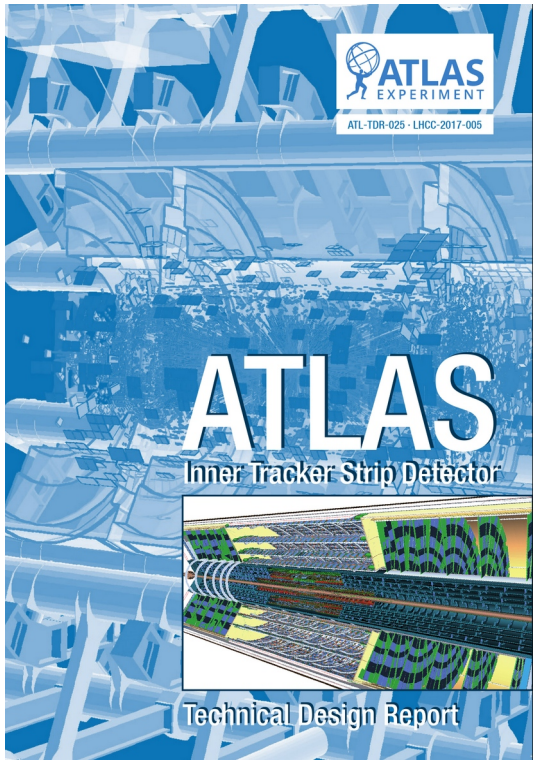
TDR (2017)

- Once approved by LHCC , ITk Strip[s becomes a full-blown project

Pre-Production & Production (2020/21-2026)

- Now it gets serious
- Installation in 2026





The known and unknown unknowns

All the things you did not have on your radar and many love to ignore

Known unknowns

- Schedule slips … always further in the future
- Difficulties getting all the funding
- One yet-to-be named key component delayed
- First final prototype needs a second iteration
- Funding delayed
- Groups pull out
- These are one you always in your risk register
  - With likeliness, mitigation strategies ...

Unknown unknowns

- A Pandemic … that wasn't in any risk register
- A global chip shortage
- Export regulations
- Legal framework changes
- These are one not in your risk register
  - But they can quickly add month of delays

NB: I consider the ATLAS ITk Strip a project that runs very well …

Lessons learned & Impact on IDT planning

My personal view

We as a community

- We're are quite ok in making a technical-driven project schedule, but notoriously optimistic, once politics, funding and sociology enter the game

Lessons learned from the upgrades

- Don't make technology choices to early in the game chances are that your technology has been deprecated once you have to really build it
  - And don't believe 1 million penalty fee is not a lot of money in the semiconductor business
- Single-vendor sourcing and non-standard solutions are a sure way to desaster …
  - This is something we're seem to relearn in every project
- Common ASIC development is the right way forward, but make sure, that this effort has sufficient design manpower
- Building up a project like ITk Strips with enough groups is challenging and takes time
  - Integrate newcomers, steer to the right activities
  - Like in real life, once money enters the game things become more complex

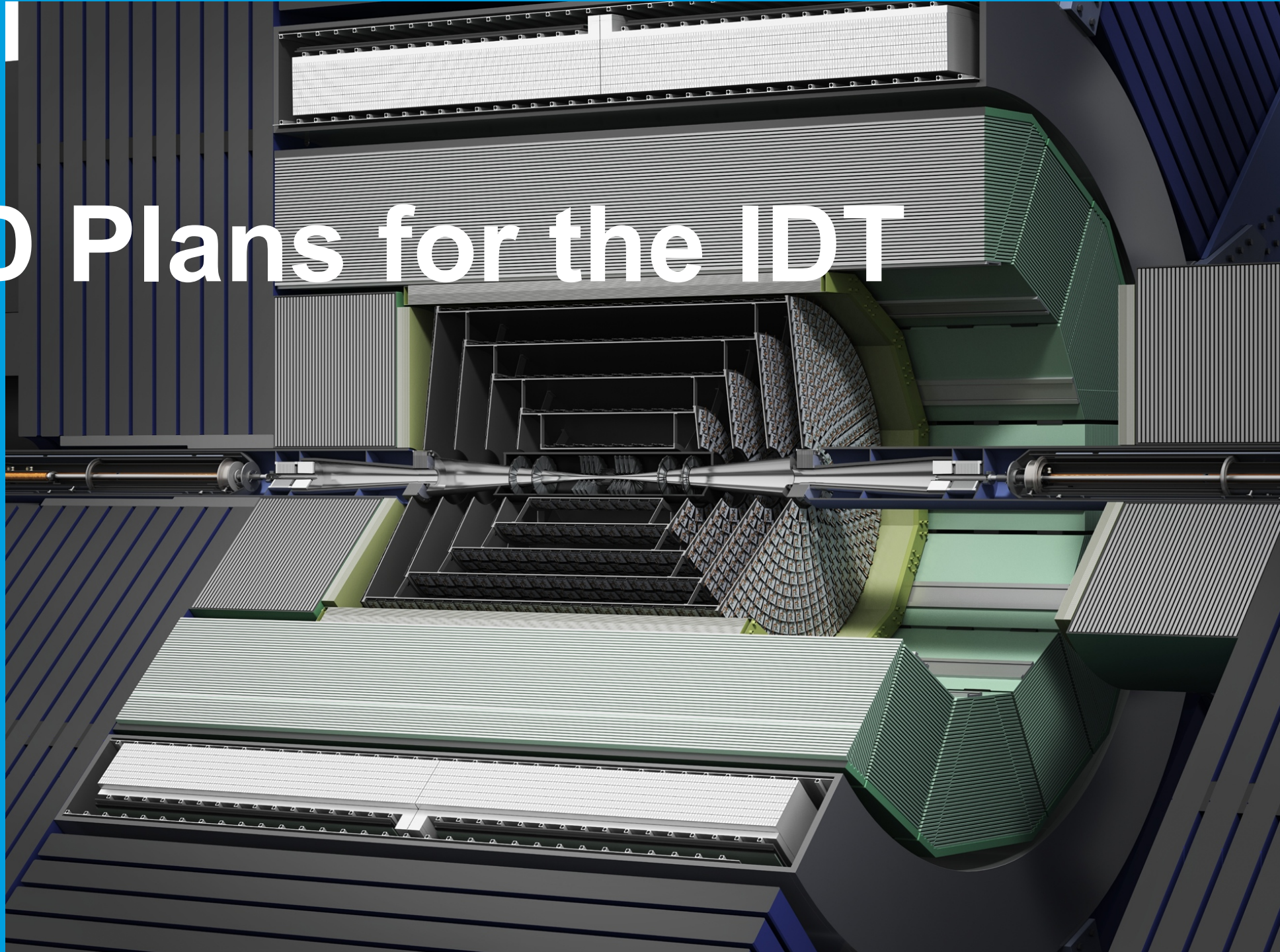
Lessons learned & Impact on IDT planning (II)

Still my personal view

Lessons learned

- It's not the "hot topics" that will give you problem …
  - DC-DC converters, connectors, cables
- A decade between a TDR and installation is a realistic timescale
  - Don't estimate all the necessary steps (and the funding necessary) for a small system prototype
  - And you need this for a "go" for production
- Having a fully functioning host lab is a huge bonus – hard to quantify this in years or Euros
  - LHCC-like organized reviews that are also well respected by the funding agencies
  - Infrastructure and engineering support
- Be technologically bold and challenging
  - This attracts the best people

The SiD Plans for the IDT

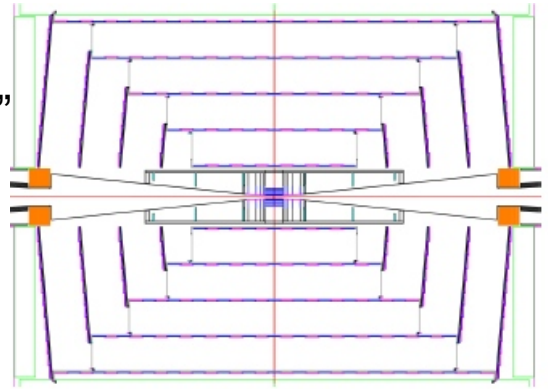


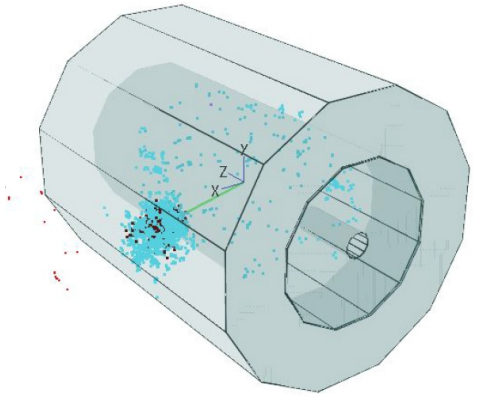
SiD – Overall Detector design choices

Which we should re-visit

Tracker Radius & aspect ratio

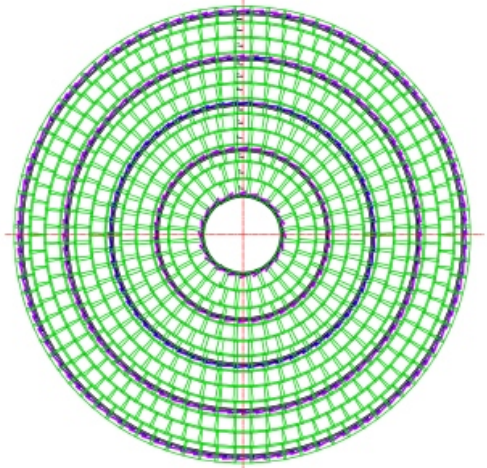
- Extensive work pre-DBD – SiD is in a “sweet valley”
- Idea to make tracker a bit longer, but vetoed by mechanics support team at the time.
- Number of Endcap disks needs to be revisited

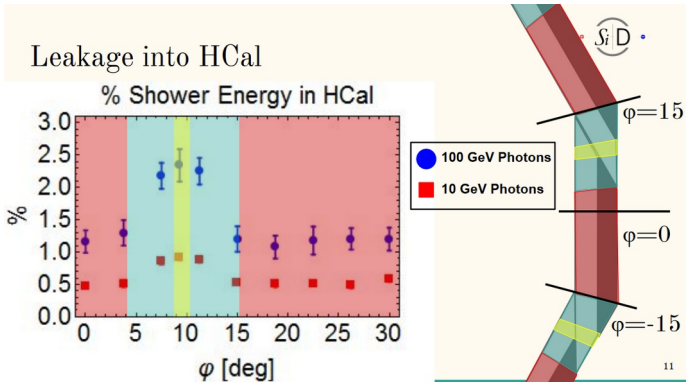




Overall Calorimeter Configuration

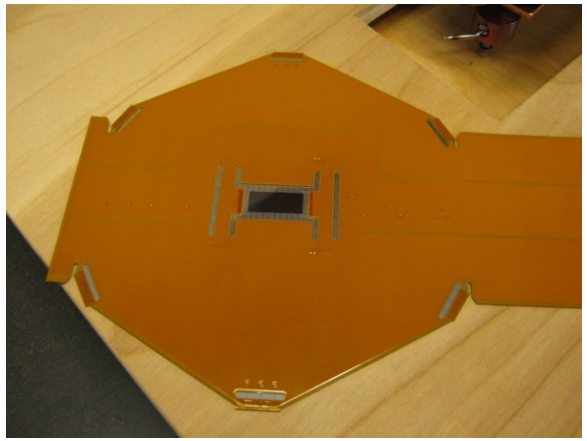
- ECAL 20+10 layers
- HCAL 40 layers
- Is this still the optimal configuration?



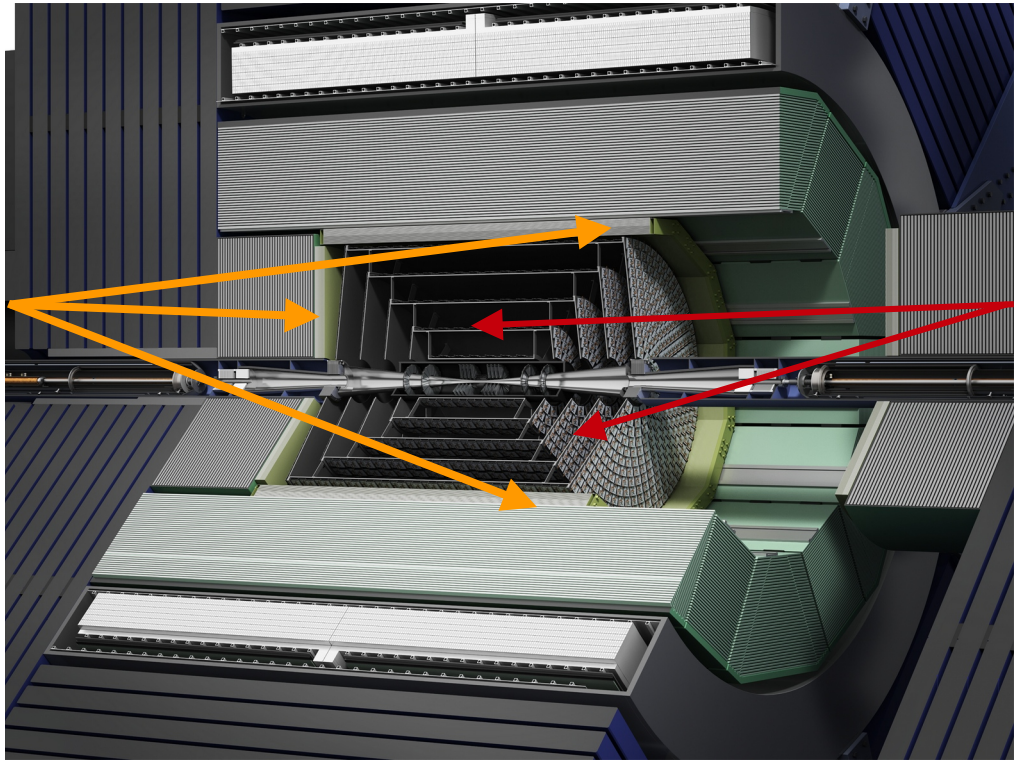


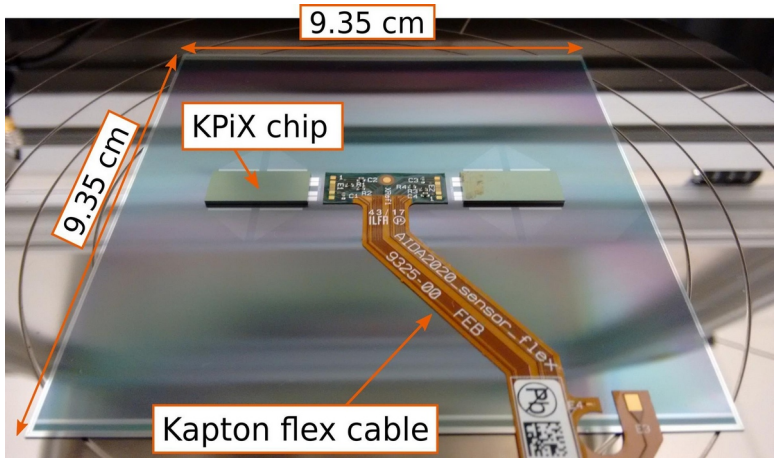
The SiD MAPS program

Using MAPS for Tracker & ECAL



ECAL:
1200 m² sensor area

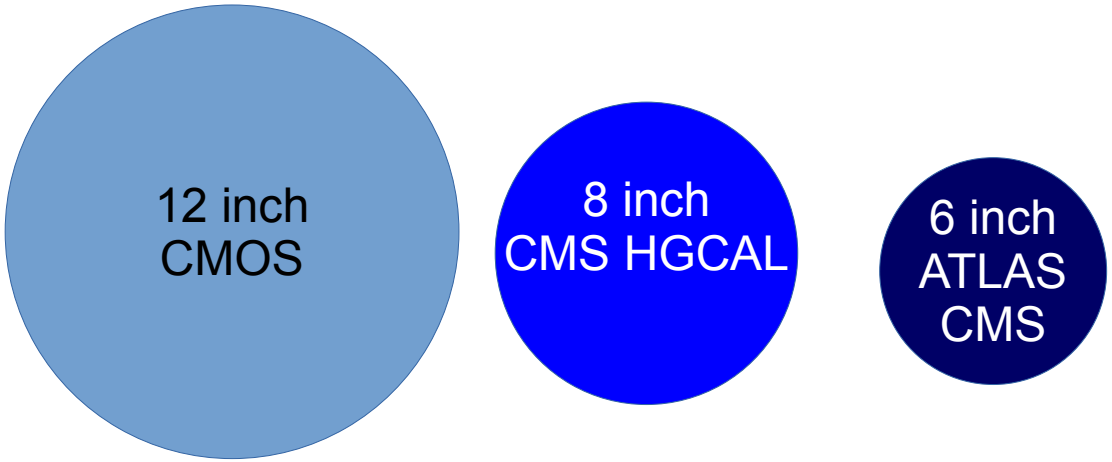




Tracker:
67 m² sensor area

The SiD MAPS program

Necessary Studies

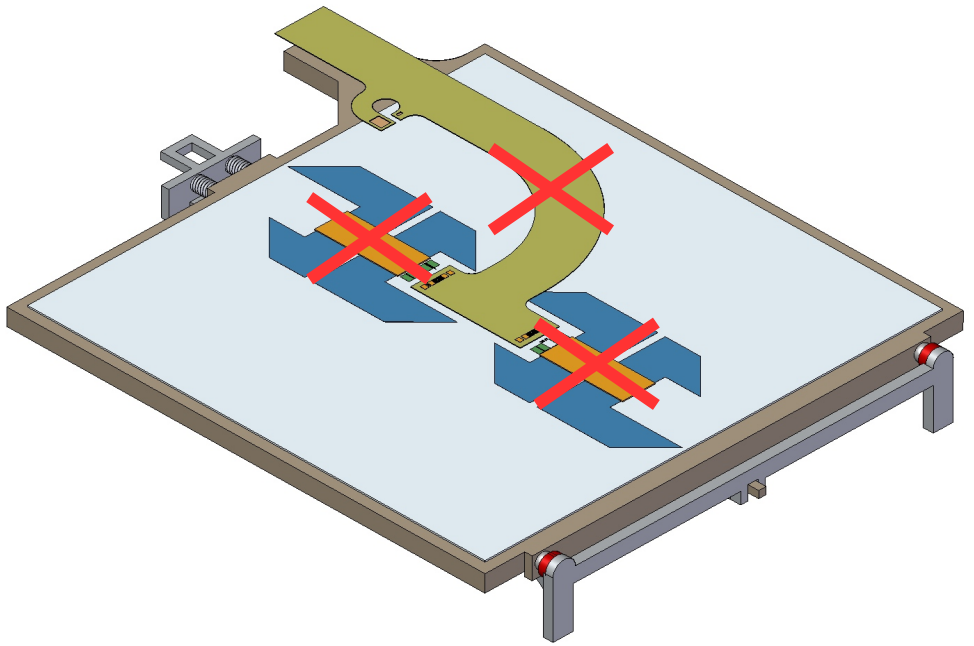


Status

- Currently MAPS is a candidate technology for the Vertex detector – it's the front-runner

The way forward for SiD

- Develop large-scale MAPS for the Tracker and ECAL
- Eliminate bump-bonding and need for readout ASICs
  - Reduces material
  - Simplifies construction
- Reduced cost and increased availability of wafers
  - 6 inch ~ 40000 wafers /year
  - 12 inch ~ 12 million a year
- Explore new processes **now**
  - Time scale of HEP project vs. lifetime of CMOS processes



The SiD MAPS program

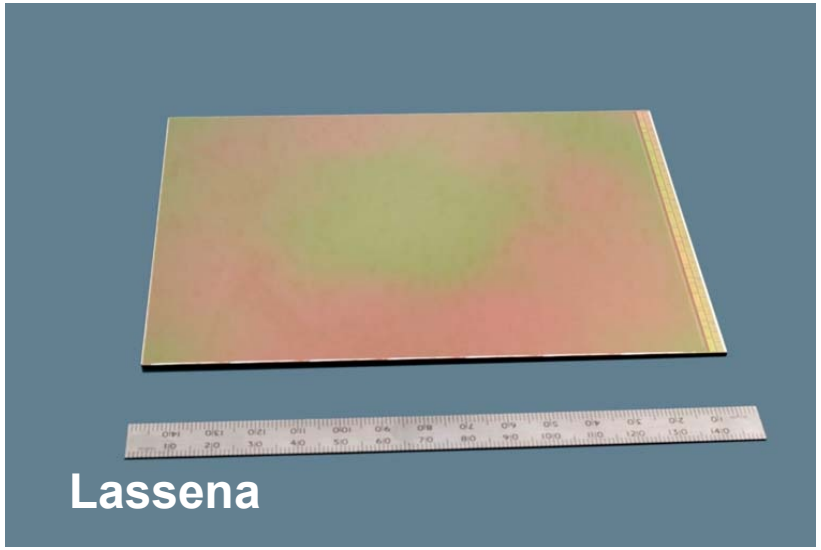
Ideas, Concepts

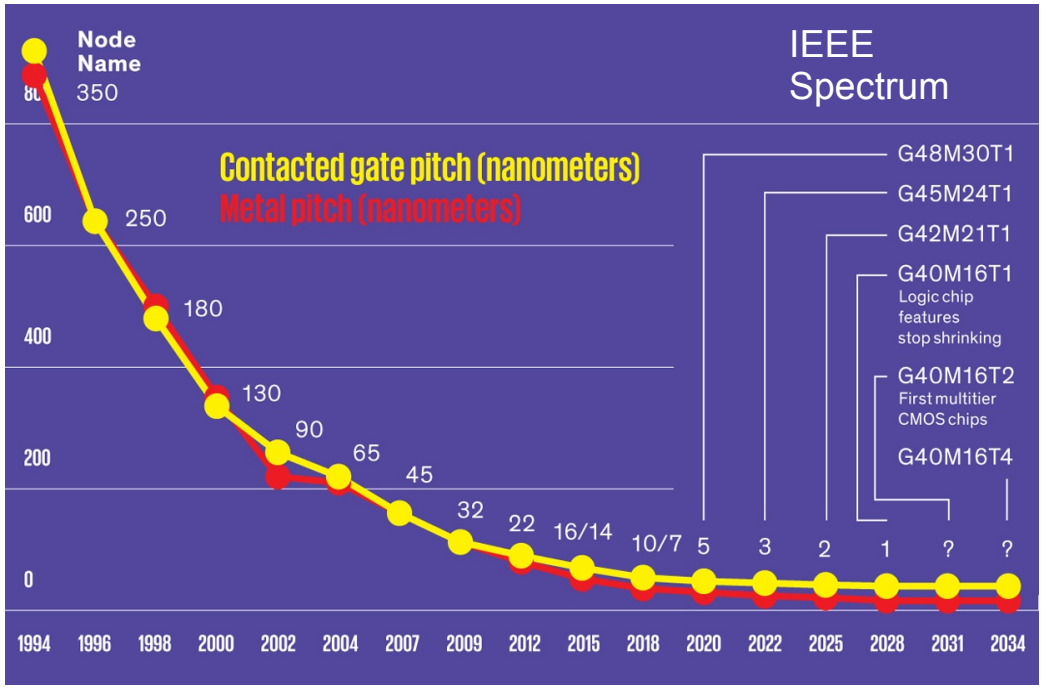
R&D Goals

- Follow closely to CERN-lead 65 nm MAPS program
- Start designing prototypes targeted for SiD
- R&D on Stitching is essential → ALICE is spearheading this
- Inform Vertex Detector R&D

Open questions

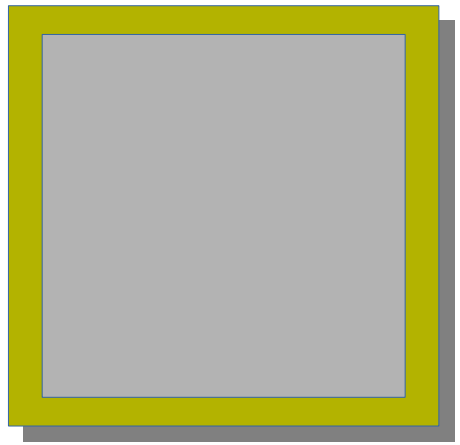
- What is the ideal pixel size for the Tracker/ECAL
  - 25 x 100 µm ?
- Pixel readout Analog(ADC) or Digital(binary) ?
  - Revisit DBD studies for digital ECAL
- Buffer sizes, occupancies → how do they change ?



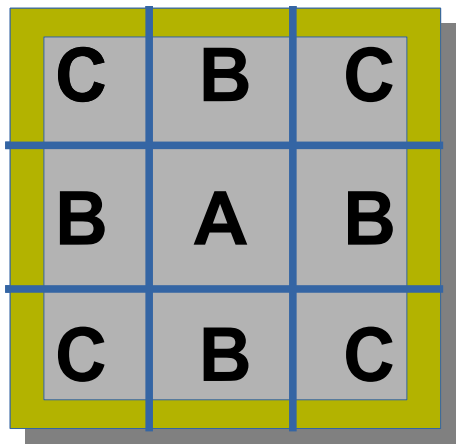


The SiD MAPS program

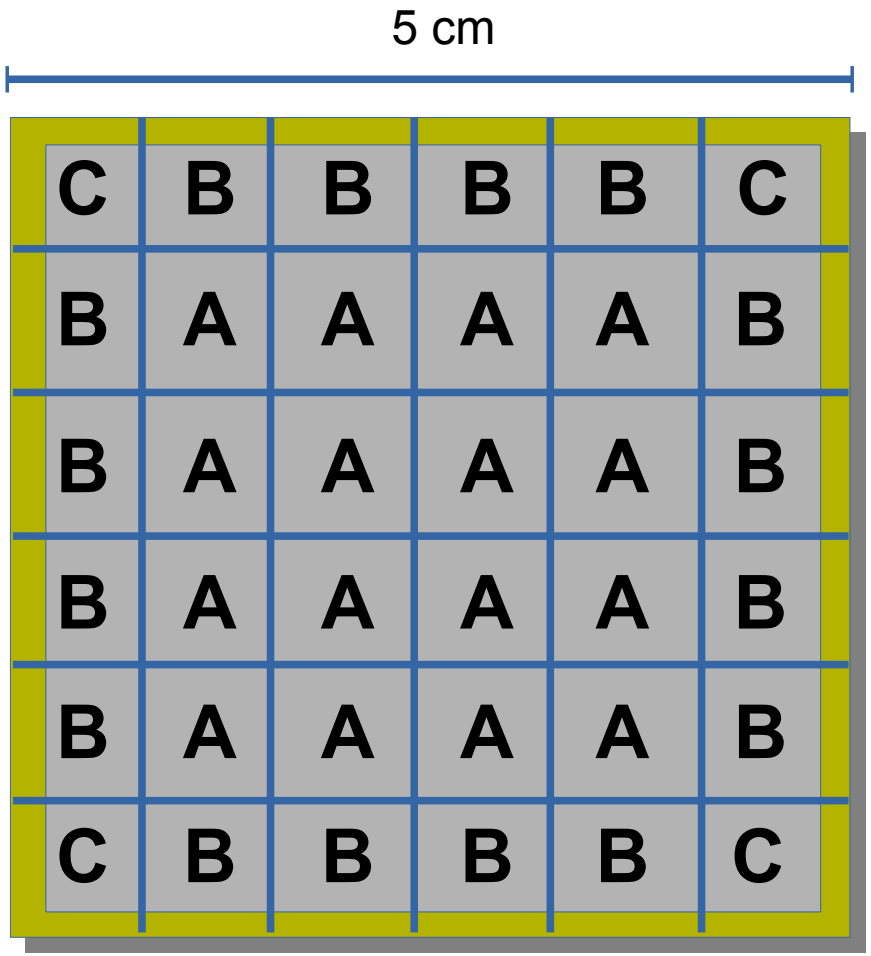
Stitching Primer



Original
Sensor Design



Stitchable
Sensor Design



Stitched
Sensor Design

HCAL & Muons

Studies and Opportunities

The HCAL

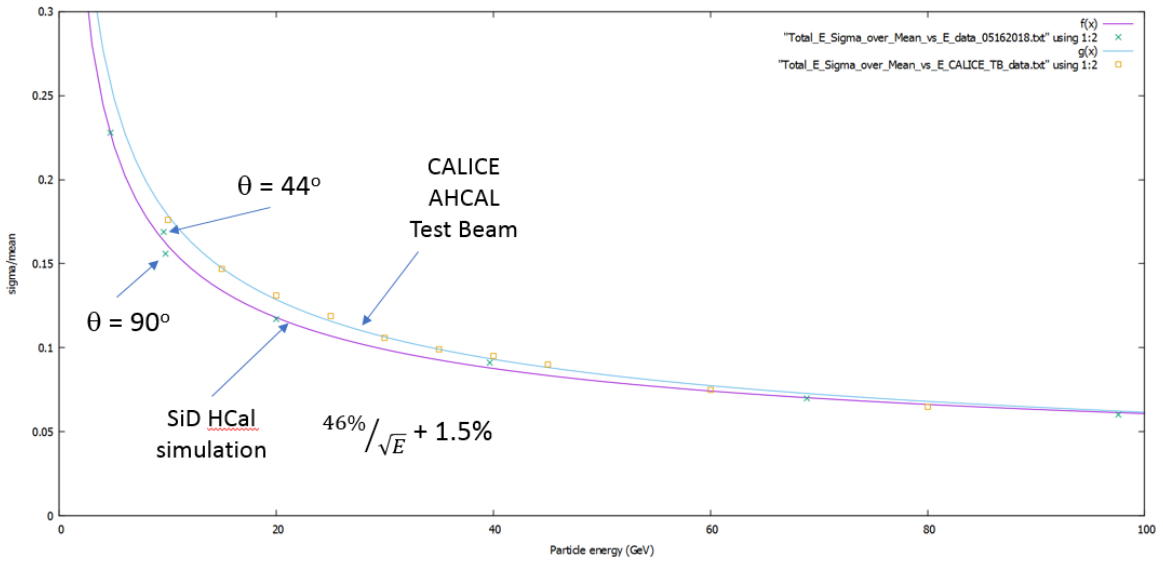
- Baseline is a AHCAL – following the CALICE design

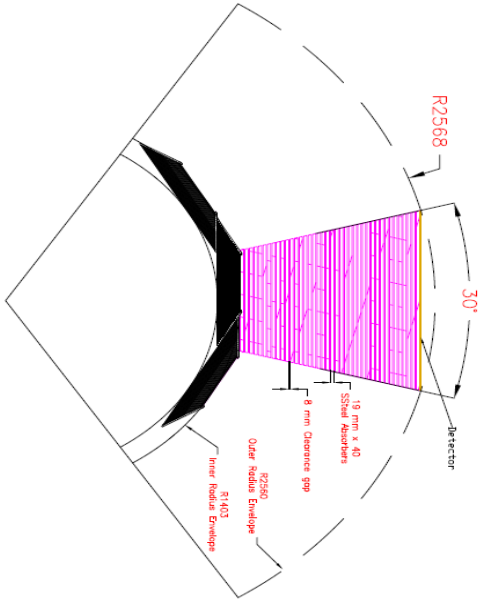
The Muon System

- SiD Baseline – long scintillator strips with WLS fiber and SiPM readout
- Consistent extension of the baseline HCAL scintillator technology
- Need to optimize number of layers, strip dimensions

Open questions

- HCAL
  - Inclusion of timing layers
  - Revisit impact of projective cracks and barrel-endcap transition
- Muons
  - Need to optimize number of layers, strip dimensions





Timing Detectors

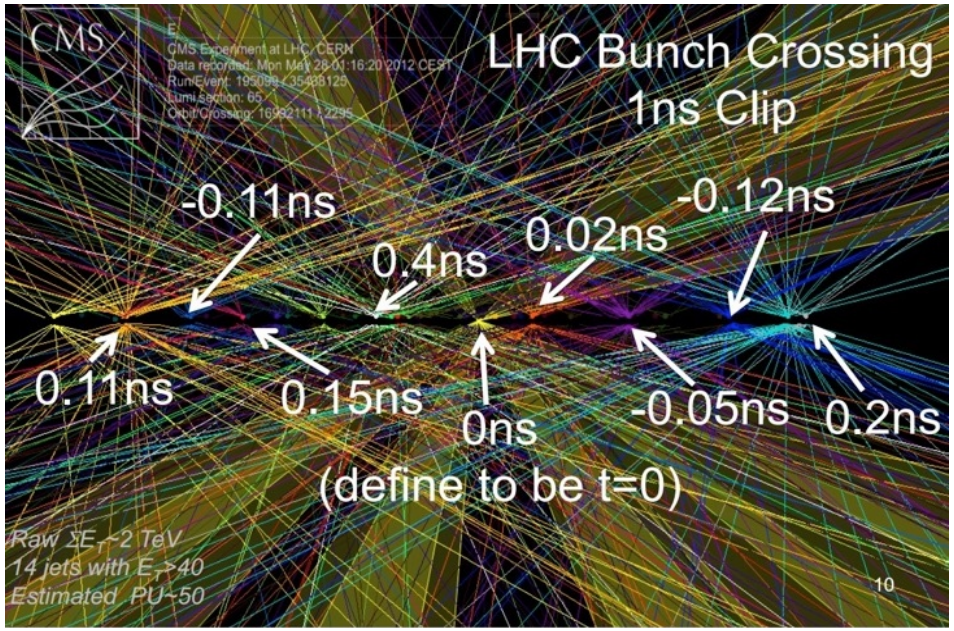
The next "hot thing?

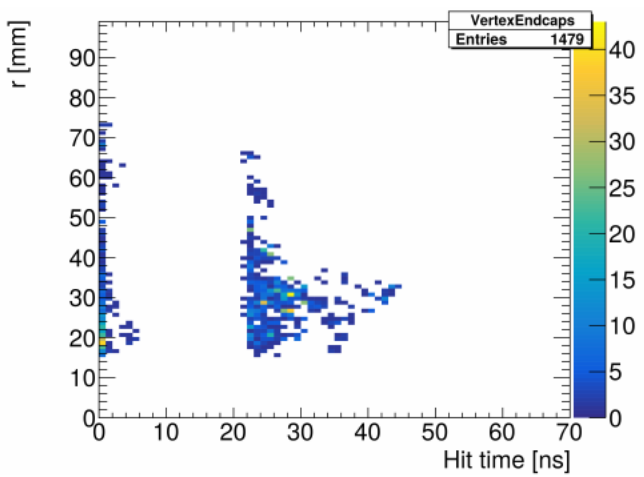
Integrated time-stamping in the trackers

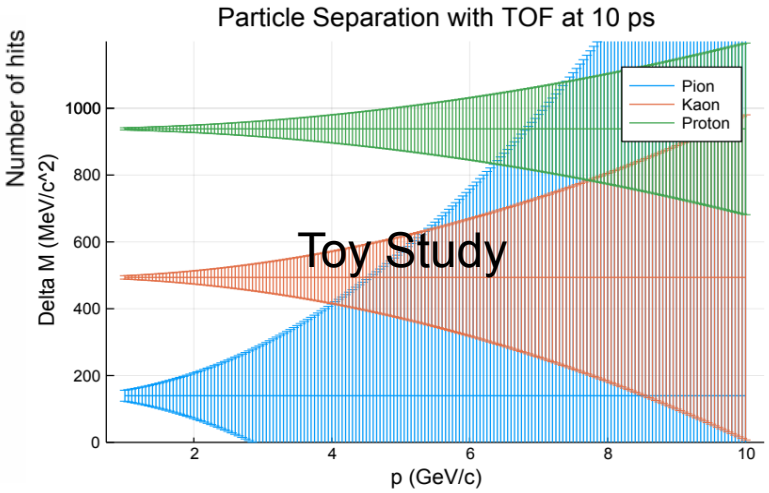
- e.g. Background rejection in the Vertex Detector
- Requires ns-level resolution
- This is doable – already today

Dedicated Timing Layers

- Full 4D Tracking – in the ILC environment
  - No as like the LHC
- Time-of-Flight systems for PiD
  - 10 ps resolution as a goal to be competitive
  - Seems about reachable in a few years
- What kind of physics does this enable?
  - For a detector designed for 250-1000 GeV
- Lots of things to study







Other items

As a short re-cap

Vertex Detector

- Technologically, it remains the most challenging sub-detector

DAQ

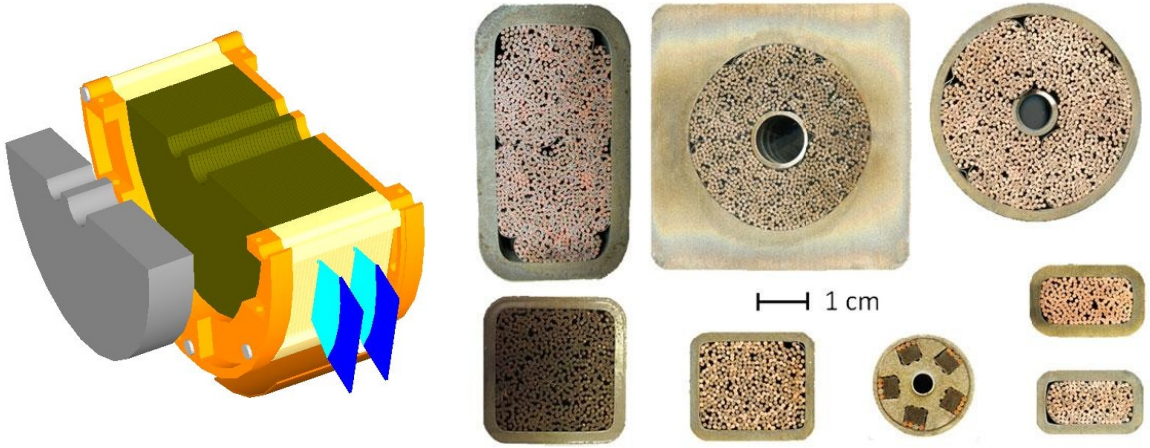
- With the “MAPSsification” the role of front-ends will change
- ASICS will most likely move to purely digital processes
- 28 nm node as being discussed in AIDAInnova

Coil

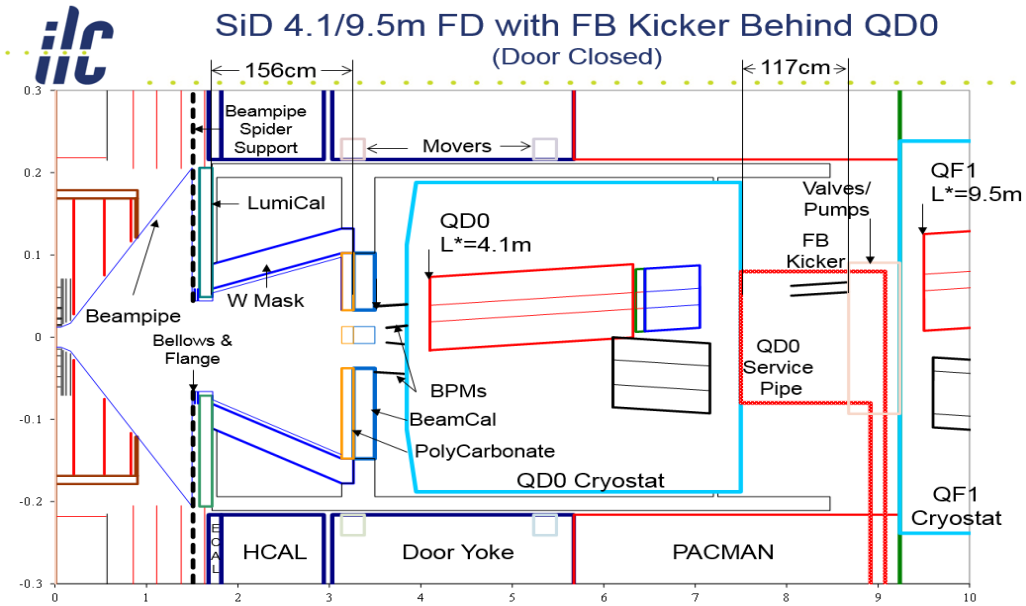
- Looking into alternative conductors like CICC
- Implications for field, Cost … needs to be studied

Alignment

- Can’t be an afterthought in the time of push-pull
- Obviously we can’t do it like at the LHC



Cable-in-Conduit Conductors



What can the IDT/pre-lab do for us ?

Some ideas ...

Sensor, ASICs R&D

- Require significant resources – submissions are expensive
- Prelab could manage MultiProjectWafer (MPW) runs for ILC detector R&D, share cost, expertise, risk
- Lower threshold for small groups to get active

Collaboration tools &infrastructure

- The obvious: Indico, Zoom, ILC accounts
- The necessary
  - Git repositories
  - Wiki Space
  - Storage
- Long-term: Build up dedicated ILC computing
- Organize reviews, liase with funding agencies

Summary

SID plan towards the pre-lab

Did start a critical review of SiD -DBD versions

- Basic concept is sound
- Revised some technology choices in light of technology advances

Plans & ideas for the IDT

- There will be increased activity in the upcoming years
- Now is the ideal time to come with new ideas and to incorporate R&D and experience from HL-LHC
- Get into a good starting position once the pre-lab start

No plan survives the first contact with the funding agencies !

Thank you