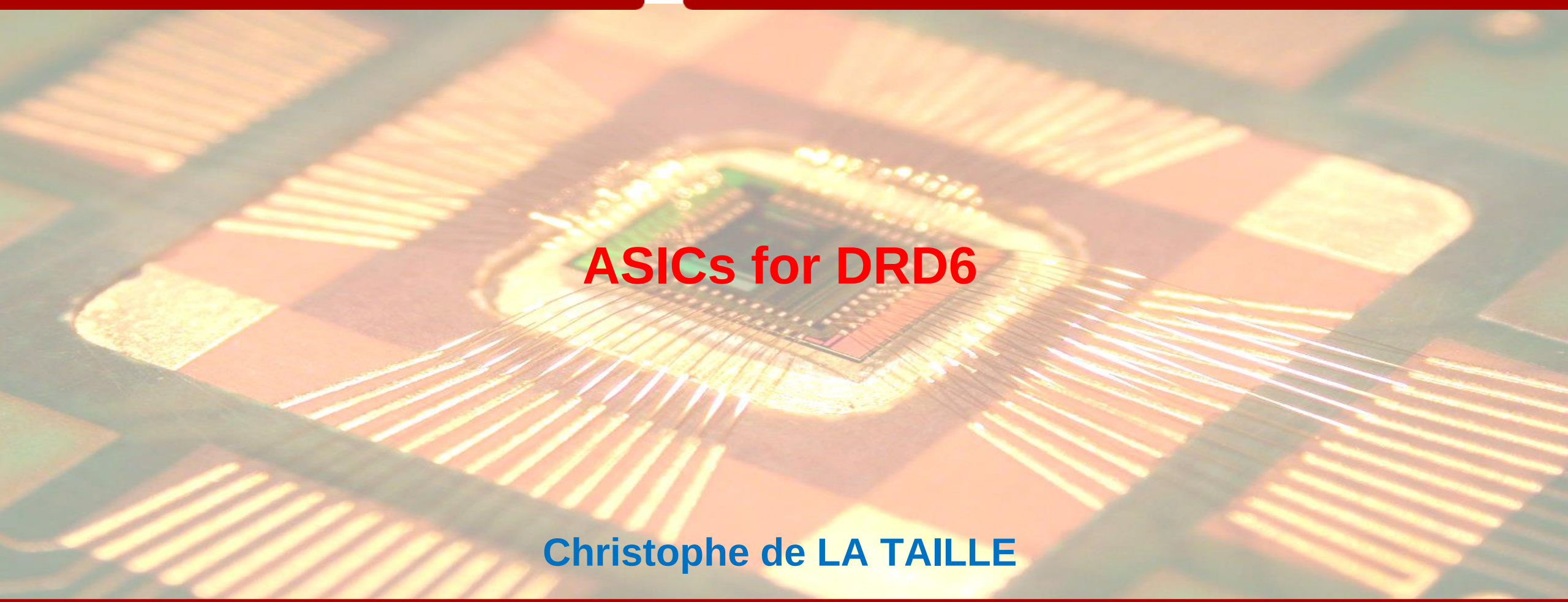


ASICs for DRD6

Christophe de LA TAILLE

Organization for Micro-Electronics desiGn and Applications

Goals

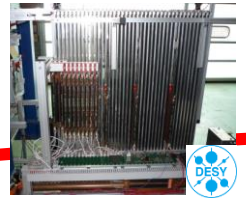
- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend

  ⇒ allows common DAQ and facilitates combined testbeam

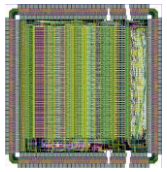
- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch
  - Allows better granularity or LAr operation
  - Extend to LAr (cryogenic operation) and MCPs (PID)
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts

ASICs produced and installed on detectors

Omega

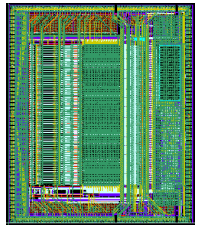


MAROC3

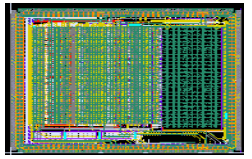


2006

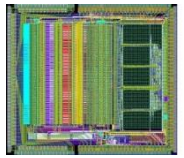
SKIROC



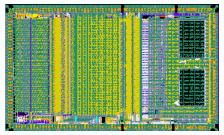
SPIROC



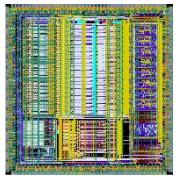
MICROROC



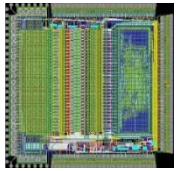
HARDROC



SPACIROC



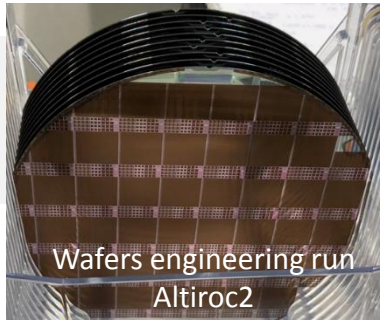
PETIROC



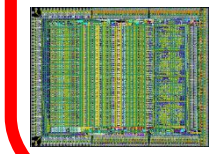
9 engineering runs in 9 years :

AMS SiGe 0,35um 2014, 2016, 2018

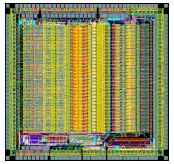
TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



TRIROC

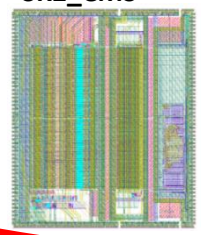


CITIROC

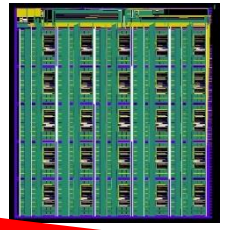


CATIROC

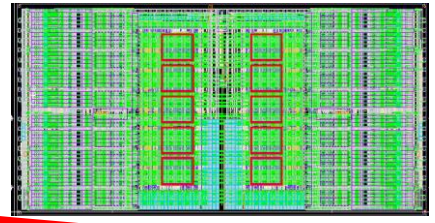
SK2_CMS



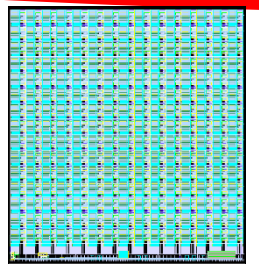
ALTIROC1



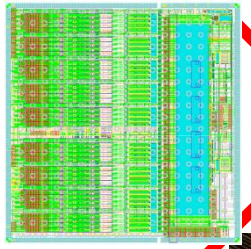
HGCROC



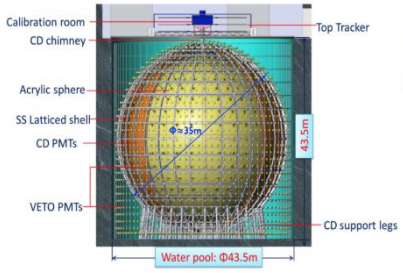
ALTIROC2

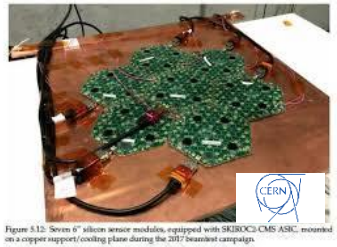


HKROC

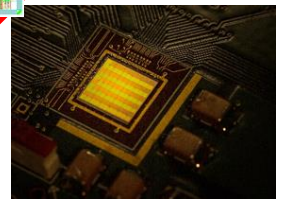


2023



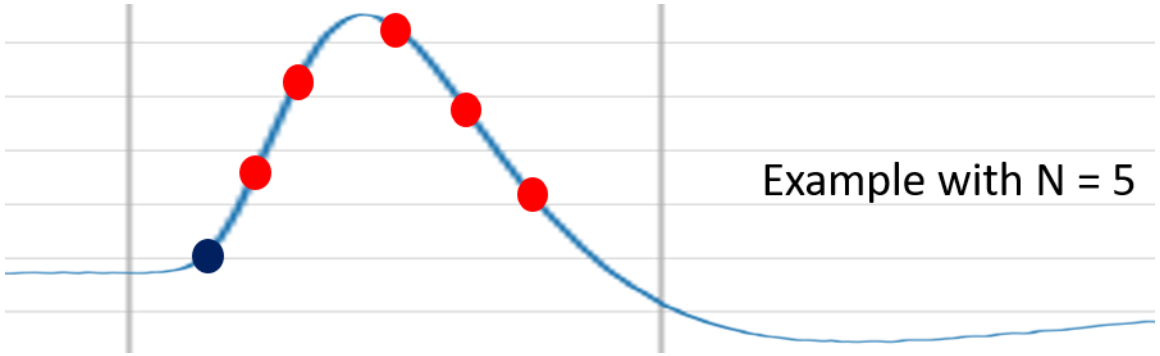


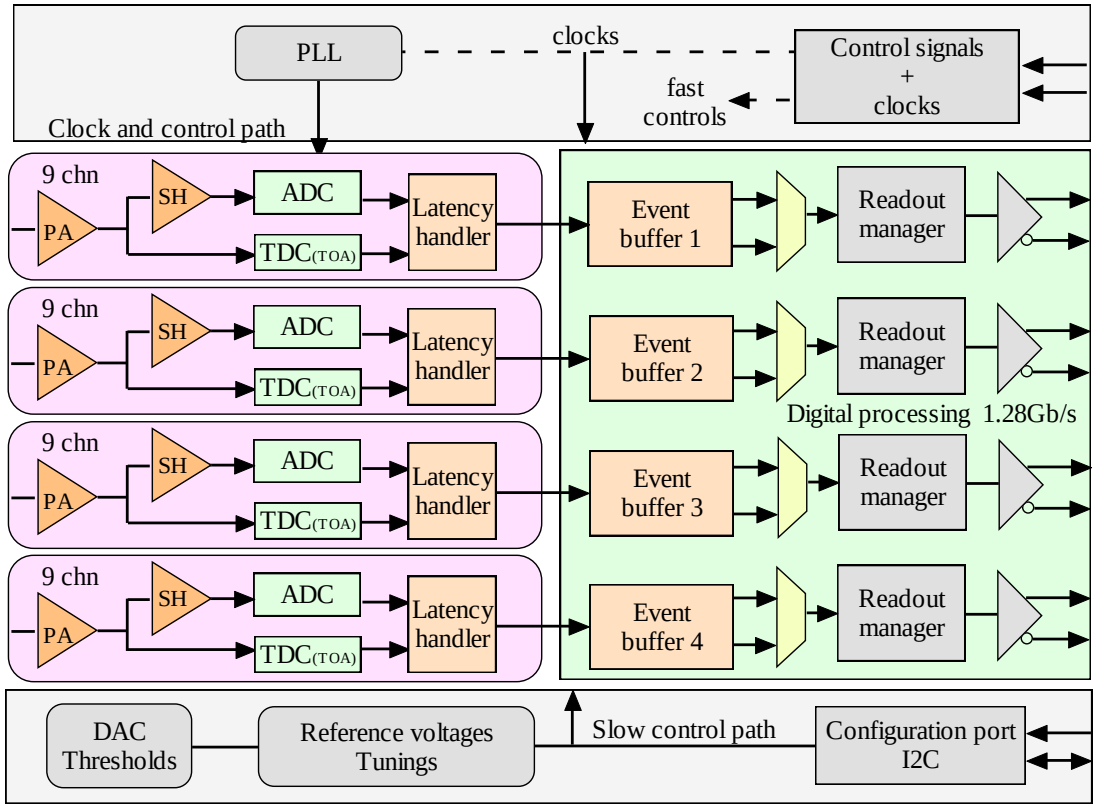
CALICE 29 mar



HKROC : starting chip

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain
  - Charge measurement with 10 bit ADC
  - Time measurement with 25 ps binning
  - Readout with high speed links (1,28 Gb/s)
  - Hit rate ~400-1000 kHz/ch in average
  - Up to 20 consecutive events possible
  - Low power : 10 mW/ch
  - BGA package
  - HKROC is a waveform digitizer with auto-trigger





DRD6 proposal

- Collaboration OMEGA + AGH Krakow + CEA Saclay
  - OMEGA : VFE and backend
  - AGH : ADC
  - CEA : TDC

- Prepare MPWs and/or engineering runs to get enough chips for calos
  - Already ~300 k€ for an engineering run in 130 nm
  - First run early 2024 with EICROCs and « DRD6 ROCs »

- Submit to DRD6 to have close interaction with physics performance
  - Embedded electronics and joint FE/detector optimization

backup

Timeline and hardware

HKROC0
2021/12

HKROC0-BGA
(x80) - 2022/06

HKROC1b-BGA
(x80) - 2022/12

HKROC production
(x4000) - 2023/04

HKROC-based acquisition system paper 2023/09

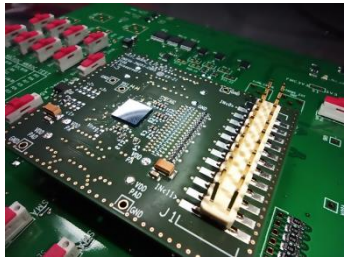
Mezzanine daughter board

Acquisition board

Acquisition board with reconstruction

2023/06

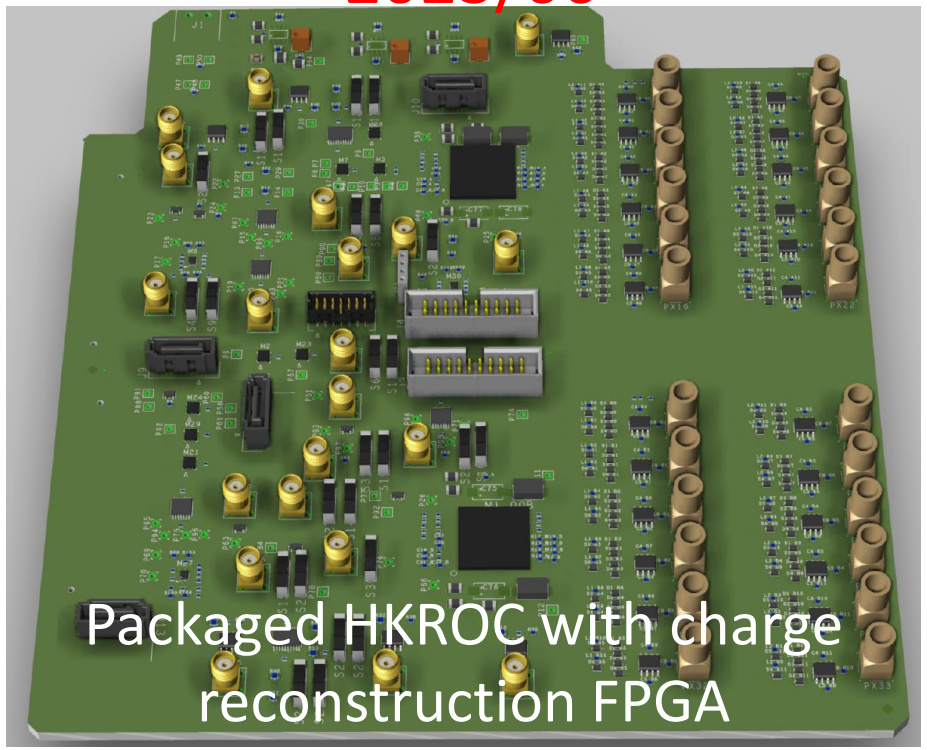
2021



Naked HKROC on mezzanine

2022

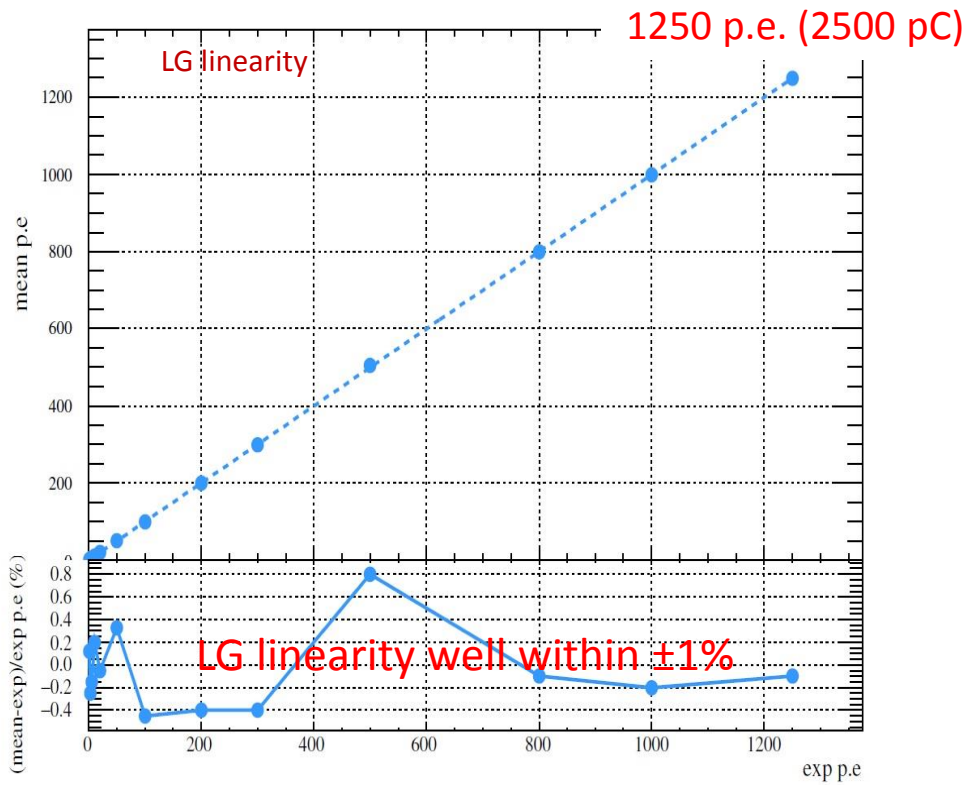
Packaged HKROC with acquisition board

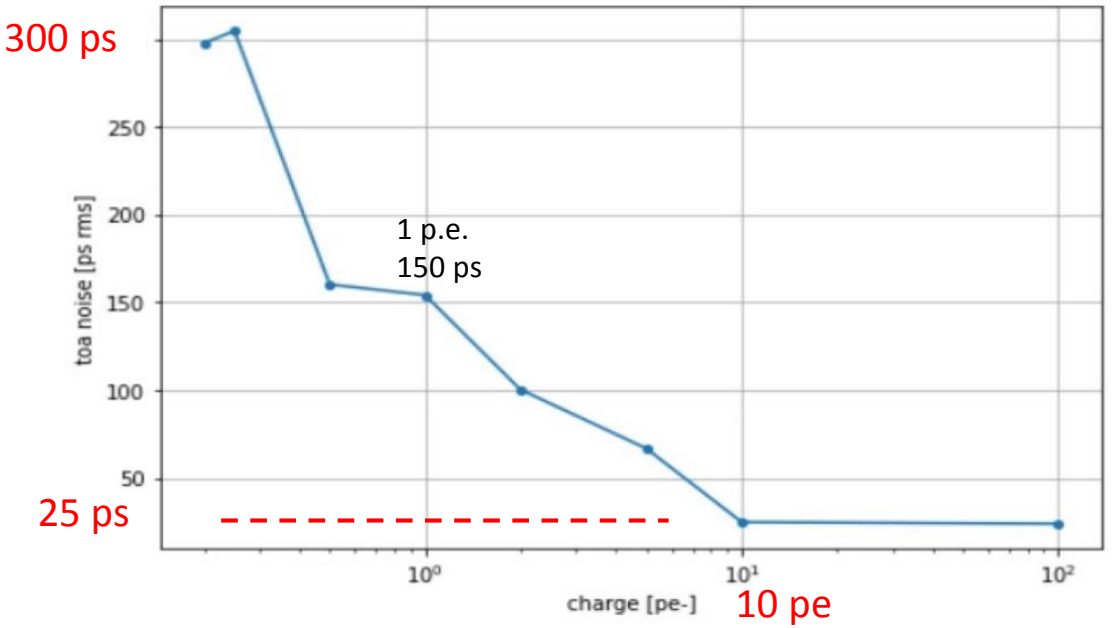


Packaged HKROC with charge reconstruction FPGA

Main experimental results with HKROC0 – Charge and Time

- Measurement with the full chain (analog + digital and reconstruction)
  - Signal auto-triggered with threshold





Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC) across the 3 gains**

TDC characterization with **1/6 p.e. threshold**

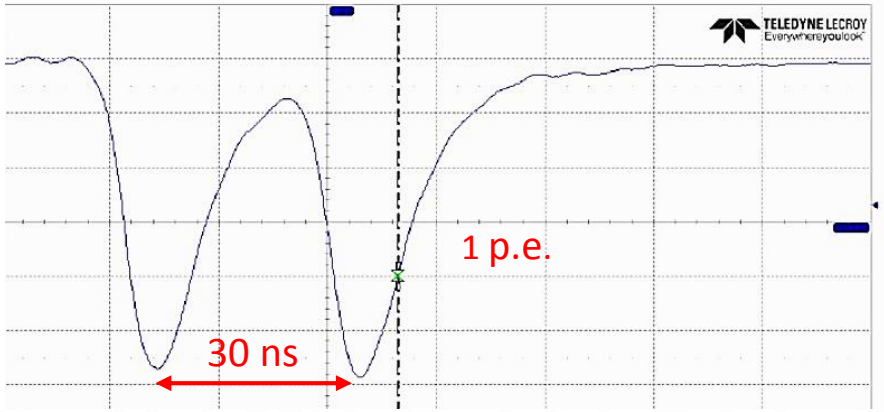
TDC resolution :

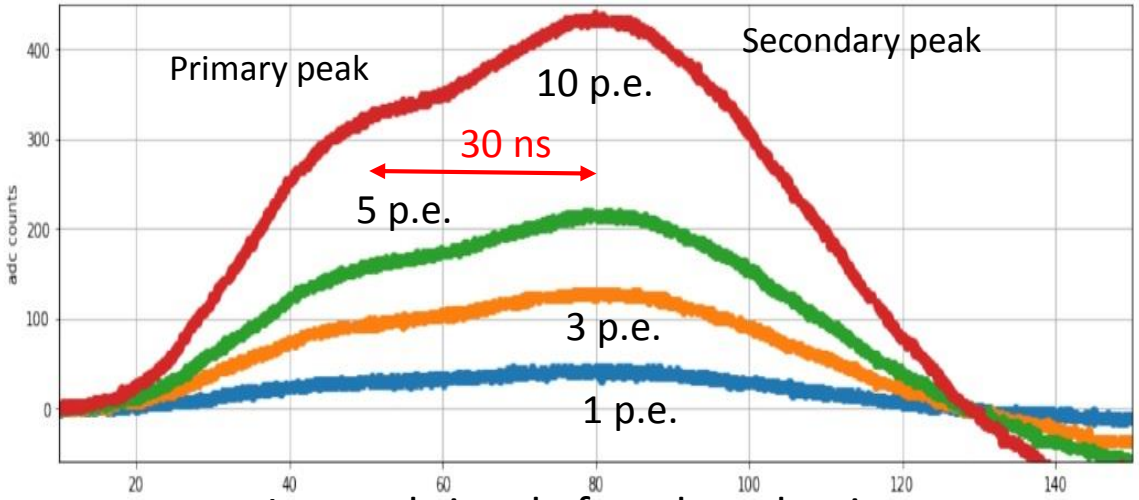
150 ps rms @ 1 p.e

≤ 25 ps rms @ 10 p.e

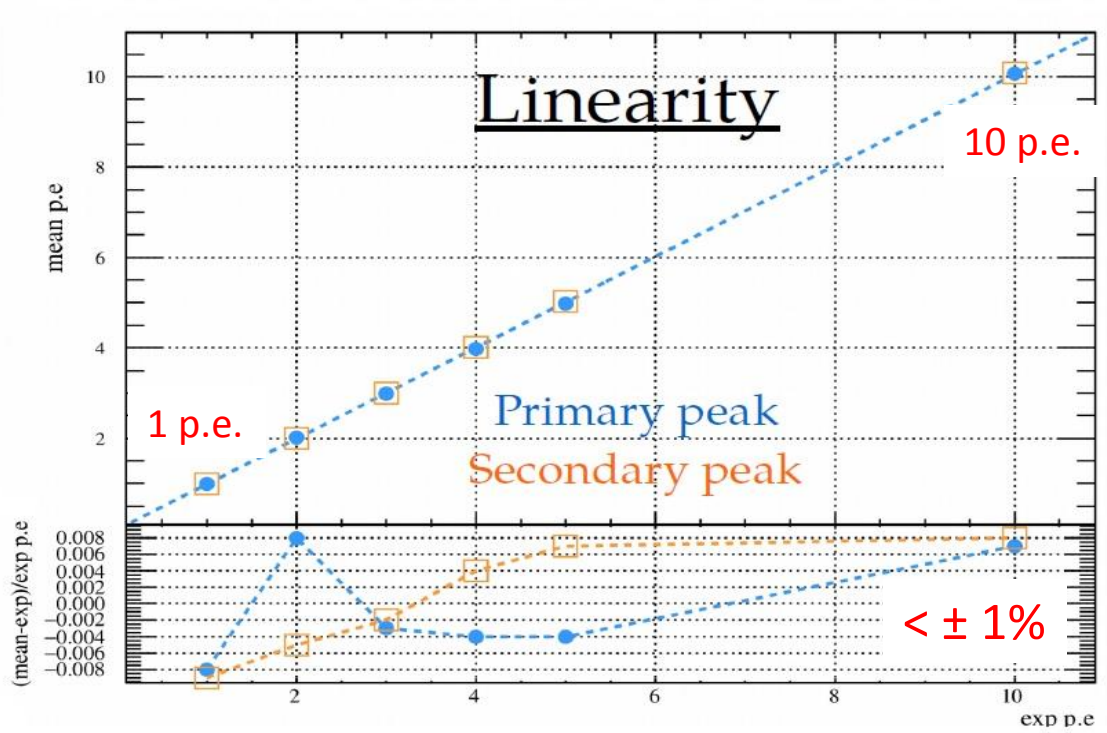
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)





Internal signal after slow shaping

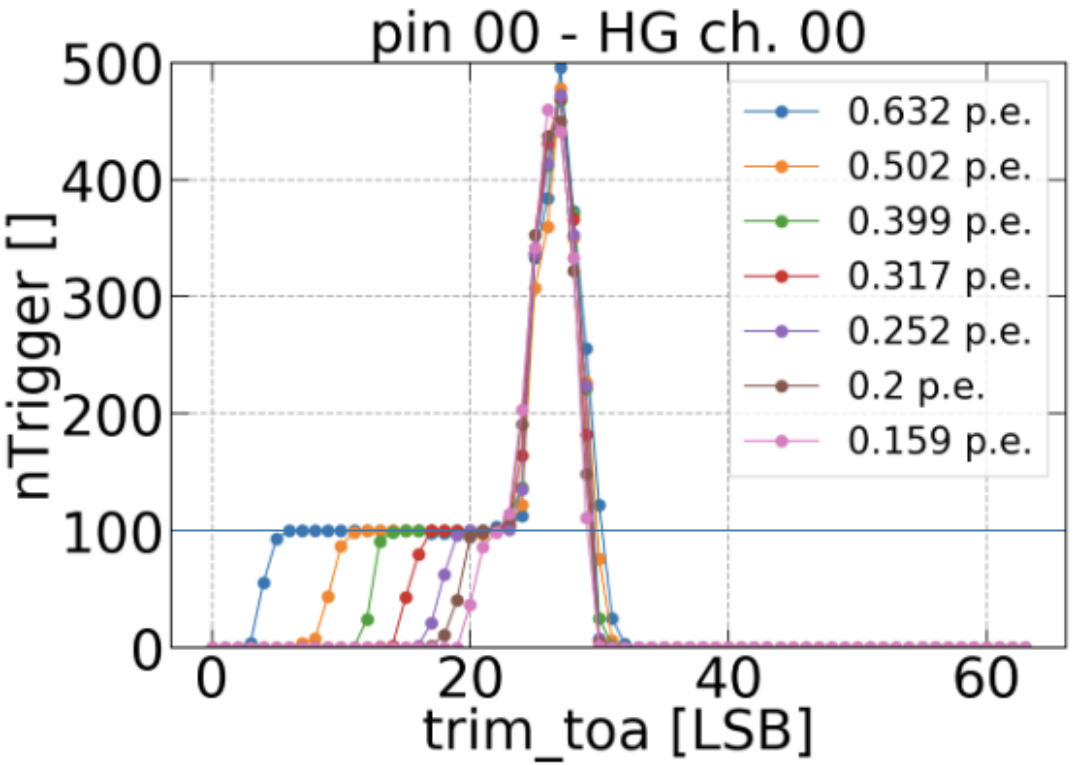


Charge reconstruction algorithm of the two peaks

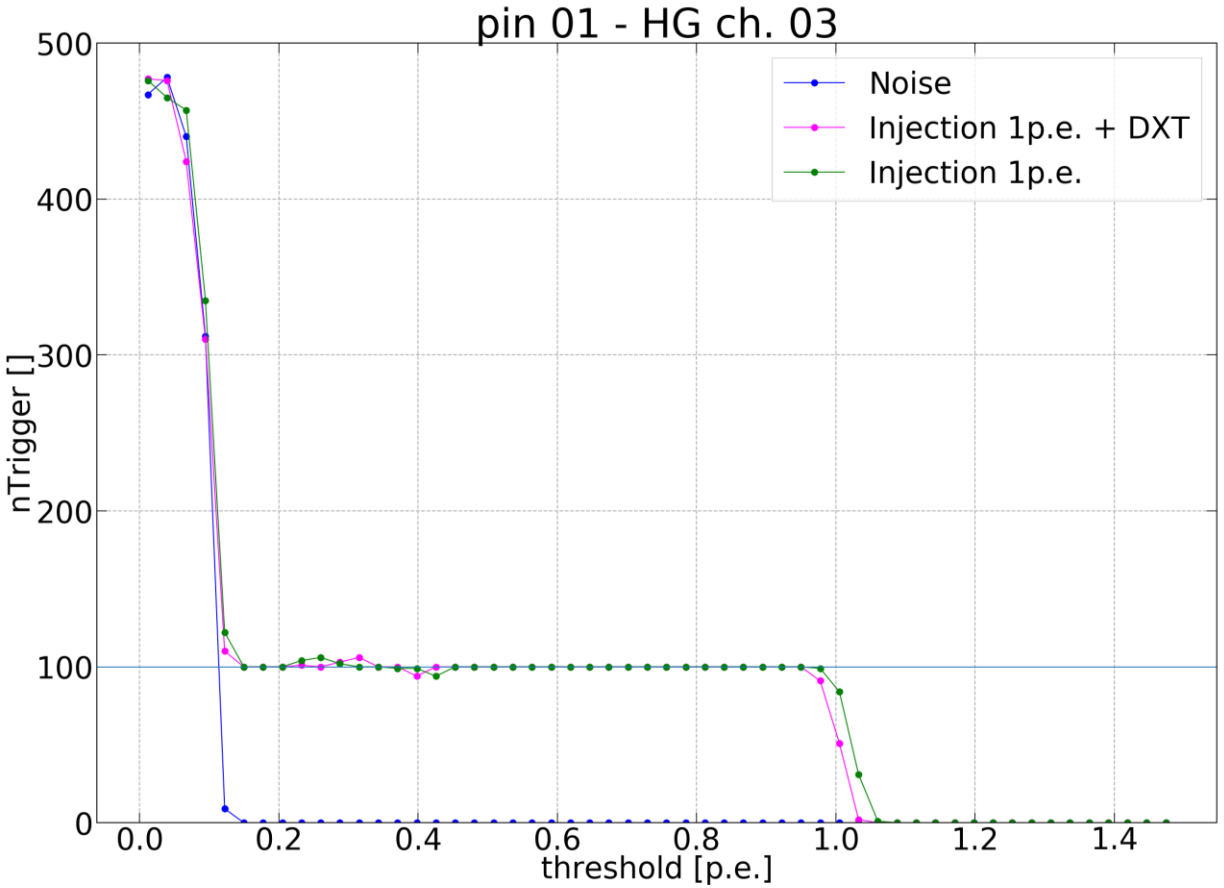
Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

Threshold measurements with HKROC1b



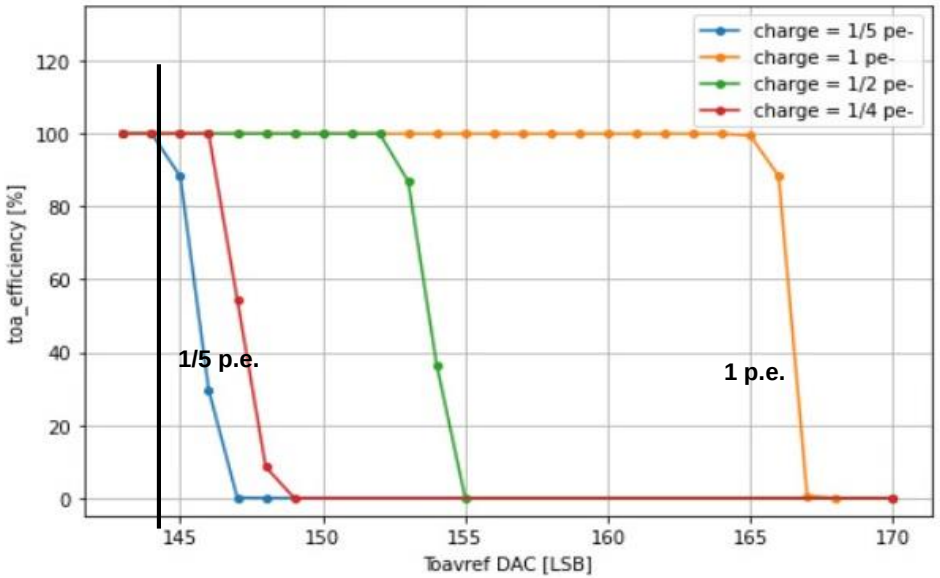
Minimum threshold of 1/6 pe



1 pe trigger efficiency with 1000 pe in another channel

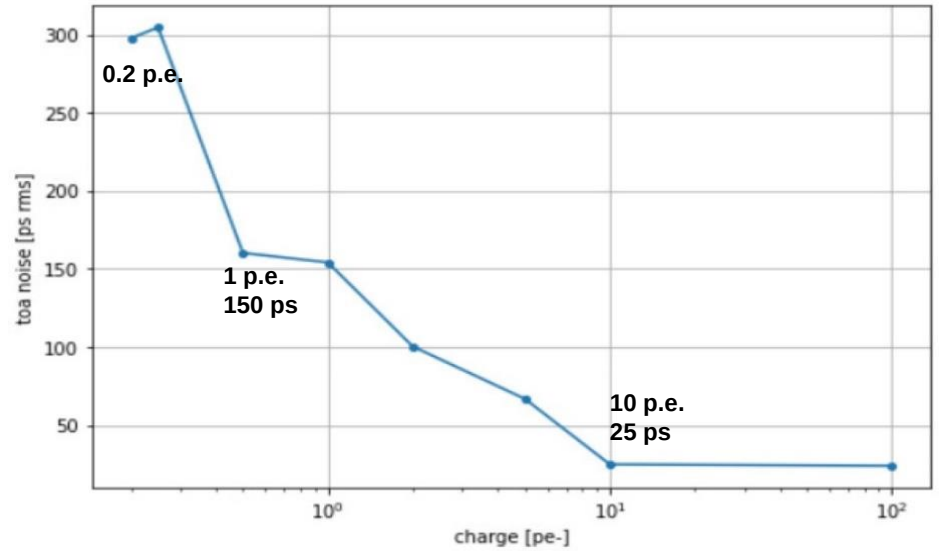
HKROC0 Trigger measurements

The HyperK specifications require the trigger **threshold** to be set at **1/6 p.e (330 fC)**



- **Hit efficiency : 90 % for 1/5 p.e events (400fC)**

  ~100 % if ≥ 1/4 p.e
- Extracted **threshold** value corresponding at **1/6 p.e**
- **Very low noise** : < 1 Hz **(0 noise hit in 10s @ 1/6 of p.e.)**



TDC characterization with **1/6 p.e. threshold**

TDC resolution :

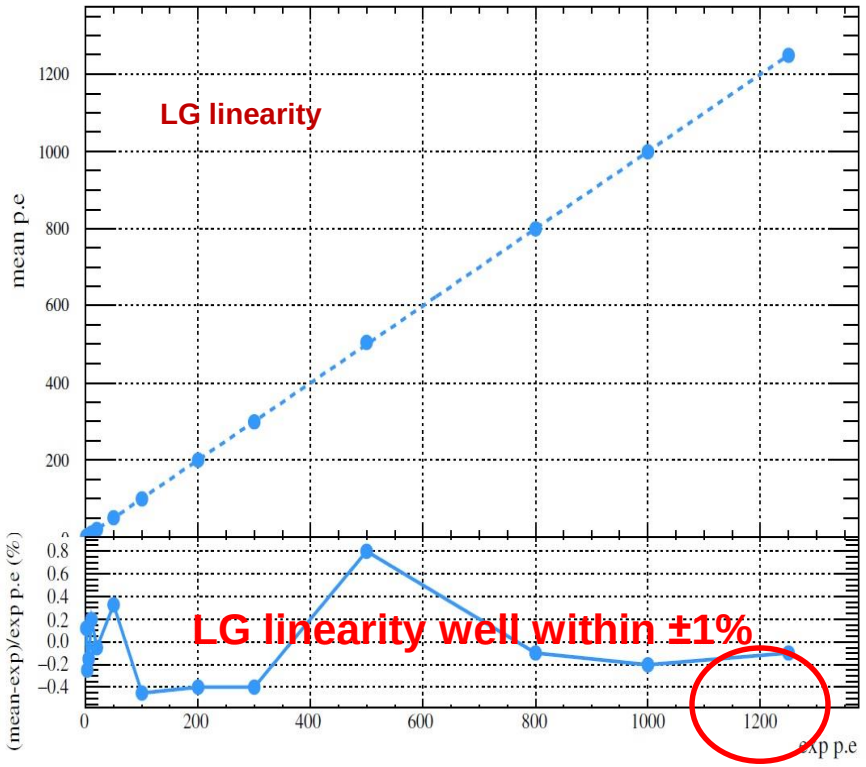
150 ps rms @ 1 p.e [300 ps required]

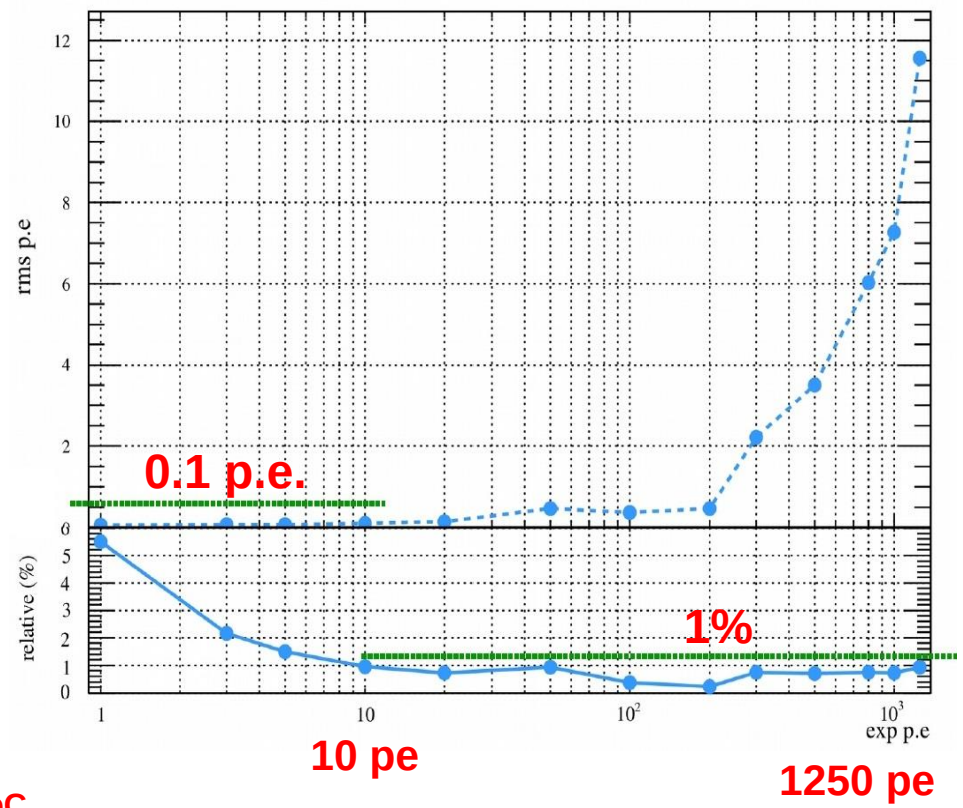
≤ 25 ps rms @ 10 p.e [200 ps required]

- Excellent agreement with HK requirements

HKROC0 Charge measurements

The **whole** acquisition **chain** is tested:
The signal is **amplified**, **auto-triggered** and **converted** by the internal **ADC**.





HG, MG and LG tested!!

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

The charge measurements Fulfill the HK requirements!!!

Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise