Towards CMOS Pixel Sensors fully adapted to the Inner & Outer Layers of an ILC Vertex Detector

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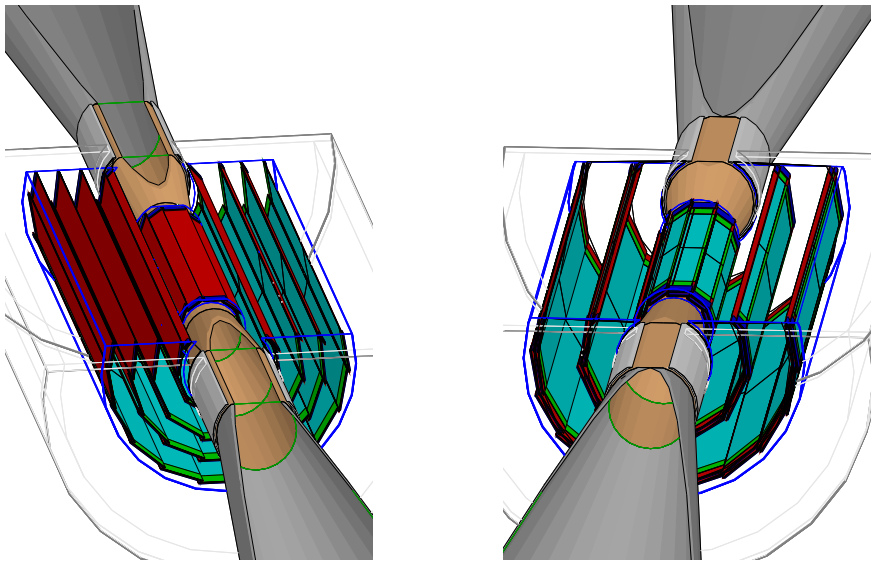
on behalf of IPHC/Strasbourg – IRFU/Saclay collaboration

▷ **More information on IPHC Web site: http://www.iphc.cnrs.fr/-CMOS-ILC-.html**

OUTLINE

- *Progress on fast column parallel sensor*
- *Development of a prototype ladder*
- *First 3D prototypes*
- *Summary*

MIMOSA Based VTX R&D Goals



Sensor requirements defined w.r.t. ILD VTX geometries

- 2 alternative geometries :
  - 5 single-sided layers
  - 3 double-sided layers (mini-vectors)
- pixel array read-out perpendicular to beam lines

Prominent specifications :

- read-out time target values (continuous read-out version) :

  SL1/SL2 /SL3 /SL4 /SL5 DL1 / DL2 / DL3

  - single-sided : 25 / 50 / 100 / 100 / 100 μs
  - double-sided : 25–25 / 100–100 / 100–100 μs
- $\sigma_{sp} < 3\ \mu m$ (partly with binary outputs)
- full ladder material budget in sensitive area ($\lesssim$ 50 μm thin sensors) :
  - single-sided : $<$ 0.2 % X_0
  - double-sided : $\sim$ 0.2 % X_0
- $P_{diss} \lesssim$ 0.1–1 W/cm^2 $\times$ 1/50 duty cycle (5 Hz, 1 ms long, bunch train frequency)

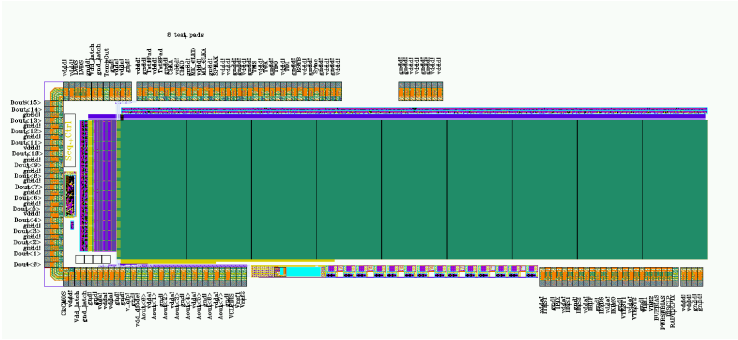
▷▷▷ R&D on swift CMOS sensors and ultra-light (double-sided) ladders

Development Strategy of Fast CMOS Sensors

- **Target values : read-out time $\lesssim$ 25 - - - - 100 μs $\rightarrowtail$** *sensors organised in pixel columns read out in //*

- **R&D organisation : 3 simultaneous R&D lines $\Rrightarrow$ 3 types of μcircuits**

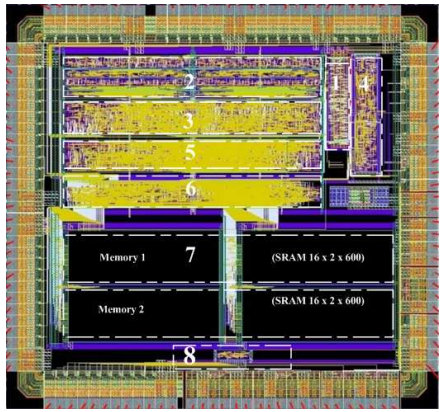
MIMOSA-22



  - *architecture of pixel arrays organised in columns read out in //*
    - ▷ *CDS and pre-amp μcircuit in each pixel*
    - ▷ *1 discriminator ending each column*

    ↪ *MIMOSA-8 (2004), MIMOSA-16 (2006), MIMOSA-22 (2007/08)*

  - *$\emptyset$ μcircuits & output memories : SUZE-01 (2007)* $\longrightarrow$



  - *4–5 bits ADCs (1000 ADC featuring 20×500 μm^2 per sensor !)*
    - ▷ *potentialy replacing each discriminator*

    ↪
    - $\sigma_{\mathbf{sp}} < 2\ \mu m$ *(4 bits)* $\rightarrowtail$ *1.7–1.6* μm *(5 bits) for 20* μm *pitch* $\rightarrowtail$ *presumably not required*
    - $\sigma_{\mathbf{sp}} \lesssim 3\ \mu m$ *in case of 30–35* μm *pitch* $\rightarrowtail$ *outer layers*

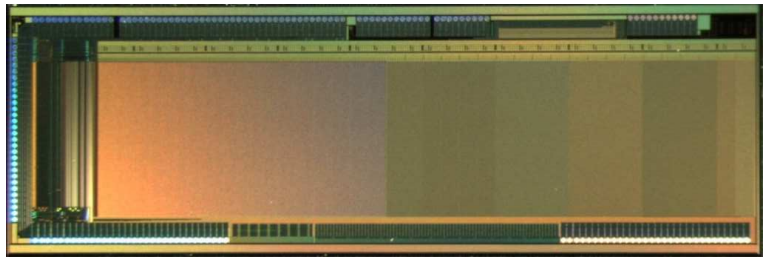
Performances of a Large Prototype with Digitised Output

MIMOSA-22 : ◇ *fabricated in 2007/08 (coll. with IRFU/Saclay)*

◇ *136 col. of 576 pixels (18.4 μm pitch, integrated CDS)*

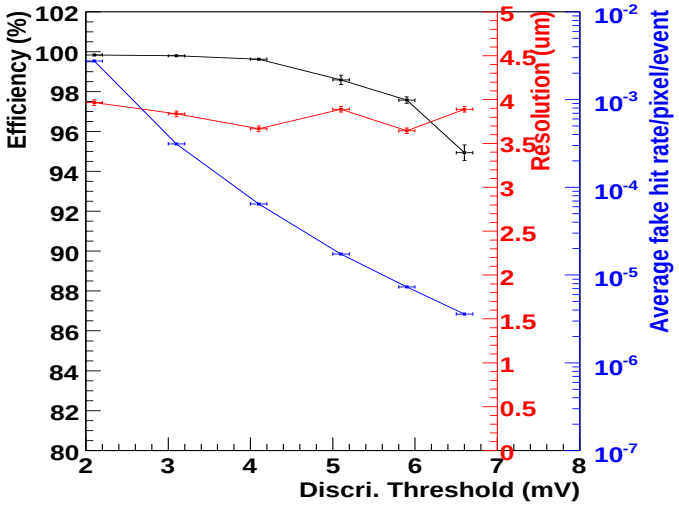
◇ *128 col. ended with an integrated discriminator*

◇ *integrated JTAG controller*

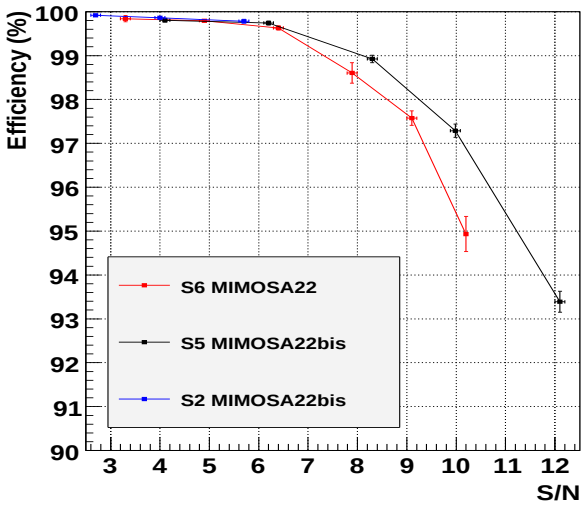


Tests at CERN-SPS ($\sim$ 120 GeV π^-) in 2008 $\longmapsto$ *results of different sub-arrays*

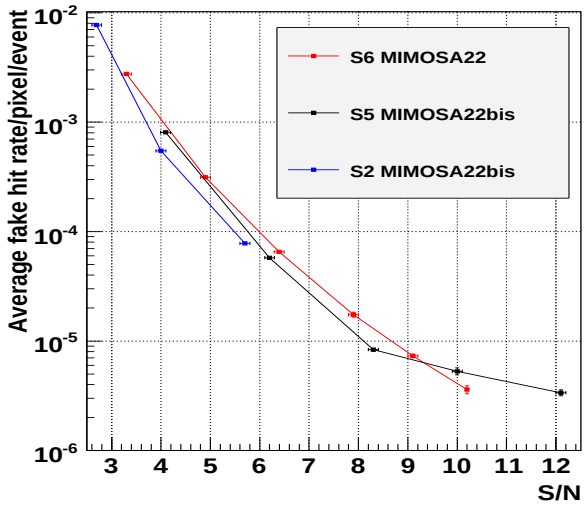
M22 digital S6. Efficiency, Fake rate and Resolution



S6 M22, S5 M22bis & S2 M22bis digital Efficiency



M22bis digital fake hit rate

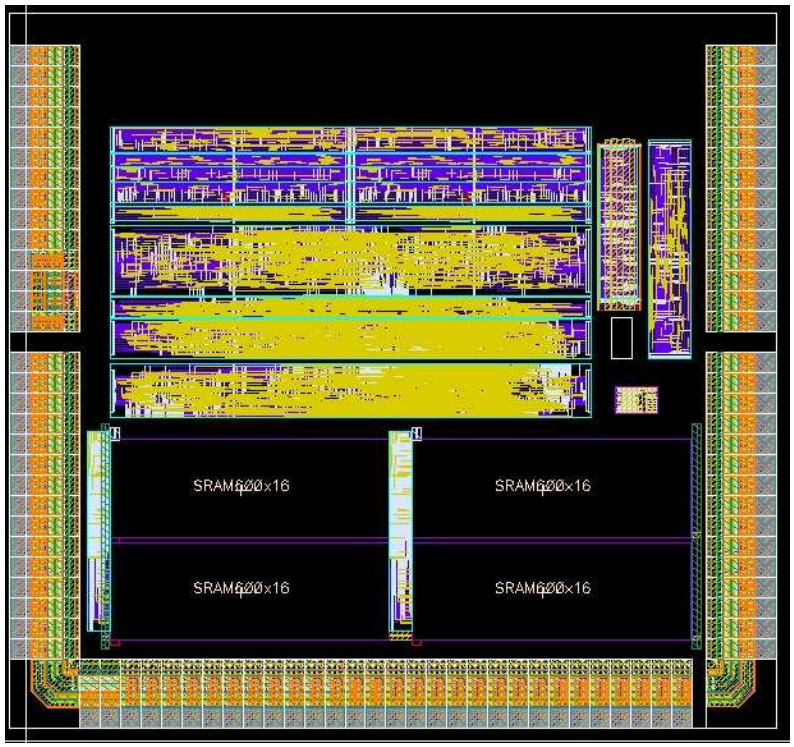


▷▷▷ **Architectures of pixel (integrated CDS) and of full chain made of ”columns ended with integrated discri. ” validated at real scale**

Zero Suppression Micro-Circuit : SUZE-01 Test Results

- **1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :**

  - ⁂ *2 step, raw by raw, logic :*
    - ◇ *step-1 (inside blocks of 64 columns) :*
      identify up to 6 series of $\leq$ 4 neighbour pixels per raw
      delivering signal $>$ discriminator threshold
    - ◇ *step-2 : read-out outcome of step-1 in all blocks*
      and keep up to 9 series of $\leq$ 4 neighbour pixels
  - ⁂ *4 output memories (512x16 bits) taken from AMS I.P. lib.*
  - ⁂ *adapted to 2 $\times$ 64 columns*
  - ⁂ *surface $\sim$ 3.9 $\times$ 3.6 mm^2*

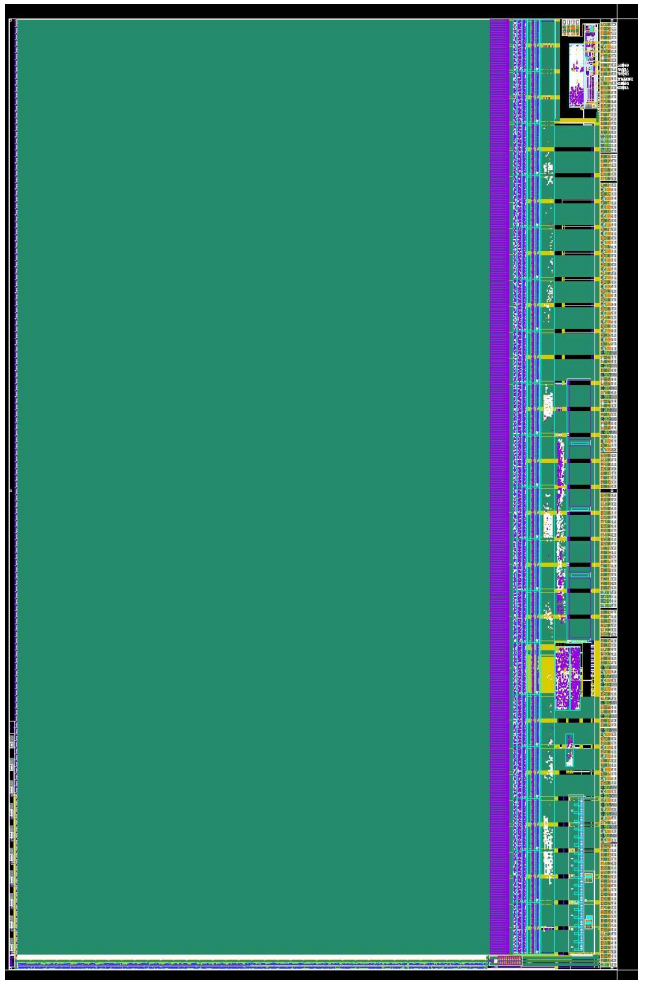


- **Test results summary :**

  - ⁂ *designed & fabricated in '07 $\rightarrowtail$ (lab) tests completed by Spring '08*
  - ⁂ *design performances reproduced up to 1.15 $\times$ design read-out frequency (T_{room}) :*
    noise values as predicted, no pattern encoding error, can handle $>$ 100 hits/frame at rate $>$ 10^4 frames/s

- **Still to do :** *evaluate radiation tolerance (latch-up) of ouput memories*

- **MIMOSA-26 $\equiv$ final sensor for EUDET telescope**
  - **MIMOSA-22 (binary outputs) complemented with $\emptyset$ (SUZE-01)**
  - **Active surface : 1152 columns of 576 pixels (21.2 x 10.6 mm^2)**
  - **Pitch : 18.4 $\mu m \rightarrowtail \sim$ 0.7 million of pixels $\rightarrowtail \sigma_{sp} \gtrsim$ 3.5 μm**
  - **Integration time $\lesssim$ 110 $\mu s \rightarrowtail \sim 10^4$ frames / second**
    $\Rrightarrow$ *suited to $> 10^6$ particles/cm^2/s*
  - *$\emptyset$ in 18 groups of 64 col. allowing $\leq$ 9 "pixel strings" / raw*
  - *Sensor full dimensions : $\sim$ 21 x 12 mm^2*
  - *Data throughput: 1 output at $\geq$ 80 Mbits/s*
    or 2 outputs at $\geq$ 40 Mbits/s

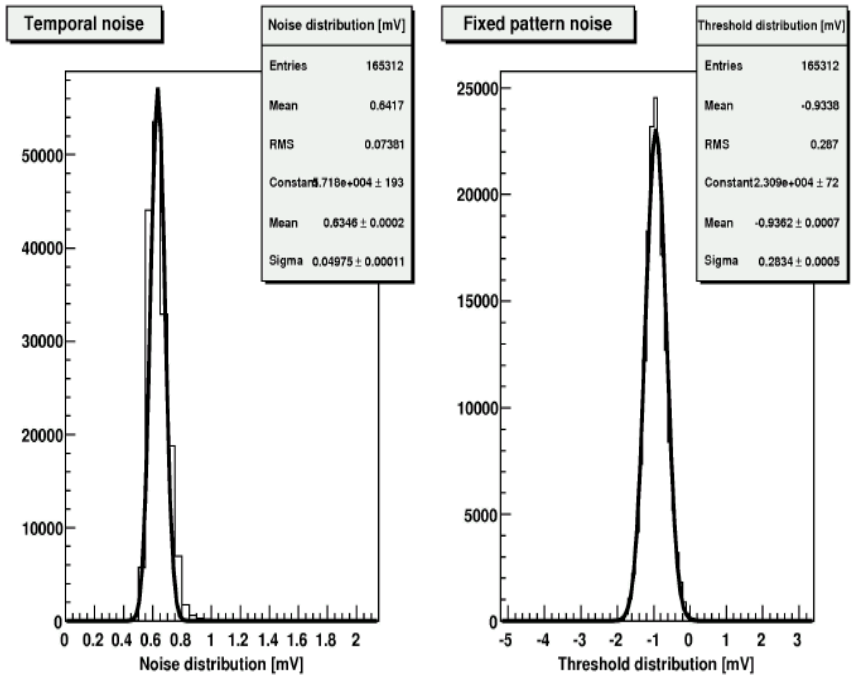


- **Fabricated in AMS-0.35 technology:**
  - Sensor currently being tested $\Rrightarrow$ preliminary test results satisfactory (see next slide)
  - Sensor foreseen to equip several beam telescopes
  - Architecture is baseline for STAR, CBM and ILC vertex detectors

MIMOSA-26 ≡ final sensor for EUDET telescope

- **9 sensors mounted on interface board and tested with/without ^{55}Fe source**
- *Noise performance assessment performed separately for each of the 4 groups of 288 columns, at nominal r.o. speed*
- *Typical value of pixel (i.e. temporal noise) ∼ 0.6–0.7 mV*
- *Typical value of FPN (discriminator) noise ∼ 0.3–0.4 mV*
- *Results are ∼ identical to MIMOSA-22 values*
- *∅ logic seems to work as foreseen*

⇛ **Sensor seems operational at nominal speed**



Next steps :

- Characterise simultaneously all 4 groups of columns together
- Run several sensors on EUDET beam telescope at CERN-SPS (Summer ’09)
- Radiation tolerance
- Yield ⟼ stitching ?

From MIMOSA-26 to the ILC Design

- **Move from AMS-0.35 μm to feature size $\leq$ 0.18 μm**

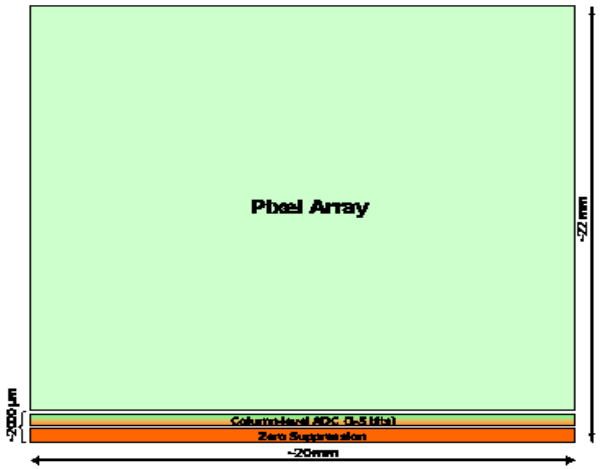
  $\Rightarrow$ improved clock frequency, more metal layers, more compact peripheral circuitry, etc.

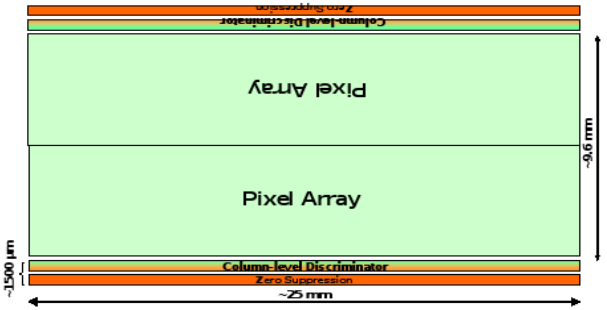
- **Outer layers (t$_{int} \sim$ 100 μs) :**

  - pitch $\lesssim$ 35 μm (need phys. studies)
  - 4-bit ADC $\Rightarrow$ $\sigma_{sp} \sim 3\ \mu m$
  - 576 col. of 576 pixels $\Rightarrow$ 2x2 cm^2

- **Inner layers (t$_{int} \sim$ 25 - 50 μs) :**

  - double-sided r.o. $\Rightarrow$ twice shorter (= faster) columns
  - pitch $\lesssim$ 15 μm
  - binary r.o. $\Rightarrow$ $\sigma_{sp} \lesssim 3\ \mu m$
  - 1600 columns of 320 pixels $\Rightarrow$ $\lesssim$ 24x0.95 mm^2

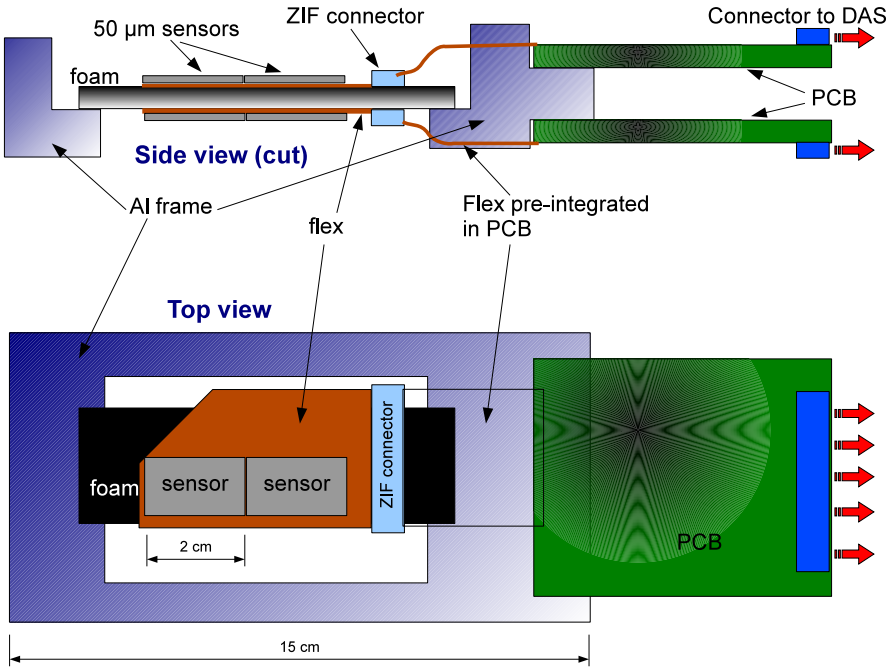




System Integration : PLUME Project

PLUME project ≡ Pixelised Ladder using Ultra-light Material Embedding

- Goals : ◇ achieve a double-sided ladder prototype by 2012
  ◇ evaluate benefits of 2-sided concept (mini-vectors) : σ_{sp}, alignment, shallow angle pointing
- Bristol - Oxford - Strasbourg (BOS) collaboration (synergies with Frankfurt/CBM)



1st step (2009) :

- 2 pairs of MIMOSA-20 sensors (4x1 cm^2, 50 μm thin)
  mounted on flex cable, assembled on SiC (8 %) support
- total material budget $\sim$ 0.5 % X_0

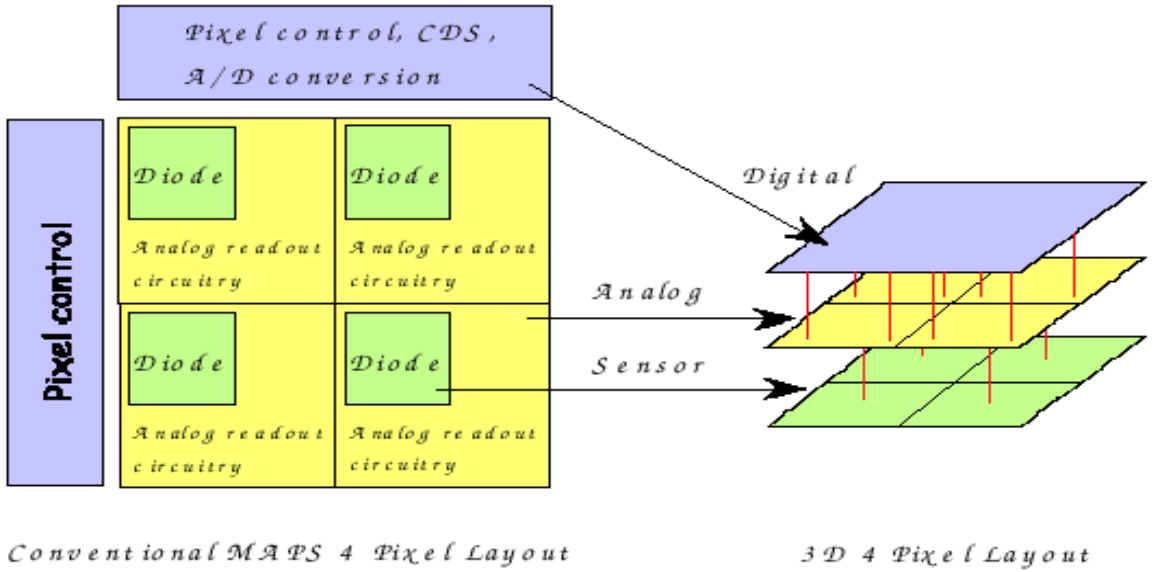
SiC foam	sensors	glue	flex
0.09 %	0.11 %	0.02 %	0.29 %

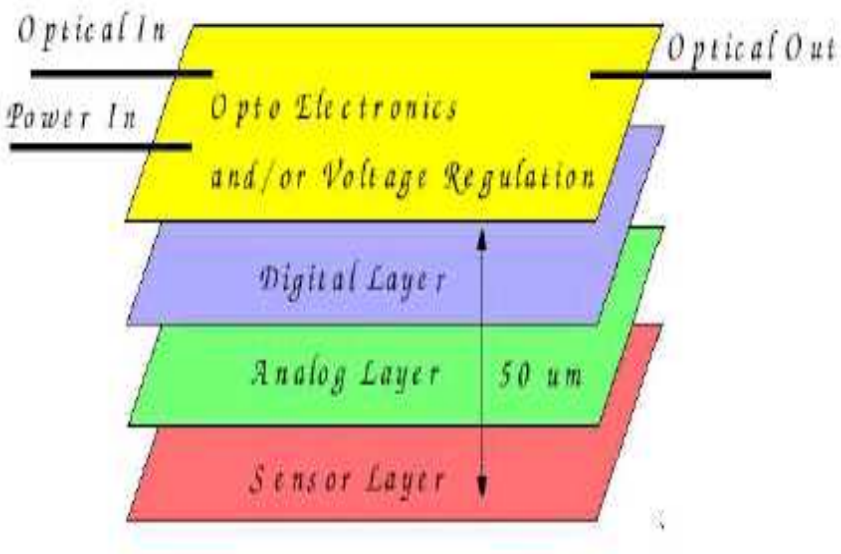
- beam tests at CERN-SPS in Novembre

2nd step (2009 – 2012) :

- 2 series of 6 MIMOSA-26 sensors (12.5x1 cm^2, 50 μm thin)
  mounted on flex cable, assembled on SiC support
- total material budget $\gtrsim$ 0.2 % X_0 (stitching ???)
- prototype for innermost layer

- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - *combine different fab. processes*
  - *alleviate constraints on transistor type inside pixel*
- **Split signal collection and processing functionnalities :**
  - *Tier-1: charge collection system*
  - *Tier-2: analog signal processing*
  - *Tier-3: mixed and digital signal processing*
  - *Tier-4: data formatting (electro-optical conversion ?)*
- **Use best suited technology for each Tier :**
  - *Tier-1: epitaxy (depleted or not), deep N-well ?*
  - *Tier-2: analog, low I_{leak}, process (nb of metal layers)*
  - *Tier-3 & -4 : digital process (nb of metal layers), feature size $\rightarrowtail$ fast laser (VOCSEL) driver, etc.*





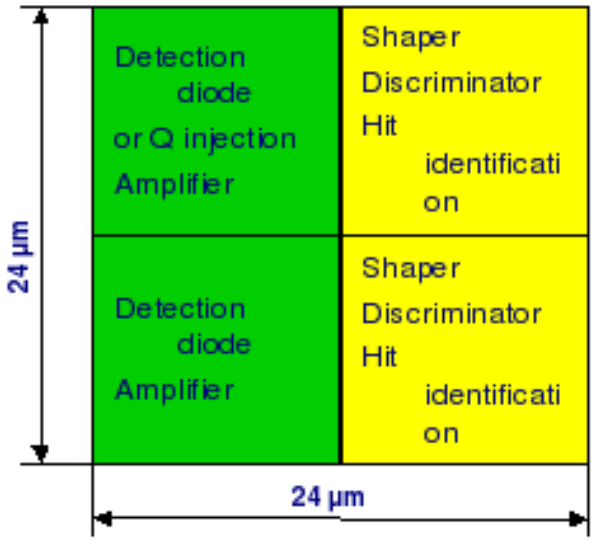
Ex: Delayed R.O. Architecture for the ILC Vertex Detector

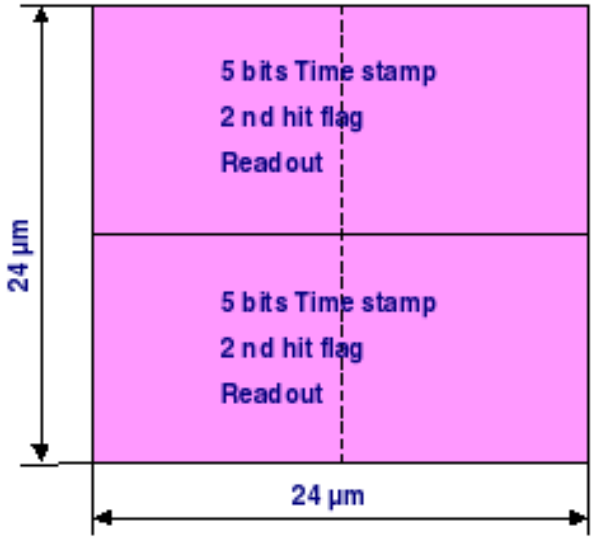
- **Run in Chartered - Tezzaron technology**
  - *2-Tier run with "high-res" substrate (allows m.i.p. detection)*
    $\Rightarrow$ *3-Tier architecture compactified in 2-Tier chip*
  - *feature size = 130 nm* $\Rightarrow$ *design foreseen for smaller feature size*
- **Try 3D architecture based on small pixel pitch, motivated by :**
  - $< 3\ \mu m$ *single point resolution with binary output*
  - *probability of* > 1 *hit per train* $<<$ *10 %*

$\Rightarrow$ *12* μm *pitch :* $\sigma_{sp} \gtrsim 2.5\ \mu m$ & $\lesssim$ *5 % proba. of* > 1 *hit/train*

- **Split signal collection and processing functionnalities :**
  - *Tier-1A: sensing diode & amplifier*
  - *Tier-1B: shaper & discriminator*
  - *Tier-2: time stamp (5 bits) + overflow bit & read-out* $\rightarrowtail$ *delayed r.o.*
- **Architecture prepares for 3-Tier perspectives :**
  - *Tier-1: CMOS process adapted to charge collection*
  - *Tier-2: CMOS process adapted to analog & mixed signal processing*
  - *Tier-3: digital process (*$<<$ *100 nm ????)*

Tier-1





Tier-2

Other ex. of chips designed in Chartered - Tezzaron technology for ILC

- FAST **architecture aiming to minimise power consumption** *(IRFU/Saclay)* **:**
  - ⁂ *subdivide sensitive area in "small" matrices running* INDIVIDUALLY *in rolling shutter mode*
  - ⁂ *adapt the number of raws to required frame r.o. time*

    $\Rrightarrow$ *few* μs *r.o. time may be reached (???)*

- **Combine 2-Tier read-out chip with Tier hosting sensitive volume :**
  - ⁂ *Tier-1: XFAB-0.6 (depleted epitaxy)* $\rightarrowtail$ *signal sensing volume*
  - ⁂ *Tier-2 /-3 : Chartered* $\rightarrowtail$ *signal processing micro-circuits*
  - ⁂ *adapted to fast (few* μs*), low occupancy, particle detection (small sub-arrays in projective geometry)*

- **Memory tolerant to SEU & SEL** *(CMP/Grenoble)*

Sensor r.o. architecture :

- final sensor for EUDET telescope (MIMOSA-26) fabricated
  (0.7 Mpix, $t_{int} \sim 110\ \mu s$, binary output with integrated $\emptyset$, $\sigma_{sp} \gtrsim 3.5\ \mu m$)
- preliminary lab test results confirm functionning with expected noise performances
- if beam test results satisfactory (Summer), the design will be adapted to required VTX performances
  $\hookrightarrow$ $t_{int} \sim$ 25–50 μs (2-sided r.o. for inner layers) & $\sim 100\ \mu s$ (1-sided r.o. for outer layers)
- Plan : move to 0.18 μm technology (6 metal layers, more compact circuitry, faster, etc.)

Sensor integration $\rightarrowtail$ PLUME project :

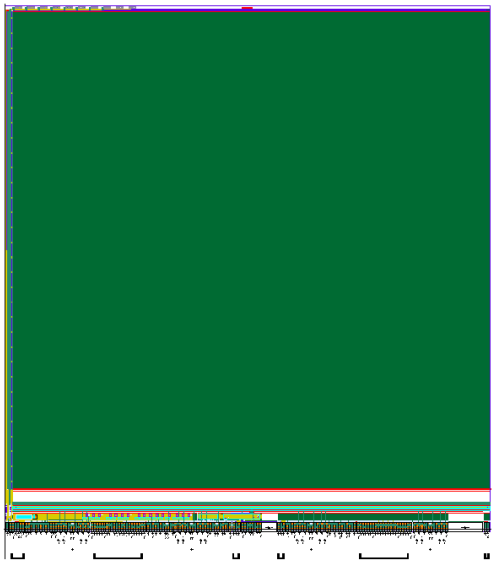
- by 2012 : double-sided ladder equipped with 2 x 6 MIMOSA-26 sensors
  (active area $\sim$ 2 x 12.5x1 cm^2, mat. budget $\gtrsim$ 0.2 % X_0)
- 2009 : 1st proto. with 2x2 MIMOSA-20 sensors mounted on flex cable and SiC ($\sim$ 0.5 % X_0 in total)
  $\rightarrowtail$ tests at CERN-SPS in Novembre

3D sensors (Chartered-Tezzaron) :

- 3 different sensors under devt : delayed r.o. with latch, fast rolling shutter, 3-Tier mixed CMOS
- submission within $\sim$ 2 weeks $\Rightarrow$ test results in Autumn

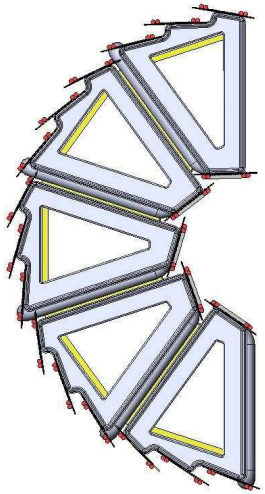
1st generationsesnor for the HFT-PIXEL of STAR (PHASE-1):

- **full scale extension of MIMOSA-22 (no $\emptyset$)**
- *640x640 pixels (30 μm pitch) $\Rrightarrow$ active surface : 19.2 x 19.2 mm^2*
- *integration time : 640 μs*
- *designed and fabricated in 2008 $\rightarrowtail$ currently under test at LBNL*
- *3 + 9 ladders to equip with 10 sensors thinned to 50 μm (1/4 of PIXEL)*
- *1st physics data in 2010 (?)*



Final HFT-PIXEL sensor :

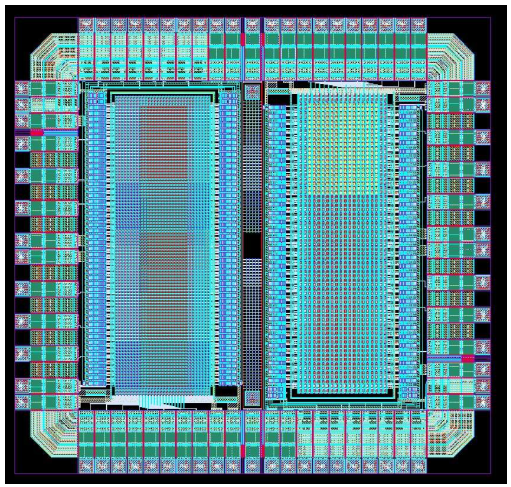
- **MIMOSA-26 with active surface $\times$ 1.8 & improved rad. tolerance**
  - $\hookrightarrow$ *1152 col. of 1024 pixels (21.2 x 18.8 mm^2)*
- **Pitch : 18.4 μm $\rightarrowtail$ $\sim$ 1.1 million pixels**
- **Integration time $\sim$ 200 μs**
- *Design in 2009 $\rightarrowtail$ fab. end 2009*
  - $\rightarrowtail$ *1st physics data expected in 2011/12*

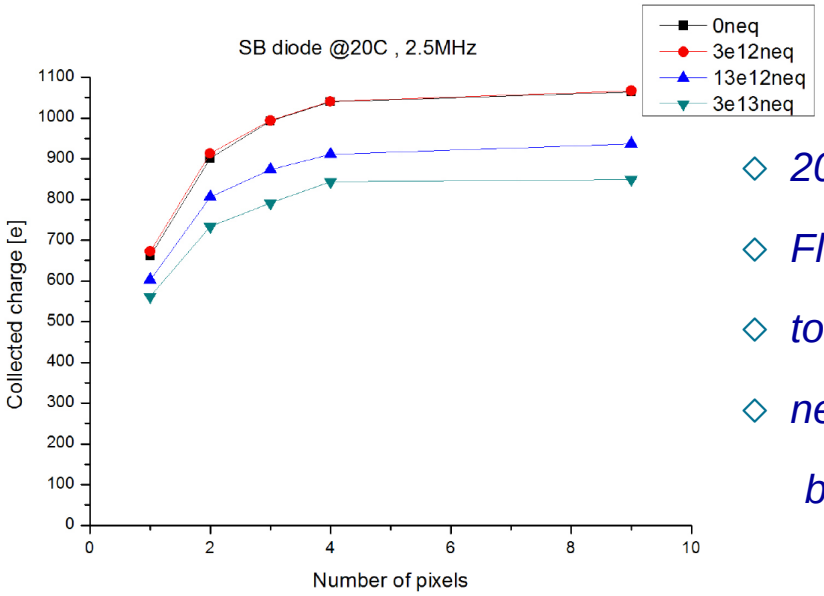


Exploration of New CMOS Technology

- **Advantages :**
  - ⁂ *faster charge collection ($<$ 10 ns) $\Rightarrow$ faster frame read-out frequency*
  - ⁂ *shorter minority charge carrier path length $\Rightarrow$ improved tolerance to non-ionising radiation*

- **Exploration of XFAB-0.6 μm techno:** $\sim$ 15 μm thick epitaxy ; $V_{dd} \leq 5$ V ; $\rho \sim O(10^3)\Omega \cdot cm$
  - ⁂ *MIMOSA-25 : fabricated in 2008 & tested with ^{106}Ru (β) source before/after O(1 MeV) neutron irradiation*





- ◇ *20 μm pitch, + 20°C, 160 μs r.o. time*
- ◇ *Fluence $\sim$ 0.3 / 1.3 / 3·10^{13} n_{eq}/cm^2*
- ◇ *tolerance improved by $>$ 1 order of mag.*
- ◇ *need to confirm ϵ_{det} (uniformity !) with beam tests (CERN-SPS in May '09)*

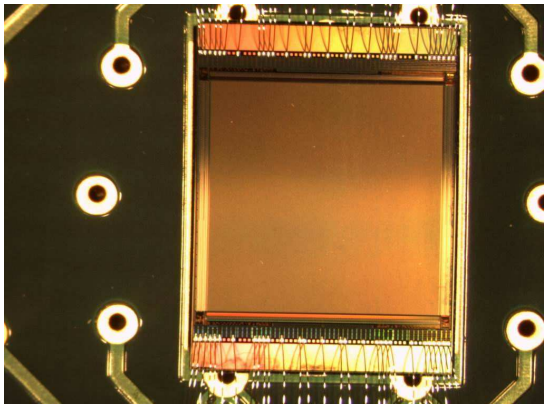
- **Exploration of a new VDSM technology with depleted substrate :**

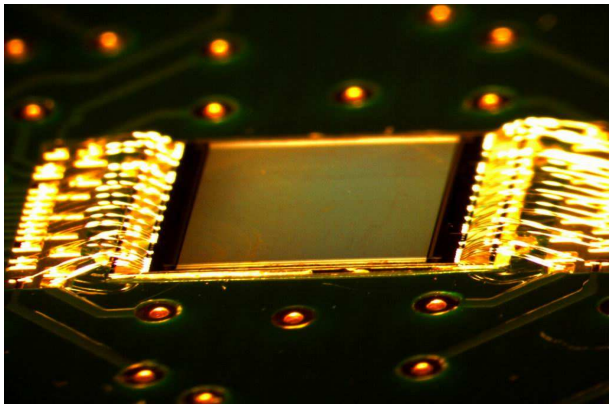
  project driven by CERN for SLHC trackers *(also attractive for CBM. ILC and CLIC Vx Det.)*

  - ⁂ *1st prototypes by the end of 2009*
  - ⁂ *thinning and post-processing of substrate ?*

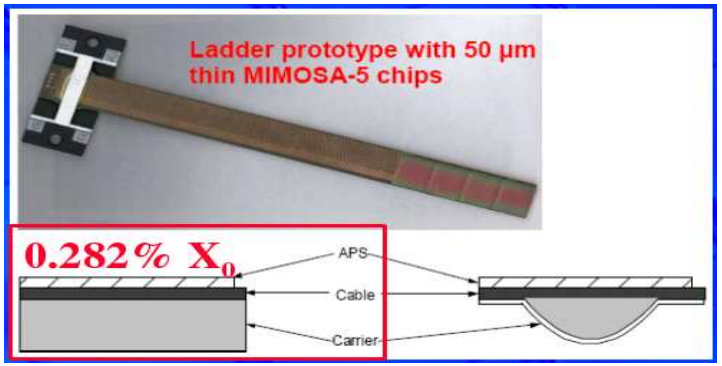
System Integration

- **Industrial thinning (via STAR coll. at LBNL)** $\rightarrowtail$ *MIMOSA-18 (5.5×5.5 mm^2 thinned to 50 μm)*





- **Devt of ladder equipped with MIMOSA chips (coll. with LBL) :** *STAR ladder ($\lesssim 0.3\ \%\ X_0$) $\rightarrowtail$ ILC ($< 0.2\ \%\ X_0$)*



- **Perspectives ?**
  - ※ accessibility of industrial thinning + post-processing of ”high-res” substrate
  - ※ stitching $\Rightarrow$ alleviates material budget of flex cable