Silicon tracking DAQ

Still preliminary thoughts on all DAQ parts but the first one (FEE)

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This work is performed within the SiLC R&D collaboration and with partial support from E.U. I3-FP6 EUDET project

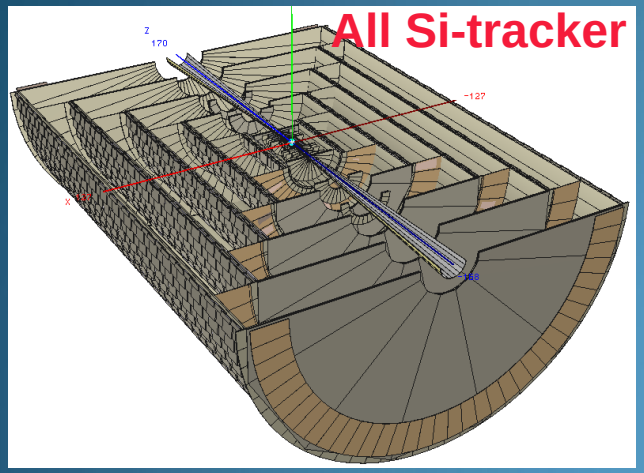
LCWS'08 Workshop at UIC Chicago, November 18 2008

TOPICS

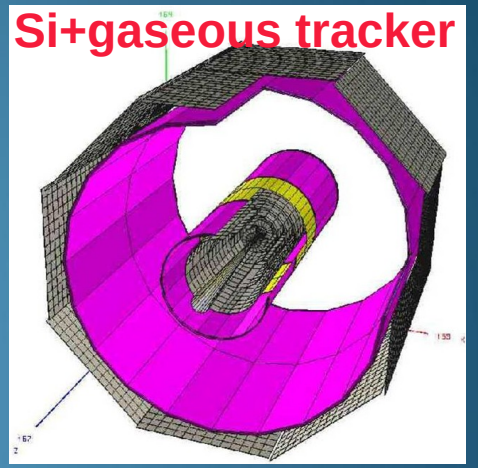
- SILICON TRACKING DAQ: 3 LEVELS
- LEVEL 1: on the chip
- LEVEL 2: on the detector sides
- LEVEL 3: in the Control Room
- Towards developing this DAQ architecture:
  the first steps

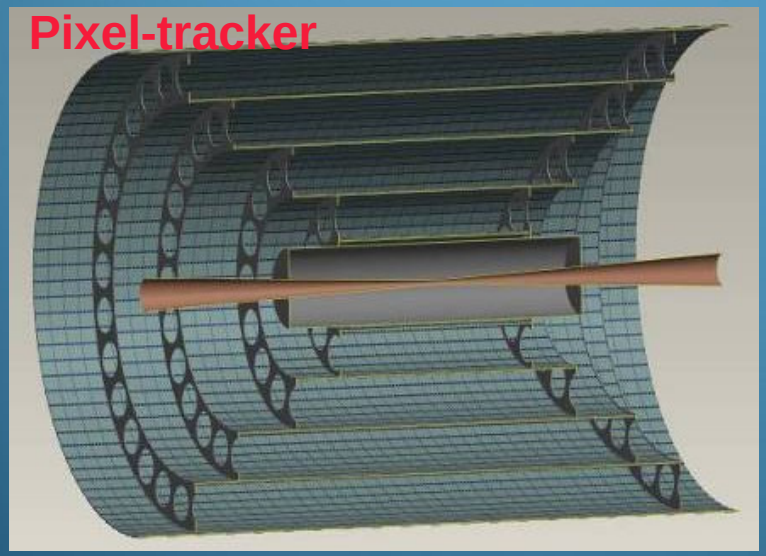
PRELIMINARY WARNING

This is developed within the SiLC collaboration, a transversal R&D collaboration:



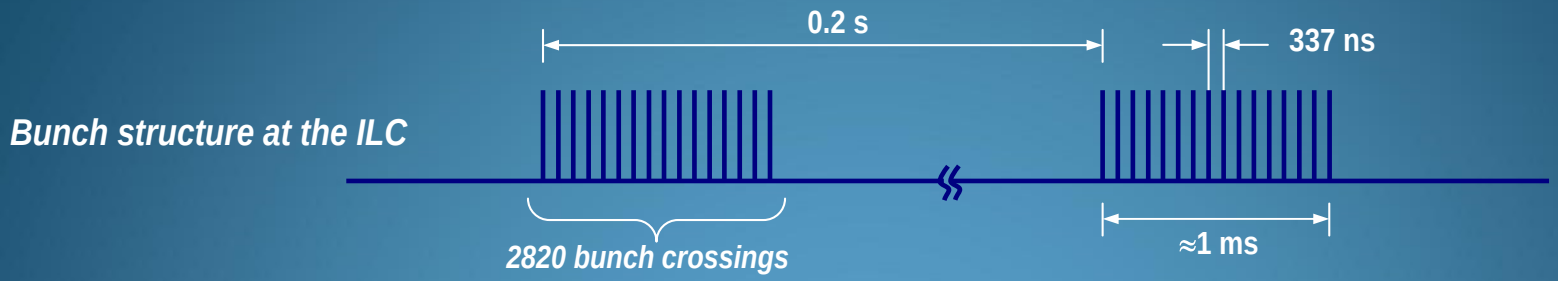
All what is presented here apply to ***any Si tracking system for ILC, made with strip sensors*** and representing a few 10**6 channels to be read out and processed





Not applied (yet)! to a all pixel large area Si tracking (30 x 10**9 pixel channels)

THE TIME WE ARE GIVEN....if ILC



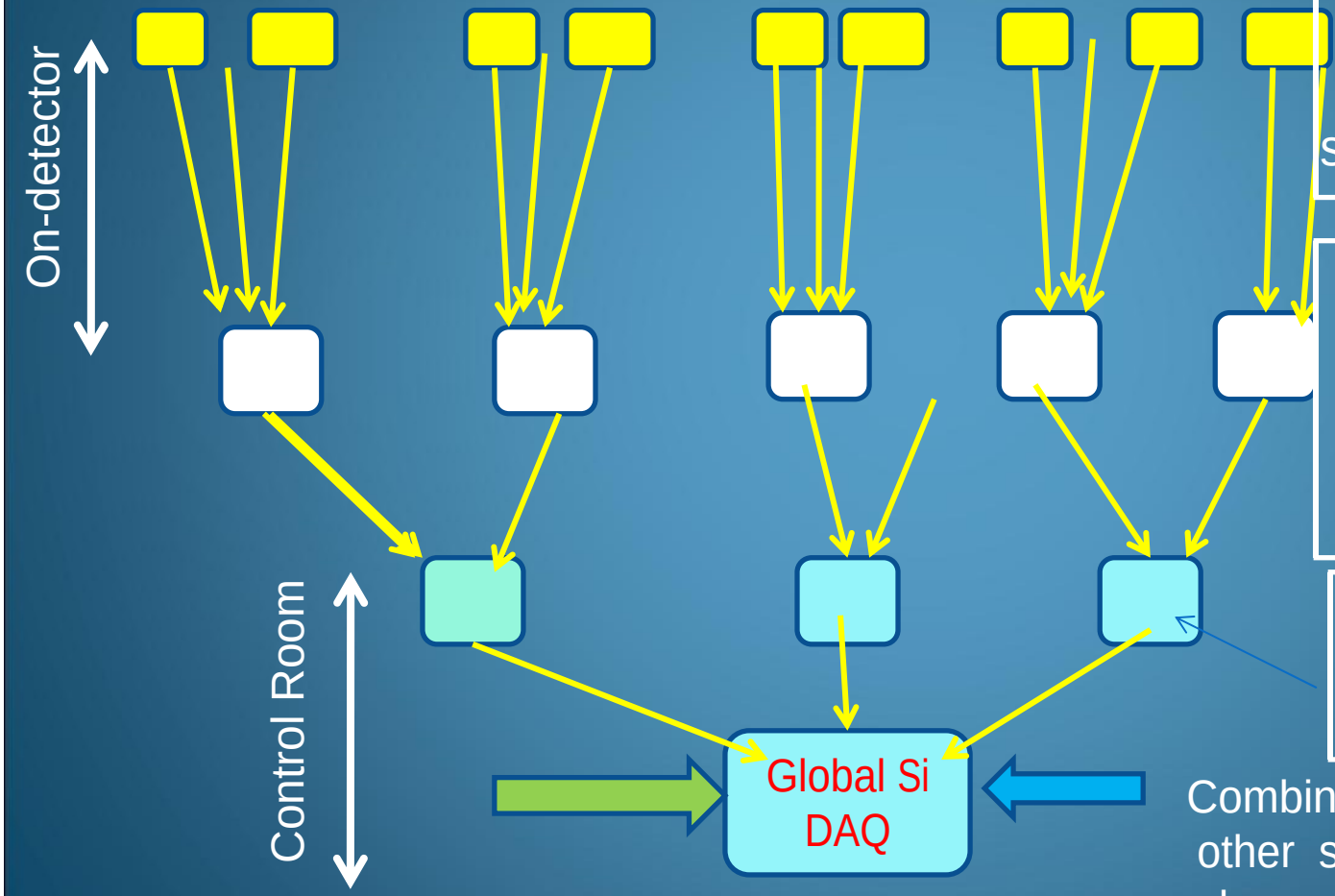
HOW DO WE USE IT?

- numerical oscilloscopy
- storing
- zero suppressing

THEN:

- A/ D conversion
- power cycling
- calibrating (?)

Si Tracking DAQ architecture into 3 Levels



L 1: chip on sensor, Full read out chain in a single chip (A/D, zero suppress, multiplexing)

L2: on detector sides, daisy chaining chips information from chips, buffering, preprocess, interface/outside world

L3: in control room, processing /azimuthal sector, trk reconstruct.

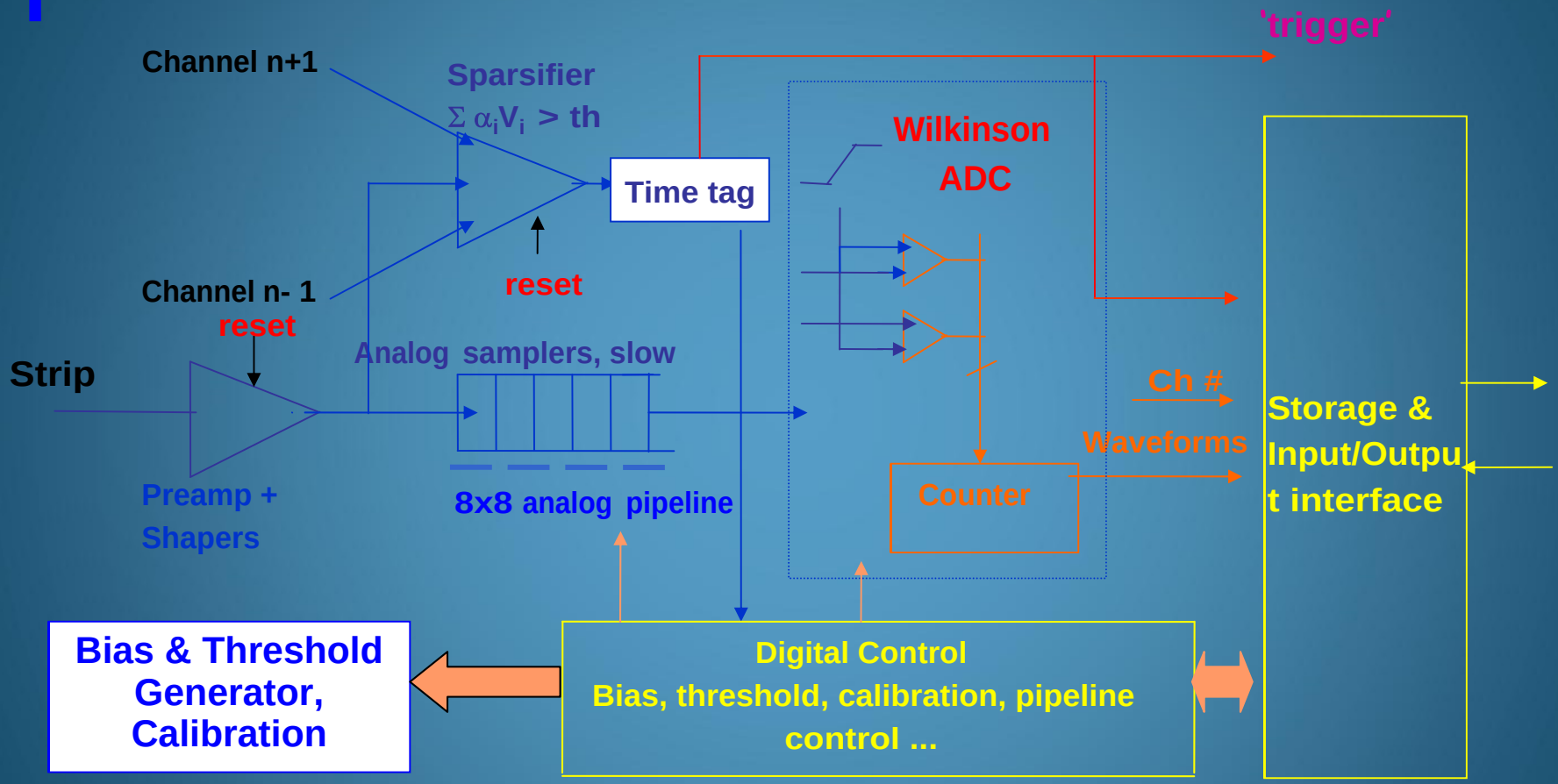
Combine with Information from other sub-detectors, handling slow control for all Si TrK system

Silicon tracking DAQ Level 1: F.E. chip on-detector = ELEMENTARY & CRUCIAL PIECE of the DAQ, it does it all (almost!!)

(University of Barcelona and LPNHE-UPMC/IN2P3-CNRS)

more details on the FEE at the tracking session

General view of the circuit



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Main features of new circuit

88 channels (1 test channel): Preamplifier, shaper, sparsifier, analogue pipeline (8x8 cells), 12 bits ADC

2D memory structure: 8x8/channels

Fully digital control:

- Bias voltage(10 bits) and current (8 bits)
- Power cycling (can be switched on and off)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration (fully programmable 10 bits DAC)
- Sparsifier threshold programmable per channel
- Event tag and time tag generation

=> High fault tolerance

=> High flexibility, robustness

.....

2 Trigger modes: Internal (Sparsification integrated)

External (LVTTL) for beam test

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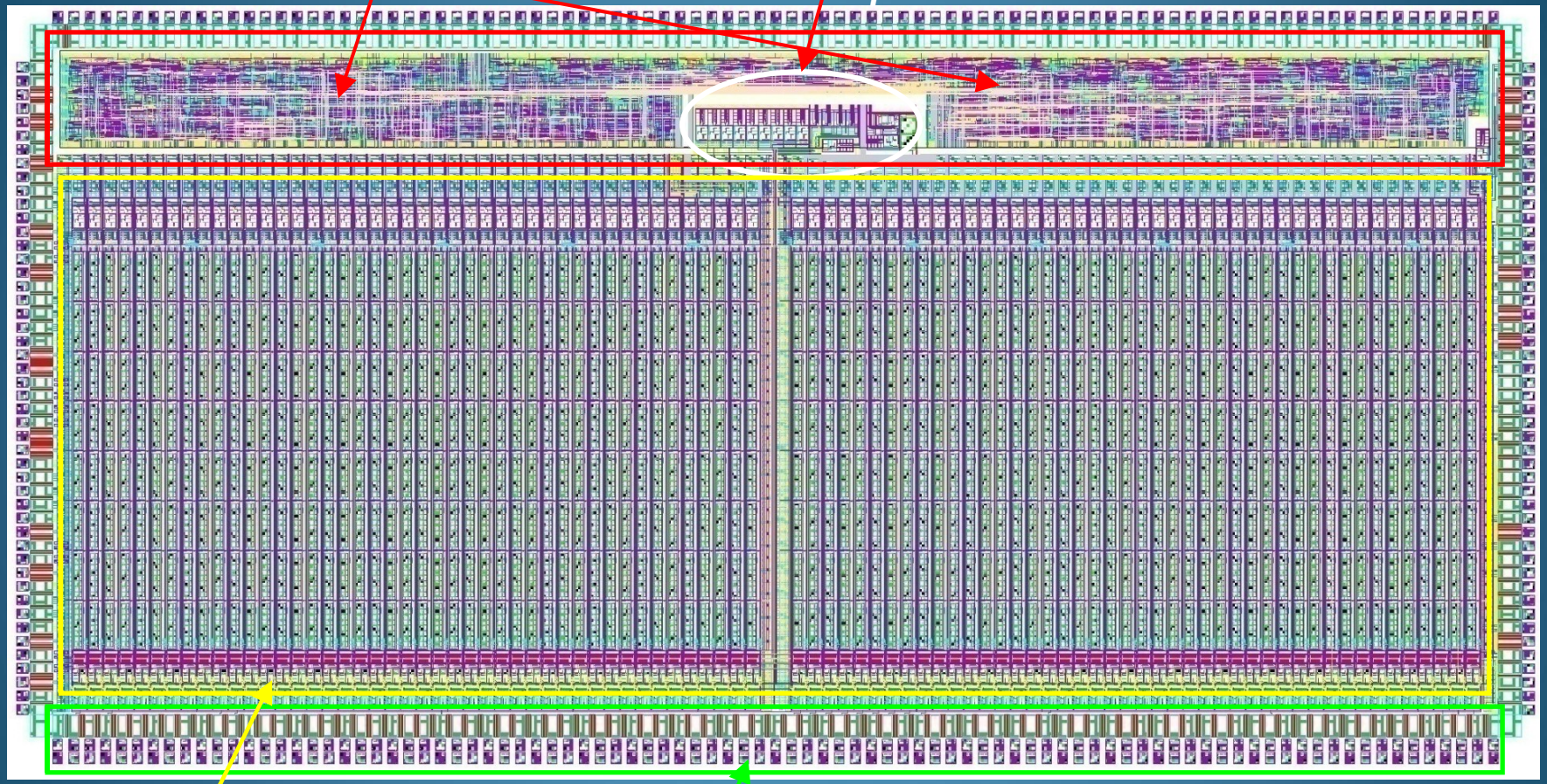
FE chip LAYOUT

Digital part 91 I/O digital (power supplies, clock, tests, serial I/O)

Common power control

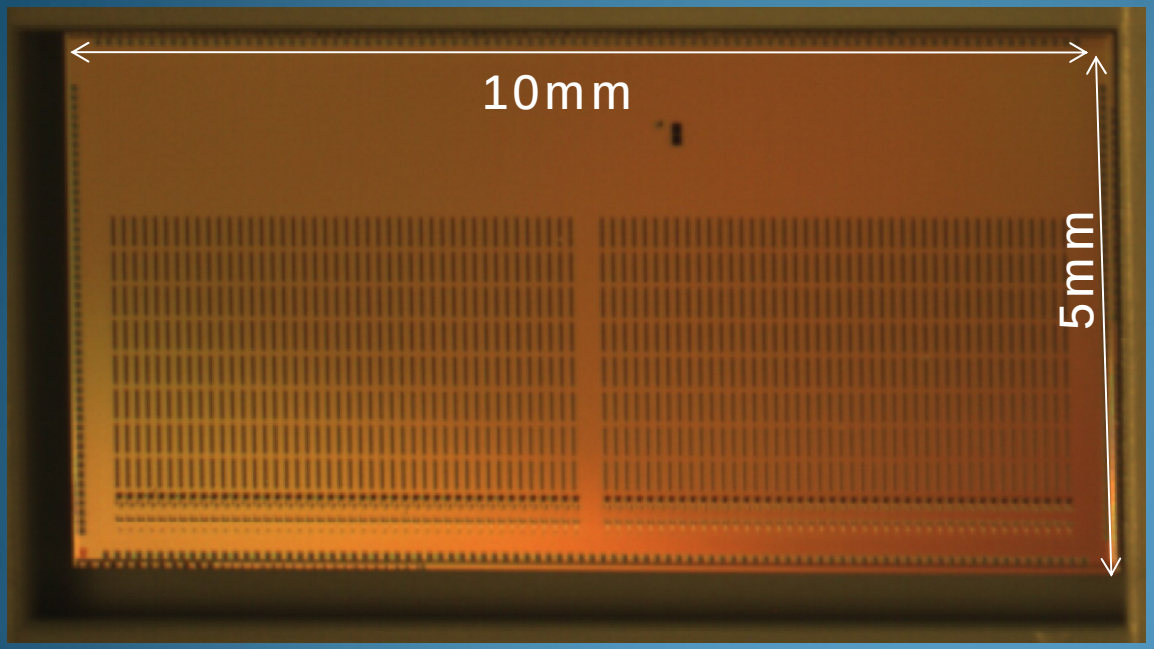


Analogue part

88 strip inputs +2 power suplies + one ground

THE PRESENT CHIP PROTOTYPE SiTR_130-88 includes all the complete desired functionality

FE chip PHOTOGRAPH



Photograph of the new chip SiTR_130-88

Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

Analogue: 9.5mmx3.5mm
Digital : 9.5mmx700um

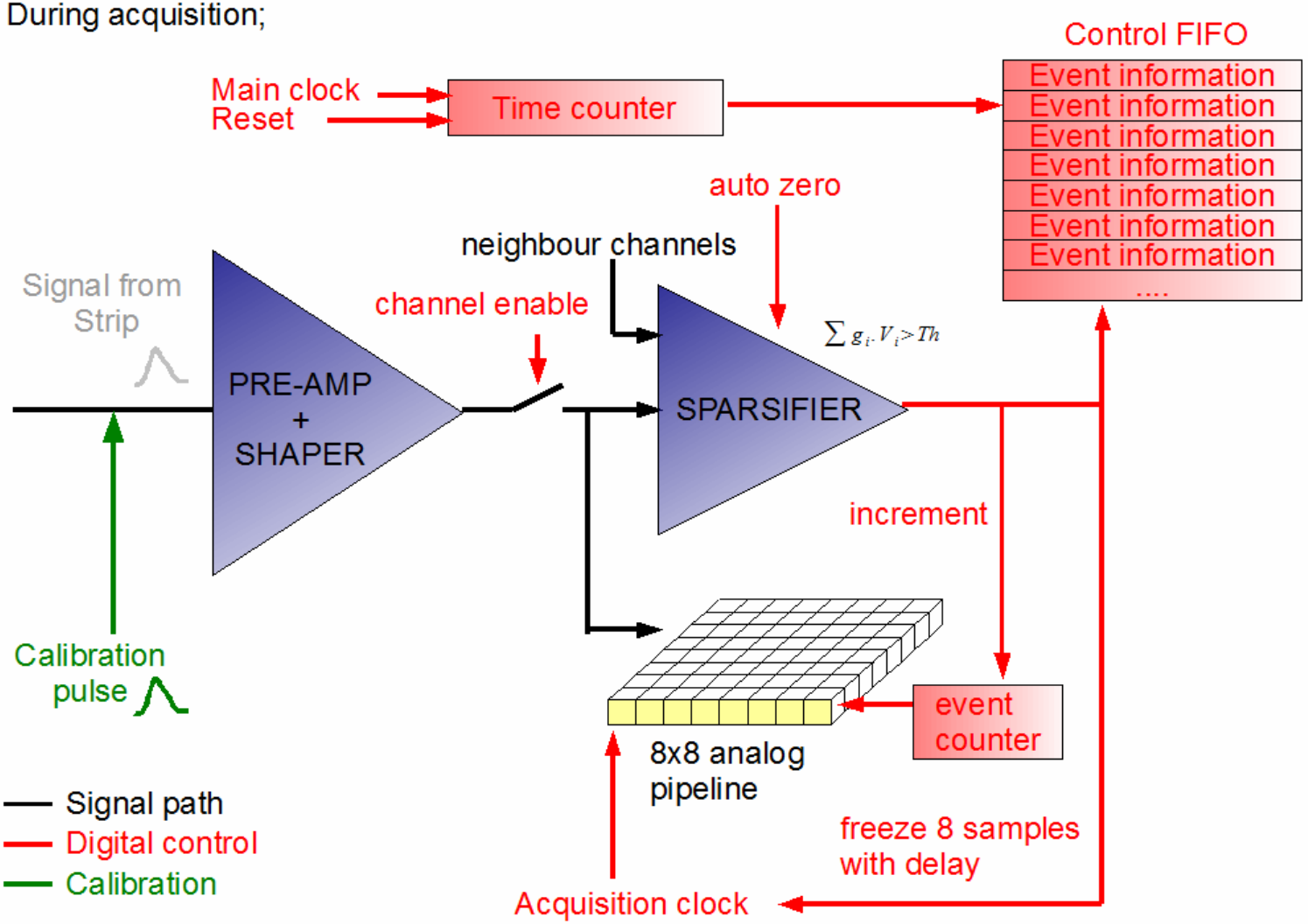
Submitted June 24th '08, received September 12 the naked chips (60),

- FEE is full custom and DSM CMOS technology (now 130nm soon 90 nm will be tried)

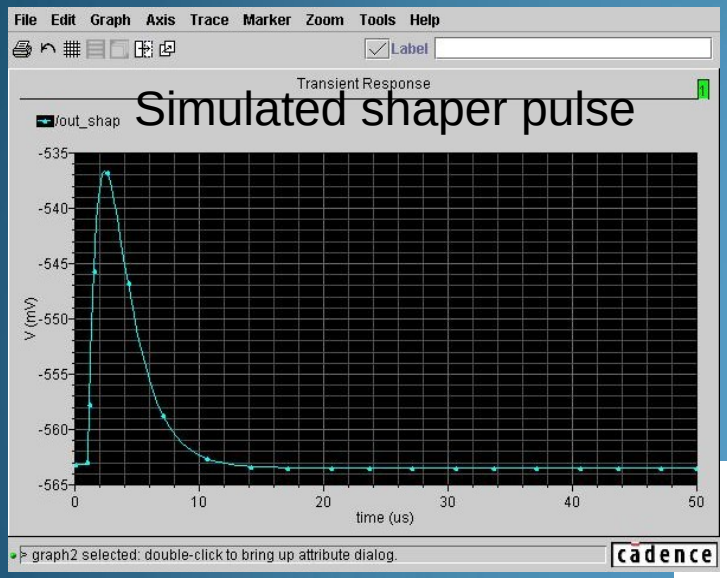
- Crucial and novel solution for direct interconnection of the chip on detector present: bump bonding for strips (as for pixels) soon trying 3D vertical interconnect

- For the rest of the DAQ: look AMAP for solutions available on the market

During acquisition;

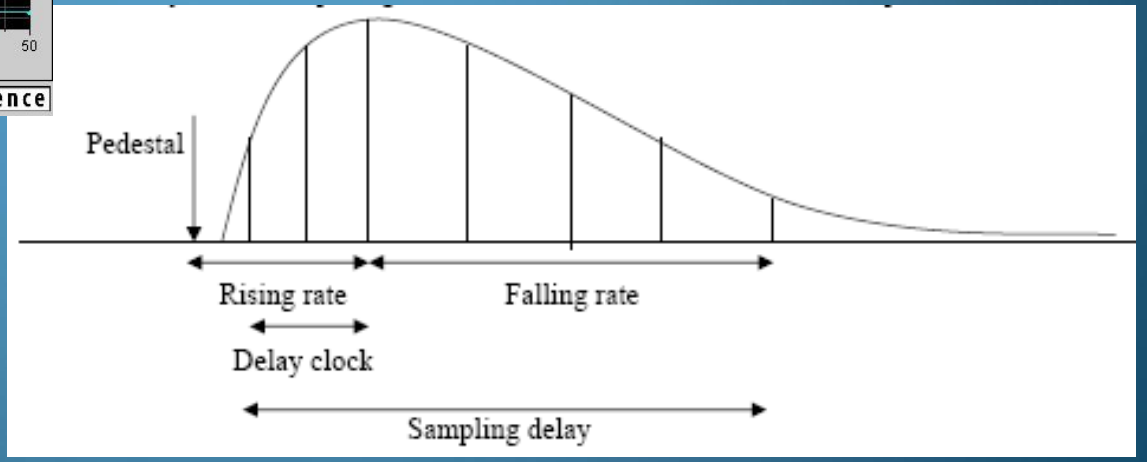


Sampling and conversion time:
All the 88 channels of the chip are converted in parallel.
There are 8x8 samples to be converted per channel; the conversion time per channel
Is approximately 85 μs thus a total of 5.44 ms is needed for the conversion

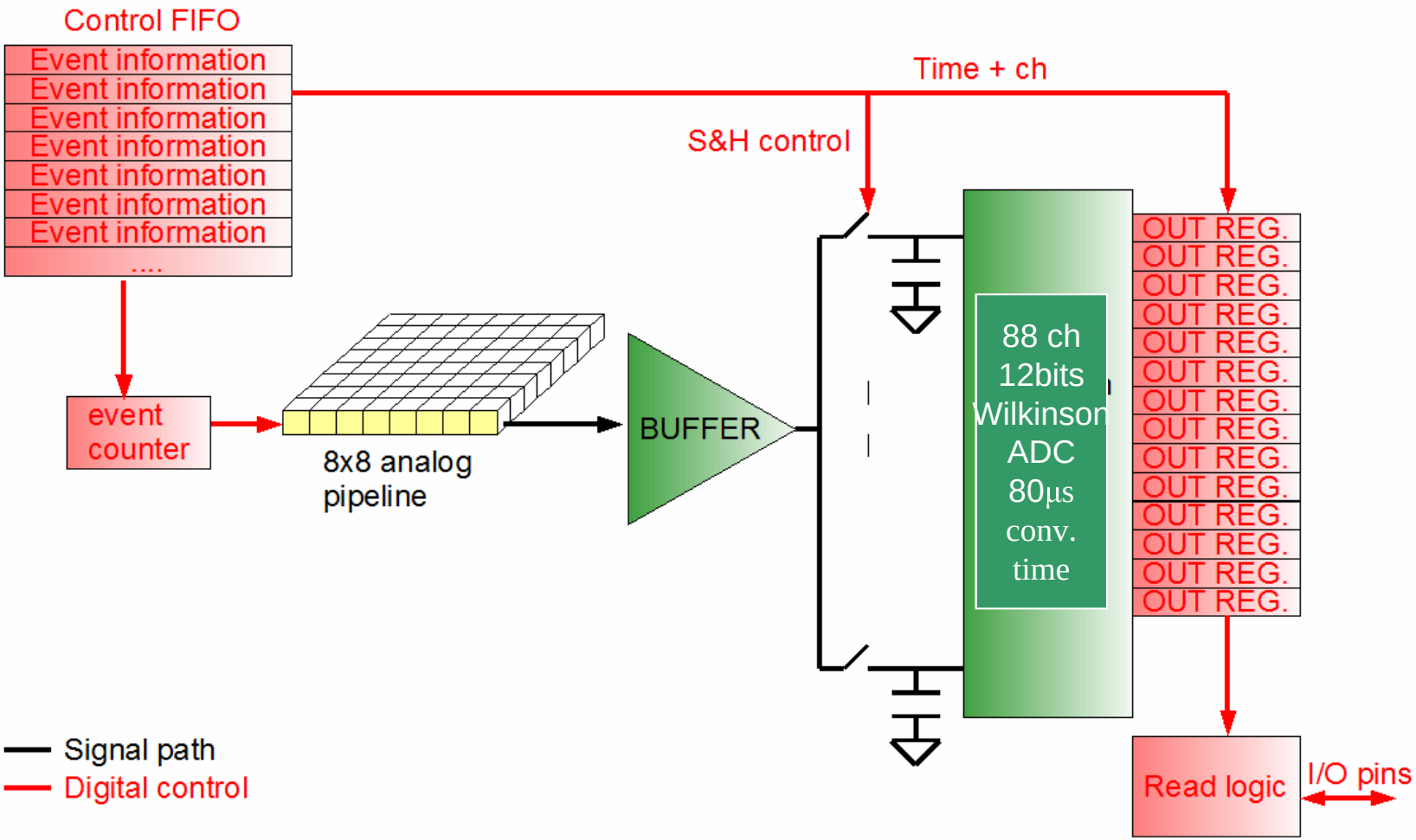


Simulated shaper pulse

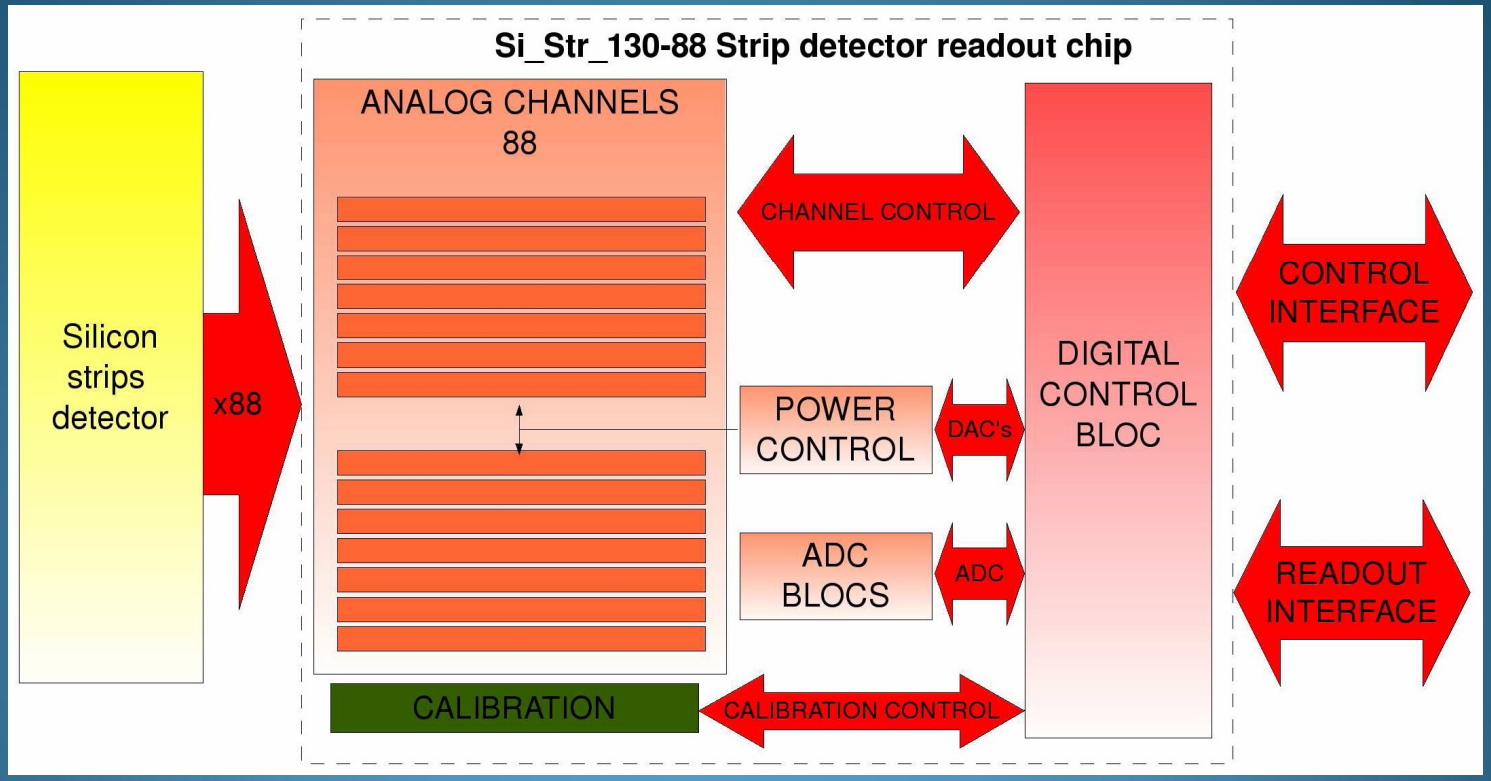
Reconstruction of the pulse height: 8 samples including pedestal



During IDLE time;



Level 1: System overview

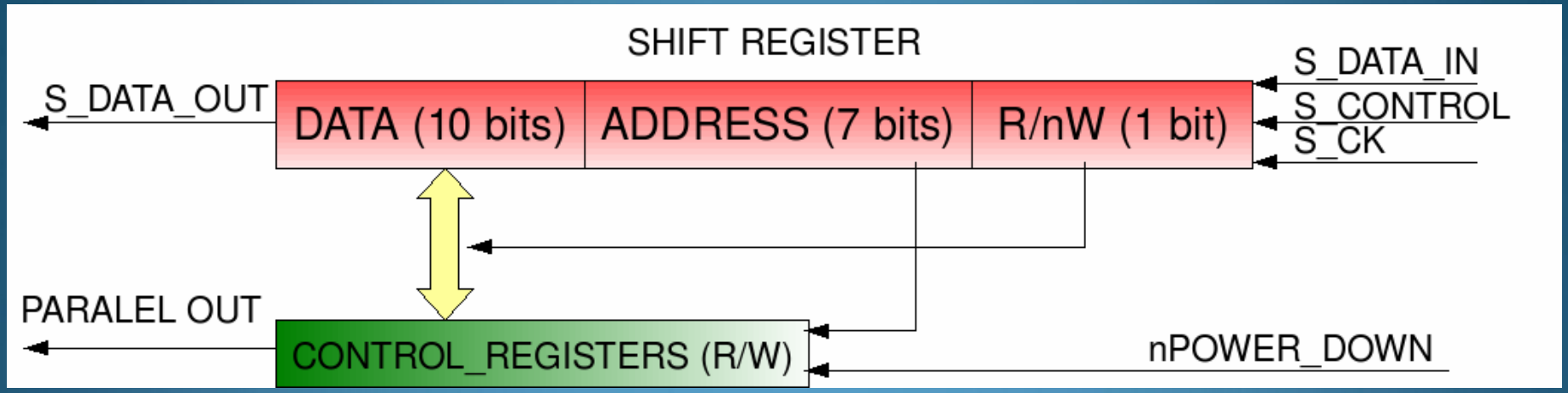


The digital part has been designed to match with the analogue part
It includes 3 main blocks:

=> The control and configuration interface
=> The acquisition control
=> The readout block

Hierarchy between the 3 elements:
The acquisition control gives control signals to the others to allow some operations
BUT: The other two have however some independence in operations between them

STR_130-88: Control and configuration Interface block

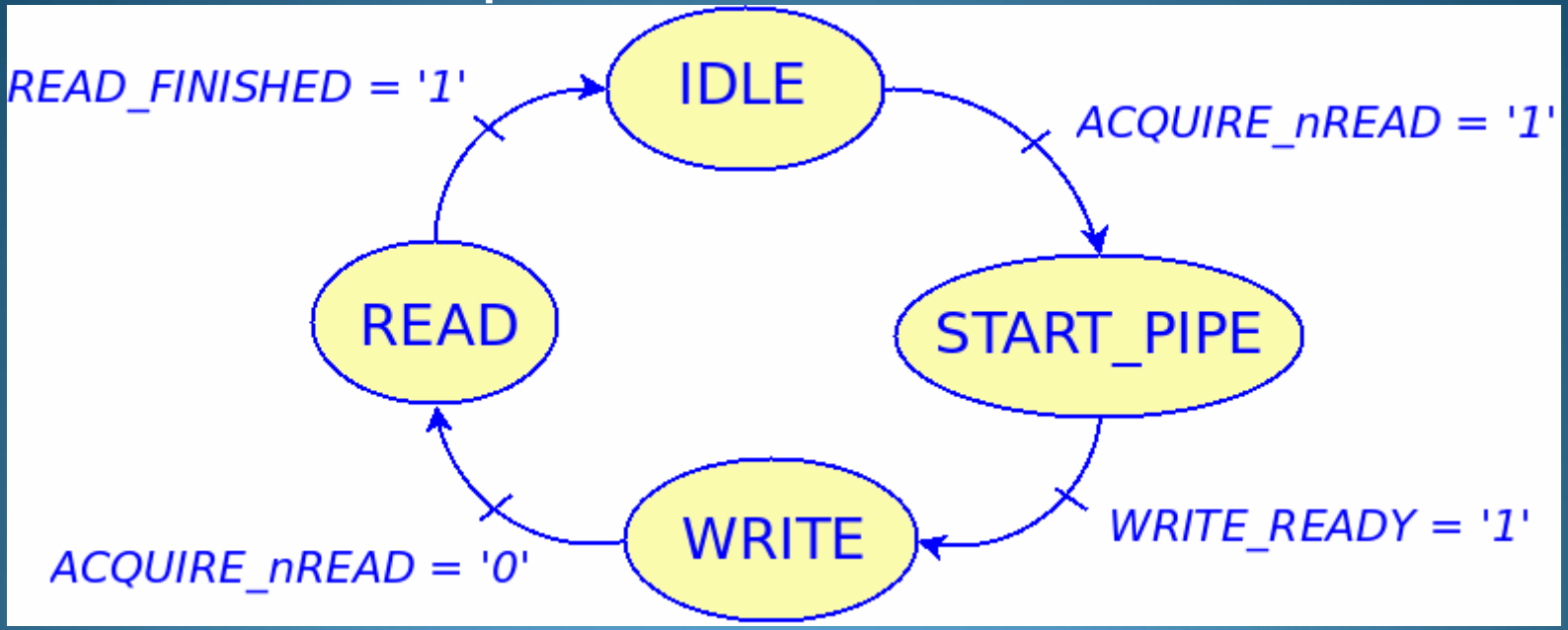


The control and configuration interface block uses a serial interface to read or write values to/from internal registers

It enables multiple devices to be controlled in a daisy chain configuration.

The total number of registers is 98, storing the configured values in 10 bits

Acquisition control block

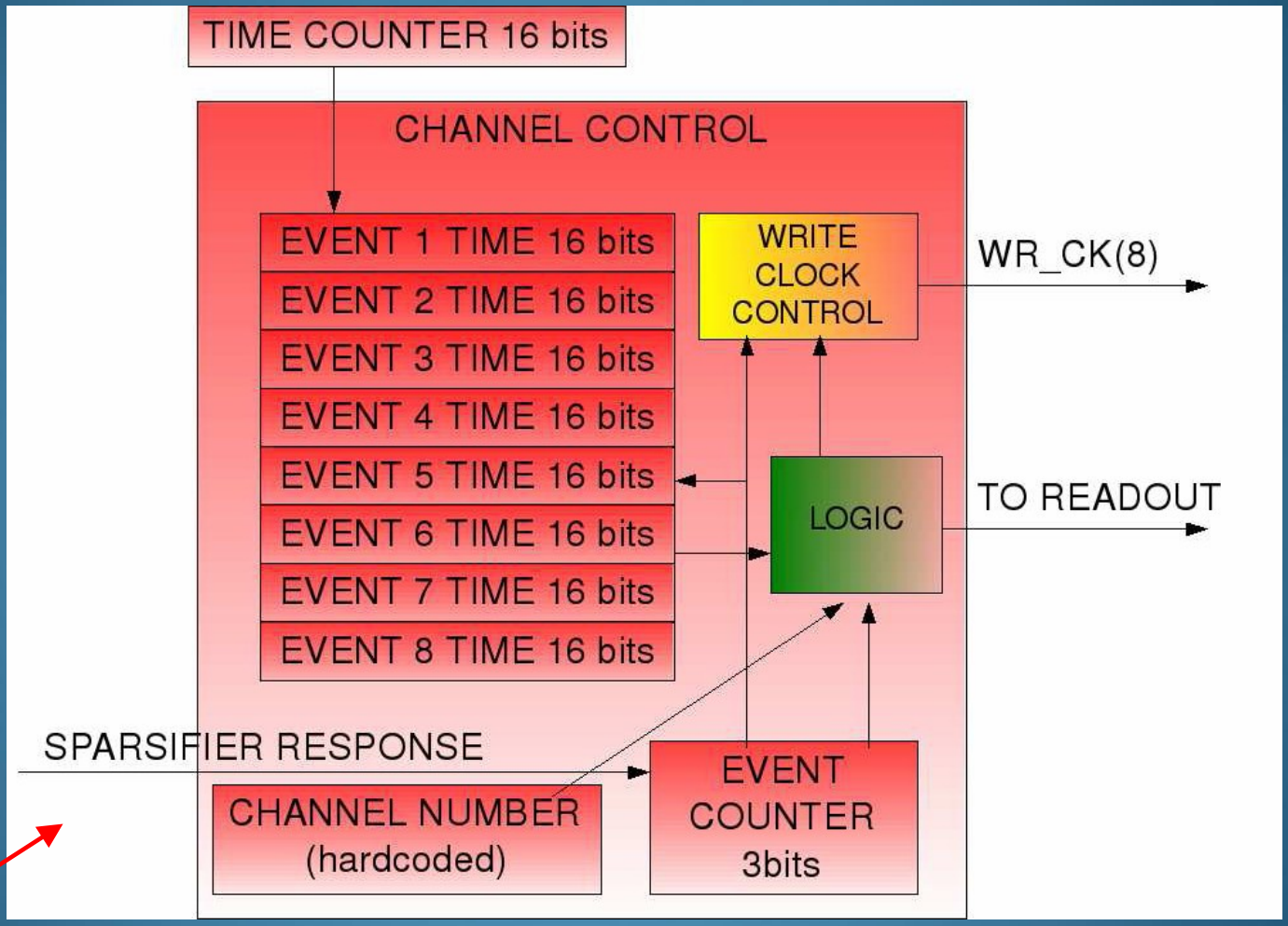


SiTR_130-88: Acquisition control FSM

The acquisition control block is constructed around a finite state machine (fsm), with 4 states:

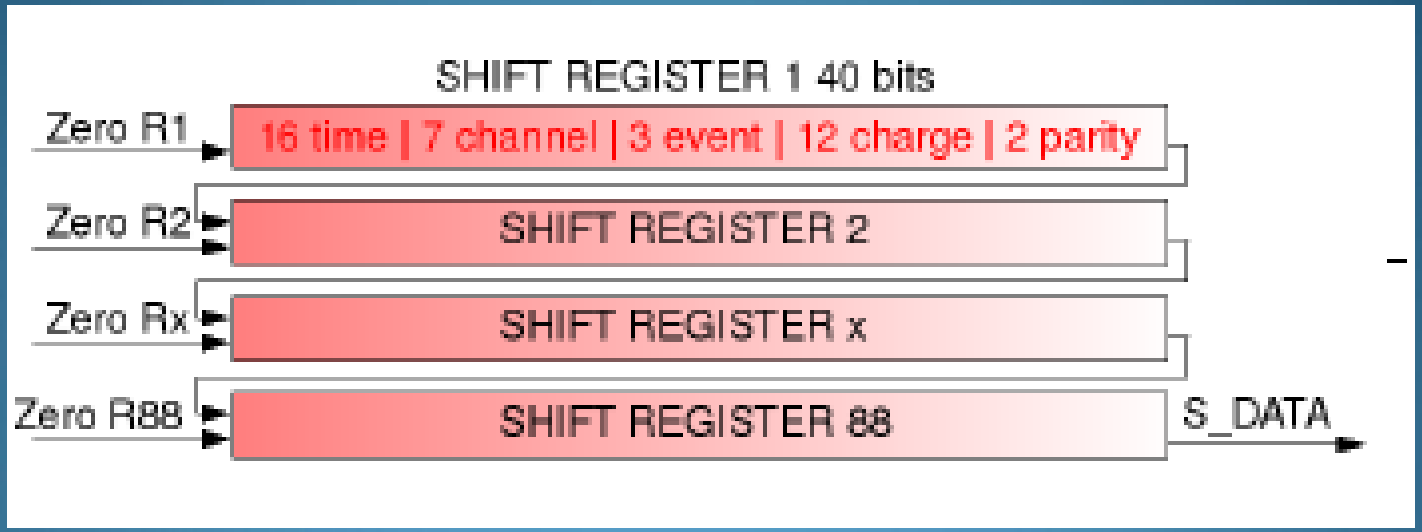
- IDLE: nothing to do, the system is waiting for starting acquisition (can be powered off)
- START-PIPE: when system comes from IDLE to ACQUISITION, first to be done=initializ the pipelines
- WRITE: after initialization, one can start writing in the pipelines; this is triggered when a sparsifier response is detected
- READ: a cycle of conversion/read is repeated until tehre is no more data

WRITE: the most important is the logic which processes the sparsifier response to enable a store sequence in the analogue pipeline



Channel control: inside every channel logic there are 8 registers to store the samples time information and a 3 bits event counter

Readout block

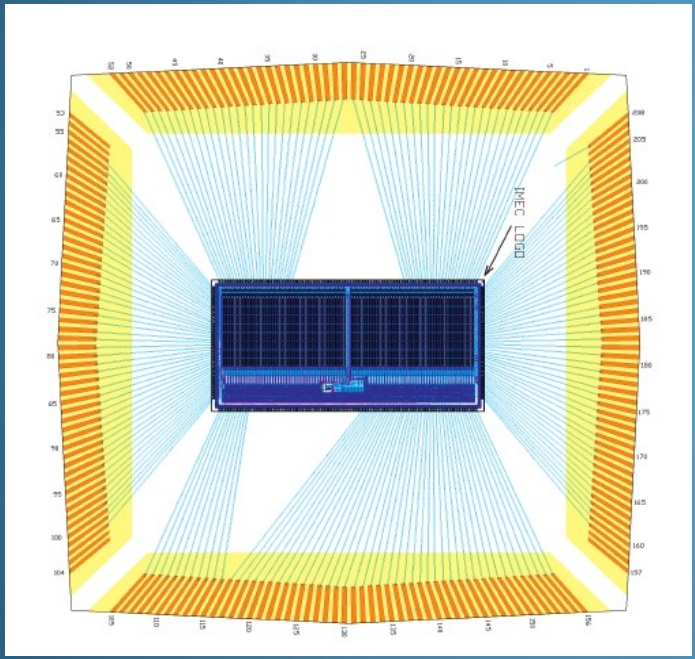


The readout block uses a serial interface to read out the data.
It is based on a group of 88 registers of 40 bits with parallel write and serial read acting as a shift register on read
Every register is divided in 3 groups:

=> 1st group: time, channe and event information (16+7+3=26 bits)
=> 2nd group: charge information (12 bits)
=> 3rd group: 2 parity bits

New readout circuit in 0.13 µm

BONDING DIAGRAM FOR CQFP208 PACKAGE



Package 208 pins
- 50 analog input
- 21 analog test out
- 33 digital pin (22 test pins)
- 107 supply pins

20 packaged chips delivered October 20:

For a a detailed test of chip functionality & performances (just starting)

Test is "easy" because the chip is "fully programmable"

Then test with naked chip onto detectors at Lab test bench and then at test beam.

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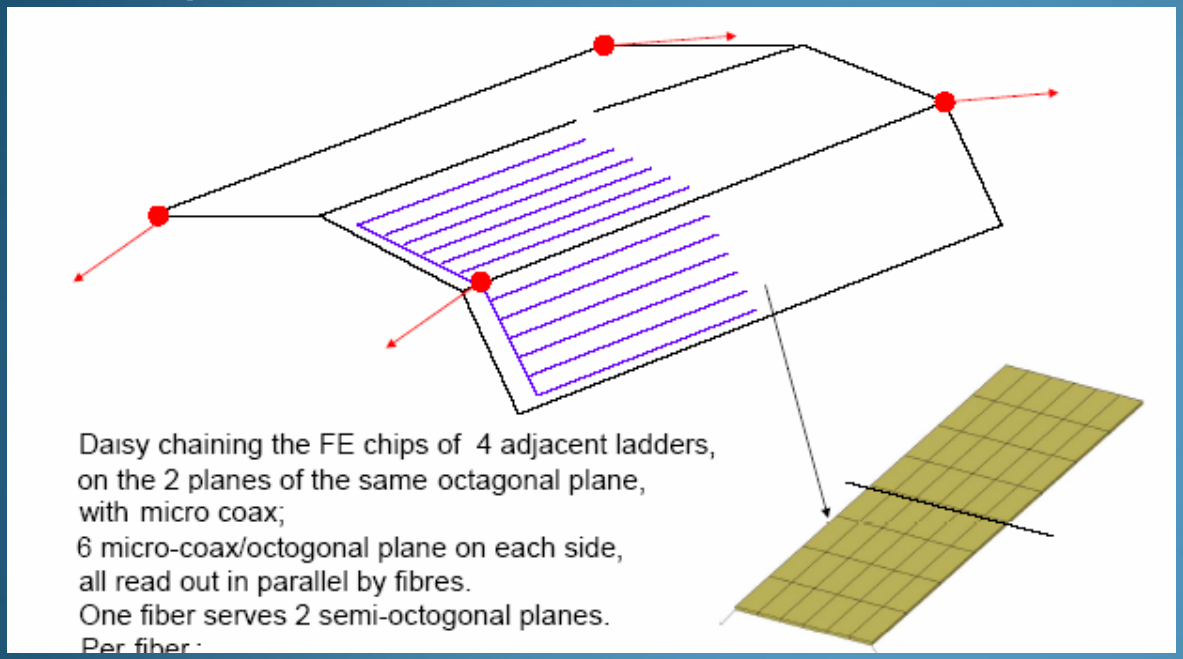
Level 2: FE-on detector edges, interface detector with external world

Example

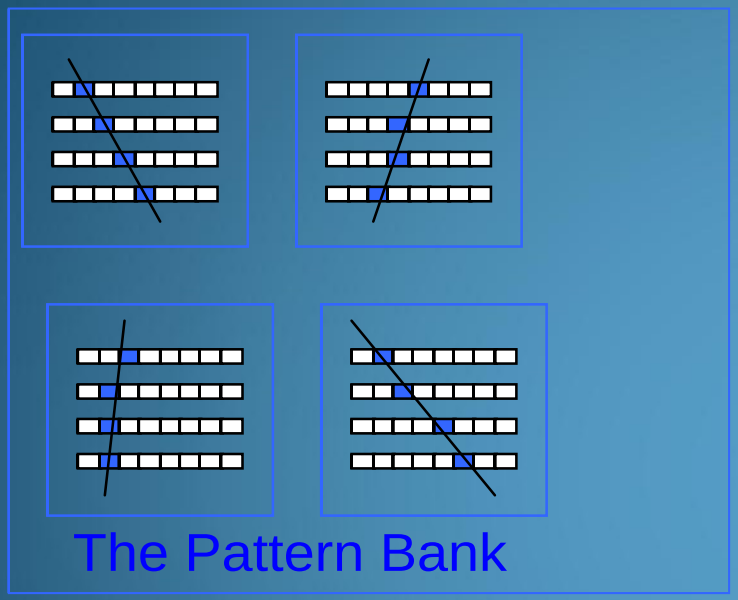


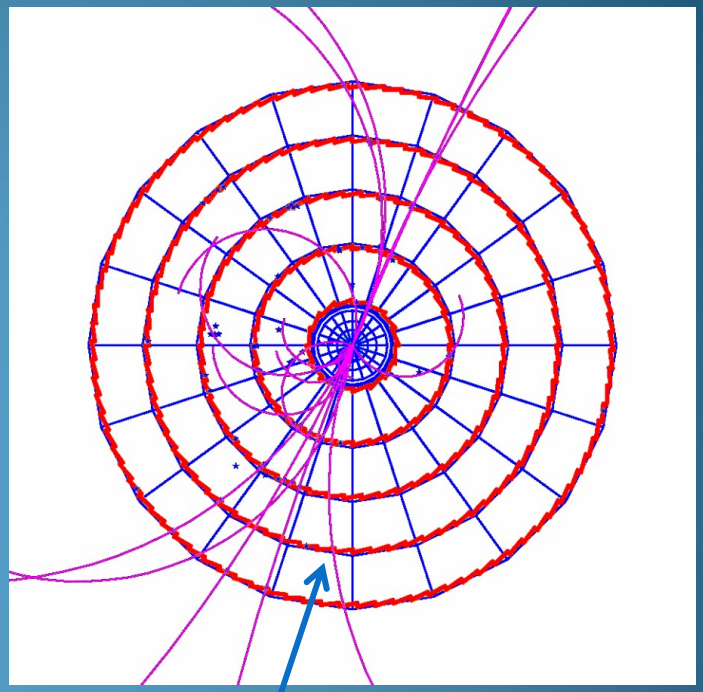
Cabling:
Level 1 to Level 2: microcoax
Level 2 to Level 3: digital fibers

Number of issues related to cabling:
Follow industrial advances
High rates and high speed, reliability, fault tolerance, robustness
Common for all sub detectors

Each red points = buffer + pre-processing 2 (re-ordering & compressing data), transceiver (digital fiber to external world = Control Room)
Sends pre-digested data at CR and get slow control and distributes it on detector

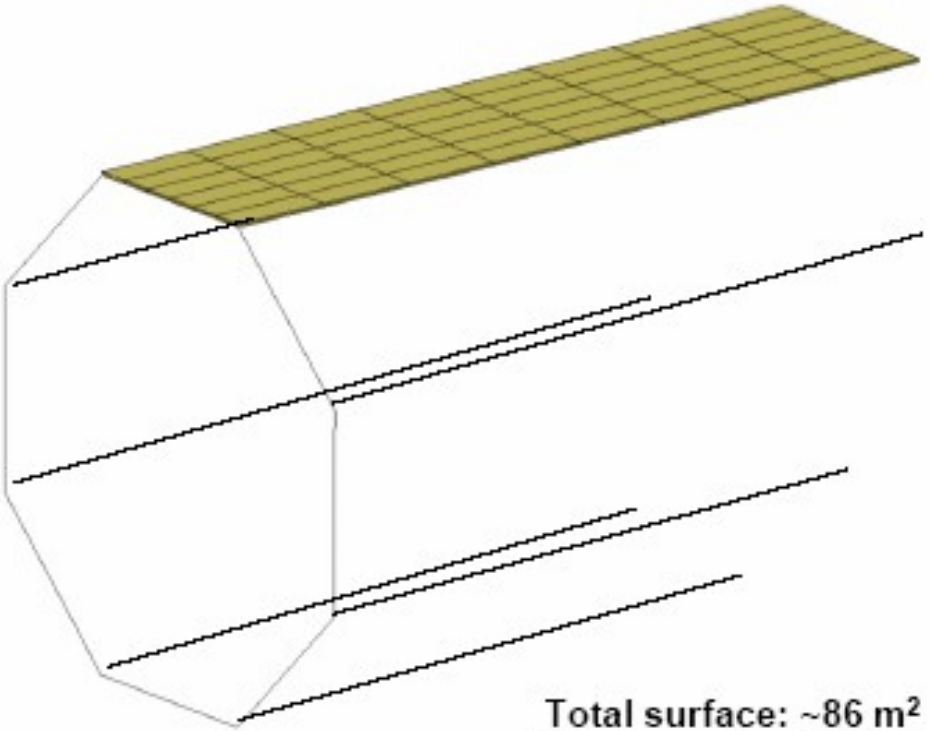
Level 3: Si TRK DAQ in the C.R.; integration phase



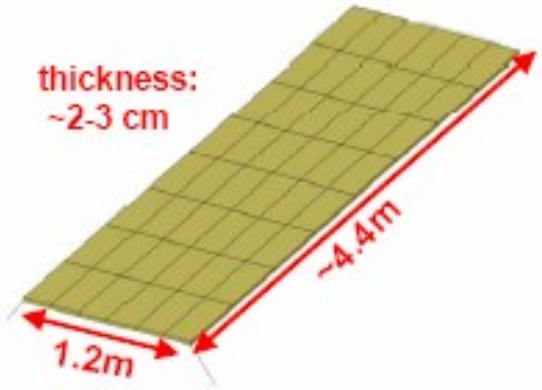


REAL TIME PROCESSING at level 3:
organize the processors for instance regrouping Level 2 elements belonging to a same azimuthal sector and perform tracking , a la CDF or FTK=FastTrack Finding (LHC).
SLOW CONTROL: synchronisation (Clock), power supplies, calibration signal, operation Parameters settings ....
COMBINE information from Si Tracking with other SUBDTECTORS

Just an educated guess example



Total surface: ~86 m²
Nb channels: 1,572864
Nb of fibres: 8 per side



# ladders/octagone	96
# sensors/octagone	288
# channels/octagone	196608
# µchips/octagone	192
# µcoax/octagone	192
# fibres/octagone	2
# µchips/fibre	96
# channels /fibre	98304

Outer Silicon tracking layer : false double sided sensors

Cabling and data flow transmission

Data Flow transmission: presently foreseen to use micro-coax Cables of typically 1'' diameter , 300 mW power dissipation at 1 GHz, can be power cycled. Kapton cables also under Consideration

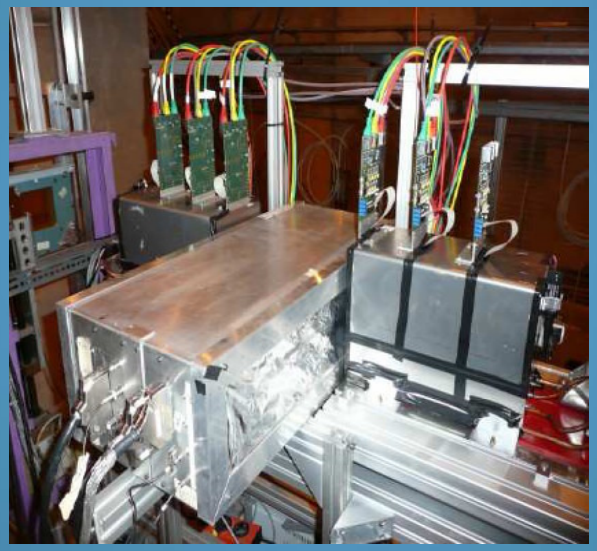
At a later stage: to transmit data from the edge of the detector to the outside, 6 GHz SCM digital optic links are presently considered

Related to this topic the data processing at all levels as described are a feature of our DAQ architecture.

DSP mounted as multichip modules would represent a very small amount of material (especially at the edge of the detector) and dissipate very little. We are starting to think on a real time track processing scenario

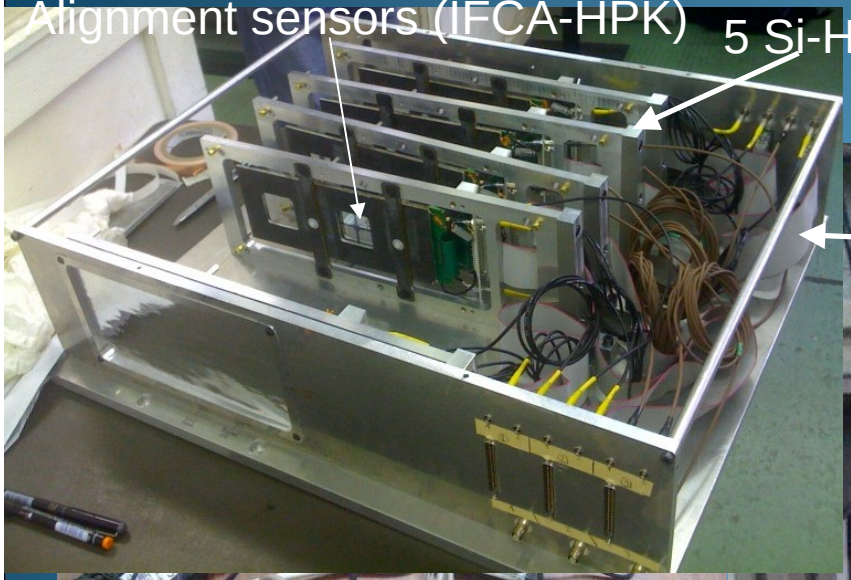
(within also EUDET framework)

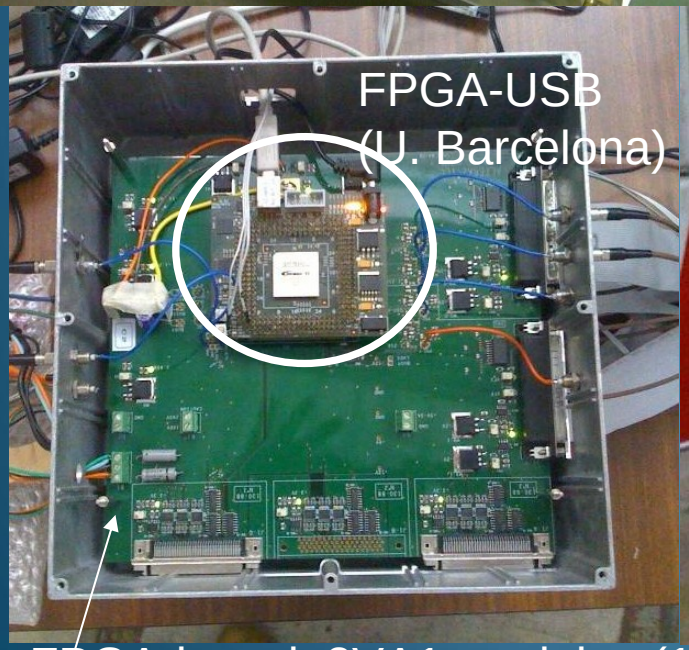
Towards developing the DAQ architecture:
first steps at the test beams or the learning stage

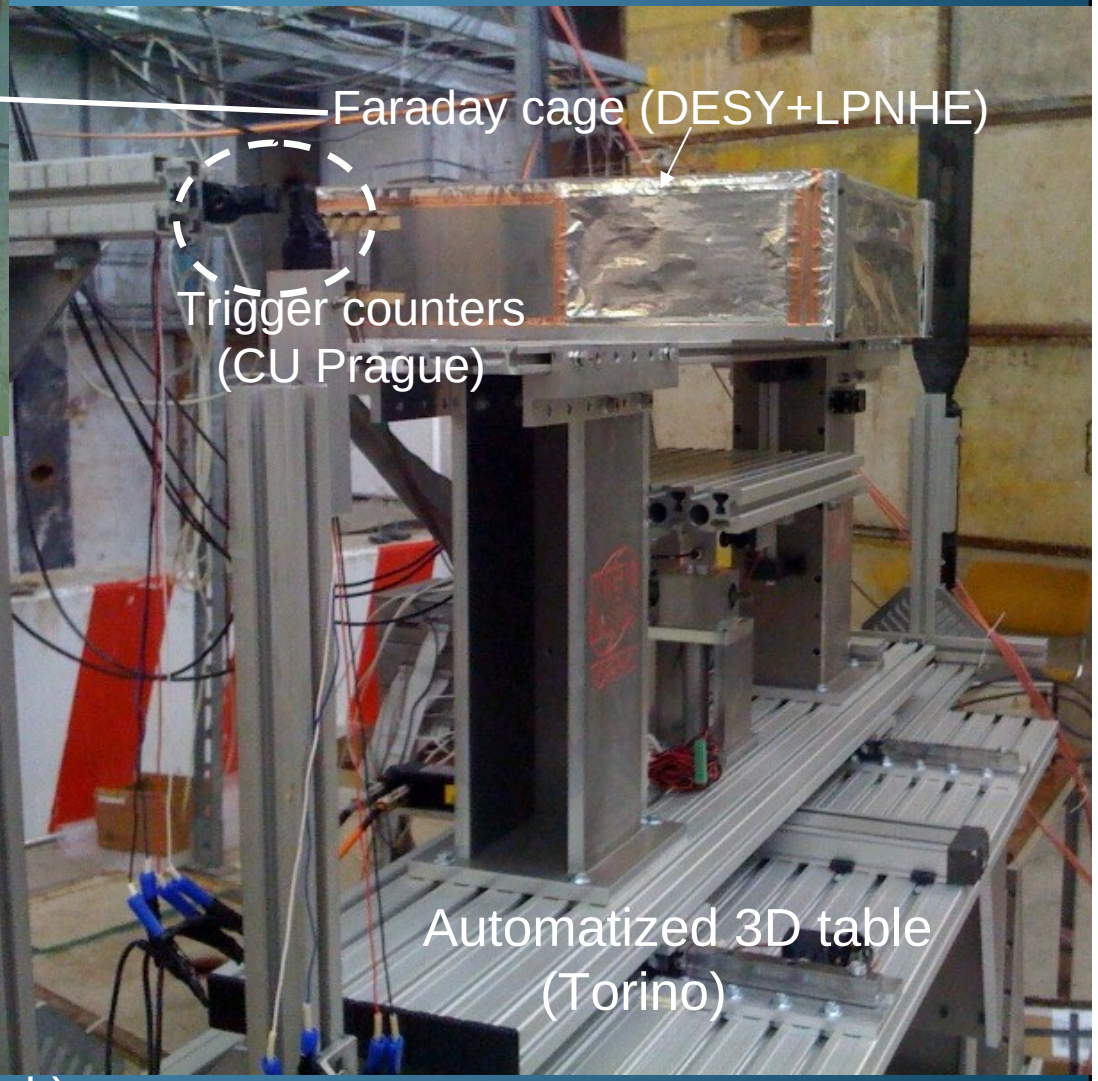


H6-SPS test beam at CERN, Oct 2007, combined test beam
SiLC modules with SiTR_130-4 + EUDET MAPS telescope

Test beam at PS-CERN, Nov 1-7 2008

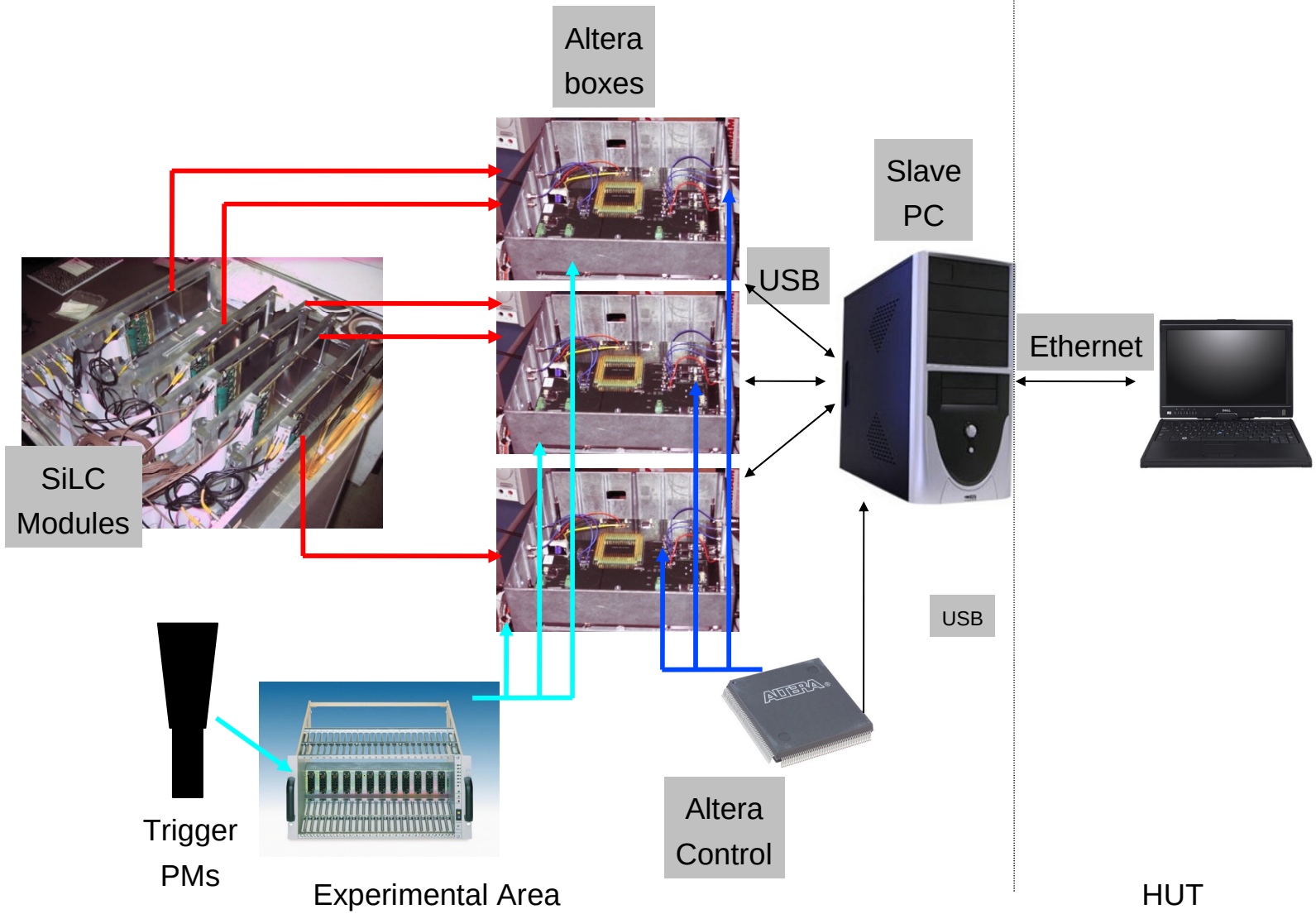






New test beam DAQ set-up for SiTR_130-88

Fully standalone tracking system



SOFTWARE: VHDL, C++, ROOT

Concluding remarks

- The FE readout chip on-detector is a crucial piece of the Si DAQ: it is well advanced; it constitutes the DAQ-LV1. This is a:
- Highly performing digitized FEE, fully programmable, with high processing capability, thus flexible and with a high degree of fault tolerance.
- This DAQ strategy includes a LV2 with track segments reconstruction and LV3 with full tracking
- Combining and unifying with the other sub detectors & global DAQ is a prerequisite
- Close contact with Industries is essential in order to avoid useless and expensive R&D work and that the system becomes soon obsolete.
- Last but not least: Cabling and data transmission / data processing
- Test beams are essential tool to develop DAQ

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