Progress with the CPCCD and the ISIS

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LCWS2007, DESY

- **Brief introduction**
- **Vertex Detector R&D**
  - **Column-Parallel CCDs**
  - **In-situ Storage Image Sensors**
- **Plans**

Introduction

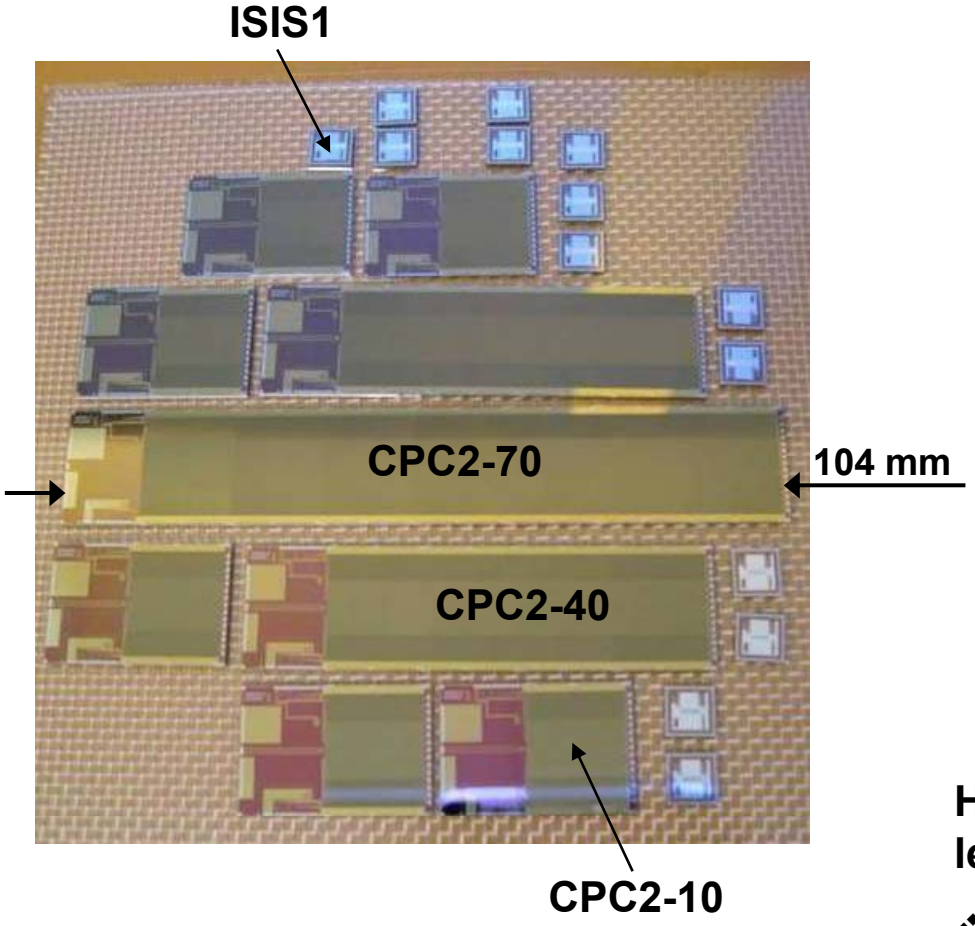
What is required for the vertex detector at ILC:

- Excellent point resolution (3.5 μm), small pixel size = 20 μm, close to IP
- Low material budget ($\leq$ 0.1% X_0 per layer), low power dissipation
- Fast (low occupancy) readout – challenging, two main approaches
- Tolerates Electro-Magnetic Interference (EMI)

What LCFI has done so far:

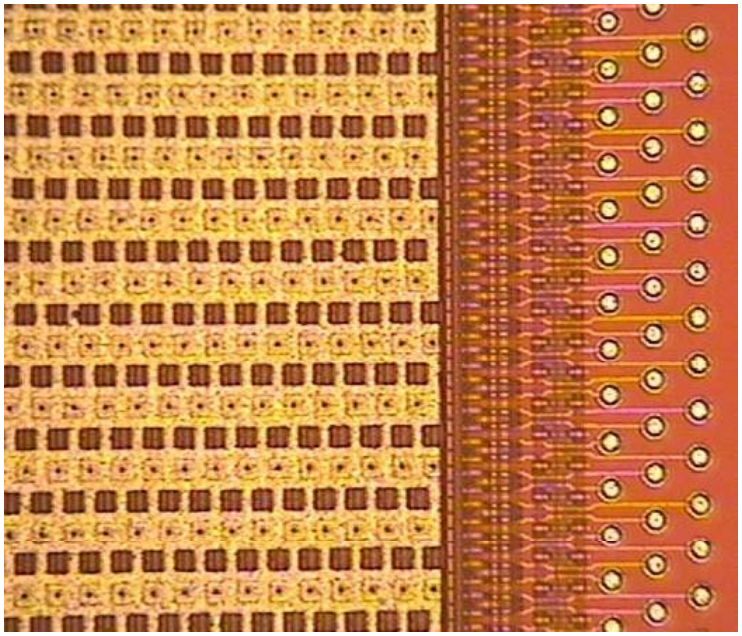
- Made 2 generations of Column Parallel CCDs: CPC1 and CPC2
- In-situ Storage Image Sensor – proof of principle device ISIS1 designed and tested
- CMOS readout chips for CPC1/2: 2 generations, bump bonded to the CCDs
- Driver chip for CPC2 designed and manufactured
- Built lots of electronics to support the detectors
- Extensive tests of stand-alone devices and hybrid bump-bonded assemblies

Second Generation CPCCD : CPC2



- CPC2 wafer (100 Ω.cm/25 μm epi and 1.5kΩ.cm/50 μm epi)
- Low speed (single level metallisation) and high speed versions

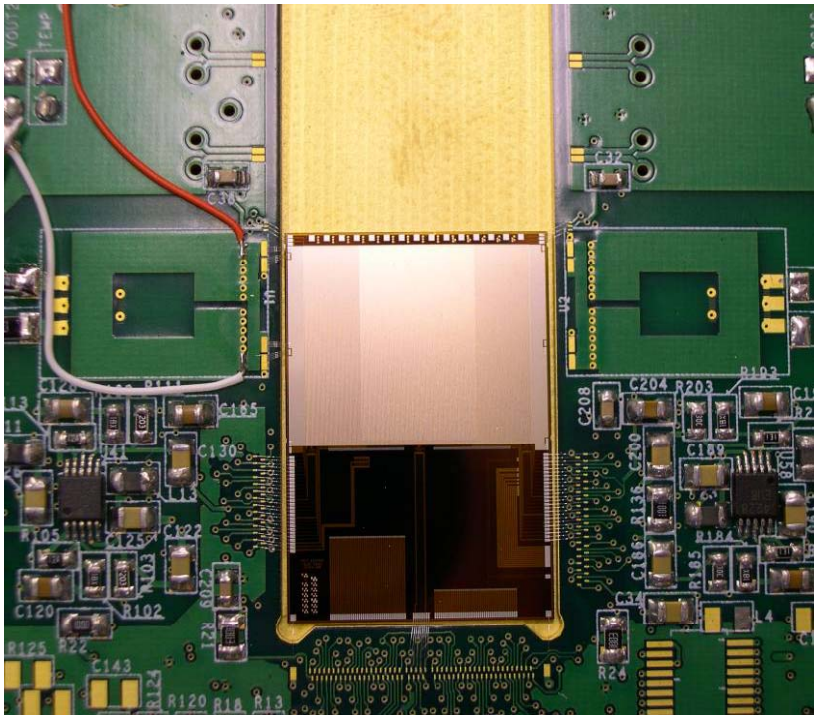
Busline-free CPC2



High speed (busline-free) devices with 2-level metal clock distribution:

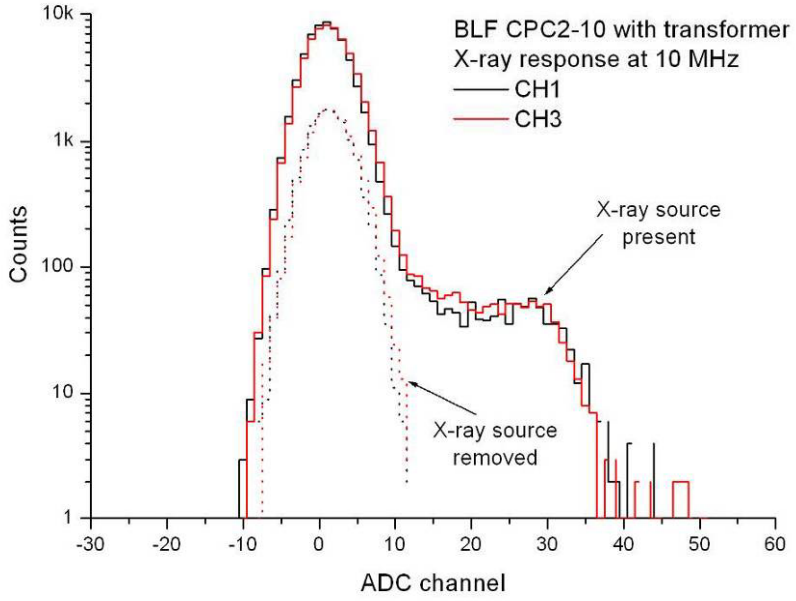
- ❖ The whole image area serves as a distributed busline
- ❖ Designed to reach 50 MHz operation
- ❖ Important milestone for LCFI

CPC2 – High Speed in Stand-alone Mode



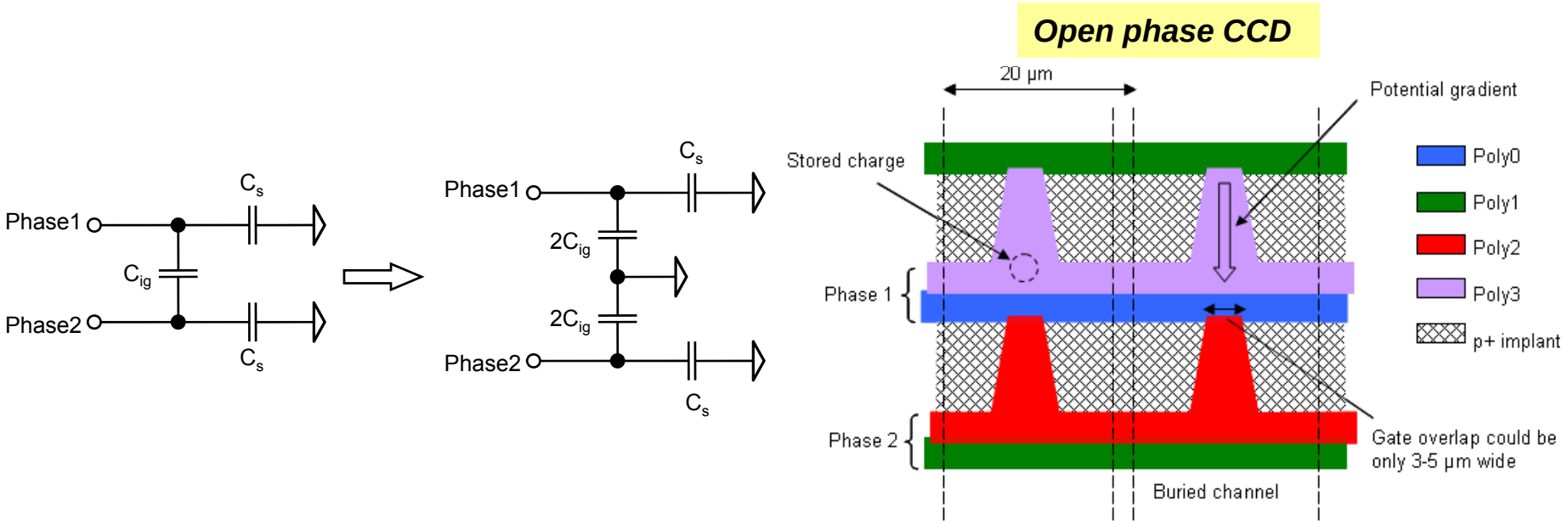
- **Busline-free CPC2-10 working at 45 MHz**
- **Clock amplitude is only 0.4 V_{pk-pk}!**
- **Using transformer driver and RF amplifier to drive the CCD**
- **Will try to improve with chip driver**

10 MHz ^{55}Fe spectrum



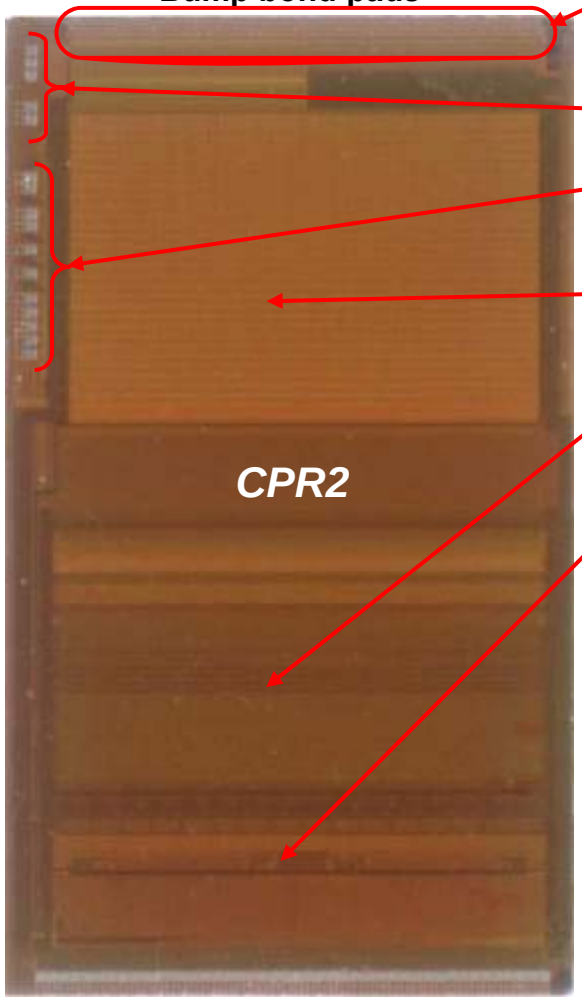
- **CPC2-10 (low speed version) works fine, 62e- noise at 1 MHz clock**
- **High-speed busline free CPC2 is most interesting**
- **140 e- noise at 10 MHz – due to excessive noise from the drive RF amplifier**
- **Numerous parasitics diminish transformer performance**

New Ideas: CCDs for Capacitance Reduction



- **High CCD capacitance is a challenge to drive because of the currents involved**
  - **Can we reduce the capacitance? Can we reduce the clock amplitude as well?**
  - **Inter-gate capacitance C_{ig} is dominant, depends mostly on the size of the gaps and the gate area**
  - **Open phase CCD, "Pedestal Gate CCD", "Shaped Channel CCD" – new ideas under development, could reduce C_{ig} by ~4!**
- **Currently designing small CCDs to test several ideas on low clock and low capacitance, together with e2V Technologies**

Readout Chips – CPR1 and CPR2



Voltage and charge amplifiers 125 channels each

Analogue test I/O

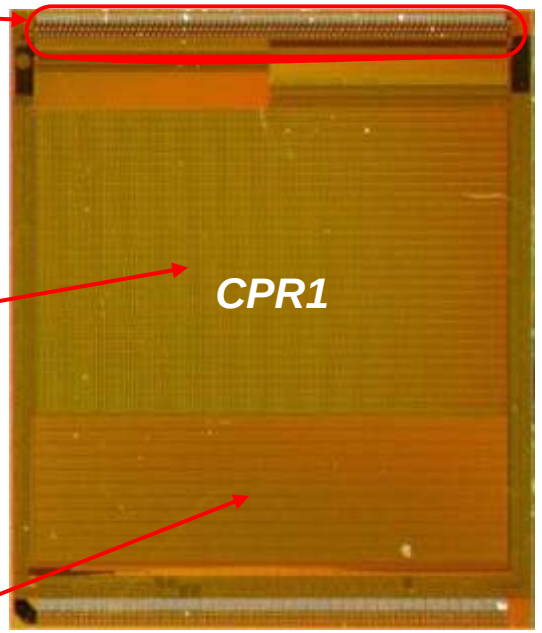
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

Sparse readout circuitry

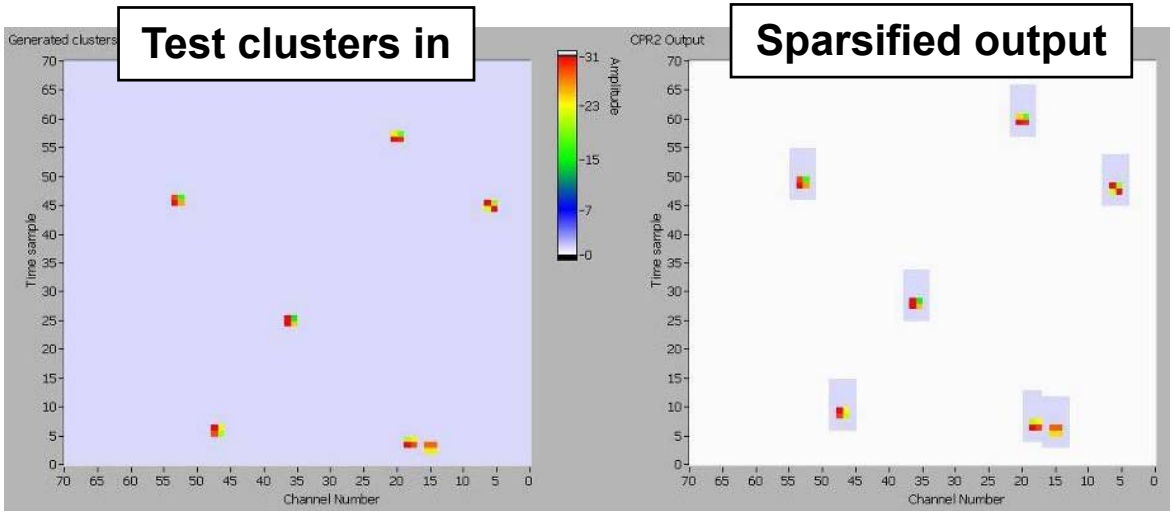
FIFO



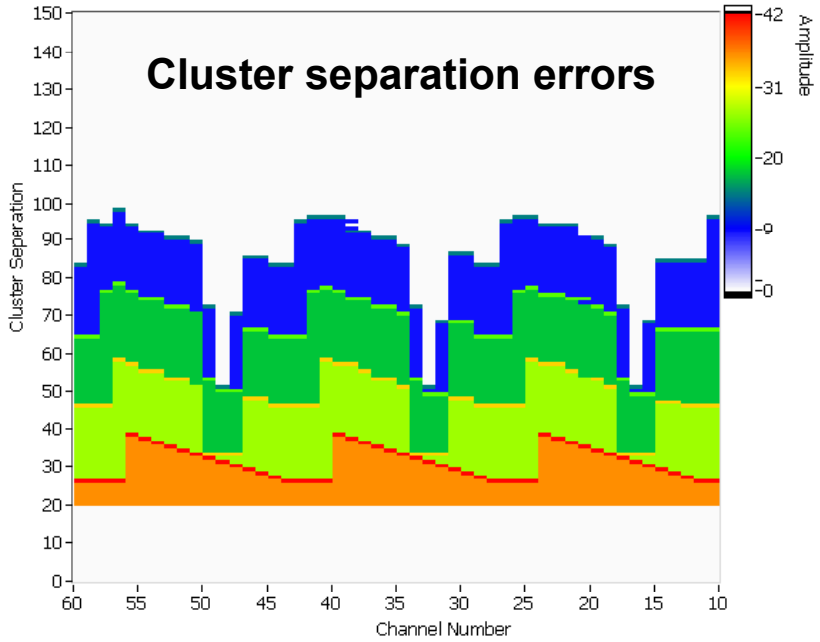
- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Manufactured and delivered February 2005

Steve Thomas/Peter Murray, RAL

CPR2 Test Results



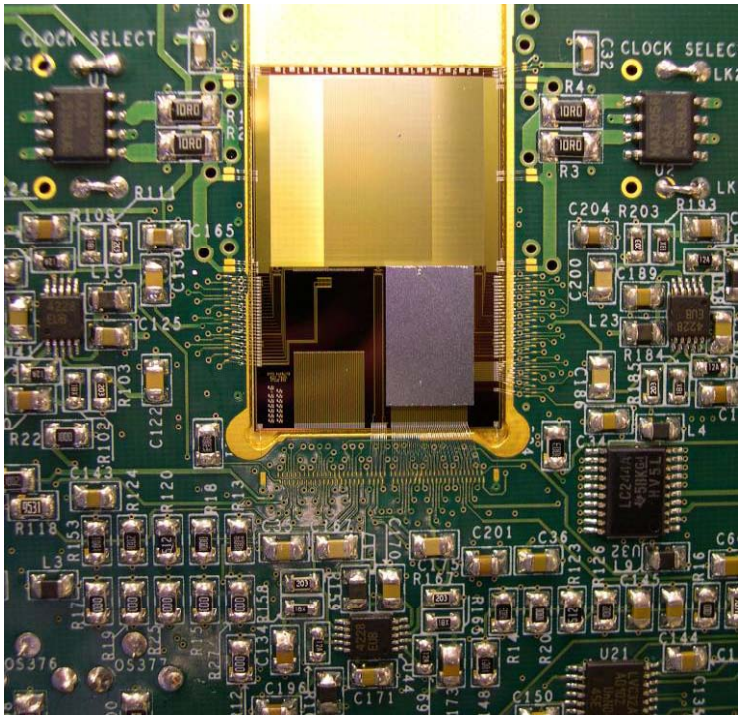
- Parallel cluster finder with 2×2 kernel
- Global threshold
- Upon exceeding the threshold, 4×9 pixels around the cluster are flagged for readout

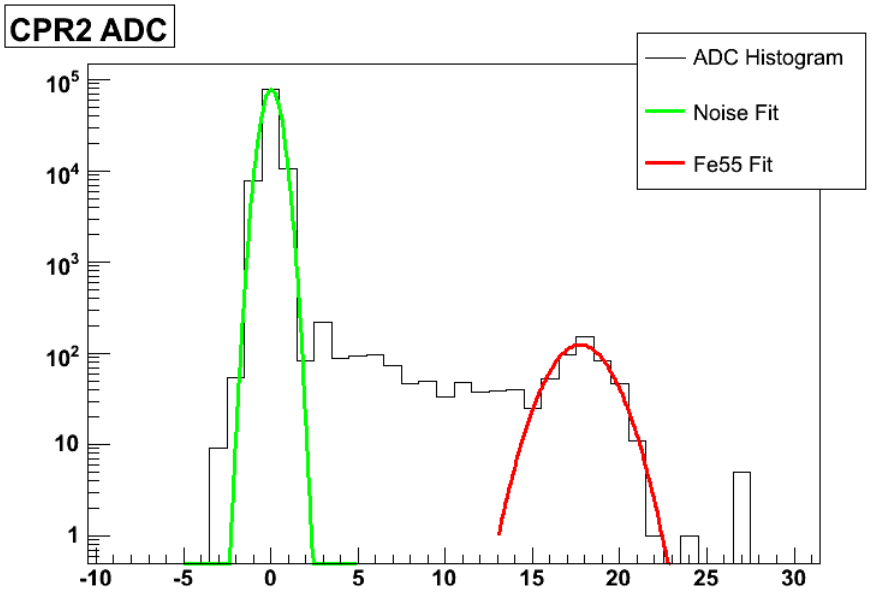


- Tests on the cluster finder: works!
- Several minor problems, but chip is usable
- Cluster separation studies:
  - ❖ Design occupancy is 1%
  - ❖ Errors as the distance between the clusters decreases – reveal dead time
- Extensive range of improvements to be implemented in the next version (CPR2A)
- CPR2A design in progress

Tim Woolliscroft, Liverpool U

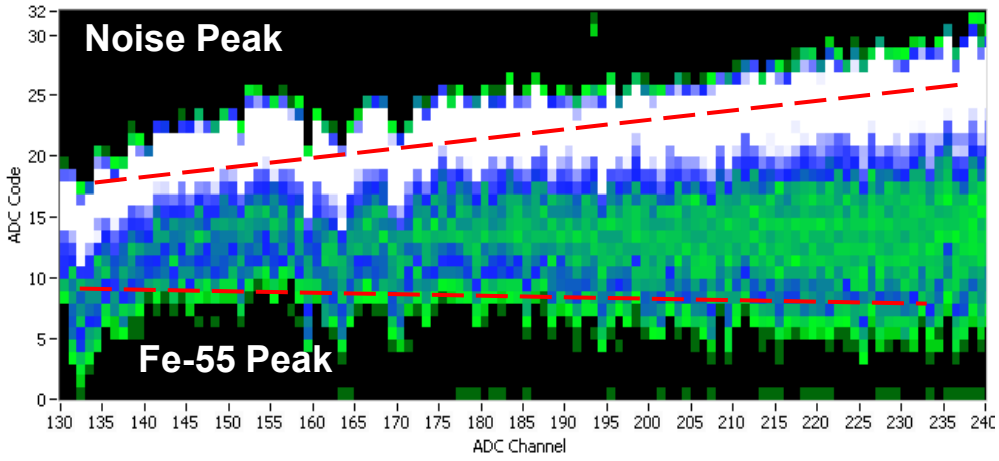
CPR2 Bump Bonded to CPC2 – Test Results



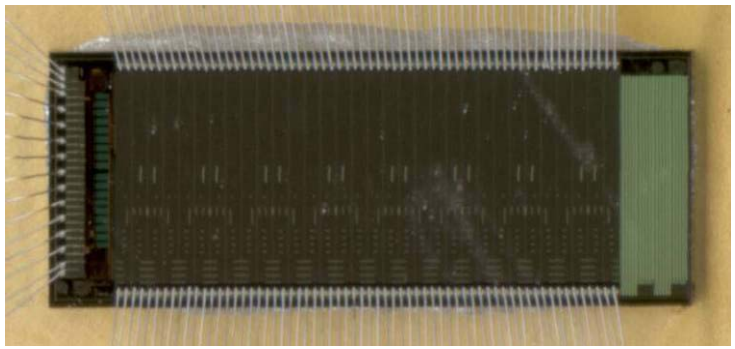


Tim Woolliscroft, Liverpool U

- **Signals from all voltage channels observed**
- **Presently at 2 MHz**
- **Gain seems to decrease away from the chip edges**
- **Noise around 60-80 e-**

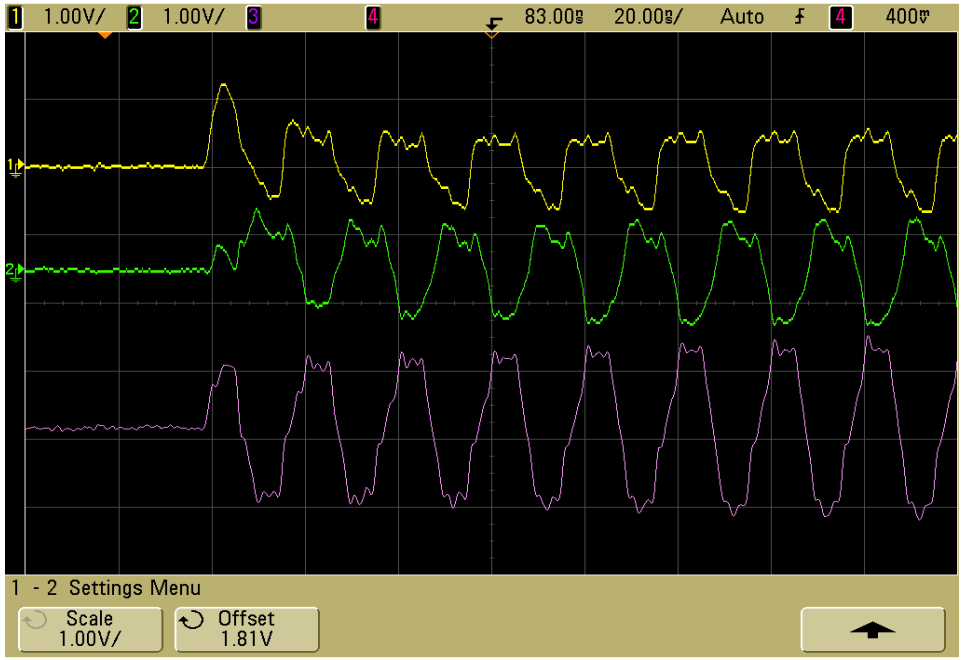


Clock Driver for CPC2 : CPD1



Steve Thomas/Peter Murray, RAL

- Designed to drive:
  - ❖ Outer layer CCDs (127 nF/phase) at 25 MHz
  - ❖ L1 CCD (40 nF/phase) at 50 MHz
  - ❖ CPC2 requires ~21 Amps/phase!
- One chip drives 2 phases, up to 3.3 V clock swing
- 0.35 μm CMOS process, chip size 3×8 mm^2
- Careful layout on- and off-chip to cancel inductance



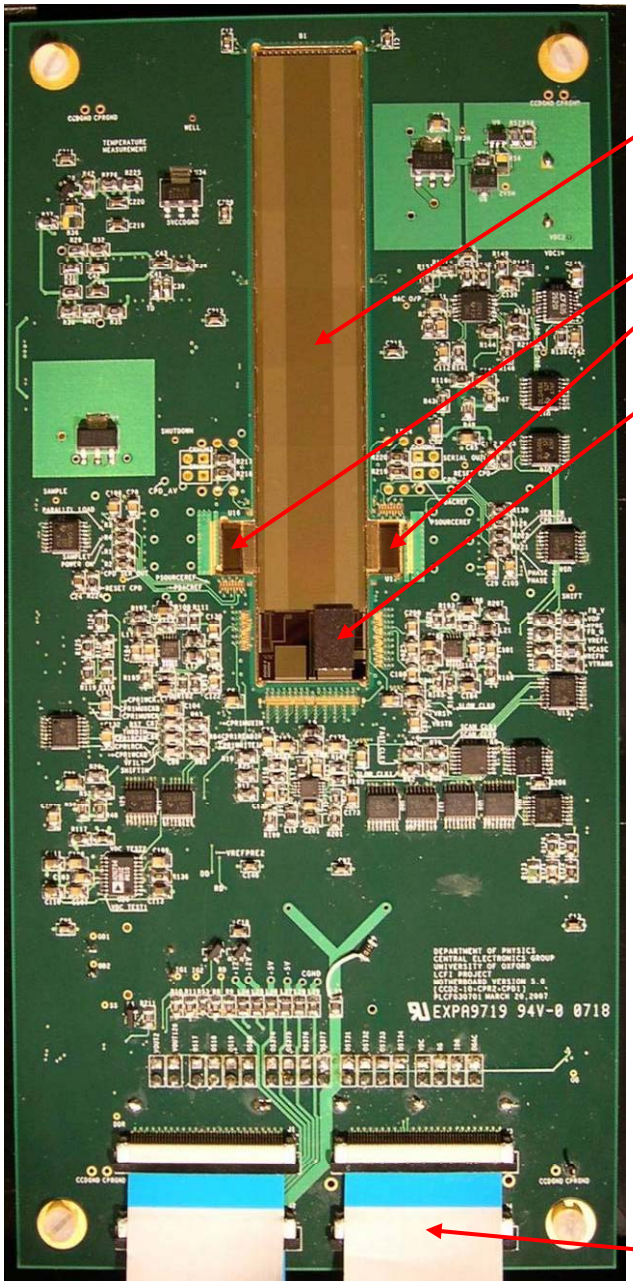
2 $V_{pk\text{-}pk}$ differential clocks

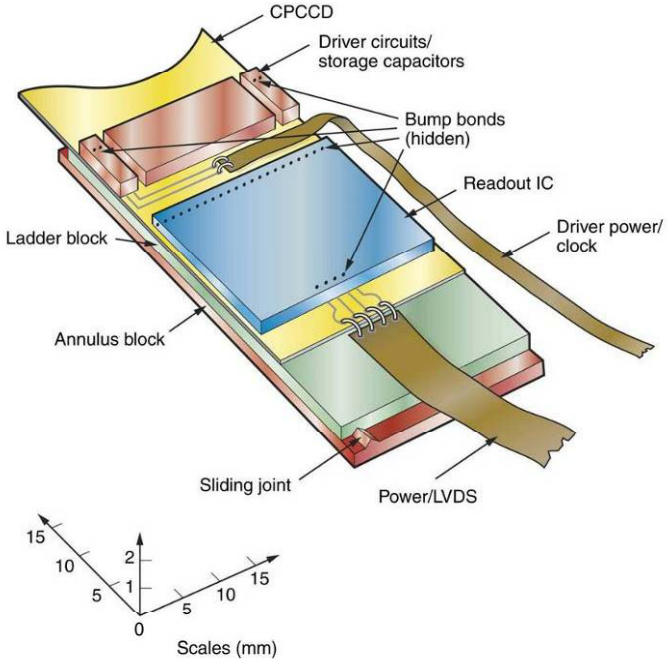
Tests:

- CPD1 driving 40 nF-equivalent internal load at 50 MHz
- Hope to maintain the same performance when bump-bonded

Rui Gao, Andrei Nomerotski, Oxford U

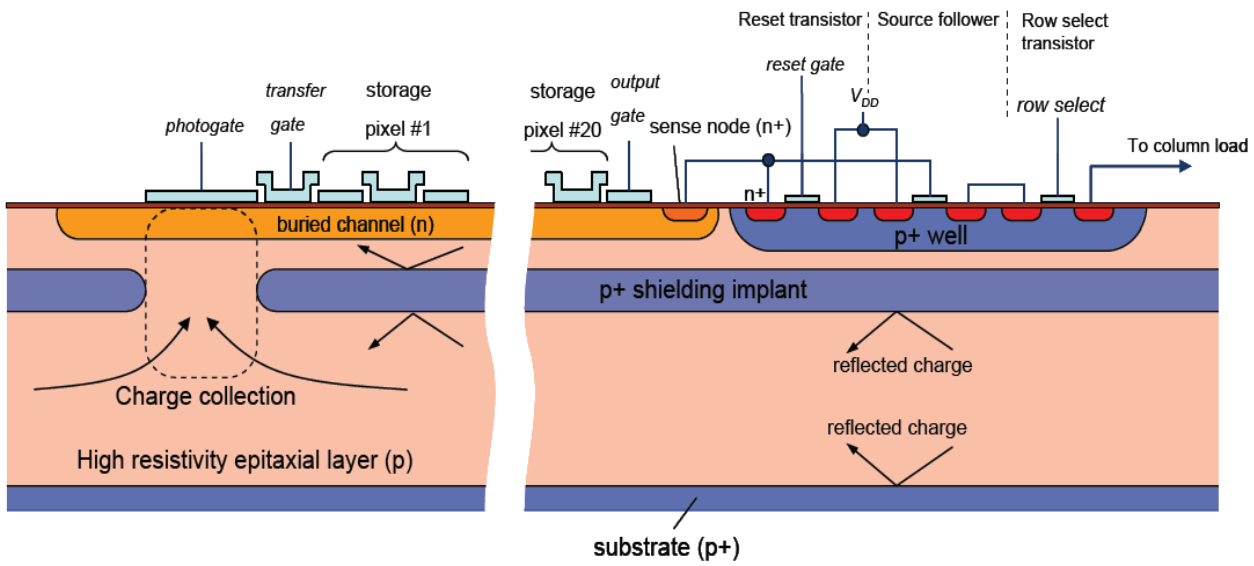
Next Big Step : CPC2, CPR2 and CPD1 All Together





- All ingredients are in place – intensive testing ahead in the next months
- Getting closer to prototype ladder
- Next generation CPR2A should make this board much smaller

In-situ Storage Image Sensor (ISIS)

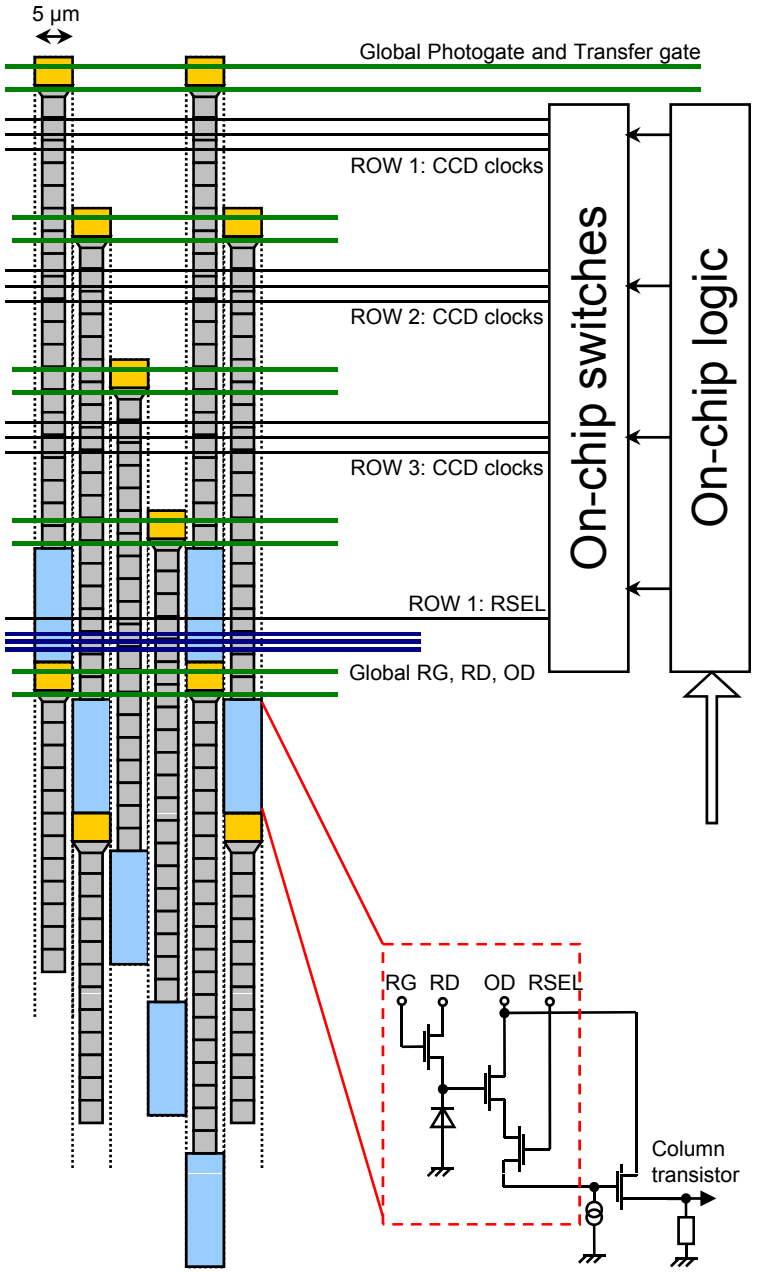


Chris Damerell, RAL

Operating principles of the ISIS:

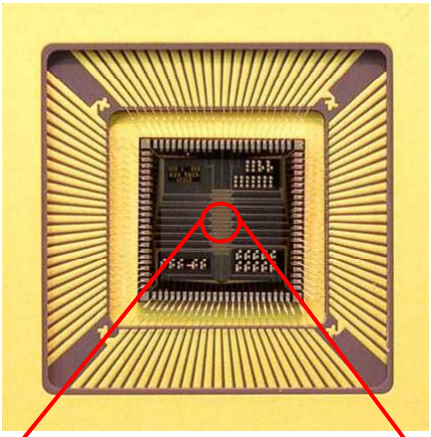
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup);**
4. **1 MHz column-parallel readout is sufficient;**

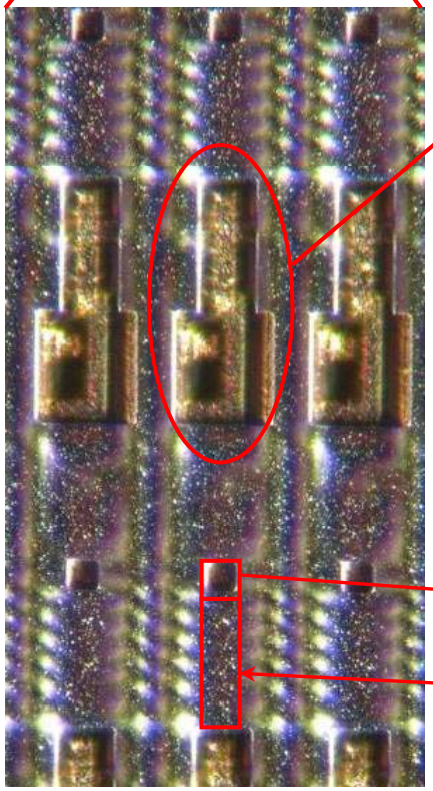
In-situ Storage Image Sensor (ISIS)



- The ISIS offers significant advantages:
  - ❖ **Easy to drive** because of the low clock frequency: 20 kHz during capture, 1 MHz during readout
  - ❖ ~100 times more **radiation hard** than CCDs (less charge transfers)
  - ❖ **Very robust to beam-induced RF pickup**
- ISIS combines CCDs, active pixel transistors and edge electronics in one device: **specialised process**
- Development and design of ISIS is more ambitious goal than CPCCD
- "Proof of principle" device (ISIS1) designed and manufactured by e2V Technologies

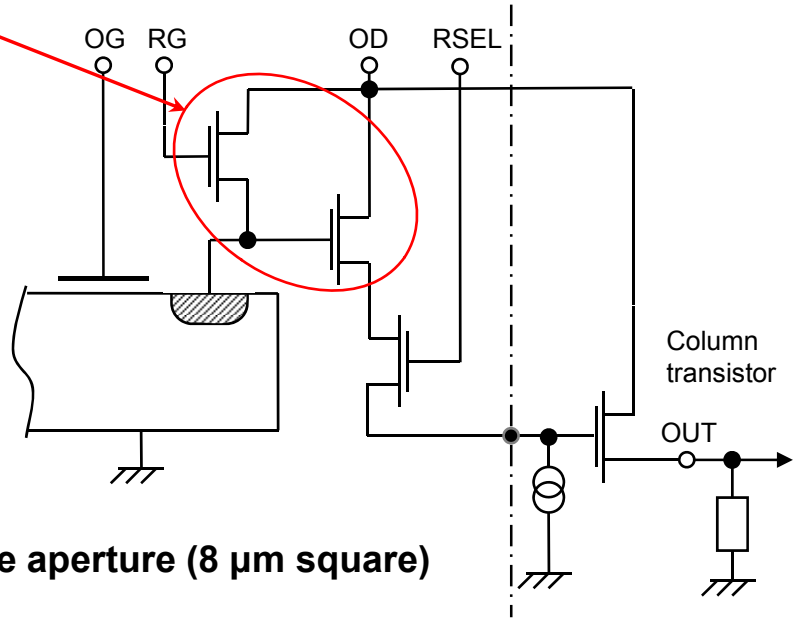
The ISIS1 Cell





- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm

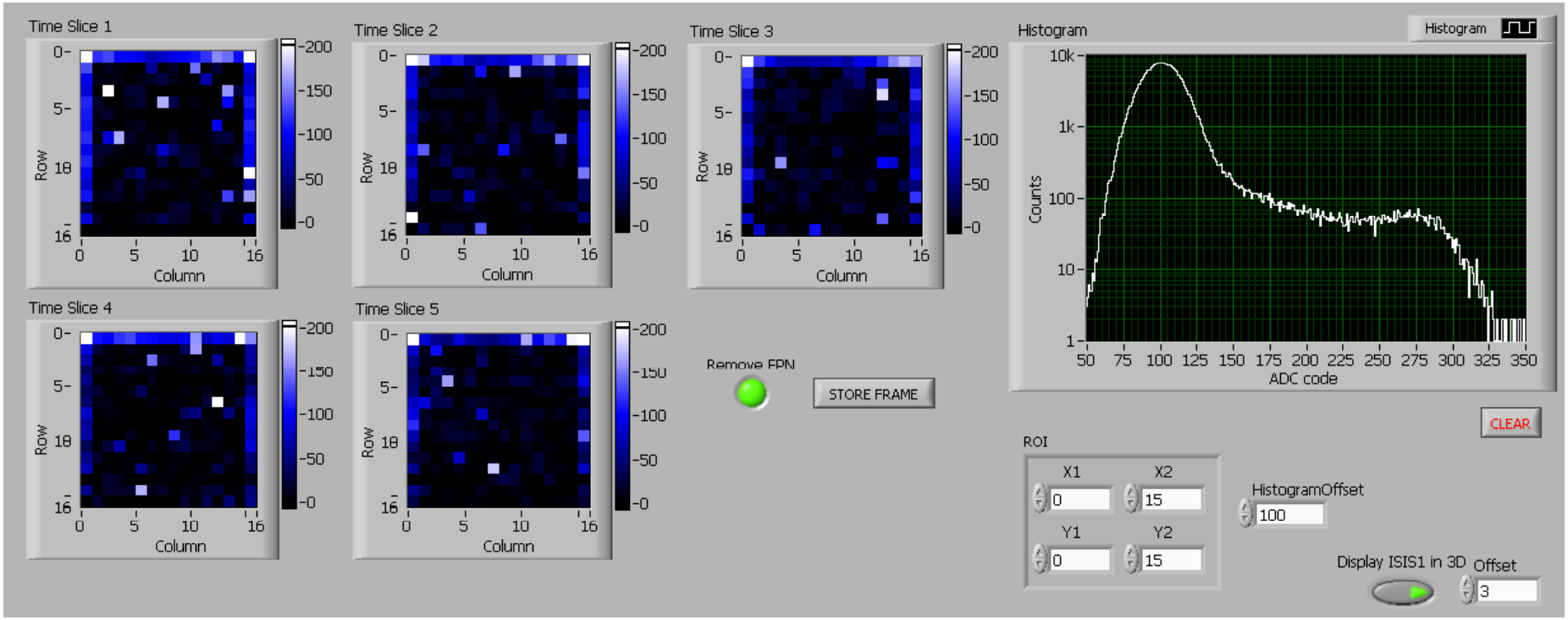
Output and reset transistors



Photogate aperture (8 μm square)

CCD (5×6.75 μm pixels)

Tests of ISIS1



Tests with ^{55}Fe source

- The top row and 2 side columns are not protected and collect diffusing charge
- The bottom row is protected by the output circuitry
- ISIS1 without *p*-well tested first and works OK
- ISIS1 with *p*-well has very large transistor thresholds, permanently off – re-run agreed with e2V

Conclusion and Plans

- Detector R&D is progressing very well
- CPCCD program most advanced:
  - ❖ Second generation high speed CPCCD is being tested – works with 0.4 V clocks, reaches 45 MHz
  - ❖ Bump-bonded assemblies CPC2/CPR2 under tests
  - ❖ Programme for capacitance and clock amplitude reduction is underway
  - ❖ Driver system under development
    - ❖ CMOS driver chip available
    - ❖ Transformer drive also used
  - ❖ Third generation CMOS readout chips CPR2A in design stage
- ISIS work:
  - "Proof of principle" device works
  - Design of second generation, small pixel ISIS2 underway
- Do not miss Erik's talk on mechanical support studies

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