Pad occupancy in LDC TPC with TDC-based readout electronics

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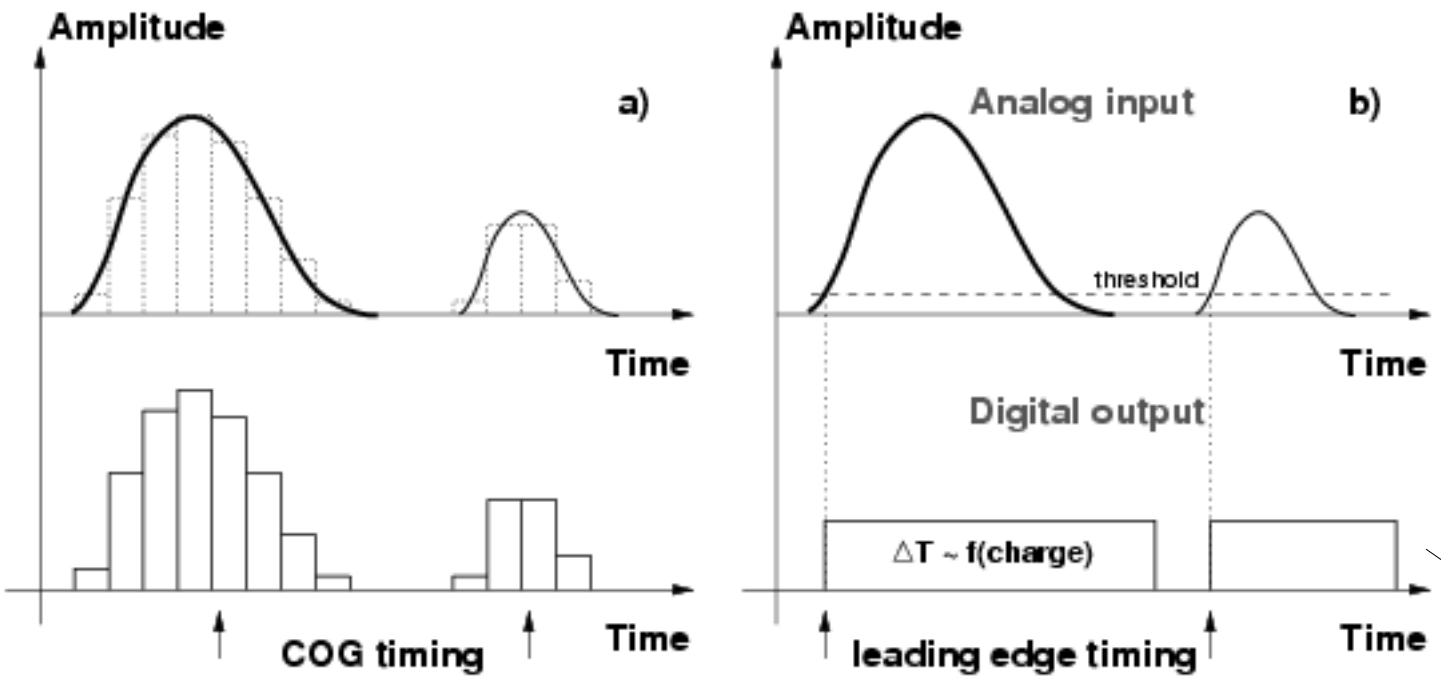
TPC readout electronics with Time-to-Digit Converter



TDC

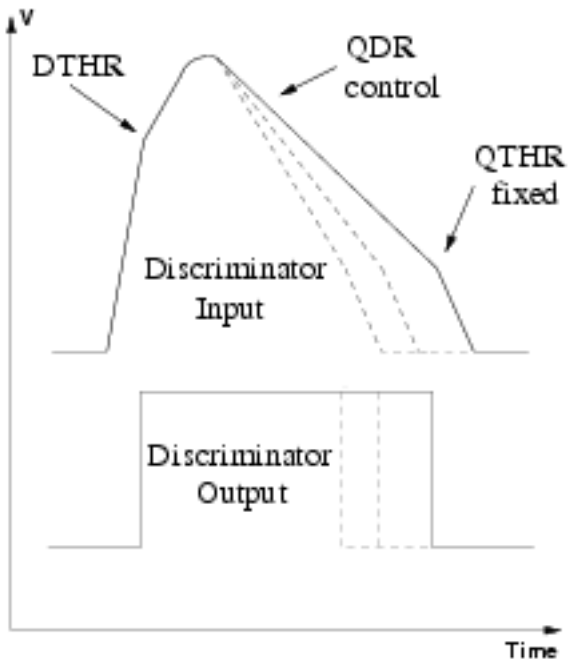
Measure arrival time of signals

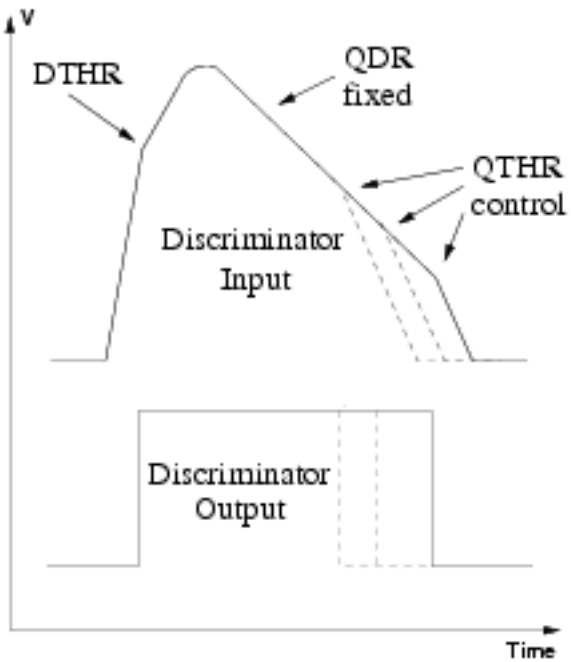
Measure charge of signals

Charge-to-time convertion with ASDQ: I

ASDQ: Amplifier Shaper Discriminator with charge (Q)-measurement

- Charge capacitor with input signal, discharge with a constant current

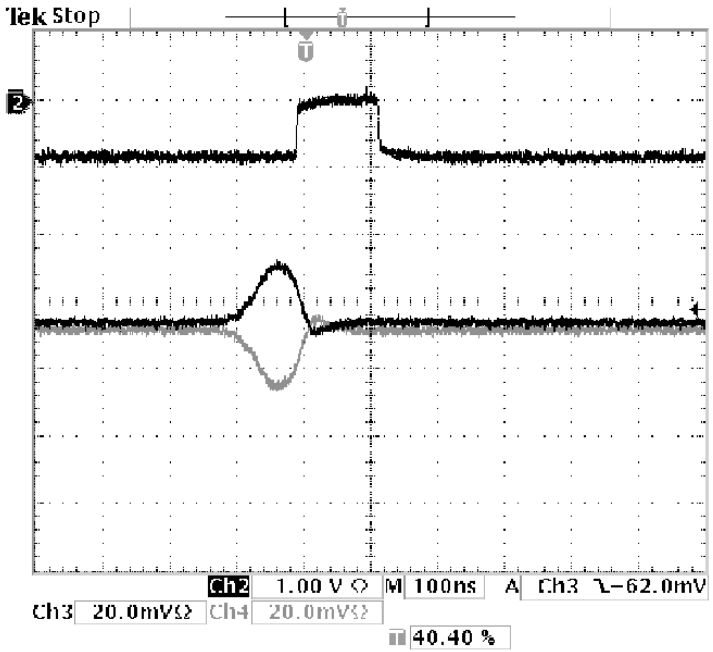




Measure arrival time of signals

Measure charge of signals

Charge-to-time convertion with ASDQ: II

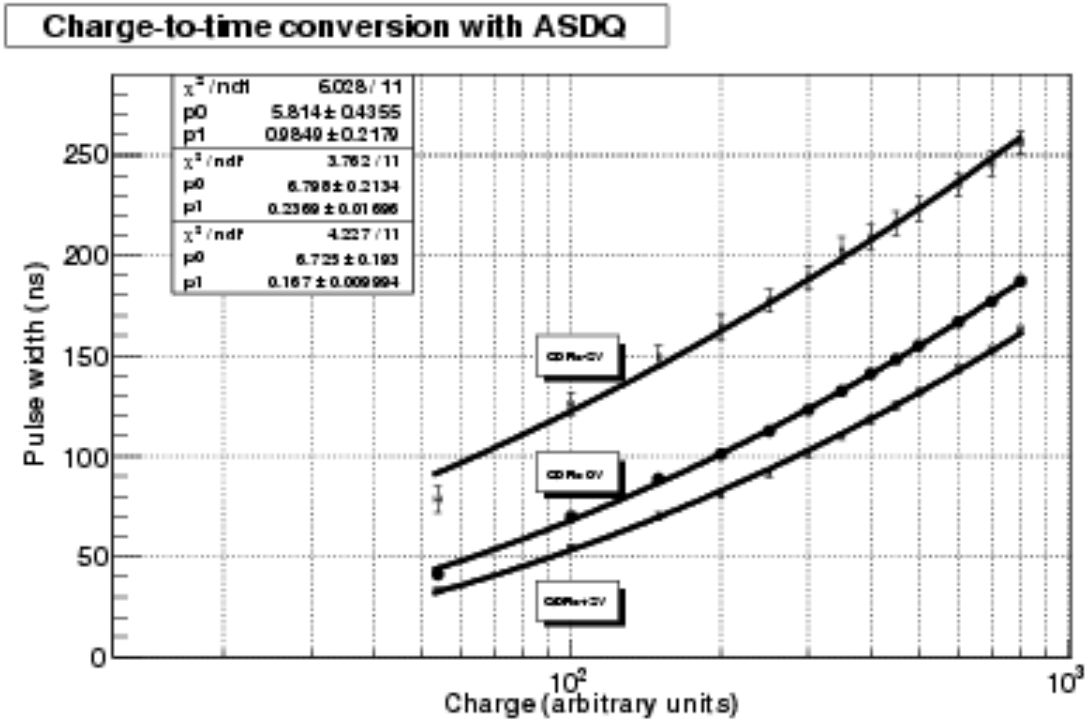


← Signal from a GEM TPC

Charge-to-Time (QT)-characteristic →

"logarithm-like function"

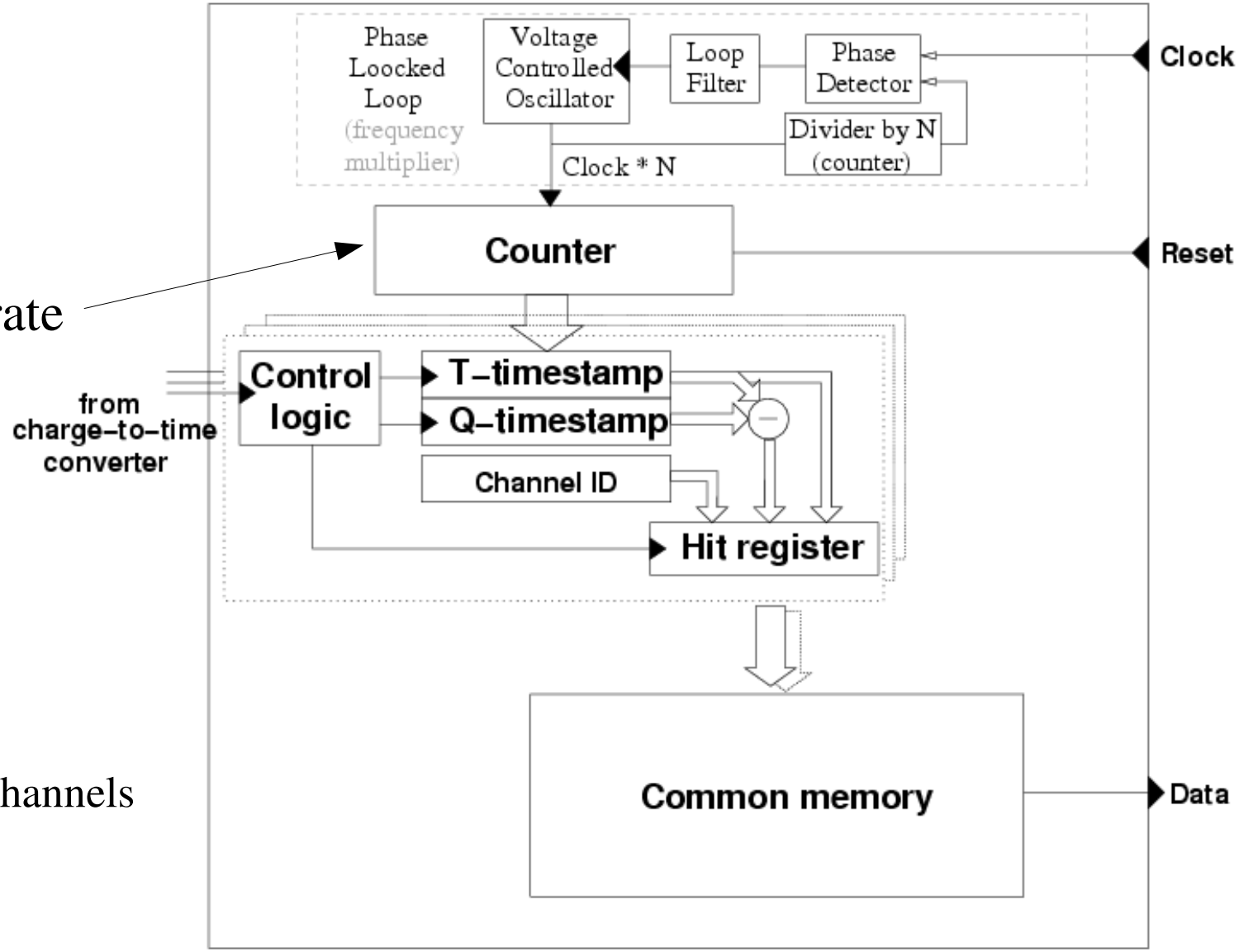
Test with a pulse generator



A possible design of Time-to-Digit Converter

200 Mhz clock rate

(5ns time bin)

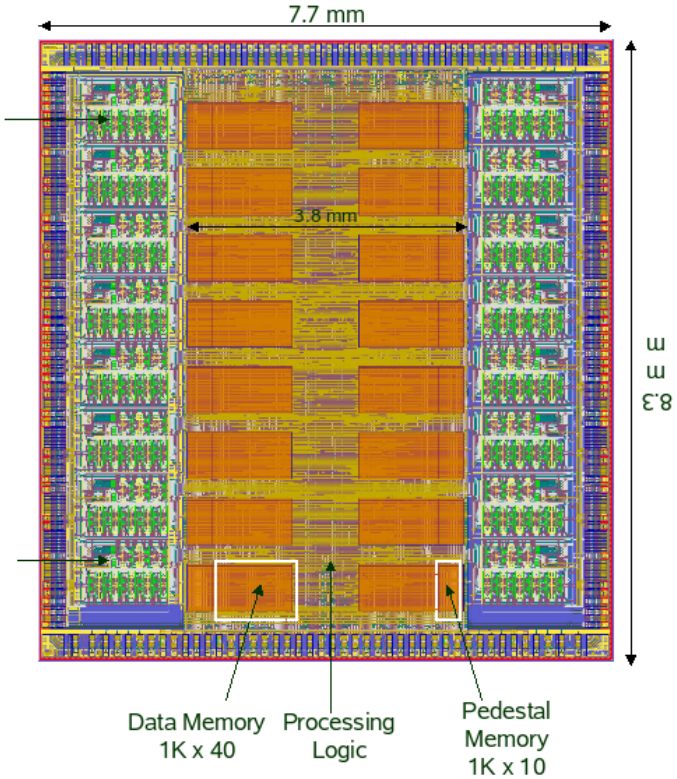


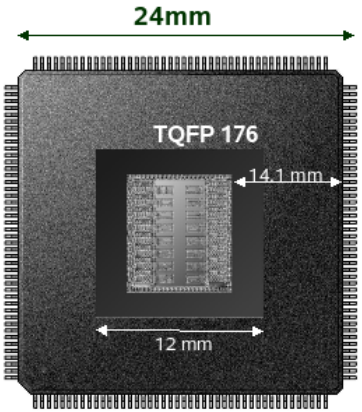
For example: 64 channels

Memory size ? Number of signals to be stored: pad occupancy

TPC readout for ALICE TPC: ALTRO chip

CERN ALTRO chip: Layout and Package





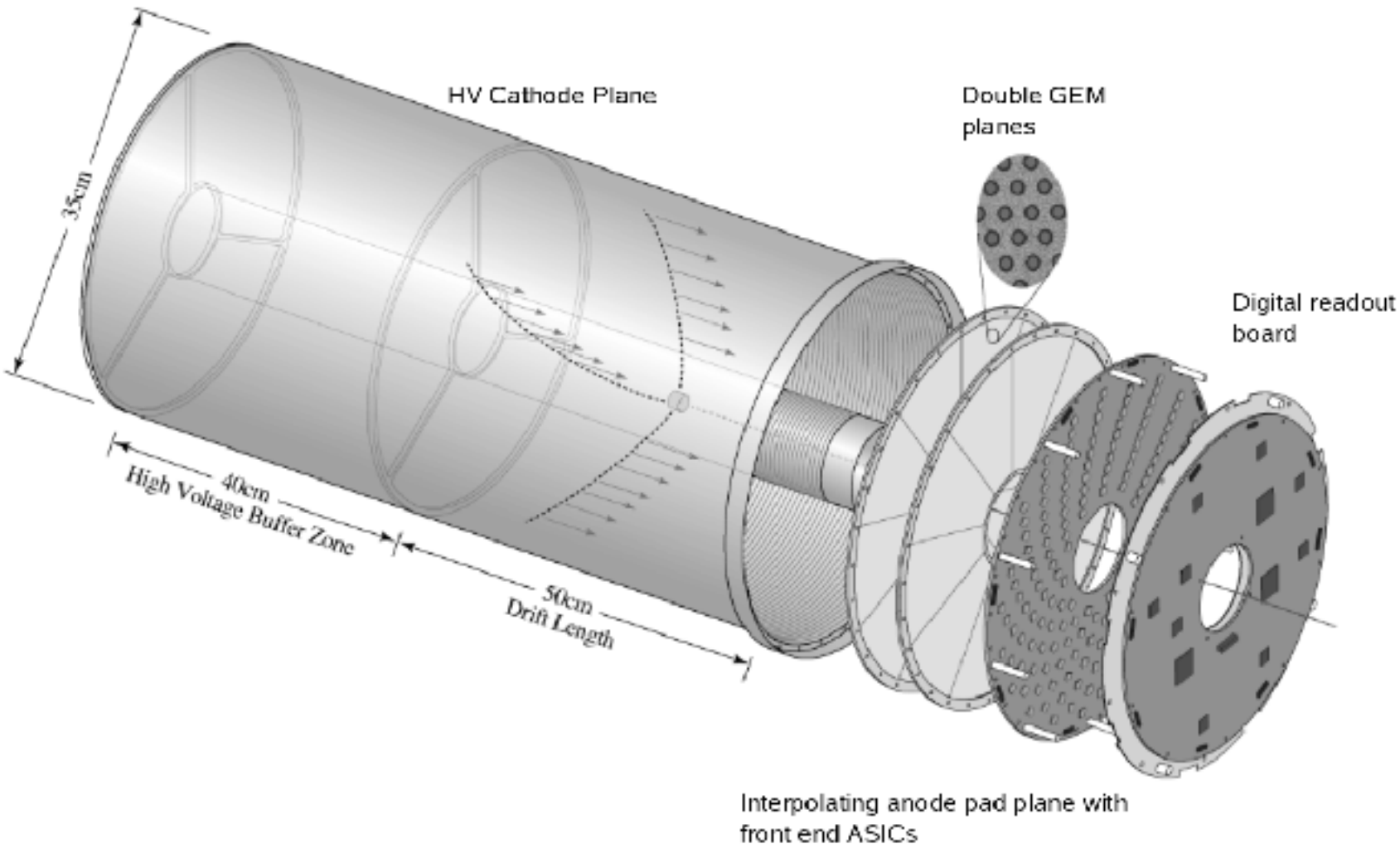
Process	STM HCMOS-7 (0.25 µ)
Area	64 mm^2
Dimensions	7.70 × 8.35 mm^2
Transistors	6 Million
Embedded Memory	800-Kbit
No. ADCs	16
Supply Voltage	2.5V
Power Consumption	260mW @ 10 MSPS
Package	TQFP-176

LECC2002 9-13 September 2002, Colmar-France

Laurent Dugoujon

Larger memory needs larger area of chip

LEGS TPC: readout electronics on the end-plate



Silicon wafers can be thinned down to 20 um

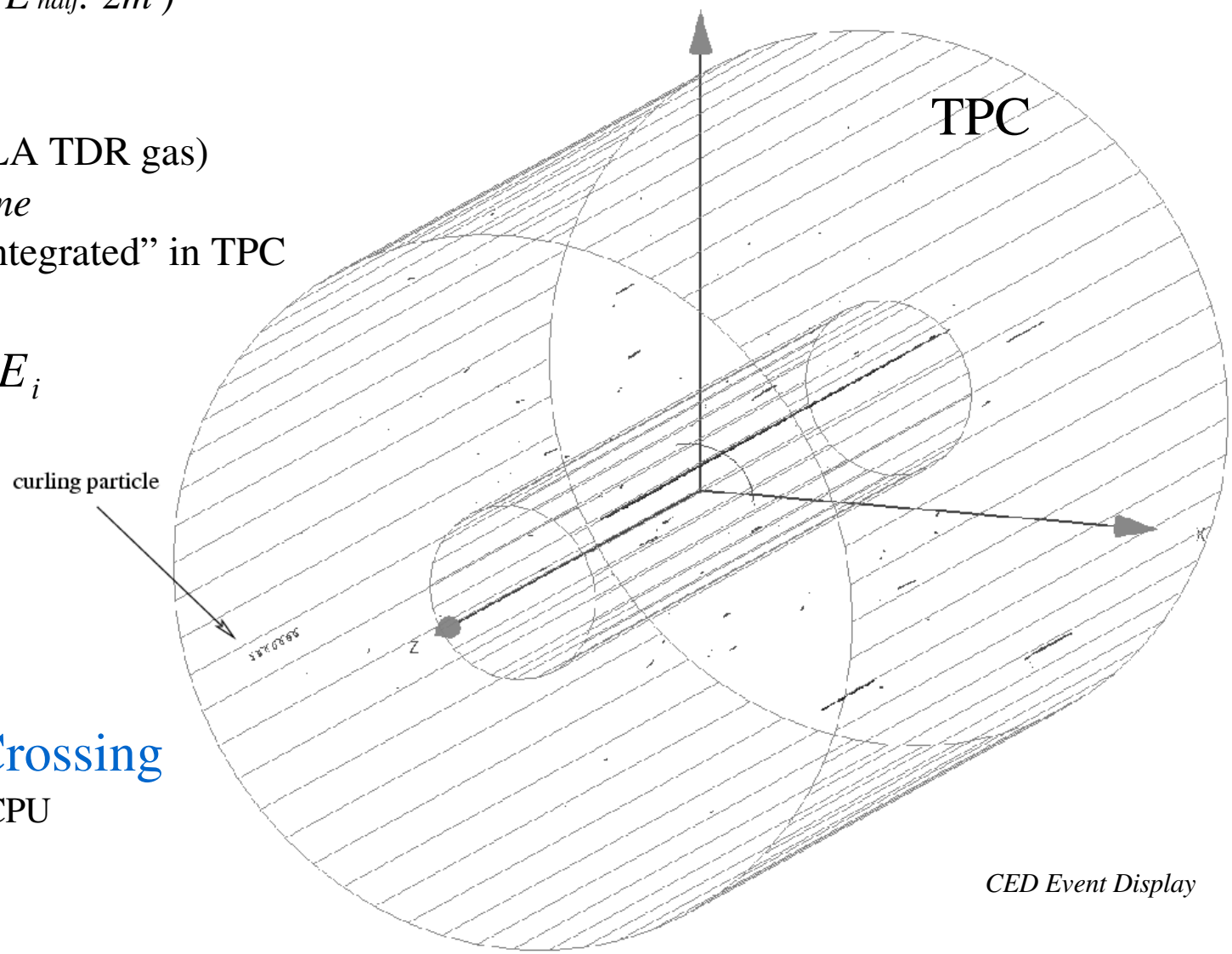
"Three-dimensional integrated circuits"
IBM J. RES. & DEV. VOL. 50 NO. 4/5 JULY/SEPTEMBER 2006

Pair background simulation: GUINEA-PIG/Mokka

GUINEA-PIG: TESLA linac parameters (close to *nominal* parameter set of the ILC RDR)

Mokka: LDC01_02Sc *(L_{half}: 2m)*
QGSP_BERT_HP
TPCCut: 32 eV
V_{drift} = 4.5 cm/μs (TESLA TDR gas)
369 ns bunch crossing time
Hits from 128 BX are "integrated" in TPC

$$X_i, Y_i, Z_i, T_i, dE_i$$



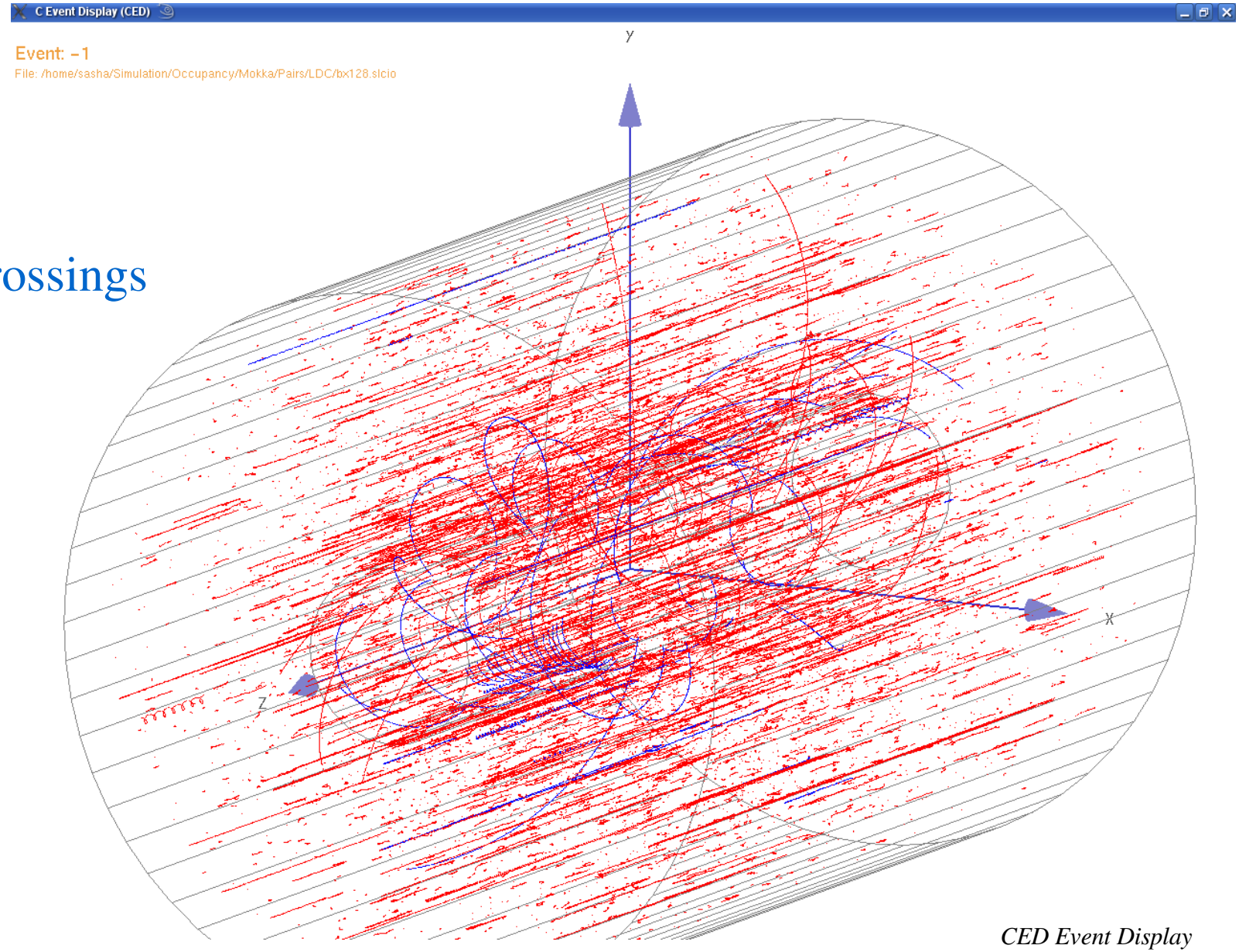
CED Event Display

A single Bunch Crossing

~3 hours on 2.66 GHz CPU

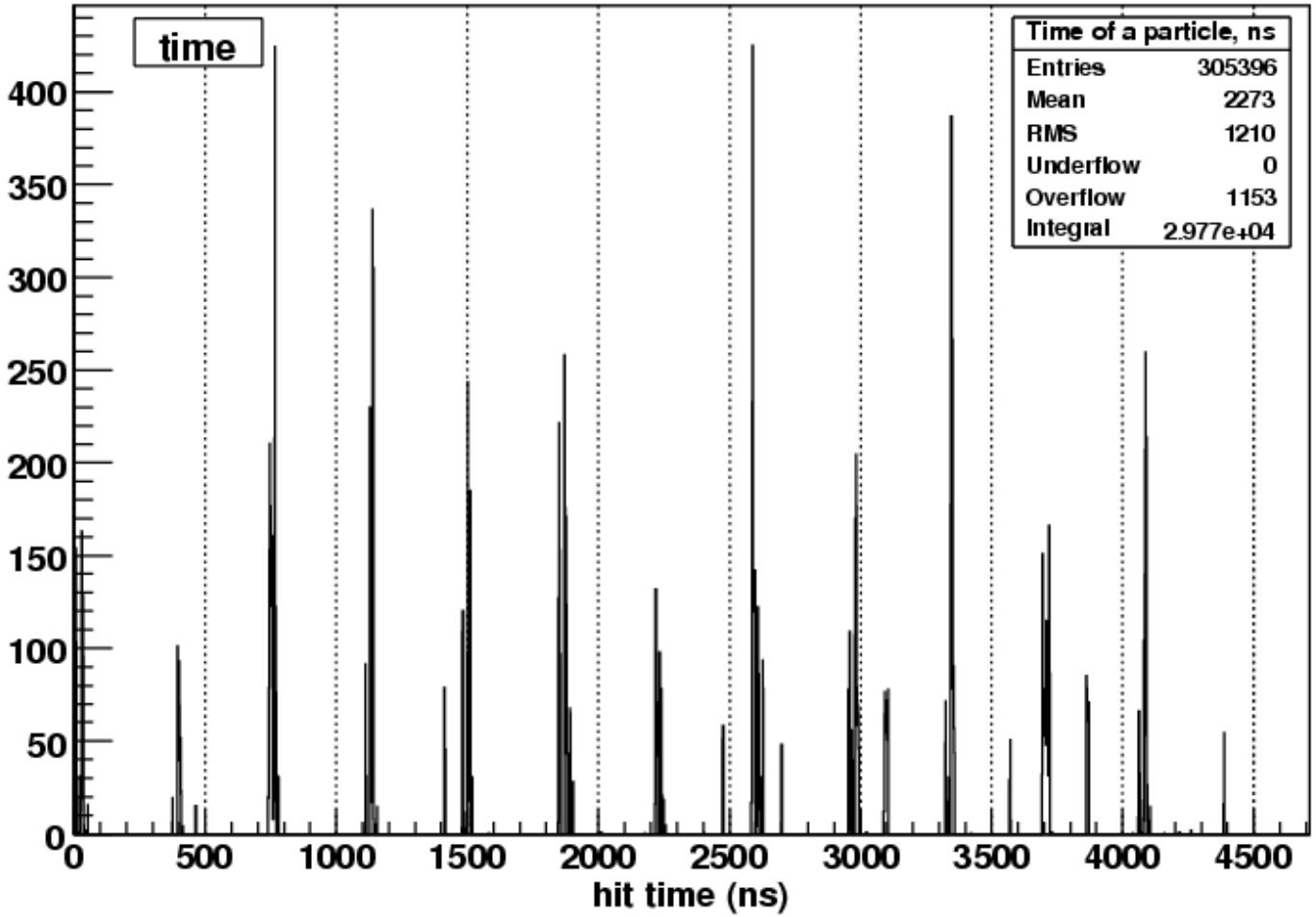
Pair background simulation: GUINEA-PIG/Mokka

128 Bunch Crossings



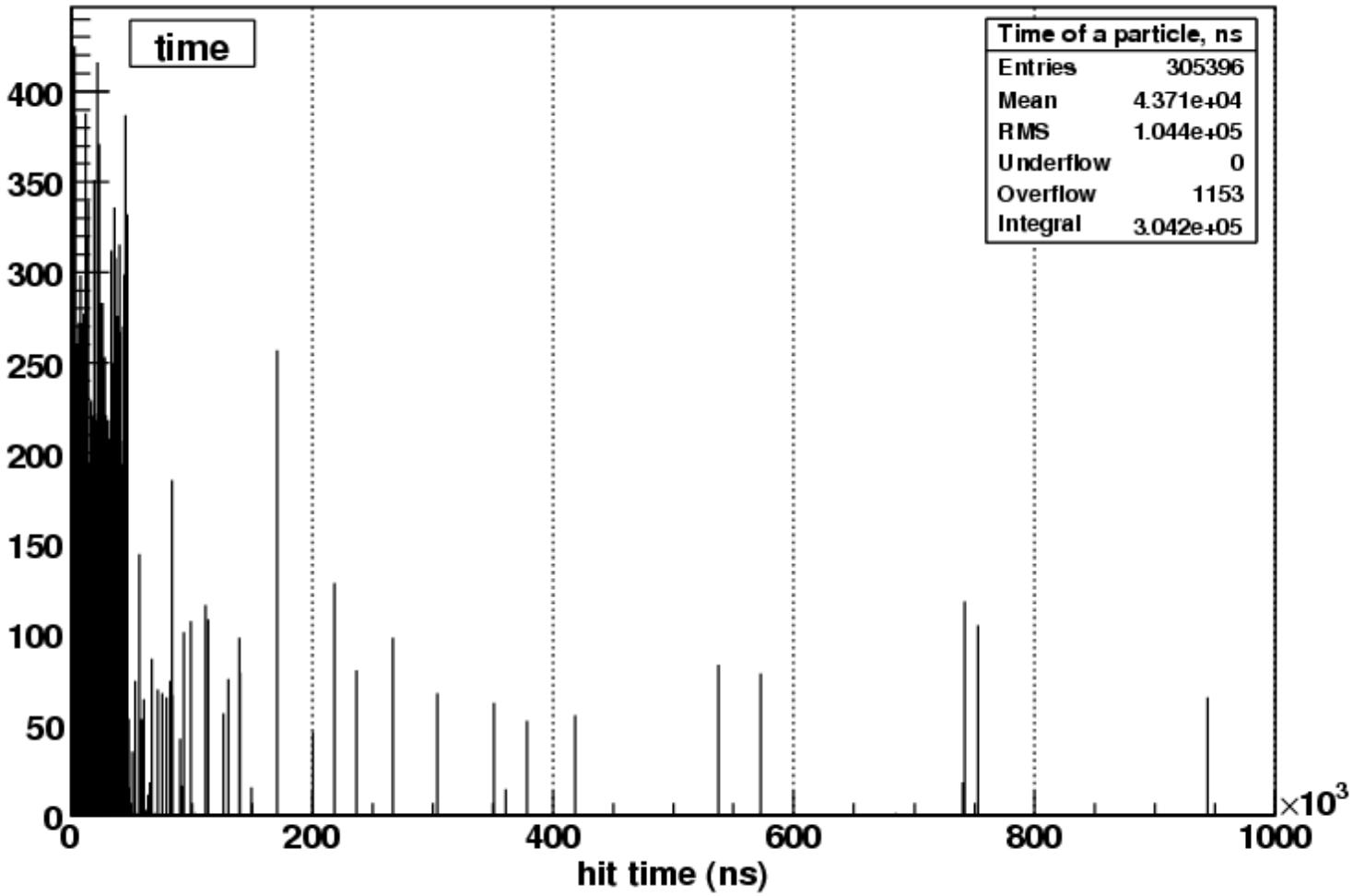
CED Event Display

Pair background simulation: GUINEA-PIG/Mokka



369 ns bunch spacing

Pair background simulation: GUINEA-PIG/Mokka



"Afterglow"

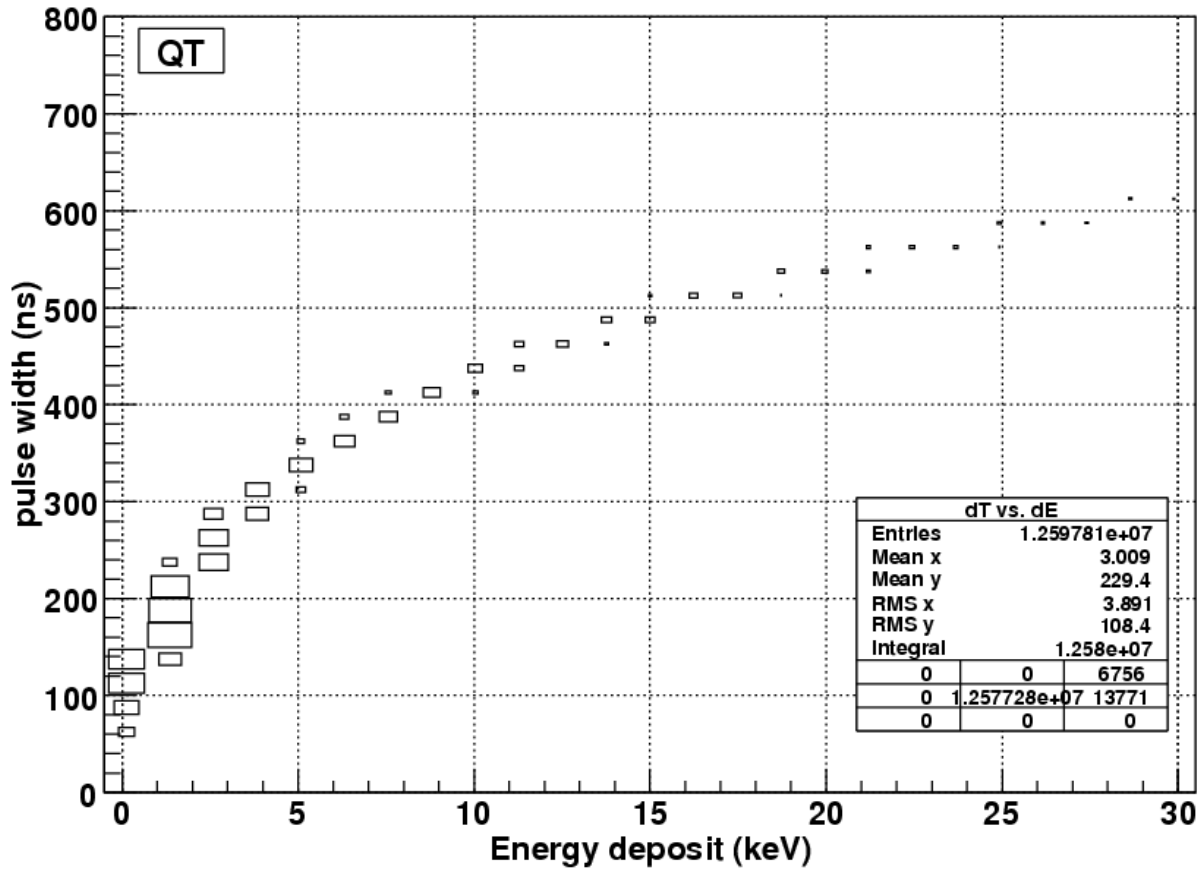
Pair background simulation: GUINEA-PIG/Mokka

Time of appearance
of a hit on a pad is calculated

$$T_{appearance} = \frac{\left(L_{half} - \left|Z_i^{Mokka}\right|\right)}{V_{drift}} + T_i^{Mokka}$$

Hit overlap is processed with knowledge of QT-characteristic

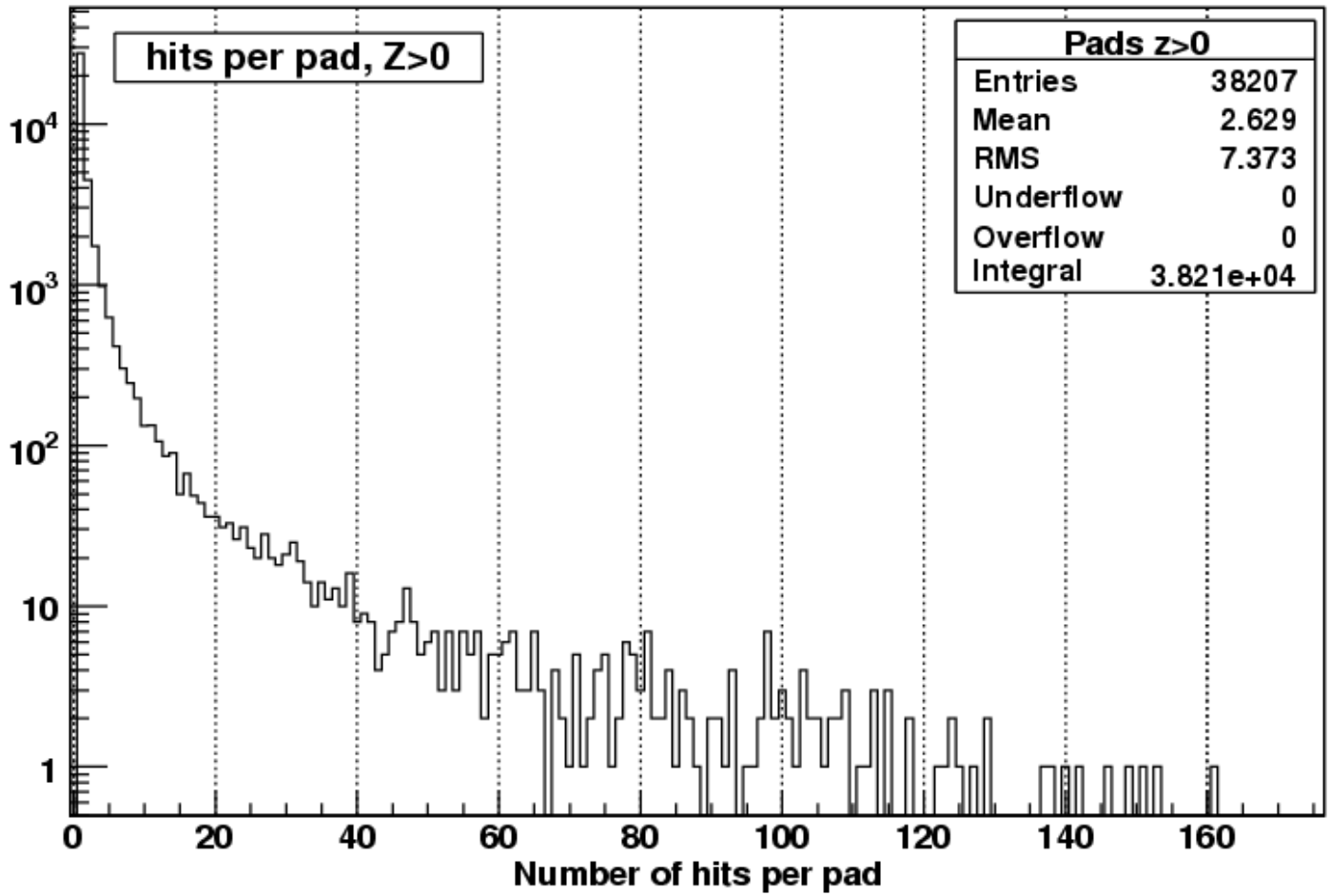
Simple integration:
Energy deposits from all hits within 50 ns time window are summed, pulse width set accordingly



Dead time is variable

hits with very large energy deposits "block" later arriving hits

Pad occupancy

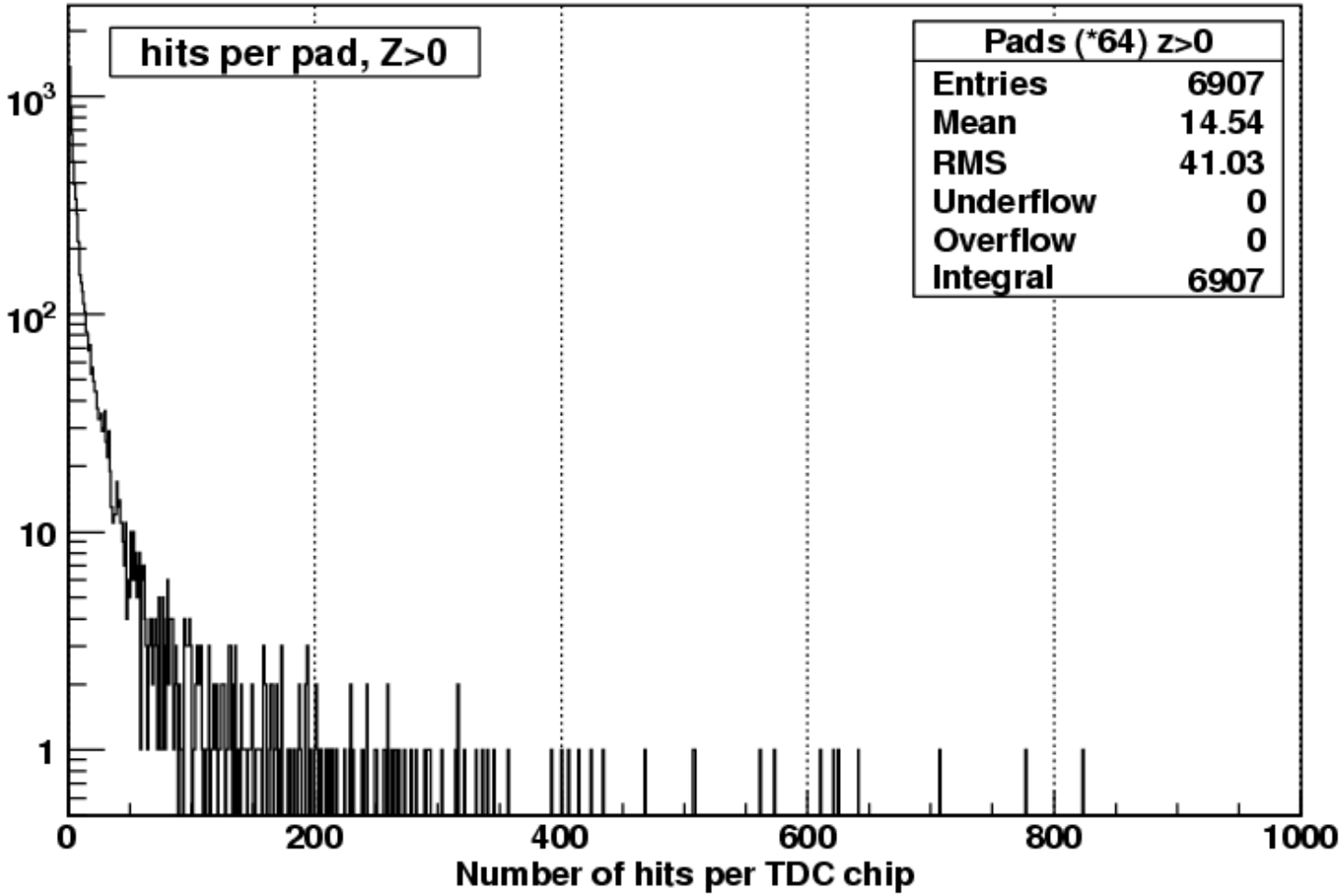


6mm x1 mm pads in LDC TPC

160 * 64 = 10240 hits

Pad occupancy

64 pads (in a pad-row) are served by a single chip



~800 hits per chip per 128 BX

For a bunch train this would give: 2625 (BX per train) / 128 BX * 800 ~ 20 000 TDC words

Conclusion

TDC-based electronics offers an interesting feature of data reduction
though performance might degrade, for example, the double pulse resolution

Simple electronics, low power, low material budget

Number of hits per 128 BX (with common memory TDC): ~ 800 (max.)

number of hits per train ~ 20 000

Even if one takes 10x safety factor, the size of the memory is still small

The *full* bunch train can be calculated easier with GRID, if necessary