WBS Plans for the LLRF System

Stefan Simrock, DESY

Collaboration

DESY

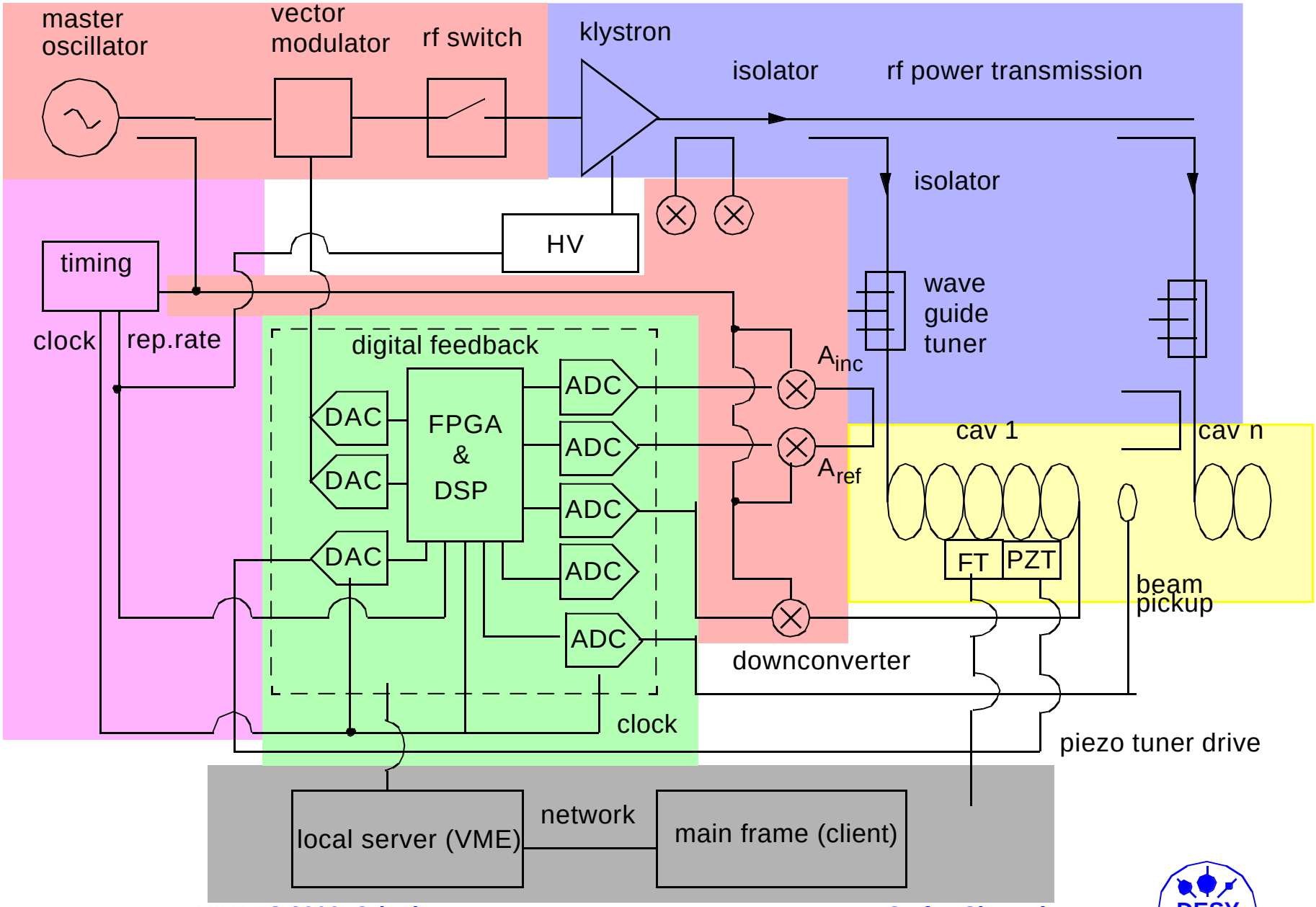
WUT-ISE

TUL-DMCS

PSI

also worldwide participation by
FNAL, KEK, IHEP, ORNL, JLAB ...

RF System Architecture (2)



Work Package Status Reports

WP No. and Name: WP-02: LLRF Preparation Project
MS Project File Reference: WP-2_Plan_V01-02_040715.mpp

Work Package Status Report

XFEL X-Ray Frti-Elsctrsn uur

Planned Tasks/Milestones/Planned Spending for this and the next Reporting Period							
WBS	Description	Milestone?	Planned		Revised End Date	% Completed	Status
			Start Date	End Date			
	Master Oscillator, Frequency Distribution, Timing	D	01.05.04	31.12.06	30.06.07	75 %	behind plan
	Downconverter, Vector-Modulator	□	01.07.04	31.12.06	31.03.07	75 %	behind plan
	Digital Feedback Hardware, Analog IO	□	01.07.04	31.12.06	31.03.07	75 %	behind plan
	Single Bunch Transient Detector	□	01.07.04	31.12.06		100 %	on plan
	Piezo Tuner and Controller	□	01.07.04	31.12.06		100 %	on plan
	Feedback Control Algorithms	□	01.07.04	31.12.06	31.03.07	75 %	behind plan
	Low Level Applications	□	01.07.04	31.12.06		100 %	on plan
	High Level Applications	□	01.07.04	31.12.06		100 %	on plan
	Finite State Machine	□	01.07.04	31.12.06	31.03.07	75 %	behind plan
	Requirement Document	□	01.07.04	31.12.06	31.03.07	75 %	behind plan
	Conceptual Design	□	01.07.04	31.12.06	31.03.07	75 %	behind plan

Milestones 2006

Operation of ACC1 with SIMCON 3.1	July 06
Operation of RF Gun with SIMCON 3.1	July 06
SIMCON 3.1 Operational at PITZ RF Gun	Mar 06
SIMCON 3.1 at FNAL	Mar 06
XFEL LLRF Requirement Document	Nov 06
Concept for Packaging (Standardisation for Crates etc.)	July 06
On-line gamma/neutron dosimetry in VUV-FEL (5x)	Mar 06
Operation of klystron 4+5 with FSM	Mar 06
On-line diagnostics LLRF at VUV-FEL	Mar 06
Transient meas. ACC1 in operation	July 06
Prototype of new downconverter with new IF scheme	Mar 06
Prototype of 8-channel downconverter with ADC , FPGA	July 06
Fiber optic reference system in operation	April 06

Highlights

- Third Generation RF Control (WUT-ISE ...)
- Single Bunch Transient Detection (TUL-DMCS ...)
- Multichannel Downconverter (WUT-ISE ...)
- Stable M.O. and Frequency Distribution (WUT-ISE ...)
- RF Gun Control (PSI ...)

- Automation of LLRF Control (TUL-DMCS ...)
- Exception handling (DESY ...)
- Data Management Development (TUL-DMCS ...)
- Control Optimisation (DESY ...)

- Cost and Reliability (DESY ...)
- Radiation Effects on Electronics (ALL)

Proposal for LLRF Development for FP7

Objectives of LLRF Development

Advance RF Control Technology in the areas of hardware and software to meet the requirements for linear collider and X-ray FEL.

- o Develop LLRF implementation as HA ATCA System
- o Develop concept for modular system
- o Develop multi-channel ASIC version of downconverter
- o Develop multi-channel downconverter board based on ASIC do standard component
- o high degree of automation for large scale system, operability
- o reliability and availability optimization and cost reduction
- o technical performance, pushing the envelope of performance

	travel	hardware [KEuro]	Personyears	
O HA (High Availability) LLRF Implementation in ATCA	17.0	680	140	
- Architecture (incl. standardization), ATCA and uTCA	1.0	20	20	DESY T.Jezynski
- Development of ATCA carrier boards with FPGA,DSP	3.0	130	20	IPNO
- Fast analog IO and digital IO (100 MHz, 14-bit)	2.0	70	10	ISE
- Ultra fast analog IO (2 Gs, 10 bit)	1.0	50	10	INFNP
- Neutron detector board with customized ASIC	4.0	100	20	DMCS
- Gamma detector board	1.0	30	10	DMCS
- Integration of downconverters and upconverters	1.0	40	10	DESY Mathias Hoffman
- Digital signal processing	2.0	30	10	DCMS
- Communication	2.0	80	20	IPNO
- Redundancy and self diagnostic	2.0	40	10	DMCS
- HA Design (HW, SW), QA and QC	2.0	90	10	DESY T.Jezynski
o High precision Timing and Synchronisation for LLRF	5.0	220		
- Integration MLO, MO, Timing	1.0	70	10	ISE
- Integration pulsed optical with RF	1.0	30	10	DESY H.Weddig
- Cal. Reference and LO to downconverters	1.0	50	10	DESY F.Ludwig
- Clock synthesizer for LLRF ADCs	1.0	30	10	ISE
- Int. with ultrast. timing and clock, event, (data ?)	1.0	40	10	ISE
o Software Architecture and Implementation Strategies	16.0	430		
Software architecture	3.0	20	20	DESY Markus Hoffman
Software development tools	1.0	50	10	DMCS
Software documentation tools	1.0	40	10	DMCS
Distribution of Algorithms (FPGA, DSP, CPU)	2.0	20	10	ISE
Software/hardware co-design	2.0	80	10	DMCS
Communication protocols	1.0	60	10	ISE
Algorithm development	5.0	100	10	DESY W.Koprek
Diagnostics (HW & SW)	1.0	60	10	DESY T.Jezynski

o Precision RF Field Measurement	5.0	190		
Low noise, low drift downconverter (field detector)	2.0	60	10	INFNP
Low cost, low real estate, multi-channel downc. (ASIC)	2.0	80	10	DMCS,ISE
Transient detection (low cost multichannel)	1.0	50	10	DMCS,DESY
P.Morozov, M.Grecki				
O Procedures for Commissioning and Operation	10.0	320		
-				
Commissioning and Operation Procedures	2.0	80	10	DESY
V.Ayvazyan				
Automation of Operation	2.0	20	10	DMCS
Cavity simulator including rf front end	2.0	90	10	ISE
Interfacing to other accelerator subsystems	2.0	40	10	DESY
P.Pucyk				
Interlocks	1.0	20	10	ISE
Monitors	1.0	70	10	ISE
Fast Frequency tuner	4.0	160		
Piezo driver	1.0	50	10	DMCS
Increased stroke of PZT	?	?	?	?
Segmented fusing of piezostacks	1.0	40	10	DMCS
Microphonics control	2.0	70	20	DMCS
Beam feedbacks for LLRF	6.0	160		
Beam feedback Concepts	1.0	20	10	PSI
Beam diagnostics and monitors (Int. with LLRF)	3.0	60	10	PSI
Beam feedback prototype impl. At FLASH	2.0	80	10	PSI
	63.0	2010		

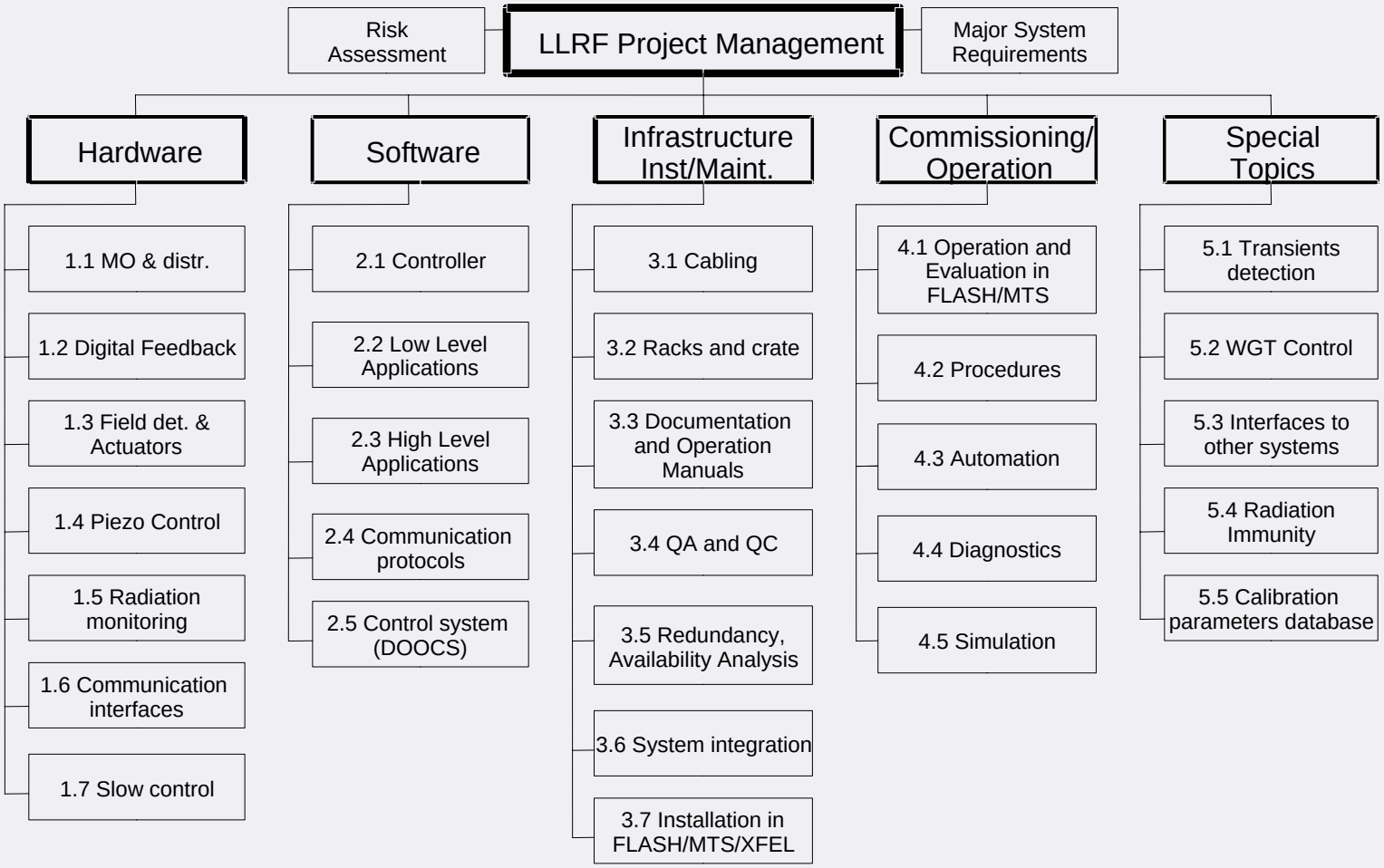
IPNO Orsay, INFN Padova, PSI, other IN2P3

1. HA (High Availability) LLRF Implementation in ATCA

   The demand for high availability, modularity, standardization and long time support favors the choice of the ATCA and uTCA standard with carrier boards and AMC modules. This technology is basis for the ILC technical design.
   Presently none of the required AMC boards for ADCs, DACs, downconverters, clock synthesizers etc. are available. Therefore a development of these boards using stete-of-the-art technology is necessary.
   a. Architecture (incl. standardization), ATCA and uTCA
   b. Fast analog IO and digital IO
   c. Integration of downconverters and upconverters
   d. Digital signal processing
   e. Communication
   f. Redundancy and self diagnostic
   g. HA Design (HW, SW), QA and QC
2. High precision Timing and Synchronisation for LLRF

   Precision timing signals in form of clocks and event triggers are required for digital control system to guarantee synchronicity of ADC data with the electron bunches and allow for digital rf field detection. The clock signals are in the 100 MHz range require stabilities of the order of a few picoseconds. Also available must be

New WBS for LLRF under Discussion



XFEL project

LLRF System
Project Plan for *WP 2.1*
Controller

Proposed by:
Name of faculty/institution: DMCS

Date: April 14, 2007
Description version: Ver. 1
Approved:

Introduction

The controller is an universal platform for algorithm integration. It provides control signals which drive vector modulator. It uses signals from other functional blocks (such as field detection, different measurements) to enhance cavity field control quality. The main goal of the project is to prepare universal and flexible cavity field controller, which can be used for XFEL facility. Controller provides preprocessed measurement signals for other blocks which execute different algorithms. There are two major timing constraints: up to 5 MHz output update frequency to match bunch repetition rate of XFEL and pulse repetition rate from 10 to 100 Hz. The controller has to provide different modes of control such as AP (amplitude-phase), IQ control and mixed solutions, together with possibility of open and closed loop operations. In addition to GDR mode the following operation modes will be supported:

- Self Excited Loop (SEL) operation,
- Frequency Sweep Mode.

It will provide interfaces to multiple external subsystems such as beam loading compensation, klystron and downconverters linearization, embedded platform and DSP processor (used for off-line algorithm execution). Controller architecture will be distributed over many subcomponents to accommodate flexible distributed systems such as ATCA system. Links between these subcomponents will be implemented using high bandwidth links (PCI Express, Gigabit ethernet, RocketIO or custom protocol when low latency is required).

During design process, the new controller's architecture will be proposed. R&D phase allows to select the most suitable link and protocol. Mathematical models of algorithms' subcomponents will be developed and simulated. This will lead to final software implementation. All the parts linked together will be ready for tests using both cavity simulator and FLASH accelerator. As a final product complete software system for field regulation will be delivered.

Background

During last months, several research projects were performed. First of all, basic implementation scheme was proposed and tested. It is flexible and parametrized, so it can be easily extended. Moreover basic tests for communication protocols were executed and latency parameters were measured. This led to the first attempts of communication between two boards (FPGA chips). After the delivery of SIMCON DSP board, fast double data rate serial protocol was implemented and tested. Currently, DSP can support FPGAs during the operation. All of presented research were used for prototype implementation of the controller which currently is installed in ACC1 module of FLASH accelerator. It supports 1 to 16 channels using IQ or AmplitudeQ control. In addition it has some basic correction modules for adaptive feedforward and klystron linearization. Basic exception handling was also implemented and some test using higher IF were performed.

During next project phases some additional research must be done. Most important from the implementation side of view are further link studies. Performance of the transmission modules built in the next generation of FPGA chips must be evaluated and the primary protocol should be chosen. Custom low latency link must be designed and implemented. Moreover some issues concerning partial reconfiguration have to be cleared. It will allow to change functionality of the controller on the fly – without the need of shutdown

of RF-station. There is some research concerning other components needed, but that is covered by other proposals.

Detailed project description

2.1 Controller

2.1.1 Data distribution scheme

For the distributed hardware system, special infrastructure for data distribution between boards must be developed. On top of the communication protocols (2.1.5), dedicated interfaces responsible for data acquisition and provision will be placed. Both subtasks below may use the same hardware resources, so they must be closely developed.

2.1.1.1 Data acquisition system

This subsystem is responsible for data transfers between operation parts of the controller and data acquisition boards. The main requirement of this system is to provide communication channels to hardware resources provided for data storage. Communication links for this purpose have high requirements on bandwidth but low requirements on latency of the links

2.1.1.2 Control parameters distribution system

Similar to the previous one, the subsystem is responsible for control parameters distribution. This includes control tables and parameters for submodules of the controller. Requirements for the module are similar to module (2.1.1.1)

For the development of the subtask 2.1.1 the following hardware components will be required:
- PCB board with FPGA and memory chips considered for final XFEL system
- logic state analyzer with sampling frequency higher than typical DDR or QDR memories

Engineers for this task: WJ

2.1.2 Implementation scheme

For the large software project, it is necessary to work out style of the implementation. This will help to integrate different modules provided by different engineers and will make the whole project more clear.

2.1.2.1 Tools

As the result of this subtask, the decision concerning software tools will be made. Consultation with engineers participating in the project will be made and the set of tools allowed for usage will be defined.

2.1.2.2 Coding styles

Coding styles will be defined, starting on source code formatting, style of module declaration and others.

For the development of the subtask 2.1.2 the following software components will be required:
- software licenses

Engineers for this task: WJ, GJ

2.1.3 User FPGA Code

User FPGA will be responsible for the core of the control algorithm. Interfaces between User and Firmware FPGA must be defined. The following functionality for User FPGA and AMC FPGAs will be provided.

2.1.3.1 Field detection

This submodule of the controller is responsible for the sampling and detection of the field components for each cavity.

2.1.3.1.1 IQ detection

IQ detection subtask will result in the development of the universal IQ detector parametrized to be used with the wide range of IF frequencies. It will be capable of continuous (full clock frequency) and pulsed (decimated clock) operation

Engineers for this task: WK

2.1.3.1.2 Rotation Matrix

Rotation matrix provides means of calibration for input channels. The main purpose of this module is to perform complex multiplication for each channel.

Engineers for this task: WJ

2.1.3.1.3 Vector sum calculation

The module is responsible for Vector Sum calculation. It uses information for each channel to provide complex vector sum of the field in the cavities in 4 crymodules. If necessary it converts the result to different coordinates (Amplitude-Phase, etc)

Engineers for this task: WJ

2.1.3.1.4 Coordinate conversion

Defining Deliverables (1)

Phase	Phase description	Month/phase	Total months	Date
Ph. 0	Project plan (MS Project)	0 m	0 m	09/2007
Ph. 1	Requirements (Rhapsody, Doors)	1-2 m	1 m	09/2007
Ph. 2	Conceptual design	1-2 m	2 m	10/2007
Ph. 3	R&D of critical components	1-6 m	6 m	2/2008
Ph. 4	Specification	2-3 m	6 m	2/2008
Ph. 5	Detailed design (documentation)	1-6 m	8 m	4/2008
Ph. 6	Prototype	1-3 m	12 m	8/2008
Ph. 7	Evaluate prototype in lab. test	1-2 m	14 m	10/2008
Ph. 8	Evaluate prototype in accelerator	1-2 m	14 m	10/2008
Ph. 9	Improve design	1-2 m	17 m	01/2009
Ph. 10	Repeat 7-9 until design is finalized	n x (1-3) m	n=0	n=0

Defining Deliverables (2)

Phase	Phase description	Month/phase	Total months	Date
Ph. 11	Procure components	1-2 m	18 m	02/2009
Ph. 12	Produce several pre-production systems	1-6 m	20 m	04/2009
Ph. 13	Perform quality control of fab. systems	1-2 m	26 m	10/2009
Ph. 14	Evaluate systems in test stand (test report)	1-2 m	28 m	12/2009
Ph. 15	Full production run	1-6 m	30 m	02/2010
Ph. 16	Quality control	1-2 m	32 m	04/2010
Ph. 17	Install systems	1-4 m	36 m	08/2010
Ph. 18	Commission systems	1-4 m	40 m	12/2010
Ph. 19	Operate systems	not spec.	?	?
Ph. 20	Maintain systems	not spec.	?	?
Ph. 21	Upgrading systems	not spec.	?	?

Project Report

The Low Level Radio Frequency System of the DESY X-Ray Free Electron Laser XFEL

(Industry Study)

by

Valeri Ayvazyan, Markus Hoffmann, Tomasz Jeyzinski and Stefan Simrock

DESY, Hamburg

and

Bachtior Aminov, Adrian Knack, Helmut Piel and Nico Pupeter

Cryoelectra GmbH, Wuppertal

Cryoelectra Internal Report March 2007

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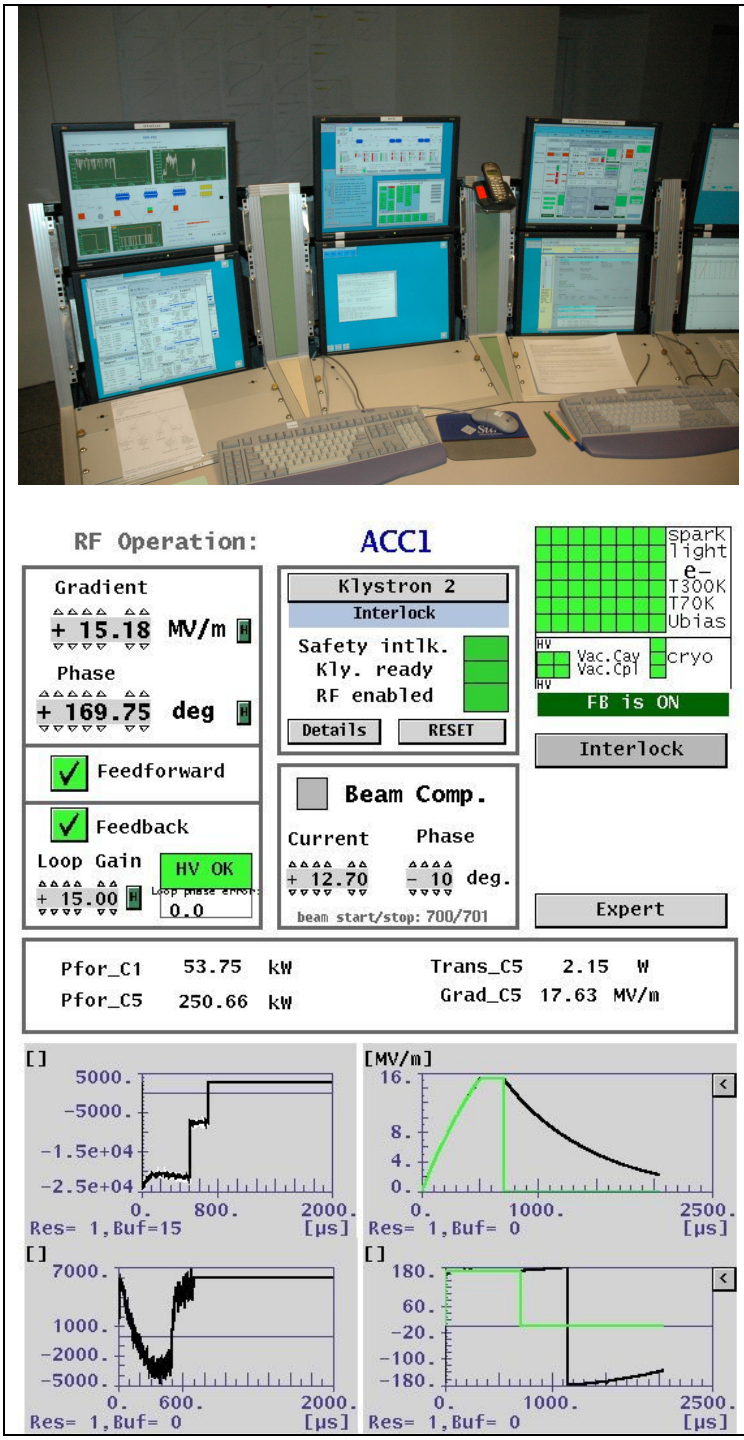


Figure 8 View into a section of the main control room of Flash showing the graphic user interfaces of DOOCS (Distributed Object Oriented Control System) and LLRF control monitor

7.1.1 The Standard RF Station

Figure 9 shows the communication links between the different elements of a standard RF station. All of these stations are controlled by the main control and receive their timing signals from a common master oscillator.

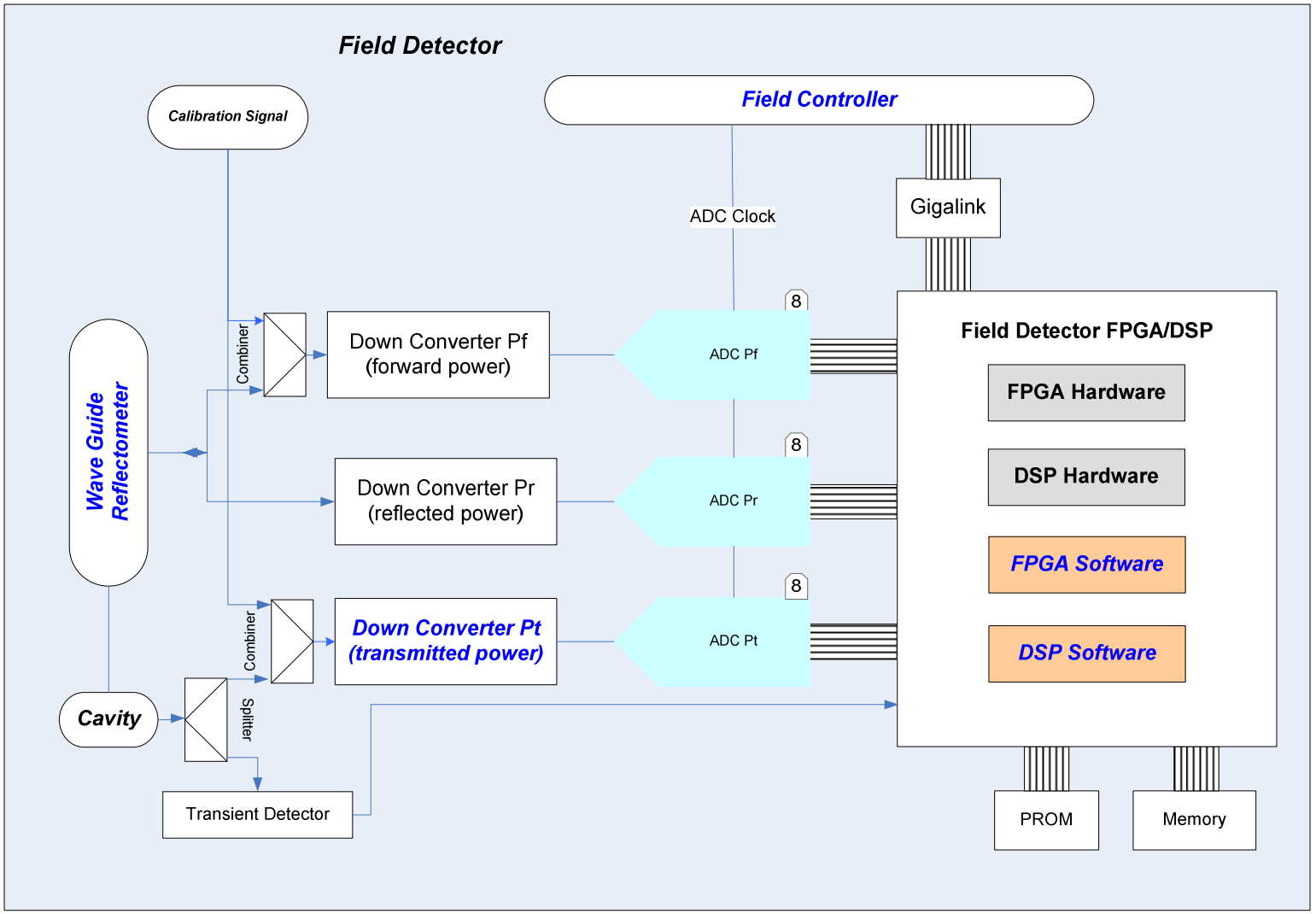


Figure 13: Block Diagram of the Field Detector

16.1 List of LLRF functions

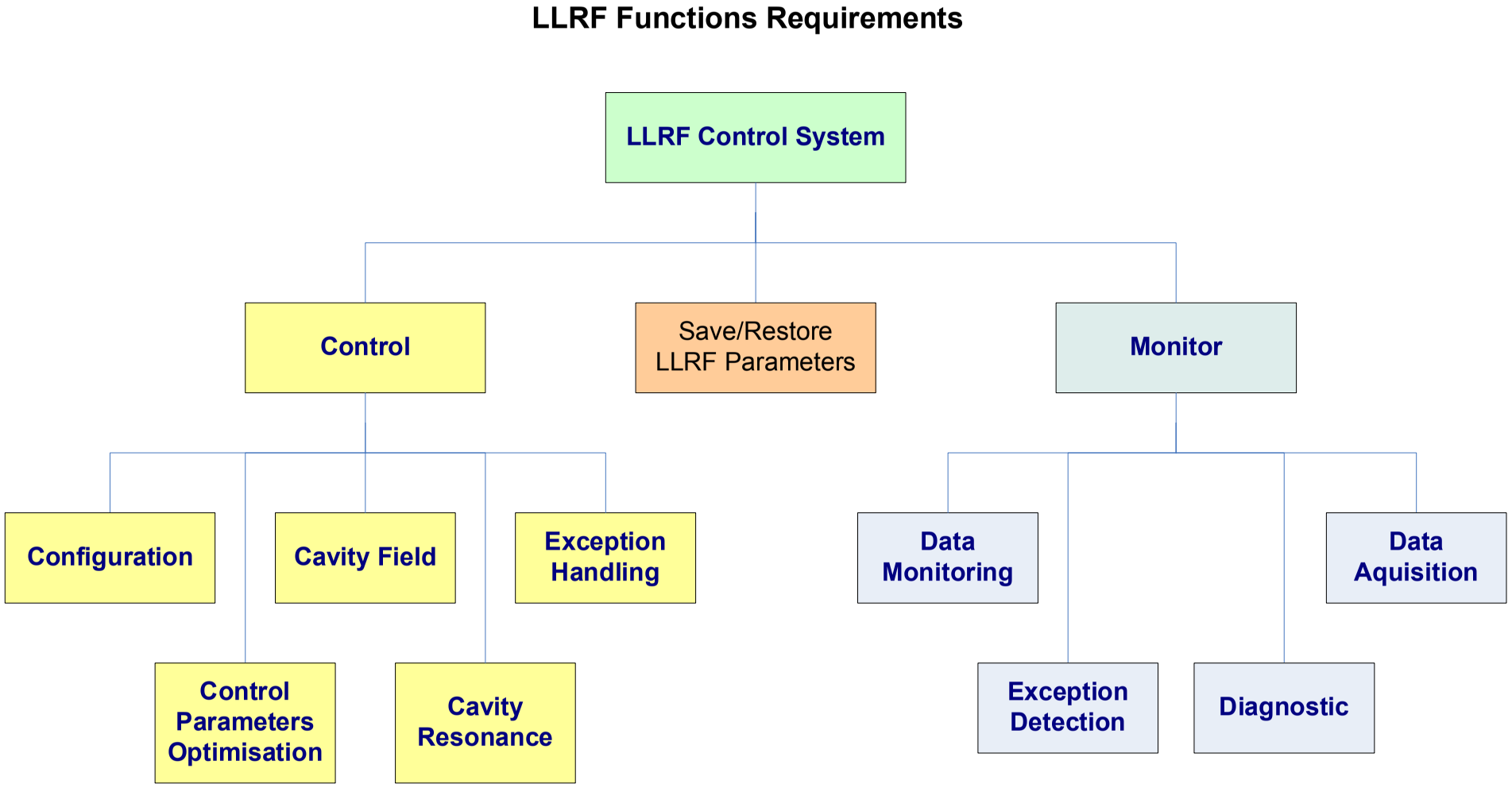
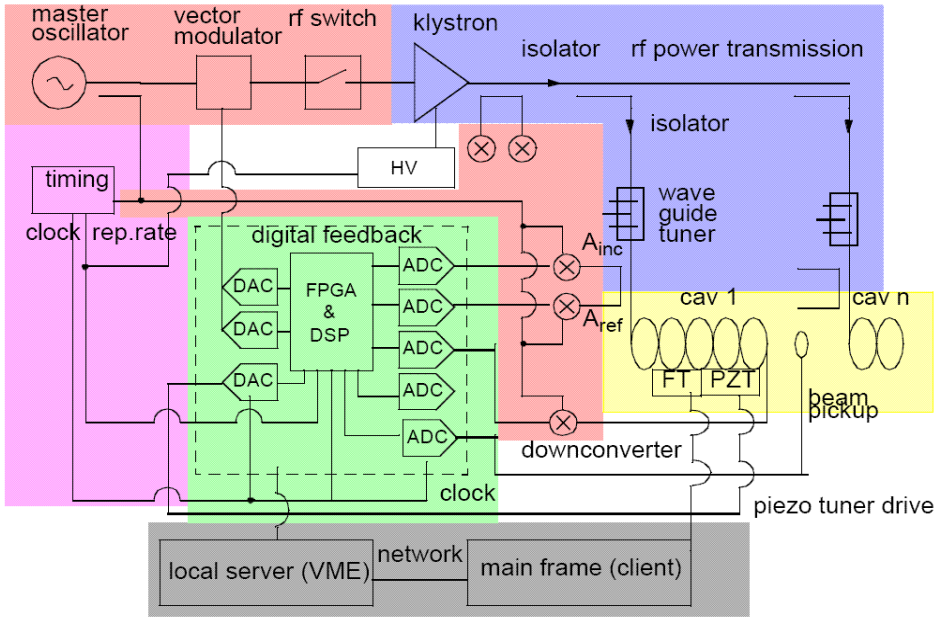


Figure 42 Communication Diagram of the LLRF software

LLRF algorithms



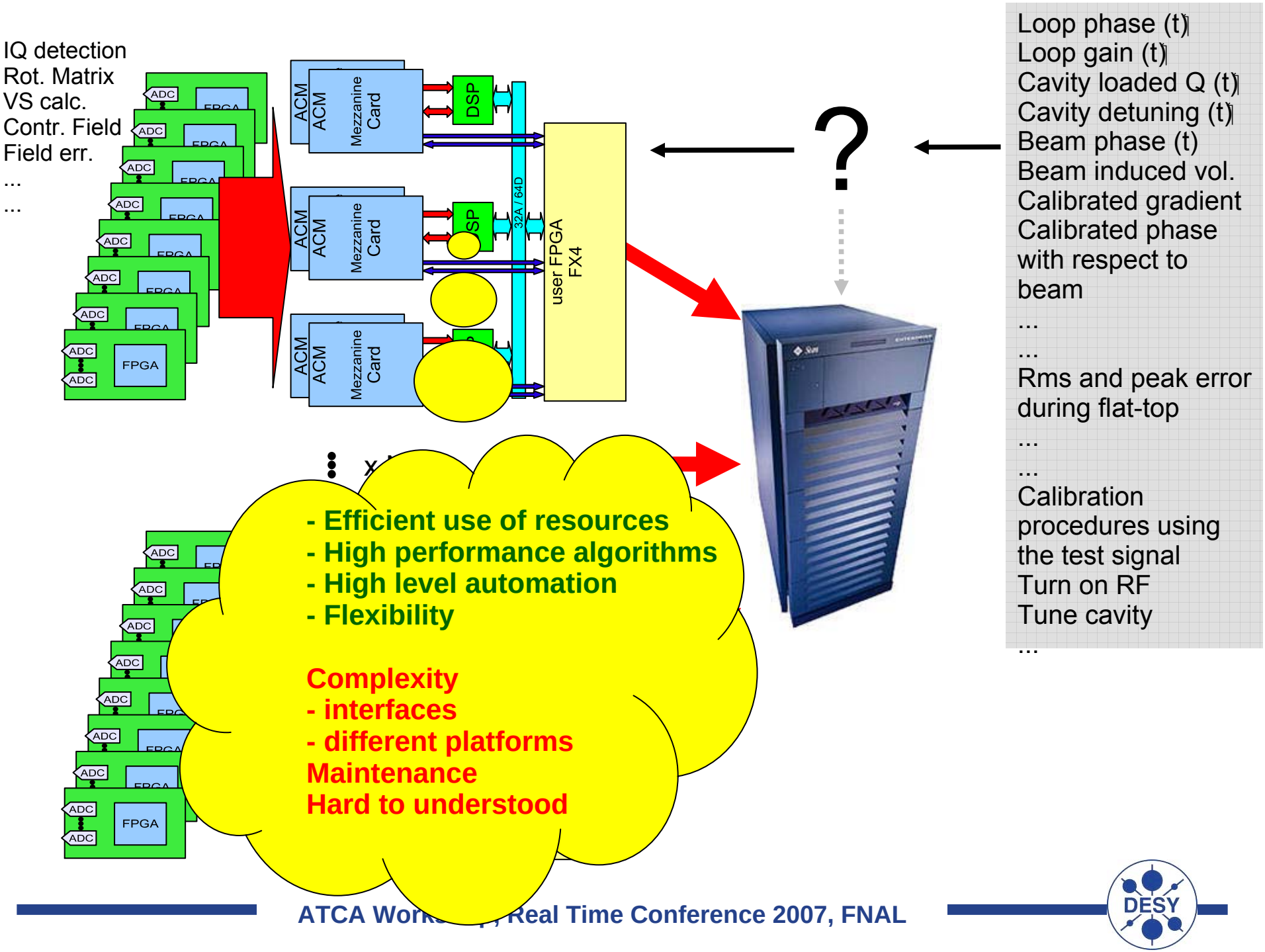
D. High level procedures
- (1) Adaptive feedforward
  - (a) response matrix or T.F. based
  - (c) robustness
  - (d) different beam modes
- (1) System identification
  - (a) beam phase and current
  - (b) loaded Q
  - (c) incident phase
- (3) Waveguide tuner control
- (4) Momentum management system
- (5) Field control parameters optimization
- (6) Operation at different gradients
- (7) Operation at the performance limit
  - (a) maximize availability
  - (b) maximize field stability
- (8) Hardware diagnostics
- (9) On-line rf system modelling
- (10) Automated fault recovery
- (11) Finite state machine

C. Cavity Resonance Control
- (1) Slow tuner
  - (a) maintain average resonance frequency (pre-detuning)
  - (b) maximize tuner lifetime
- (2) Fast tuner (ex. piezoelectric tuner)
  - (a) dynamic Lorentz force compensation
  - (b) microphonics control
  - (c) minimize rf power required for control

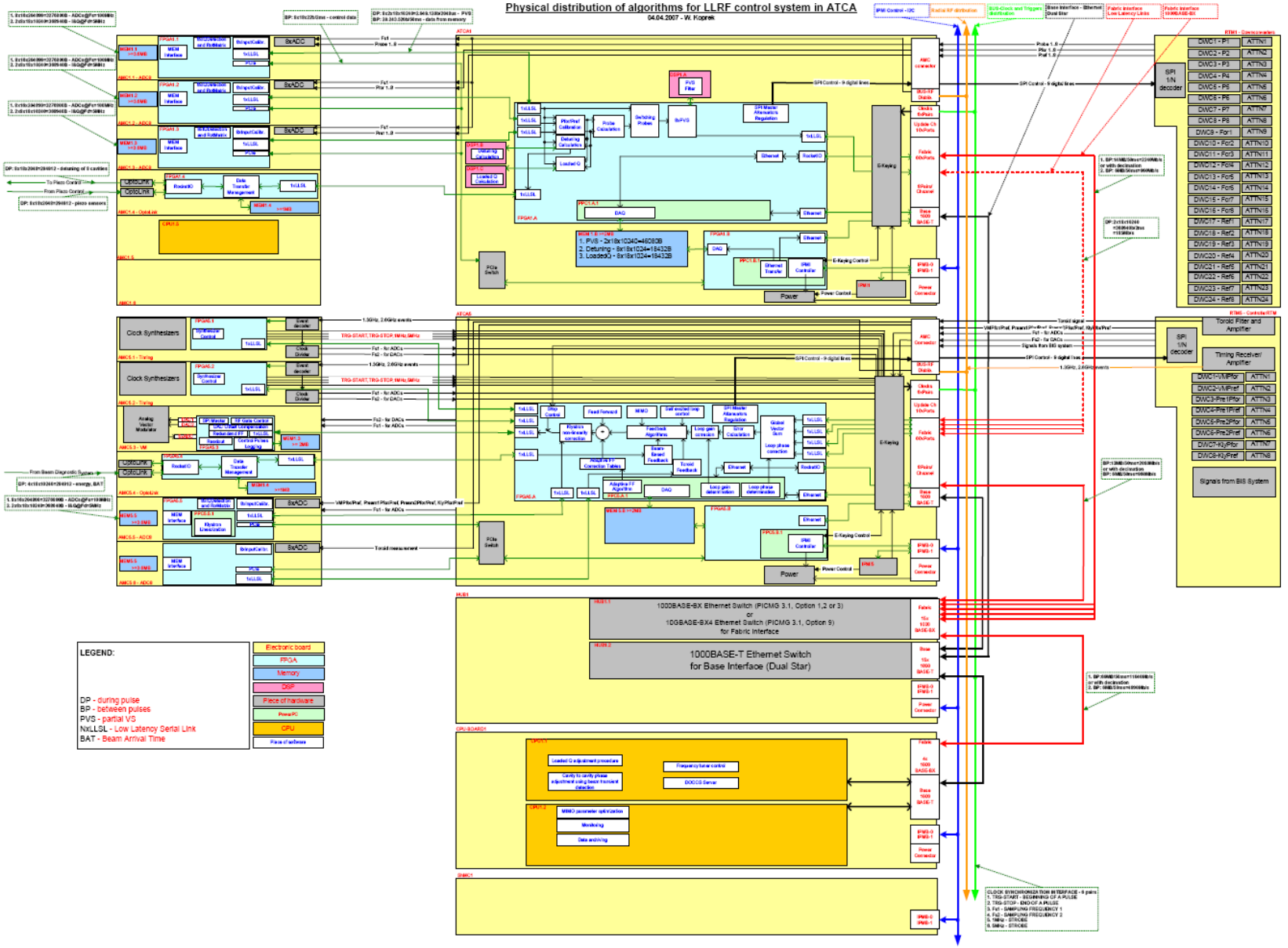
E. Other
- (1) RF System Database
  - (a) calibration coefficients
  - (b) subsystem characteristics
- (2) Alarm and warning generation
- (3) Control System functions

A. FIELD CONTROL ALGORITHMS
- (1) Feedback
  - (a) PID filter
  - (b) Kalman filter
  - (c) adaptive filters
  - (d) optimal controller
- (2) Feedforward
  - (a) beam loading compensation
- (3) Beam based feedbacks
  - (a) rf phase feedback
  - (b) beam energy feedback
  - (c) bunch length feedback
- (3) Klystron linearization
- (4) Exception handling
  - (a) quench detection and handling
  - (b) error from beam loading

B. LLRF System Measurement Algorithms
- (1) Loop phase rotation matrix
- (2) Field calibration rotation matrix (based on rf, beam based transients, and spectrometer)
  - (a) gradient calibration
  - (b) phase calibration
- (3) Vector-sum calculation
- (4) Meas. of incident phase (vector-sum !)
- (5) Beam phase measurement
- (6) forward/reflected power calibration
  - (a) correct for directivity of couplers
- (7) Cavity detuning
  - (a) average during pulse
  - (b) detuning curve during pulse
- (8) Loaded Q


IQ detection
Rot. Matrix
VS calc.
Contr. Field
Field err.
...
...
ADC
FPGA
ACM
Mezzanine Card
DSP
32A / 64D
user FPGA FX4
?
Loop phase (t)
Loop gain (t)
Cavity loaded Q (t)
Cavity detuning (t)
Beam phase (t)
Beam induced vol.
Calibrated gradient
Calibrated phase with respect to beam
...
...
Rms and peak error during flat-top
...
...
Calibration procedures using the test signal
Turn on RF
Tune cavity
...
- Efficient use of resources
- High performance algorithms
- High level automation
- Flexibility
Complexity
- interfaces
- different platforms
Maintenance
Hard to understood

Software topology



Software topology