Laboratoire de
Physique Corpusculaire
de Clermont-Ferrand

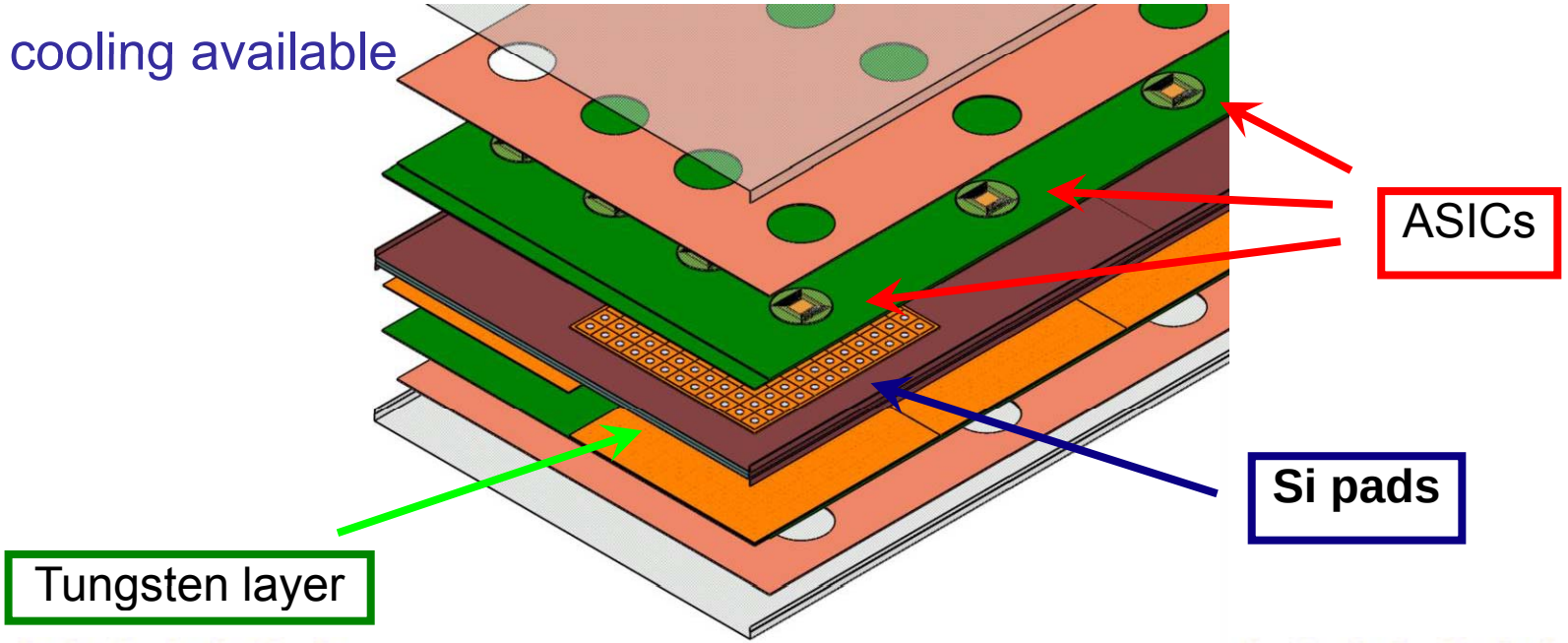
A 10-bits pipeline ADC dedicated to the VFE Electronics of Si-W Ecal

Laurent Royer, G. Bohner, R. Cornat, P. Gay, J. Lecoq, S. Manen
IN2P3/LPC Clermont-Ferrand
in Collaboration with LAL (Orsay)

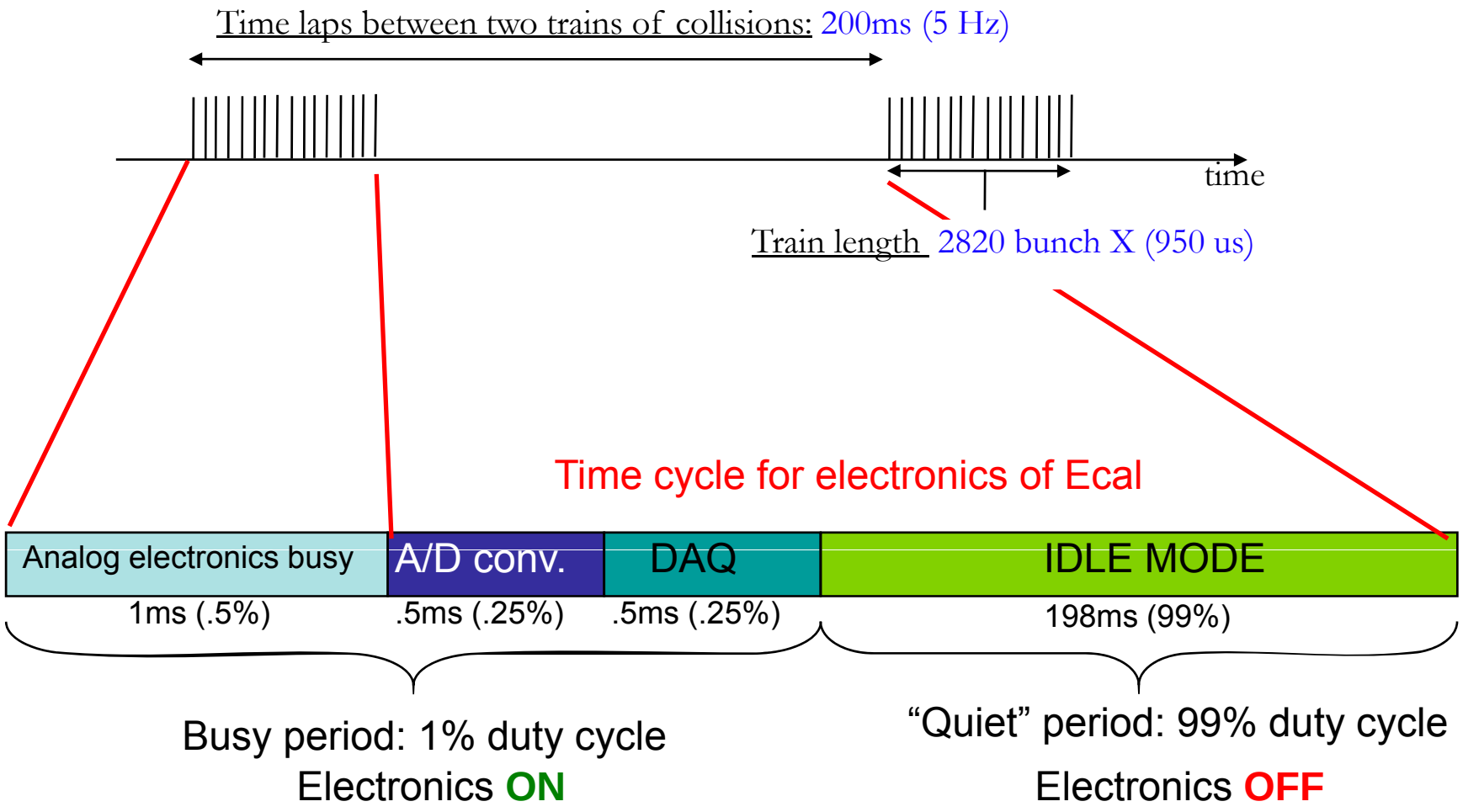
Linear Collider Workshop – Hamburg 2007

The Silicon-Tungsten Ecal

- Sandwich structure of: thin wafers of silicon diodes (~200 µm)
  & tungsten layers
- High granularity : diode pad size of 5x5 mm^2
- High segmentation : ~30 layers
- Embedded VFE electronics
- Minimal cooling available



Time considerations

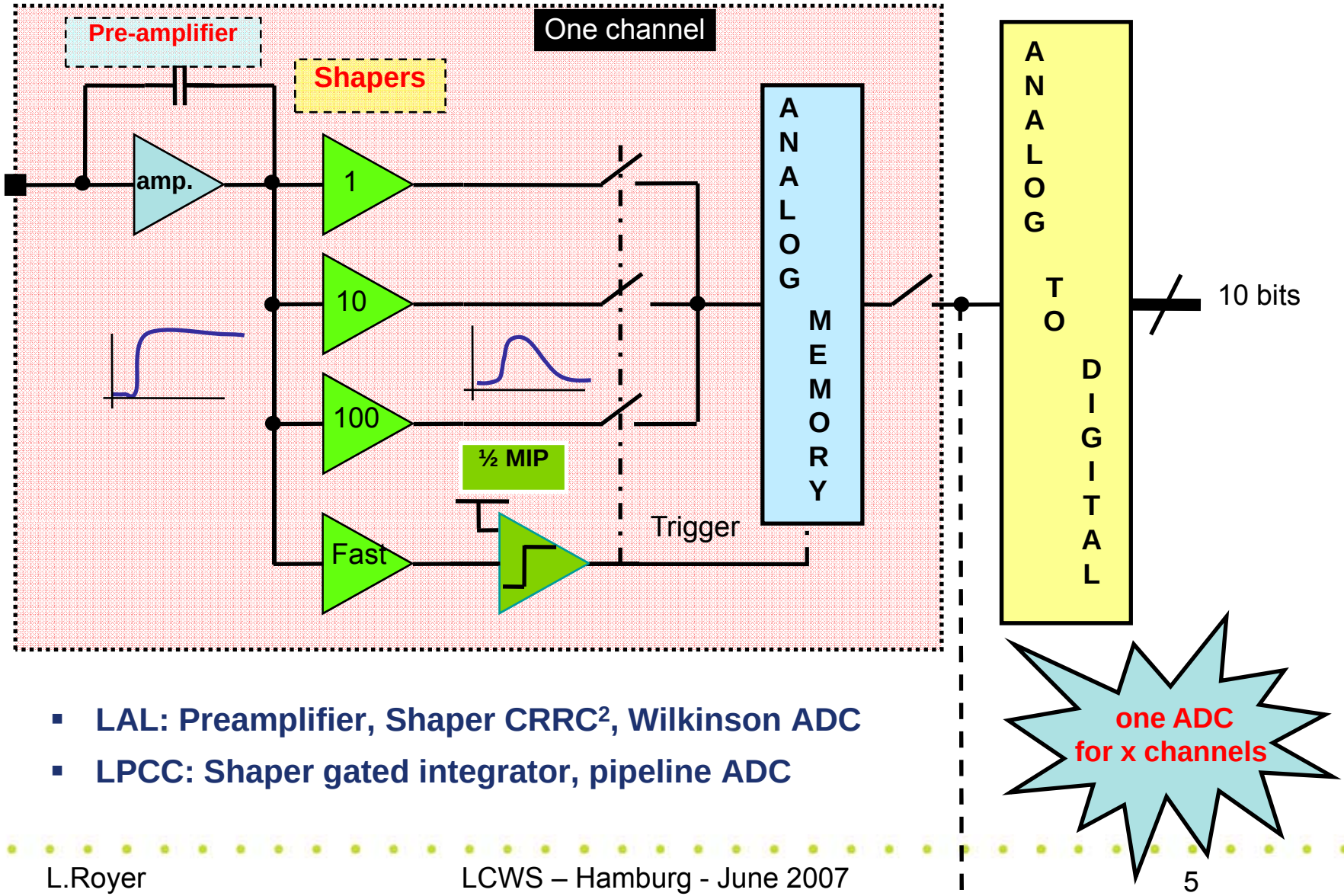


Ecal VFE Electronics: requirements

- Large dynamic range:
  → 0.1 MIP to 3000 MIP → 15 bits
- Precision of 8 bits
- Zero suppress on-chip
  → Auto-trigger on ½ MIP
- Front-end embedded in detector
- 2.10^8 channels (5x5 mm^2 pads)
  → Compactness
- **Ultra-low power : 25 µW/ch max.**
  → power pulsing: ON 2ms - OFF 198 ms

Ultra-low POWER is the KEY issue (C. de la Taille)

Ecal VFE Electronics: one channel

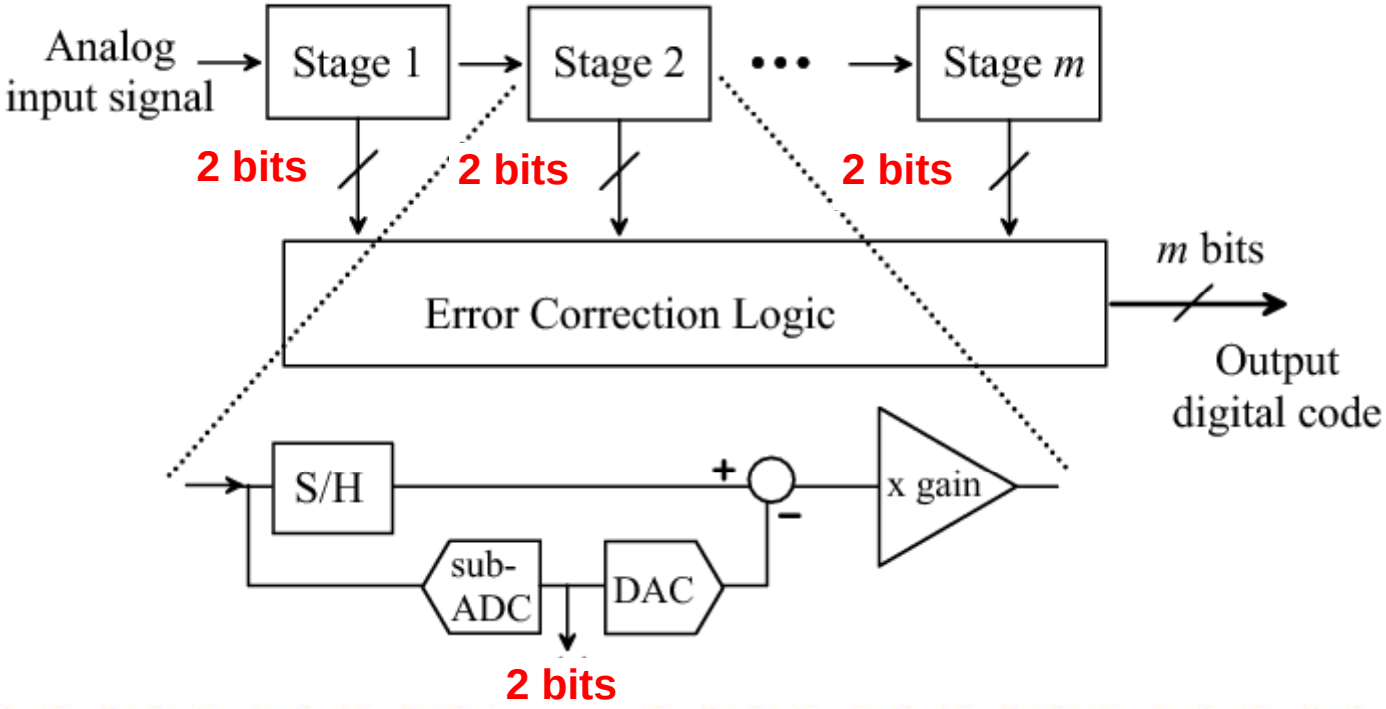


- **LAL: Preamplifier, Shaper CRRC², Wilkinson ADC**
- **LPCC: Shaper gated integrator, pipeline ADC**

General ADC pipeline architecture

- The conversion operation is divided into *m* steps, with *m* the number of bits of the output code. The most significant bits are resolved in the first step, and the least significant bits are resolved in the last step.
- Each step is processed by a dedicated stage; *m*-bits ADC ➔ *m* stages
- Each stage converts the input signal into *n* bits (sub-ADC) and delivers an amplified residual voltage to the next stage.
- The Error Correction Logic Block processes the *m* *n*-bits to deliver the output digital code.

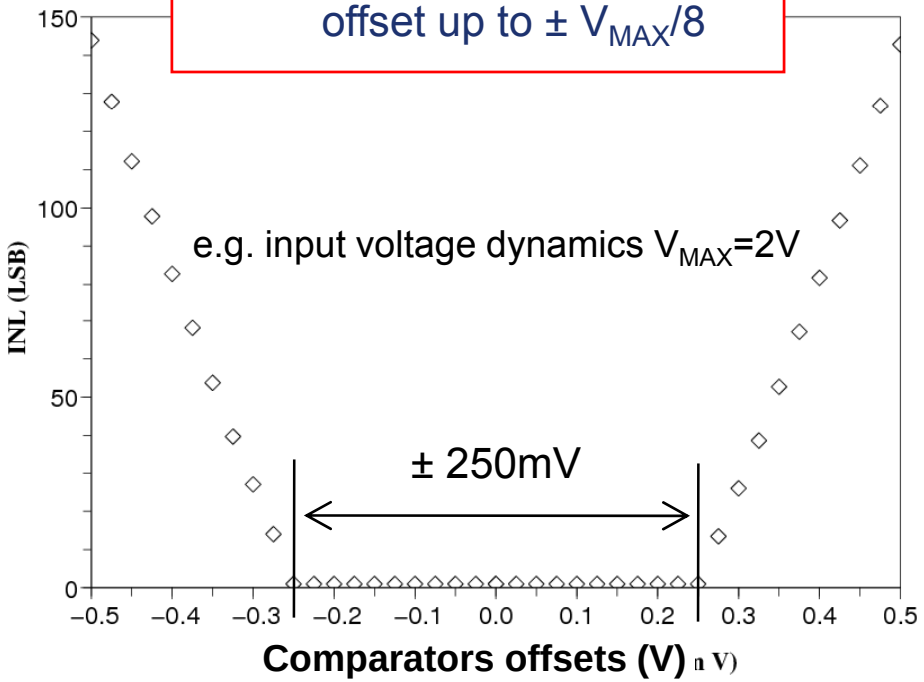
Linearity mainly affected by the comparator offset and the precision of the amplifier gain.



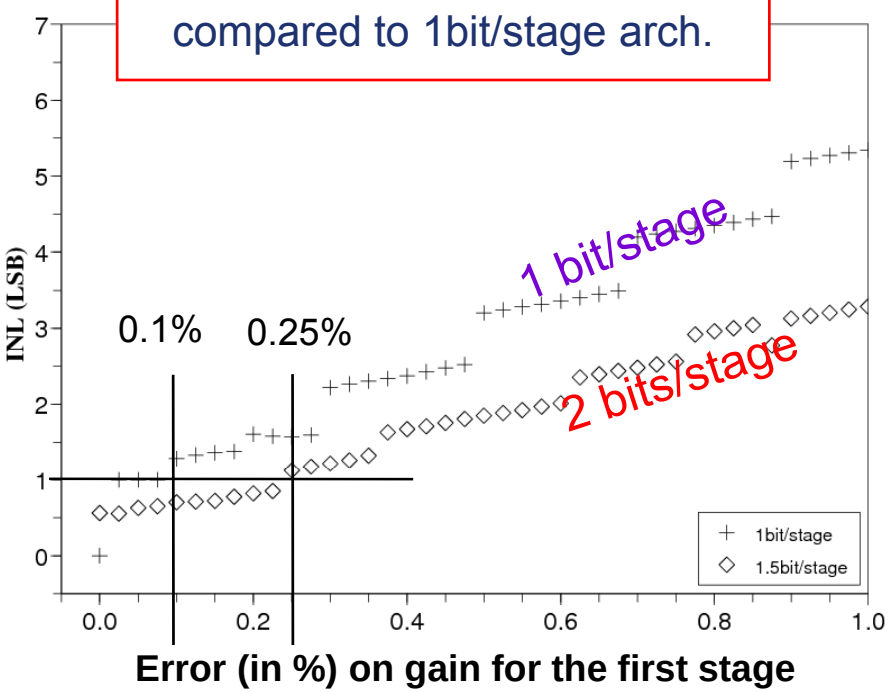
Why two bits per stage ?

Algorithmic simulations
Integral NonLinearity (INL)

Not sensitive to comparator offset up to ± V_{MAX}/8



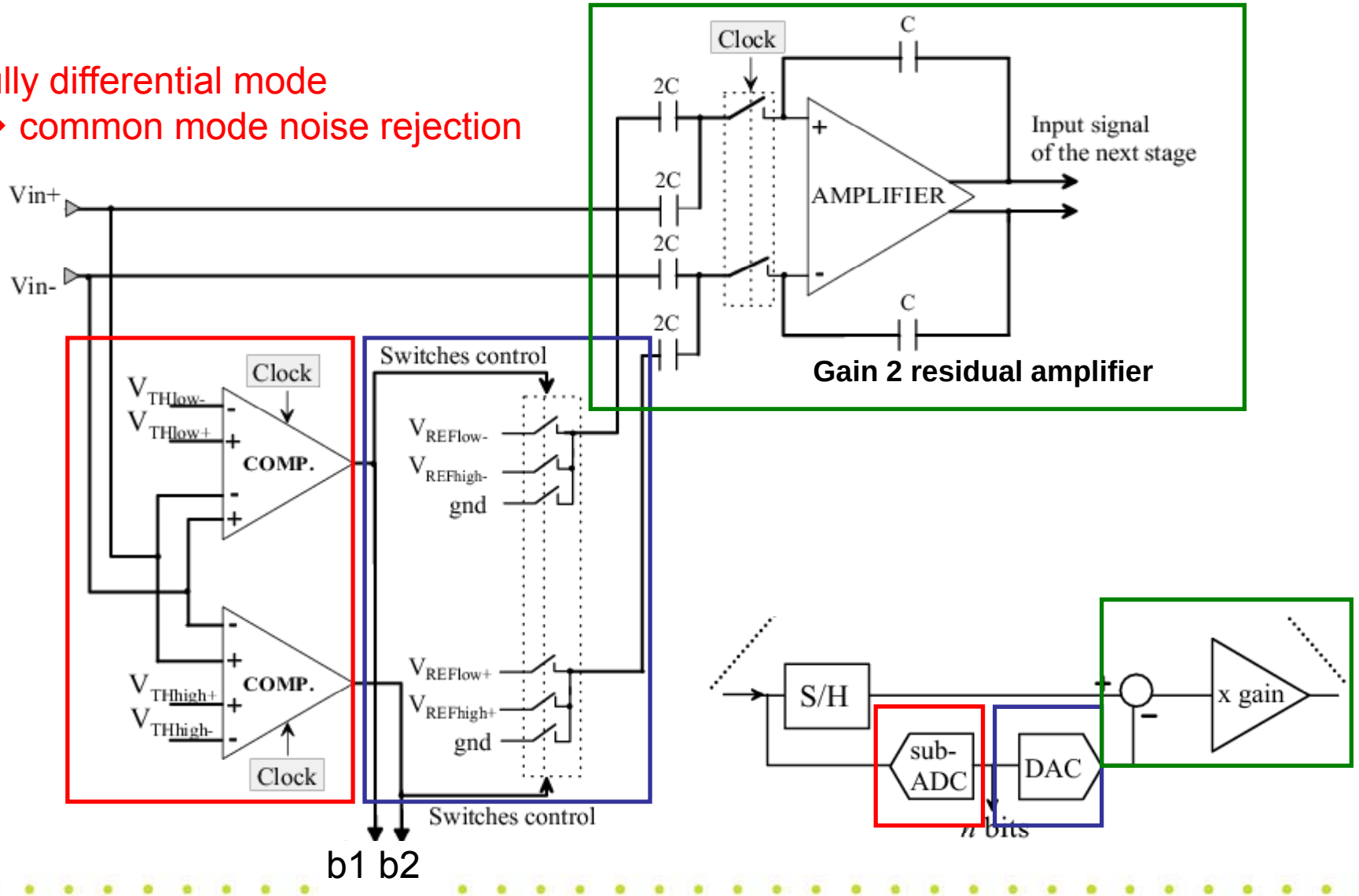
Less sensitive to error on gain compared to 1bit/stage arch.



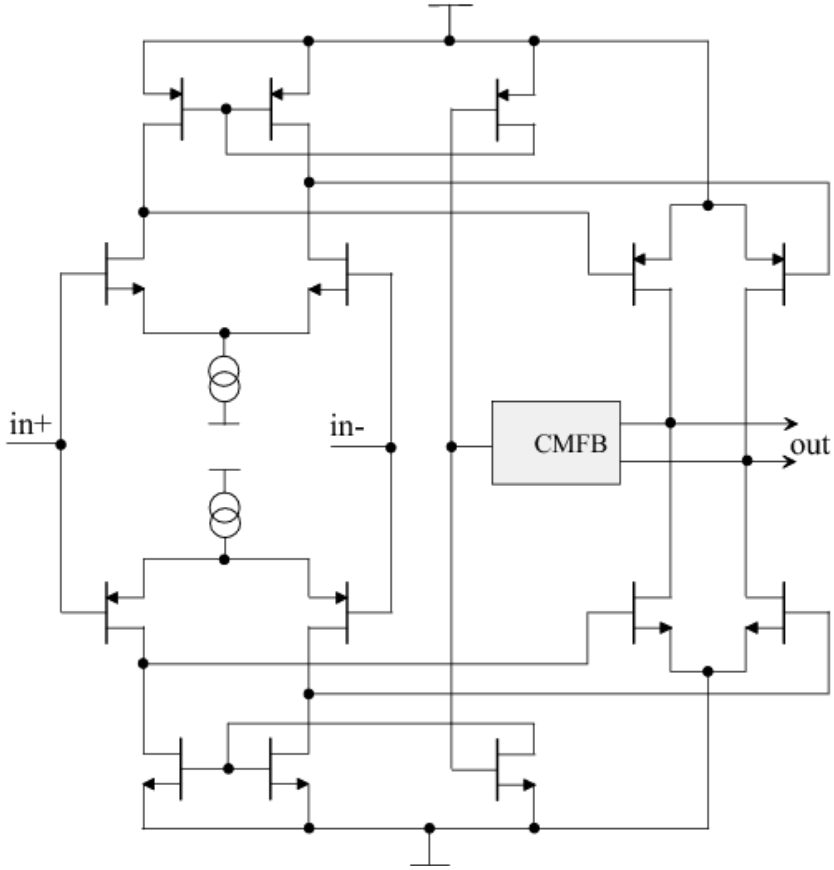
Arch. w/ a resolution of 2 bits per stage but the combination "11" avoided ➔ 1.5 bit /stage

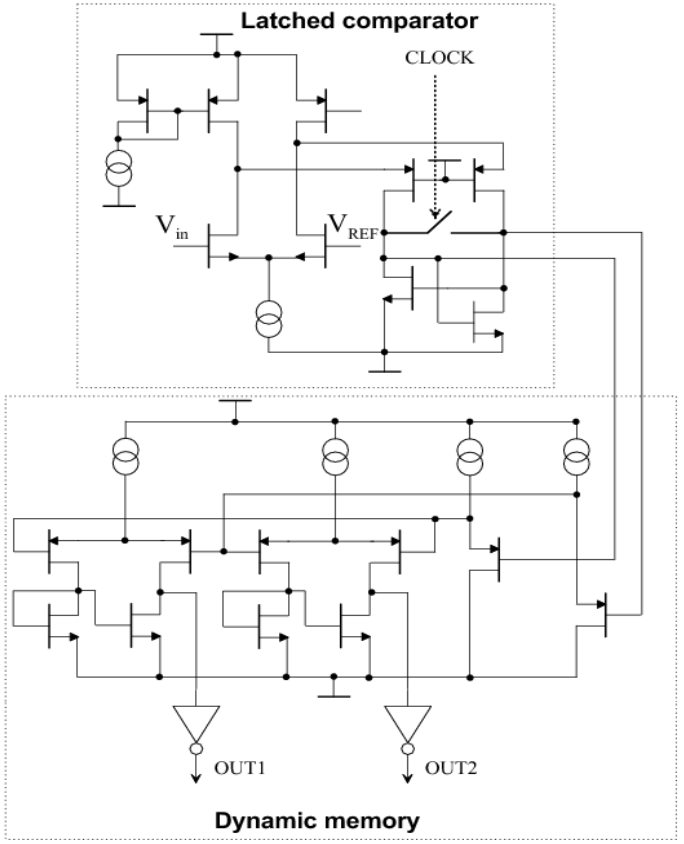
Pipeline ADC : one stage schematics

fully differential mode
→ common mode noise rejection



Amplifier and comparator





- **Amplifier**
- Fully differential and rail-to-rail
- Gain-Bandwidth product: 50 MHz
- Power consumption: 1.9 mW /5V

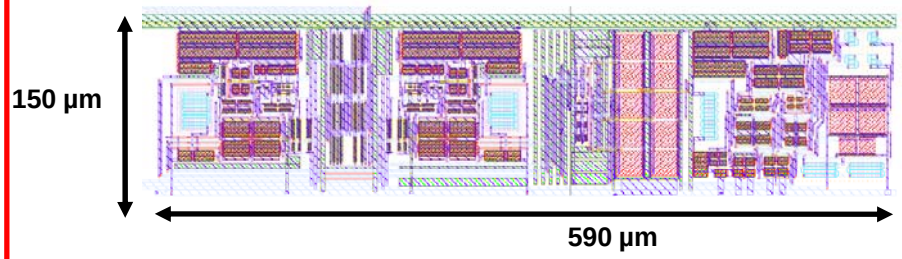
Comparator

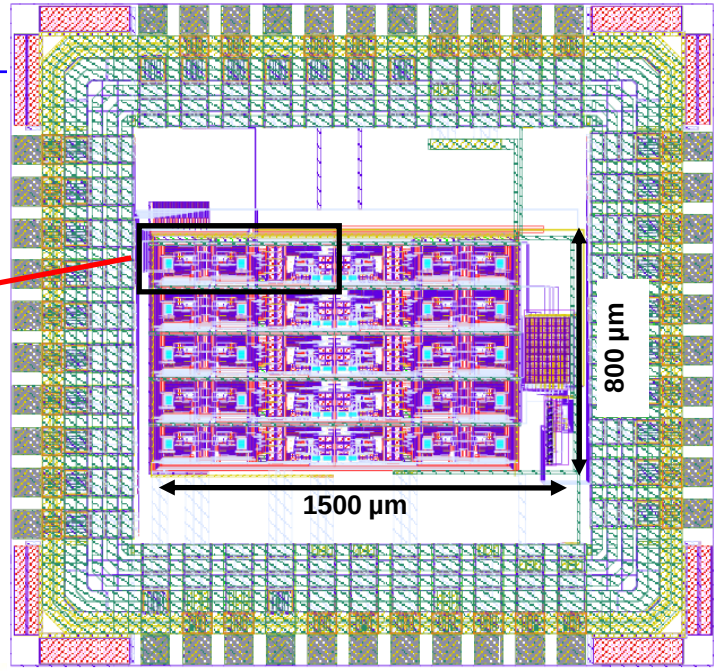
- Sensitivity = input noise : < 280 µV (95% C.L.)
- Offset: (20 ± 9) mV (± 68% C.L.)
- Power consumption: 815 µW @ 4 MHz

A 10-bits ADC prototype

- Characteristics:
  - **10 bits ➔ 10 stages**
  - **1.5bit/stage and differential architecture**
  - **Technology: Austriamicrosystems CMOS 0.35µm**
  - **Power supply: 5V (digital: 2.5V)**
  - **Clock (sampling) frequency: 4 MHz (MS/s)**
  - **Die area: 1.2 mm²**

Layout of 1 stage

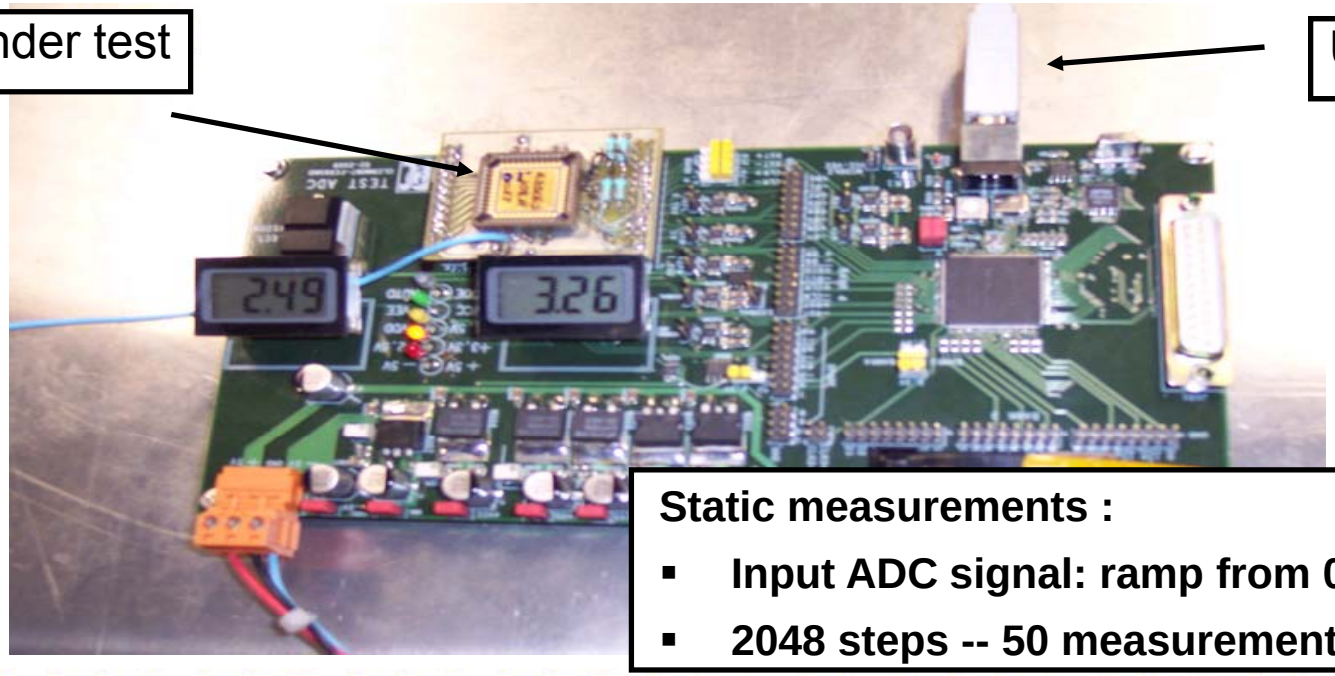




Measurement setup

Test Bench:

- Generic board for ADC tests
- Analogue signal generator: DAC 16 bits (DAC8830)
- PC/LabView Slow Control through USB interface
- Data processing with Scilab package

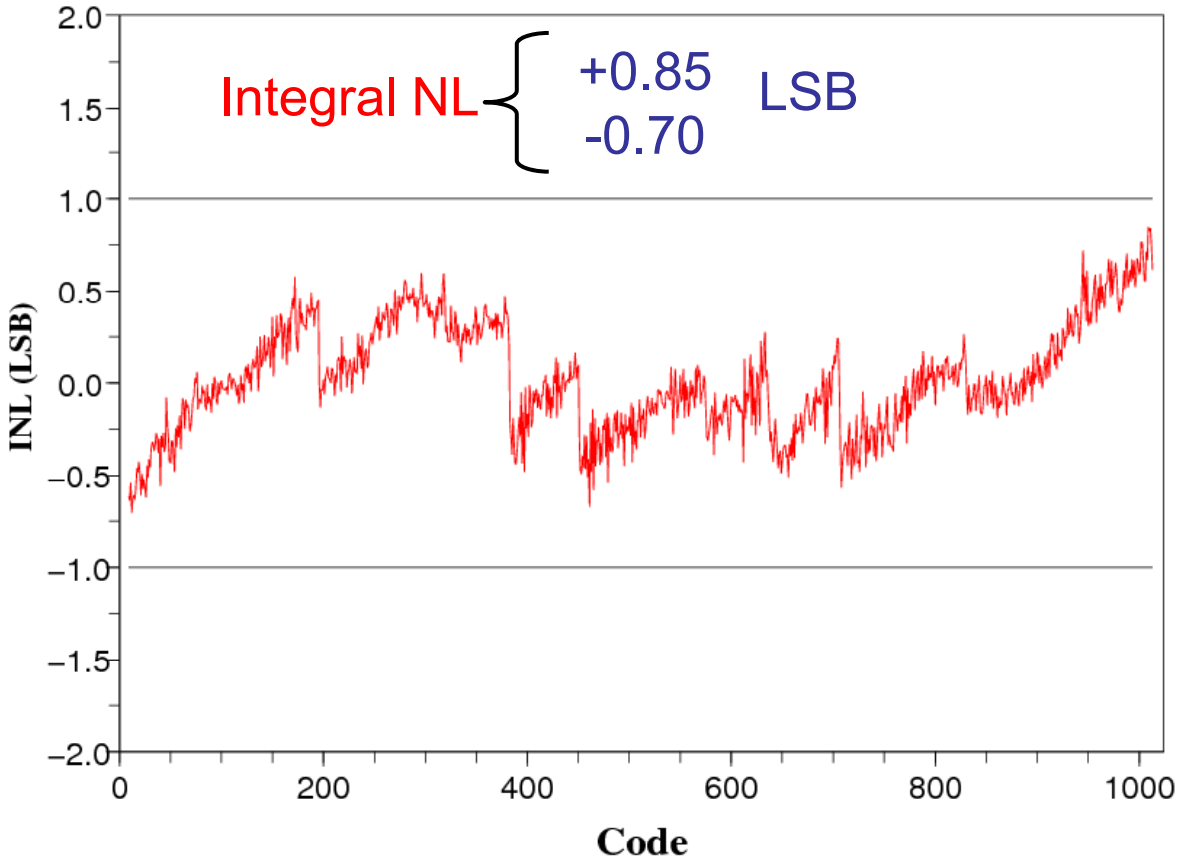


Static measurements :

- **Input ADC signal: ramp from 0 to 2V**
- **2048 steps -- 50 measurements / step**

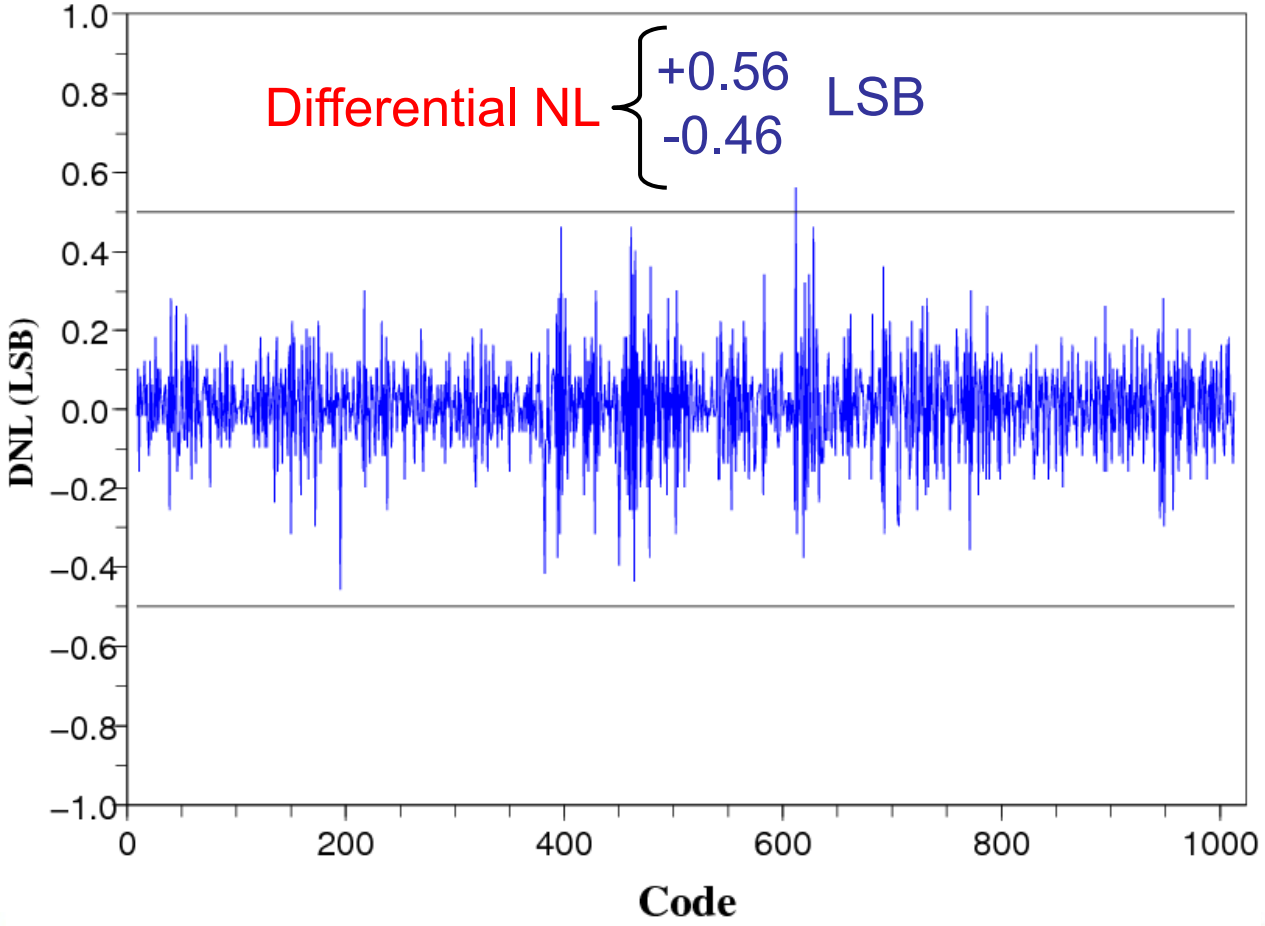
Linearity performance (1)

The Integral Non-Linearity (INL) refers to the deviation, in LSB, of each individual output code from the ideal transfert-function value.

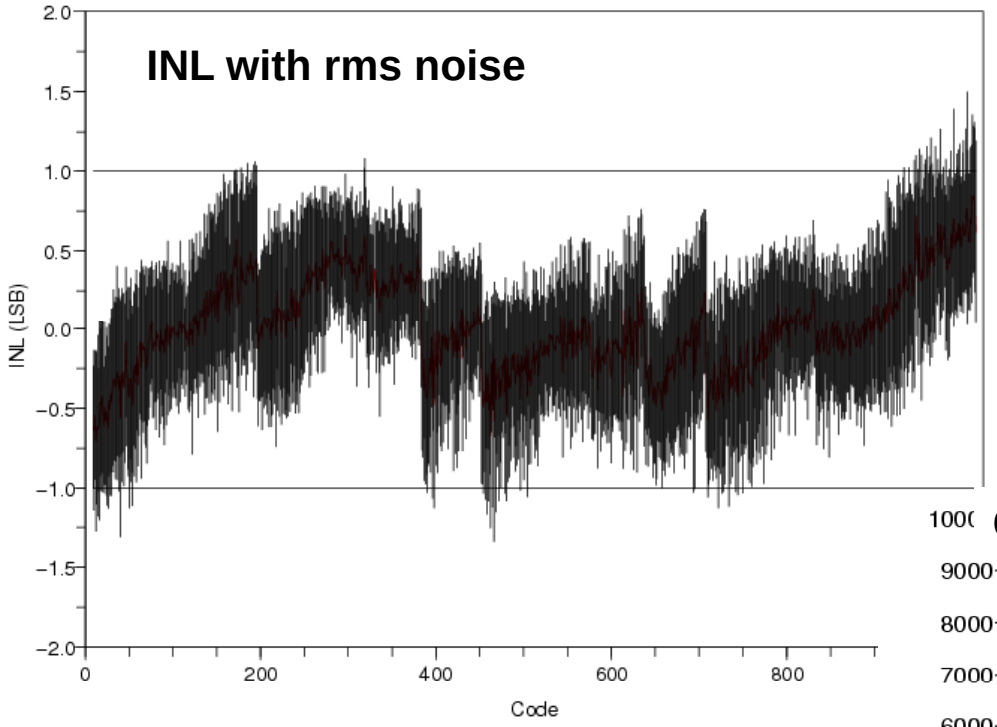


Linearity performance (2)

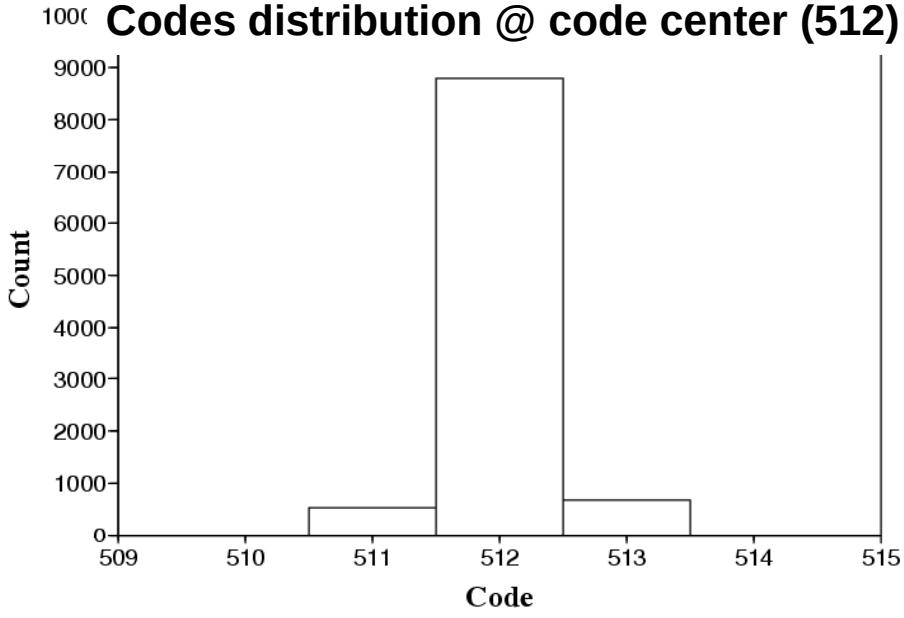
This Differential Non-Linearity (DNL) is defined as the difference between an actual step width and the ideal value of one LSB.



Noise performance



Measured noise
(including the setup noise):
< 0.5 LSB @ 68% C.L.



Consumption ("the key issue")

- **Dynamic consumption : 35 mW (clock @ 4MHz)**
- **Conversion time: 1 clock period = 250ns**
- **Assuming:**
  - **128 channels per VFE chip**
  - **1 ADC per chip**
  - **5 events max per channel (memory depth)**

➧ **With power cycling, the integrated consumption per channel of the A/D conversion can be estimated by:**

$$\frac{Pw \times Tconv \times Mem.}{Time\_cycle} = \frac{35mW \times 250ns \times 5}{200ms}$$ **= 0.22 µW/ch**

with

***Pw*:**	**power cons. of one channel**
***Tconv*:**	**time for one conversion**
***Mem*:**	**memory depth of one channel**
Time_cycle:	**time between two trains**

The ON-setting time and pipeline latency effects can be neglected.

Summary

ADC requirements

- 10 bits ADC precision

ADC measured performance

- ADC: precision of 10 bits
  - INL:-0.70/+0.85 LSB
  - DNL: -0.46/+0.56 LSB
  - Noise: <0.5 LSB

- Compactness

- One pipeline ADC per chip (128 ch)
- Die area of 1.2mm^2 for 128 ch.

- Total cons. of VFE: 25 µW/ch max

- Power cons.: 0.22µW/ch

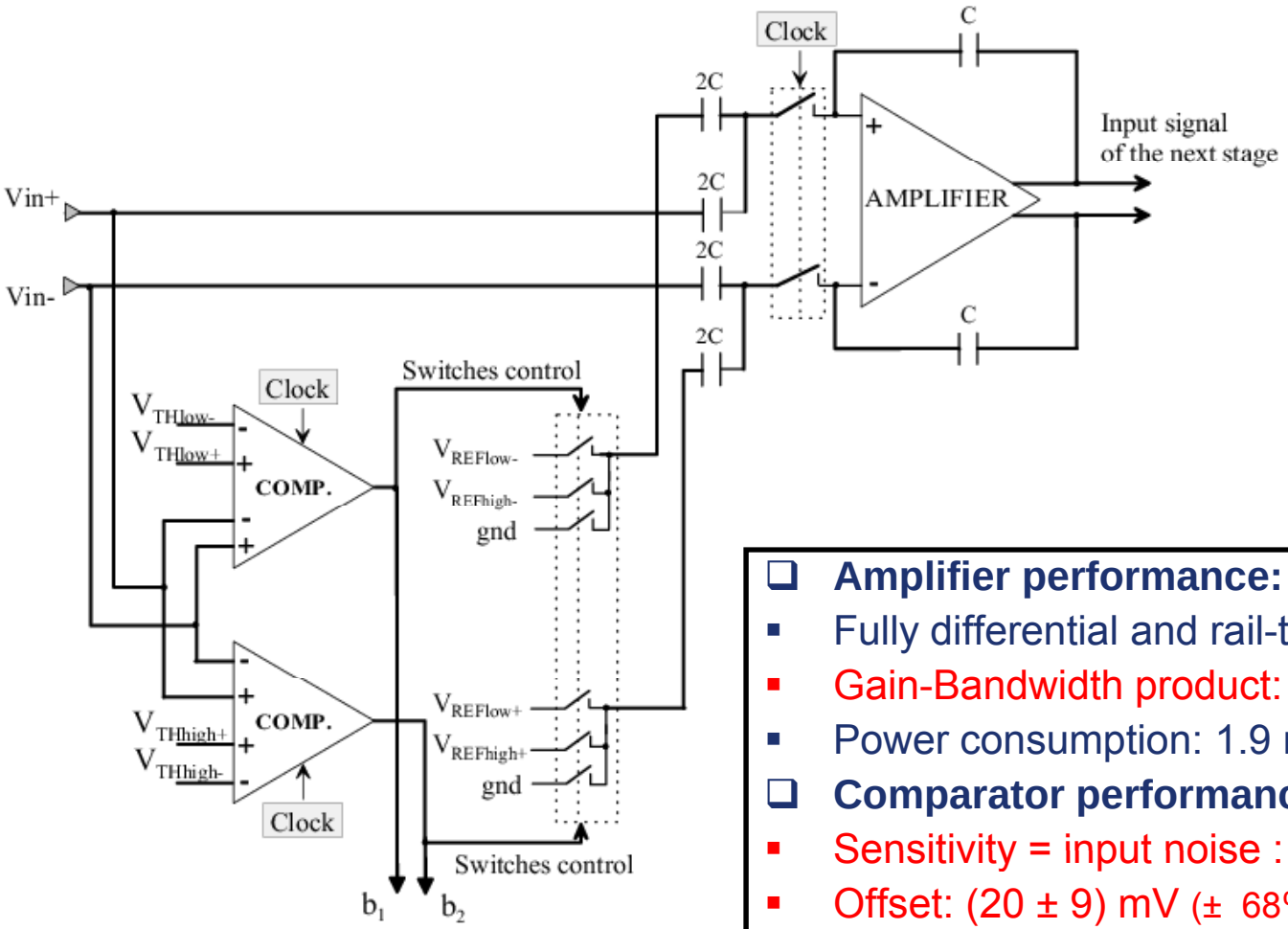
⇨ ≈ 1% total power of one channel

- Foreseen improvements:
  - **Reduce power supply voltage (power cons.) from 5V to 3.5V (from 35mW to 25mW)**
  - **Increase precision to 12 bits in order to have only a bi-gain shaping**
  - **Implement and test the power pulsing**

A Pipeline **A**nalog-to-**D**igital **C**onverter (ADC) dedicated to the Ecal Very Front-End Electronics of ILC

Linear Collider Workshop – Hamburg 2007

Amplifier & comparator performance



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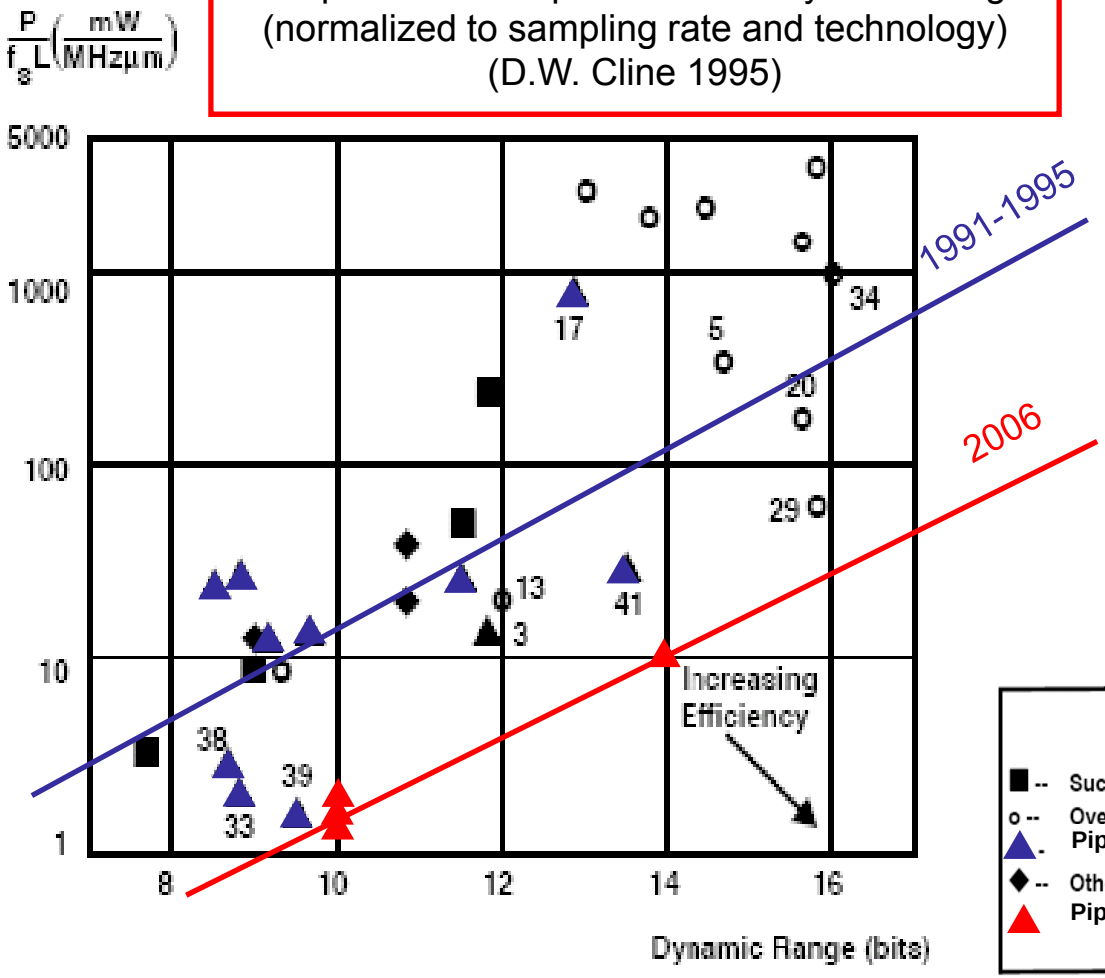
  - Fully differential and rail-to-rail
  - Gain-Bandwidth product: 50 MHz
  - Power consumption: 1.9 mW /5V
- **Comparator performance:**
  - Sensitivity = input noise : < 280 µV (95% C.L.)
  - Offset: (20 ± 9) mV (± 68% C.L.)
  - Power consumption: 815 µW @ 4 MHz

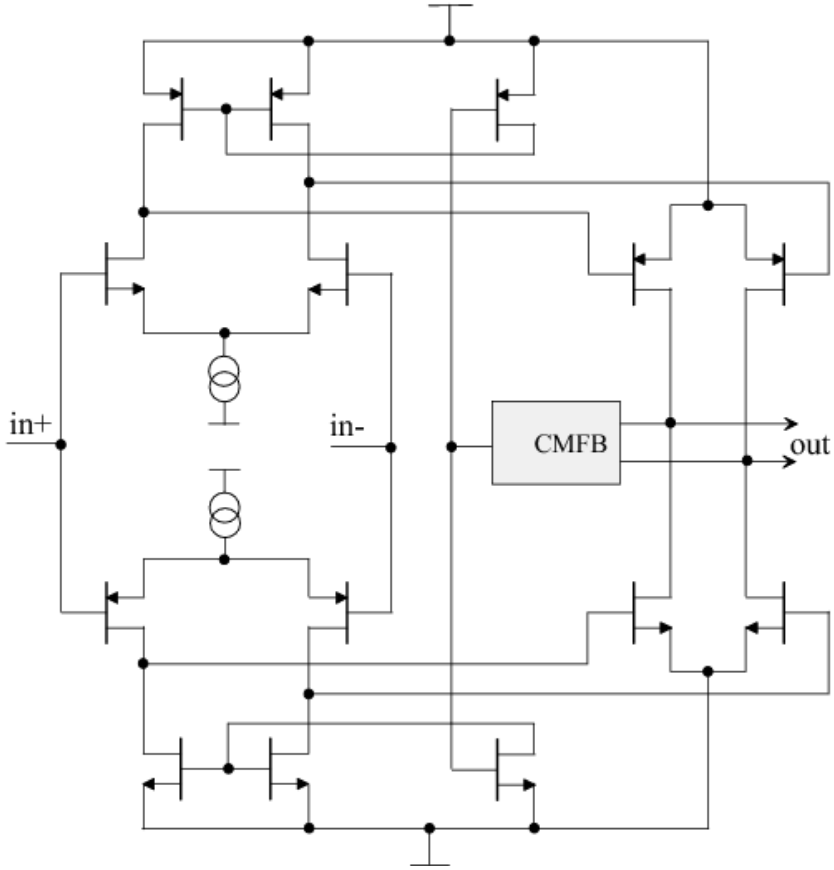
Performance of pipeline ADCs

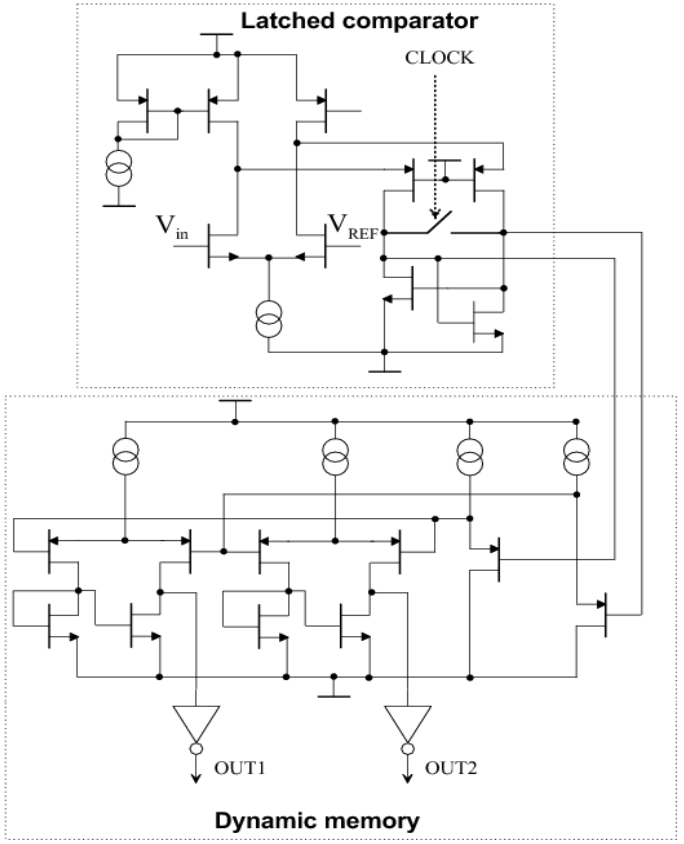
Comparative ADC power versus dynamic range
(normalized to sampling rate and technology)
(D.W. Cline 1995)



- Wide capabilities range for Pipeline ADCs (▲ ▲)
- Trade-off between:
- **Resolution: 8 - 14 bits**
- **Sampling rate: few MHz to hundreds of MHz**
- **Consumption: few mW to tens of mW**
- Power divided by a factor 10 on ADC power in 10 years

Amplifier and comparator





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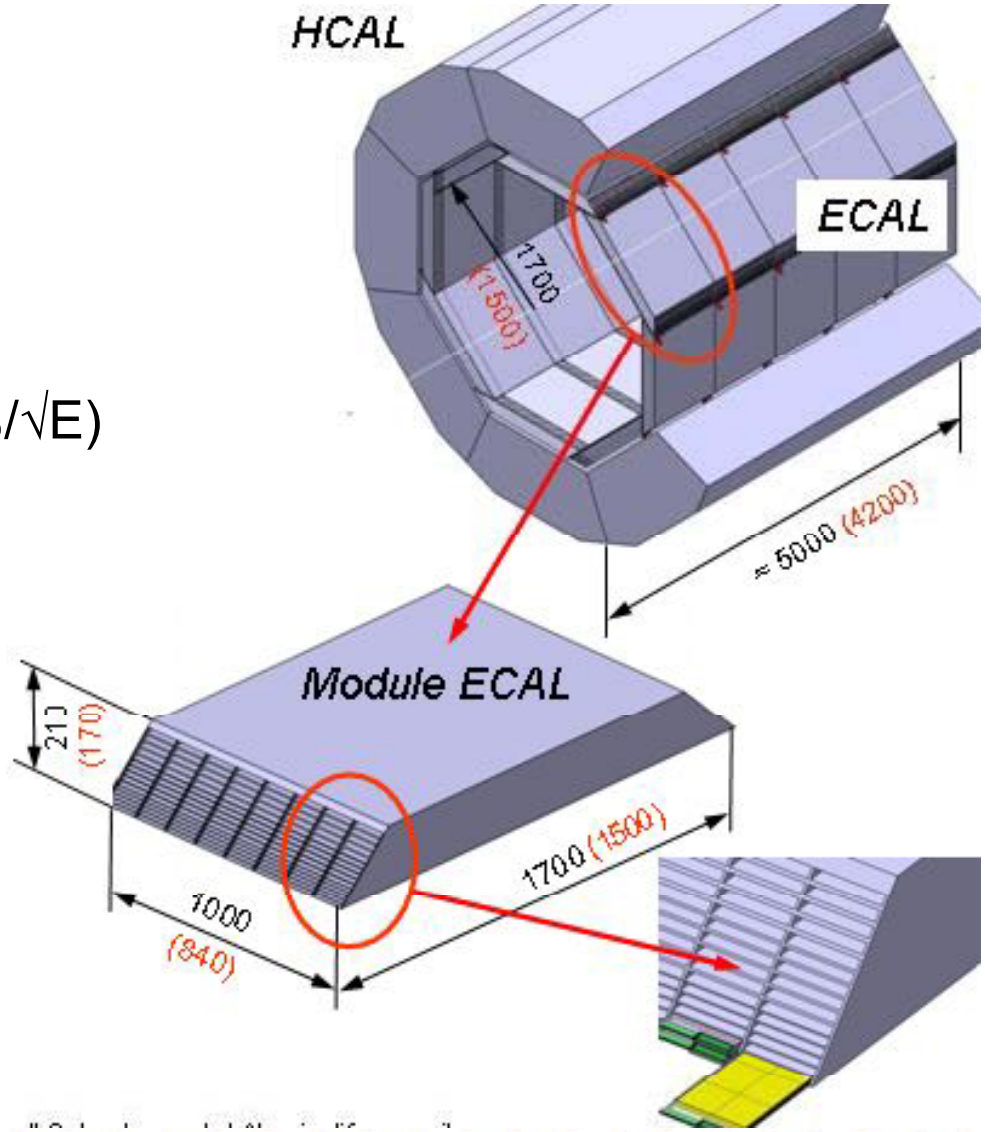
The Silicon-Tungsten Ecal

- Measure photons and hadrons
- High granularity : typ < 1 cm2
- High segmentation : ~30 layers
- Moderate energy resolution (10%/√E)



1.5 bit/stage pipeline architecture

- 2 comparators and one amplifier per stage required
- 2 threshold voltages and 3 reference voltages required