

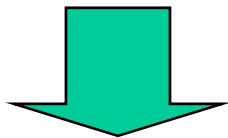
# Pair Monitor Studies

'07 6/1 Y. Takubo  
(Tohoku university)

# Introduction

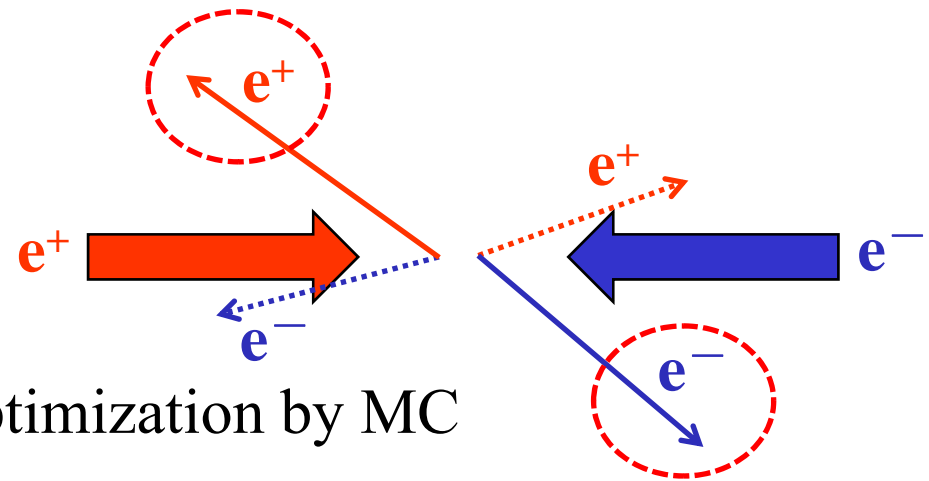
## Pair monitor

- Monitor of the beam size, position and crossing angle at IP.
- Measurement of the  $e^+e^-$  pair background
  - $e^+e^-$  distributions from beam crossing have the beam information at IP.
  - The same charge with respect to the oncoming beam is scattered with large angle.



## Activity of Tohoku group

- Performance check and detector optimization by MC
- Development of the readout ASIC



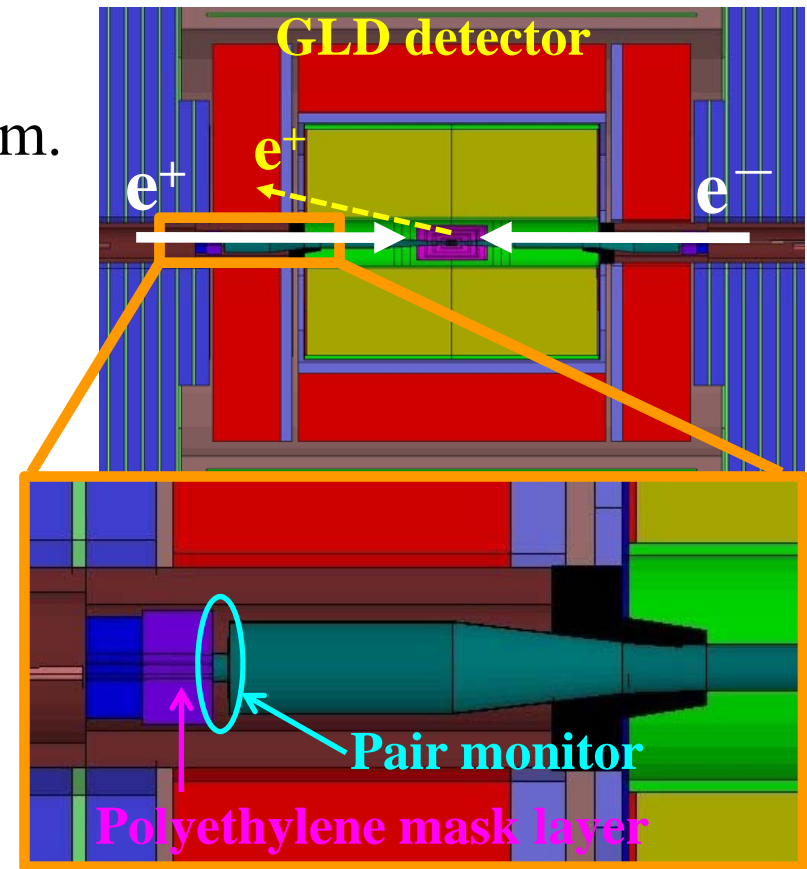
Current status of these items are shown.

# Simulation Study

# Simulation setup

## Simulation setup

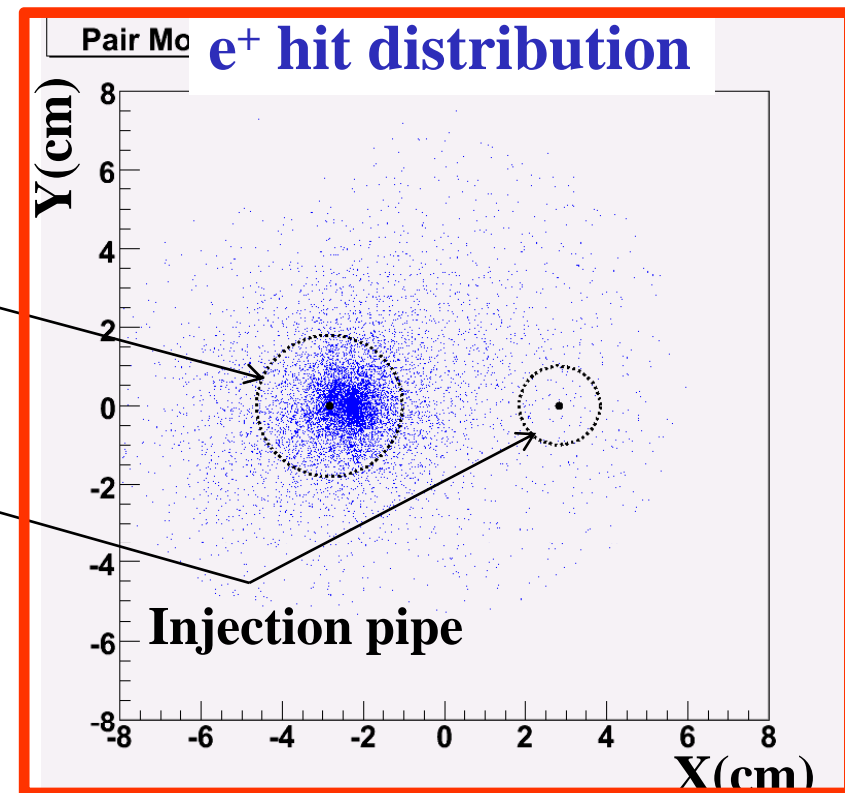
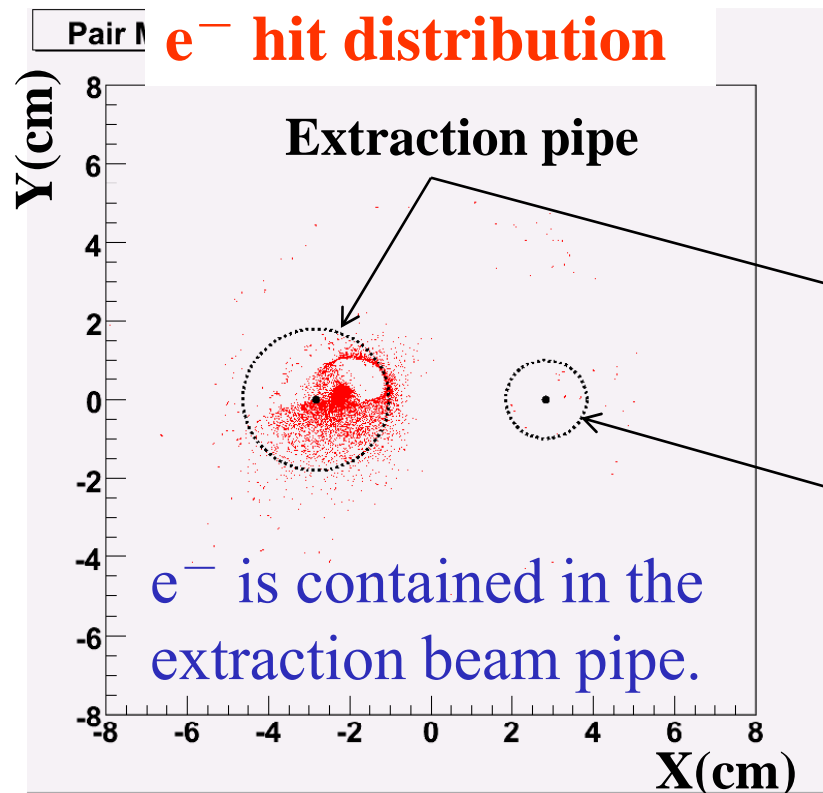
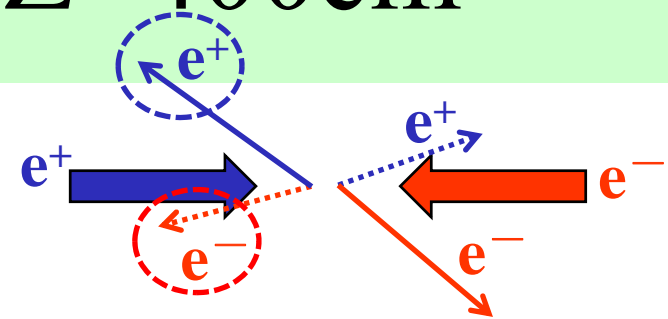
- $e^+e^-$  pair generator : CAIN
  - Beam size : 639nm x 5.7nm x 300 $\mu$ m.
- Tracking simulator : Jupiter
  - Simulator for GLD
  - Simulation based on Geant4
  - Magnetic field : 3T with anti-DID
- Pair monitor
  - Located at 400 cm from IP.
  - In front of Polyethylene mask layer
- Scattered  $e^+$  distribution is studied.



# $e^+e^-$ distributions at $Z=400\text{cm}$

$e^+e^-$  distributions are checked at  $Z=400\text{cm}$ .

- $e^-$  is not scattered so much.
- $e^+$  is scattered with large angle.

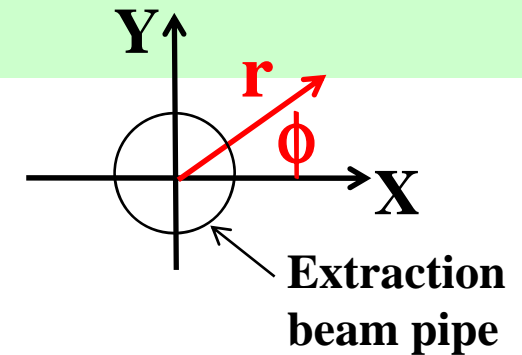


$e^+$  hit distribution around the extraction beam pipe is studied.

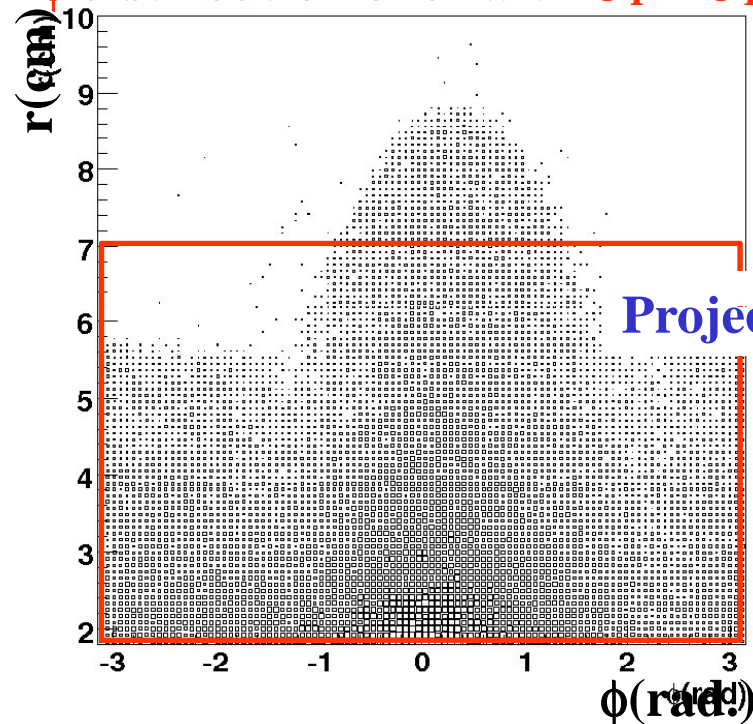
# $e^+$ hit distribution

The hit distribution around extraction beam pipe is compared with different vertical beam size.

- Standard vertical beam size :  $\sigma_{Y0} = 5.7\text{nm}$

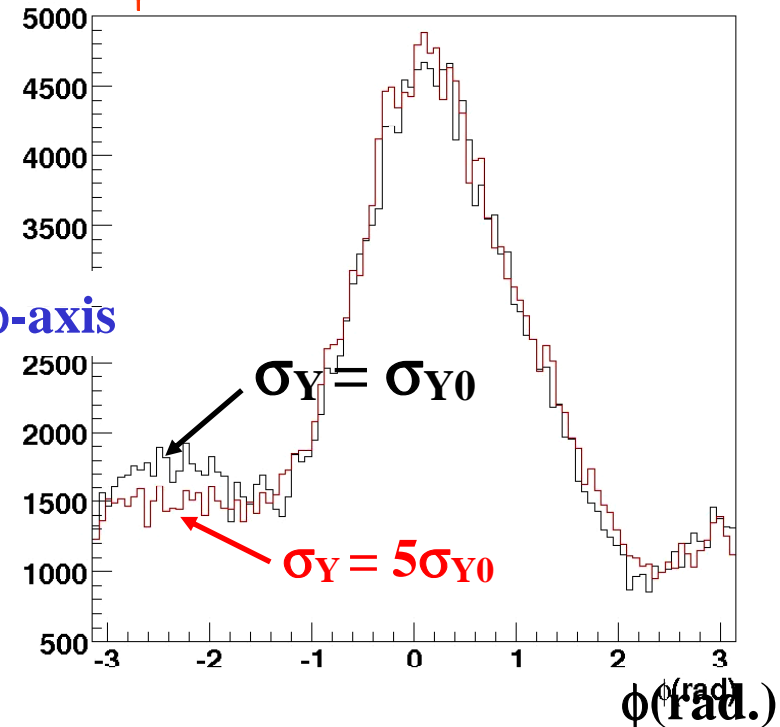


$r$ - $\phi$  distribution of  $e^+$  with  $\sigma_Y = \sigma_{Y0}$



Projection to the  $\phi$ -axis

$\phi$  distribution in  $r=2\sim 7\text{cm}$



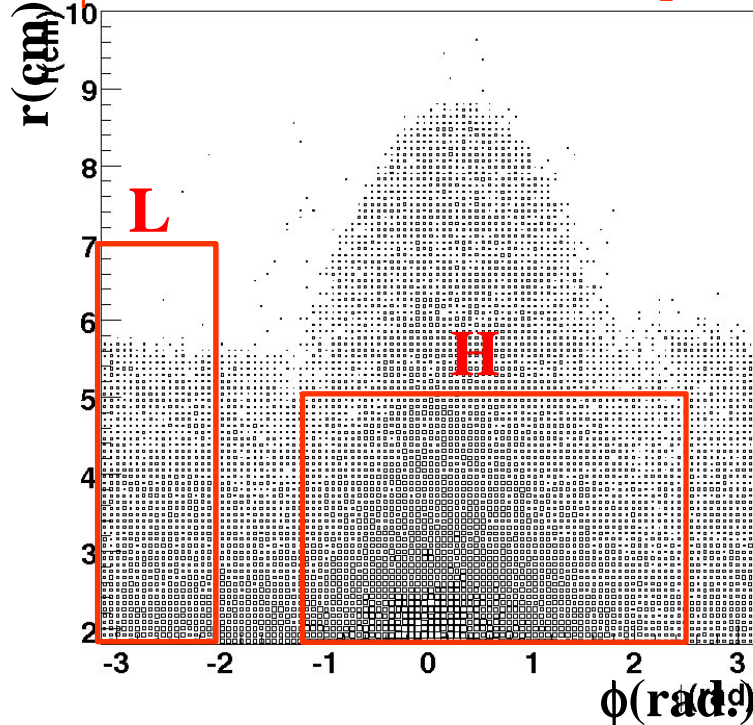
The hit distributions have information of the beam size.

# Peak-to-valley ratio

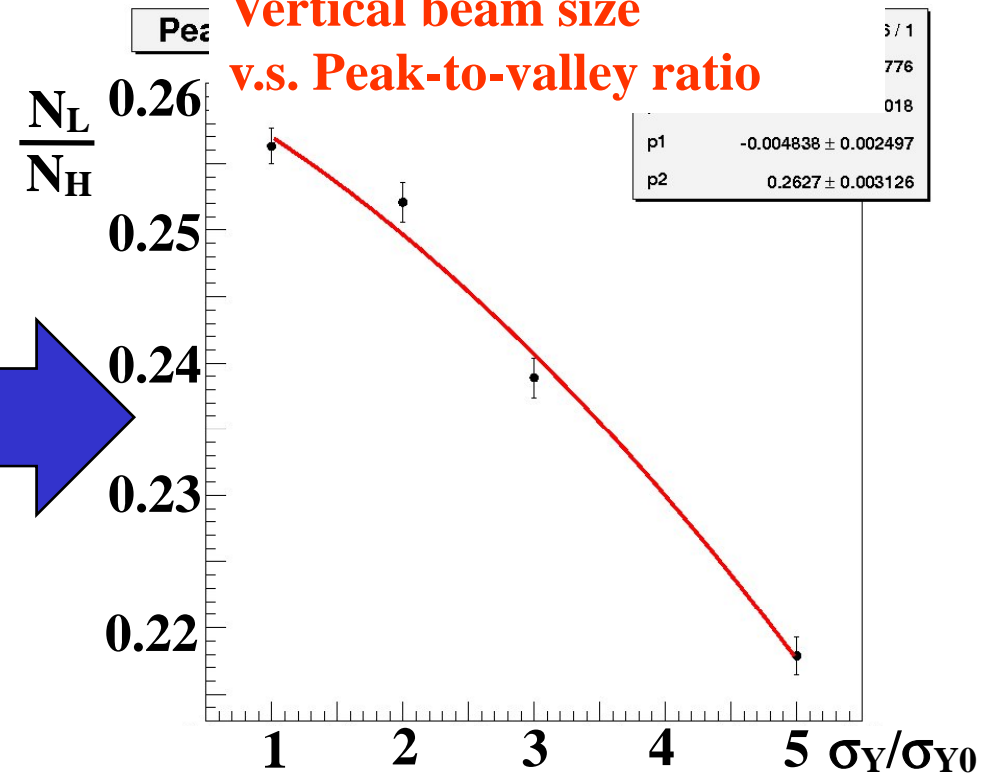
Peak-to-valley ratio is used to obtain the relation with  $\sigma_Y$ .

**Peak-to-valley ratio :  $\frac{N_L}{N_H}$**

**$r$ - $\phi$  distribution of  $e^+$  with  $\sigma_Y = \sigma_{Y0}$**



**Vertical beam size  
v.s. Peak-to-valley ratio**

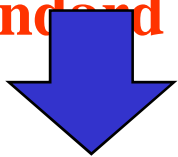


By using this relation, the resolution of beam size measurement is estimated.

# Resolution of the vertical beam size

## Estimation of beam size resolution

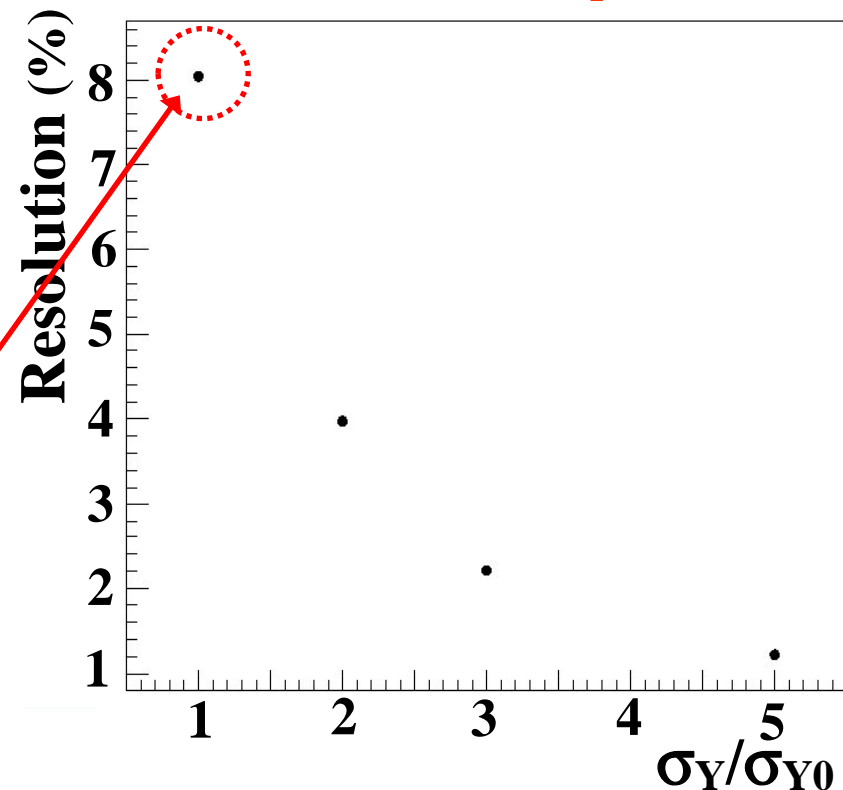
- The statistical error is scaled to that of 150 bunches.
  - Data will be taken for each 150 bunches to get enough statistics.
- **$\sigma_Y$  can be measured by 8% for the standard beam size.**



## The next step

- Estimation of the  $\sigma_X$  resolution.
- More optimization of analysis method and pair monitor setup

Vertical beam size v.s.  $\sigma_Y$ -resolution



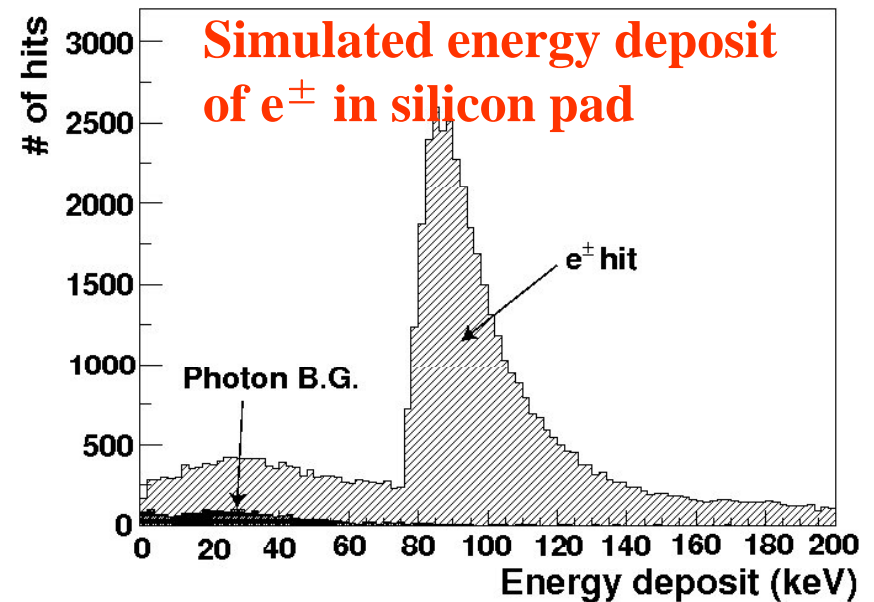
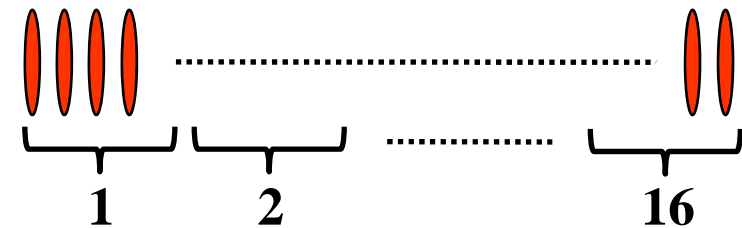


# Development of Readout ASIC

# Design concept of readout ASIC

## Design concept of readout ASIC

- Counting a number of the hit
  - Hit distribution is obtained.
- Measurement for each timing in a train
  - 16 timing parts in one train.
- Data is read within a each train.
  - Timing width : ~200 ns.
- Si detector is assumed as a detector.
  - Thickness : 200  $\mu\text{m}$
  - Signal : 15000 electrons.



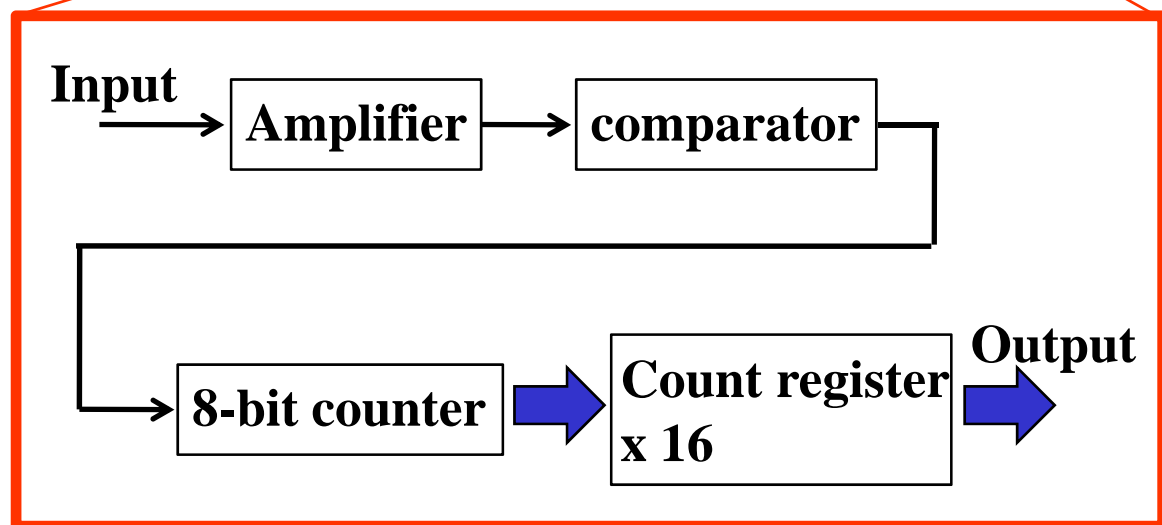
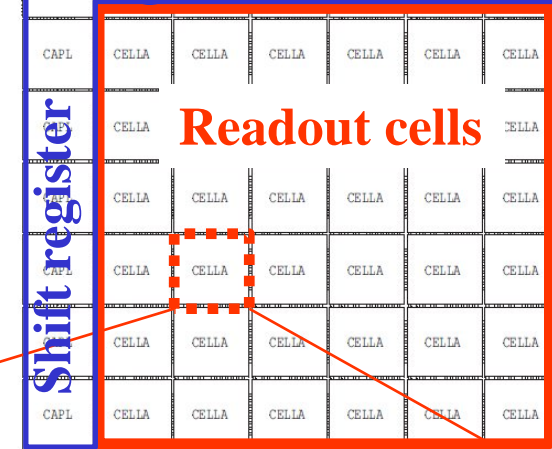
The readout ASIC is designed to satisfy these design concept.

# Design of the readout ASIC

## Structure of readout ASIC

- Distributor of the operation signals.
- Shift register to specify a readout cell
- Data transfer to the output line
- 36 readout cells
  - Amplifier
  - Comparator
  - 8-bit counter
  - 16 count registers

Operation signal distributor  
Shift register & Data transfer

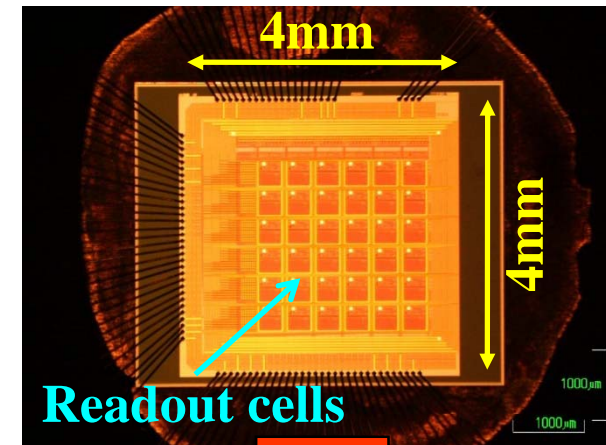


# Prototype of readout ASIC

## Prototype of readout ASIC

- Produced with 0.25 $\mu\text{m}$  process
- Size : 4 x 4 mm<sup>2</sup>
- Readout cell size : 400 x 400  $\mu\text{m}^2$
- Readout chip is covered with package
  - MQFP produced by I2A Technologies
- So far, the 1<sup>st</sup> and 2<sup>nd</sup> prototypes were developed as explained later.

The response test of the readout ASIC is performed.

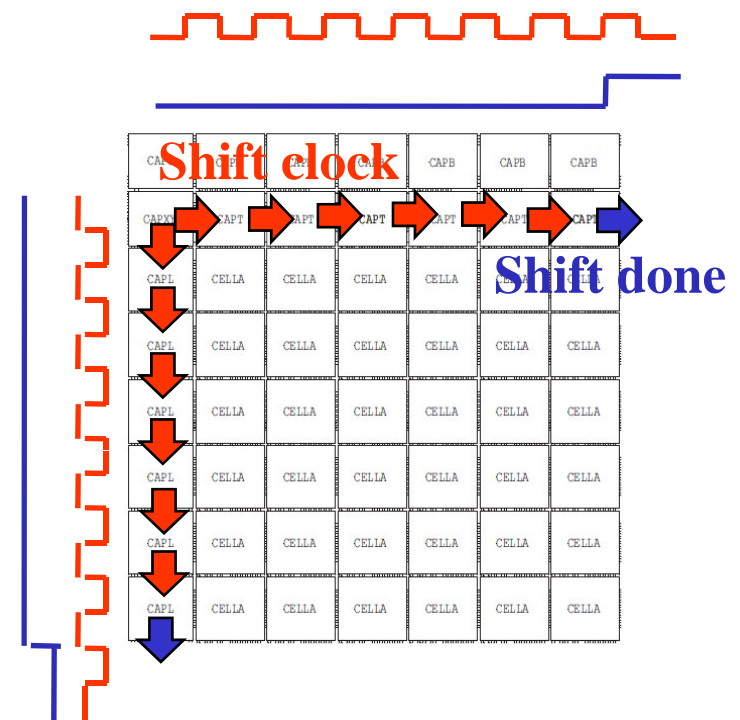


# Test of the shift register

For the first test, response of the shift register was checked.

## Shift register

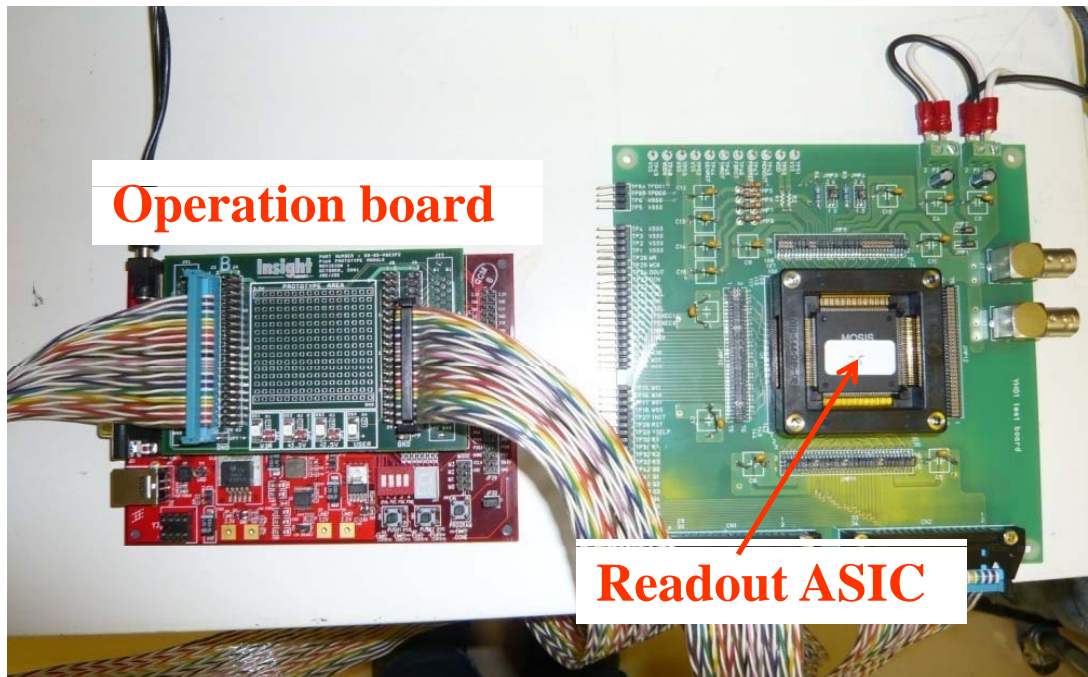
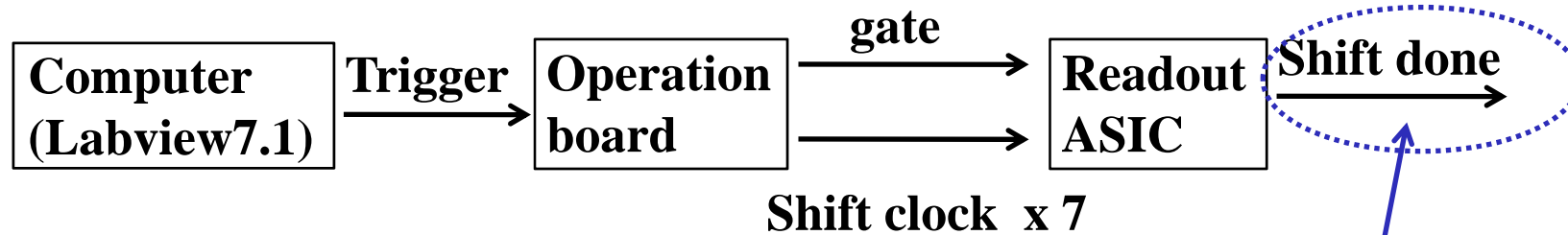
- Specification of the readout cell
  - Specification is done by shift clocks for X and Y direction.
- At the timing of the 7<sup>th</sup> shift clocks, shift done signal is output.



**Response of the shift register can be confirmed by checking the shift done signal after inputting the 7 shift clocks to one direction.**

# Test bench to check shift registers

## Block diagram of test bench

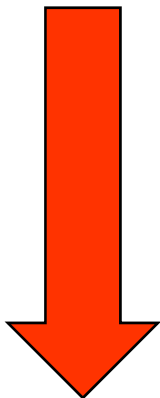


Shift done signal from readout ASIC is checked.

# Shift register test for the 1<sup>st</sup> prototype

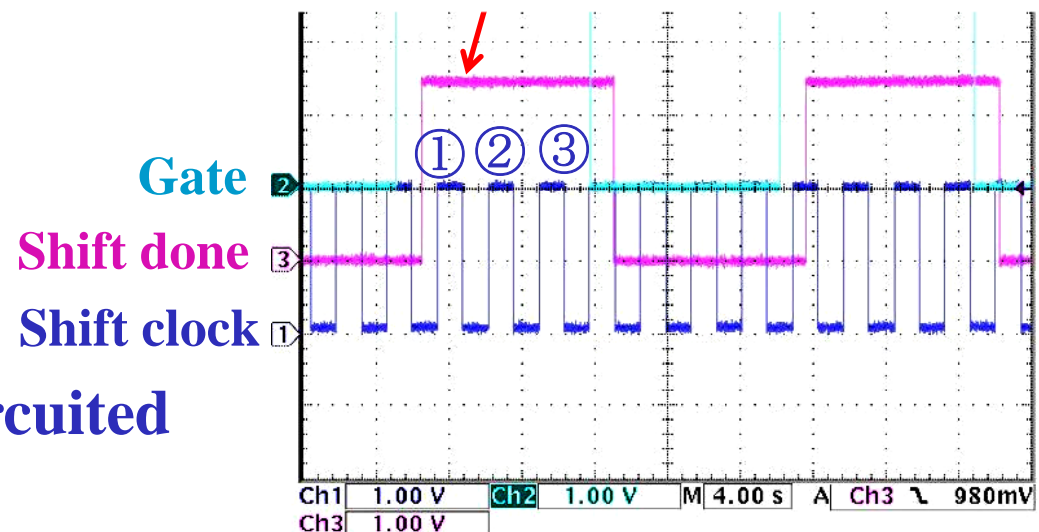
## Shift register test for the 1<sup>st</sup> prototype

- Produced in February, 2005
- Shift register did not work correctly.
- The resistance for the protection of the digital input was insulated.



The digital input was short-circuited  
in the 2<sup>nd</sup> prototype.

Shift done signal is not output at  
the timing of the 7<sup>th</sup> shift clock.

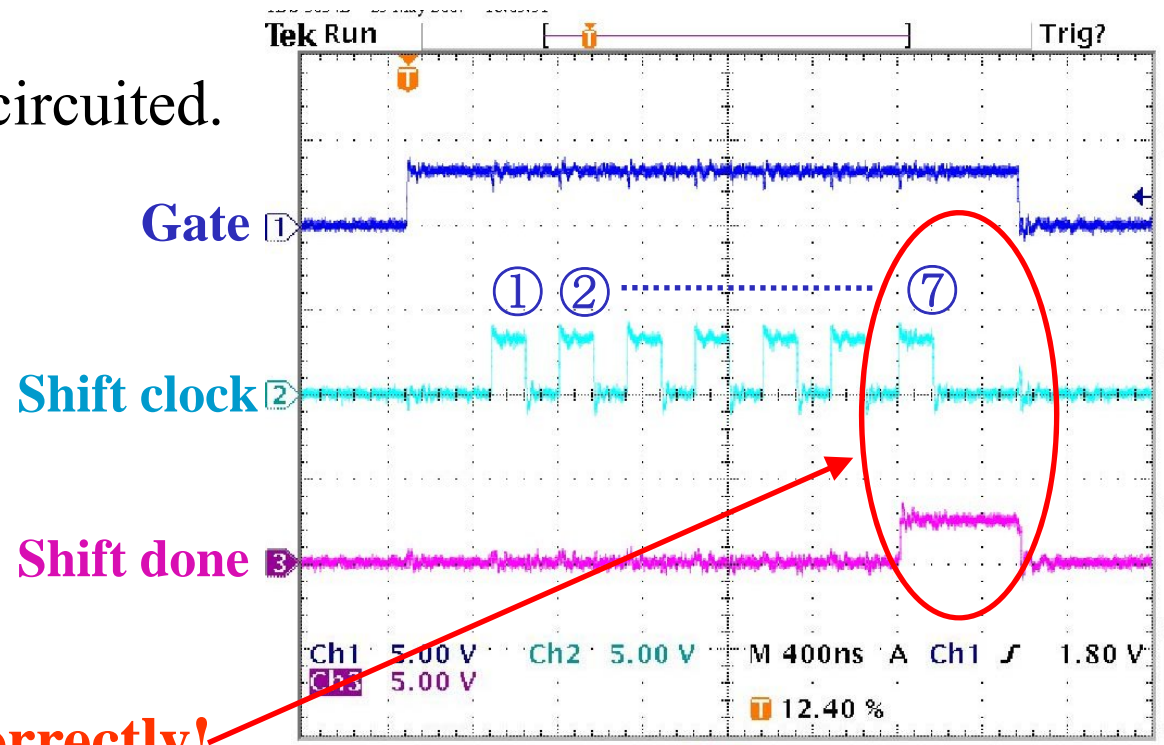




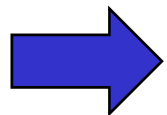
# Shift register test for the 2<sup>nd</sup> prototype

## Shift register test for the 2<sup>nd</sup> prototype

- Produced in May, 2007
- The digital input is short-circuited.



**The shift register works correctly!**



The next step is response test for the readout cell.



# Summary

- We continue to study the pair monitor.
- Performance of the pair monitor is studied by MC.
  - The beam size can be measured with 8% accuracy.
- Prototype of the readout ASIC is developed.
  - Response of the shift register was checked.
  - The problem was found in the digital input of the 1<sup>st</sup> prototype.
  - The shift register work well in the 2<sup>nd</sup> prototype.

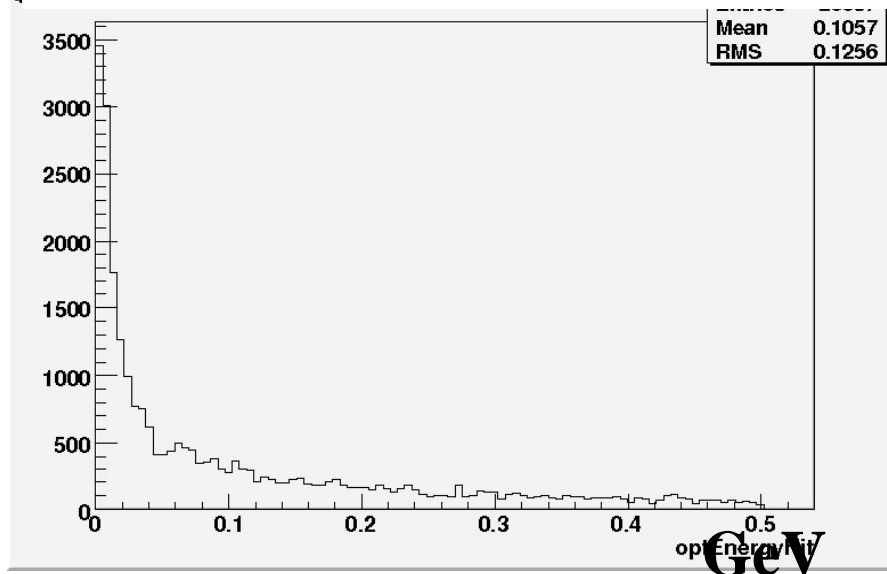


# Simulation parameter

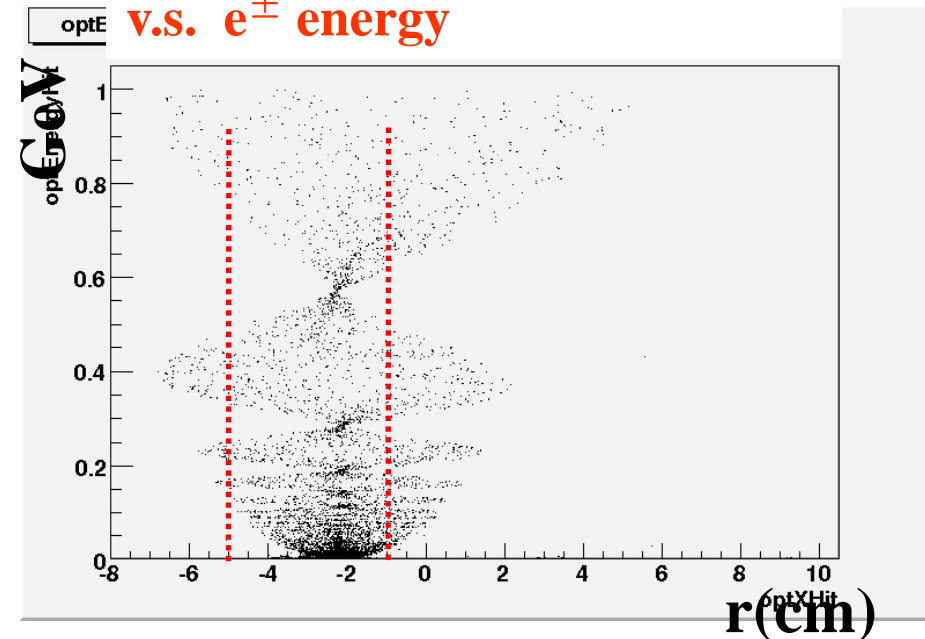
- Injection beam pipe :  $r=1.0\text{cm}$
- Extraction beam pipe :  $r=1.8\text{cm}$
- anti-DID parameter : 1.2

# Energy distribution of $e^\pm$

Energy of  $e^\pm$  hitting the pair monitor



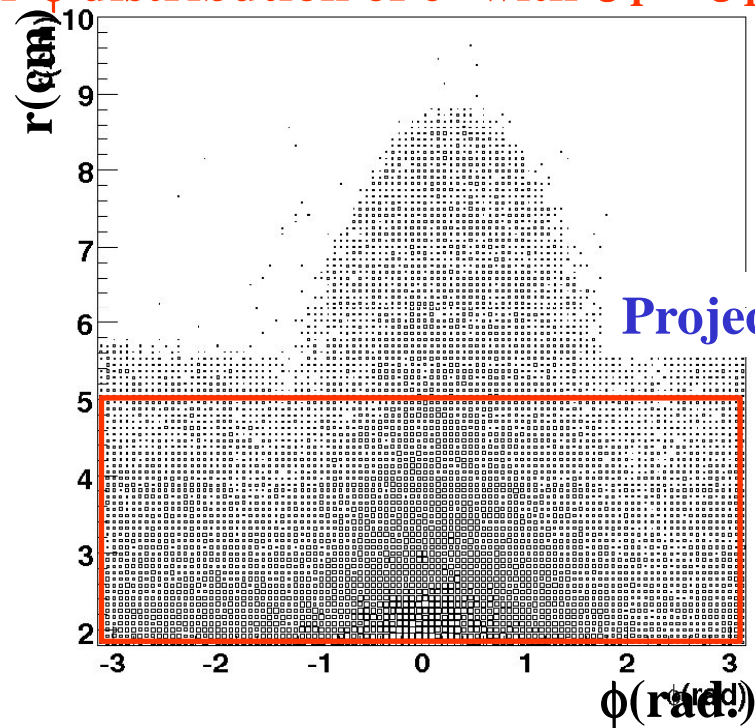
r of the extraction beam pipe  
v.s.  $e^\pm$  energy



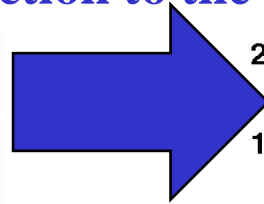
Low energy particles are in the extraction beam pipe.

# r- $\phi$ distribution

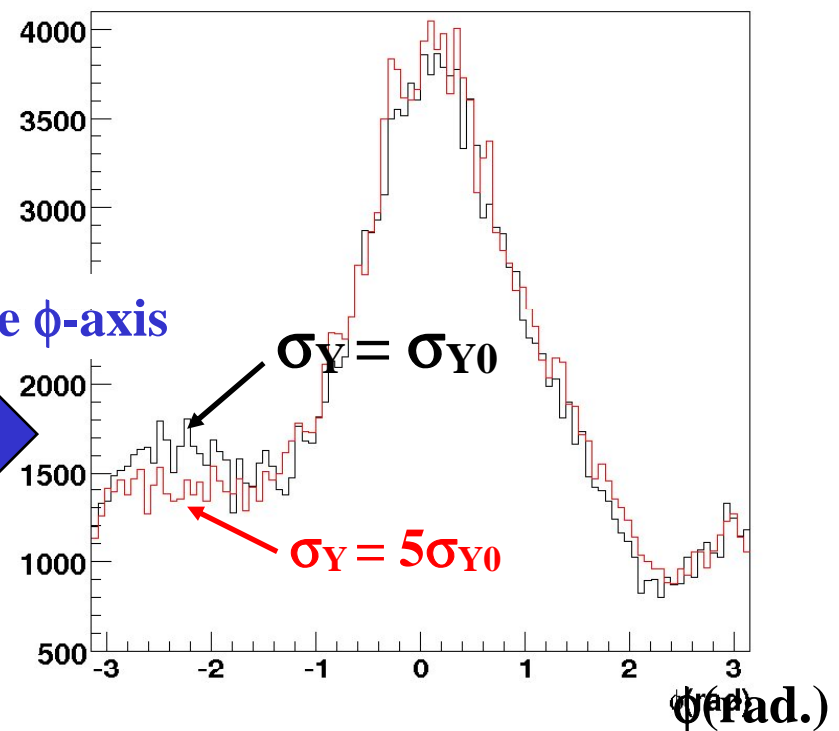
r- $\phi$  distribution of  $e^+$  with  $\sigma_Y = \sigma_{Y0}$



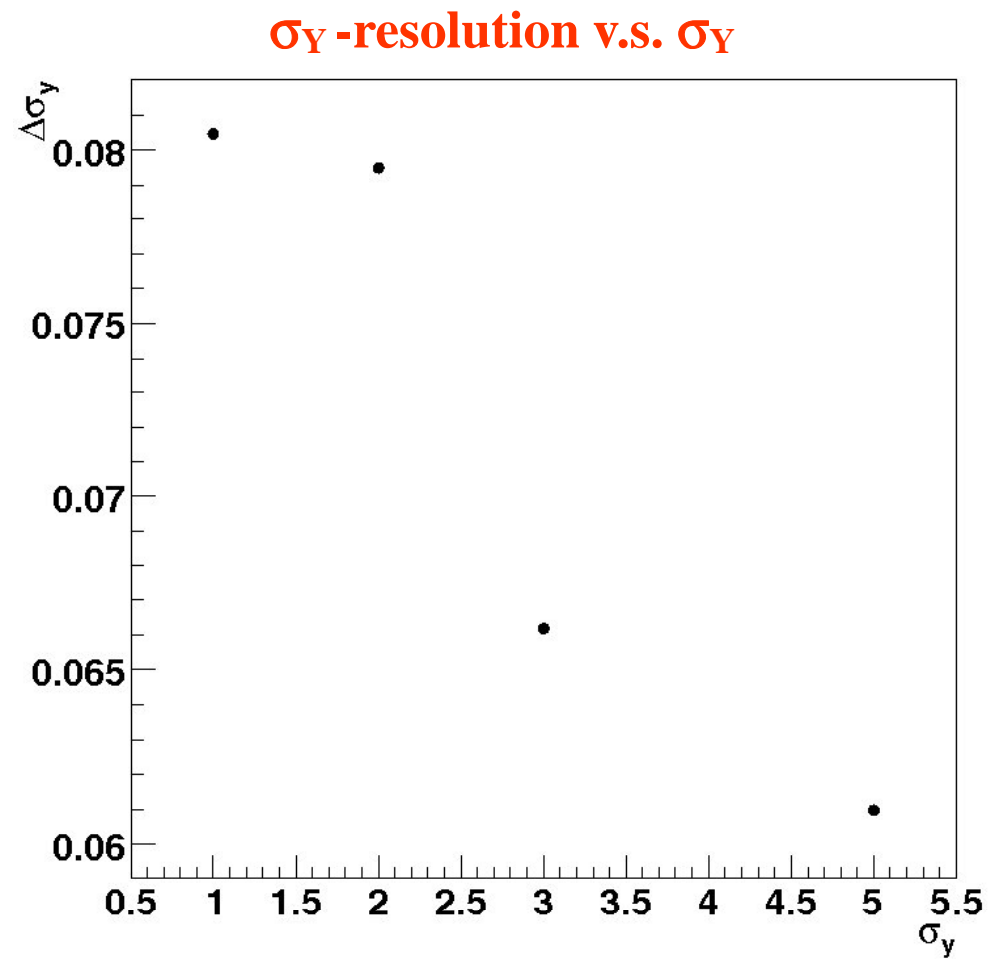
Projection to the  $\phi$ -axis



$\phi$  distribution in  $r=2\sim 5\text{cm}$



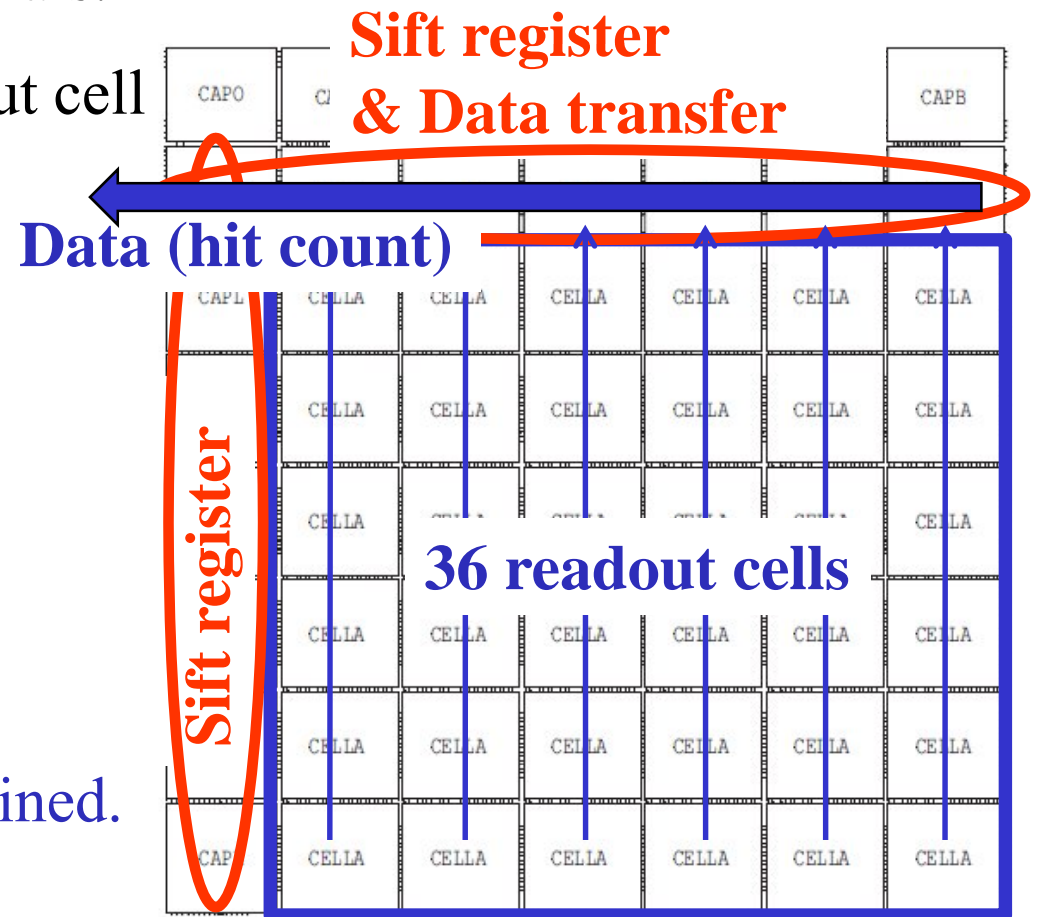
# $\sigma_Y$ resolution



# Design of the readout ASIC

## Structure of readout ASIC

- Cells to distribute operation signals.
- Shift register to specify a readout cell
- Data transfer to the output line
- 36 readout cells

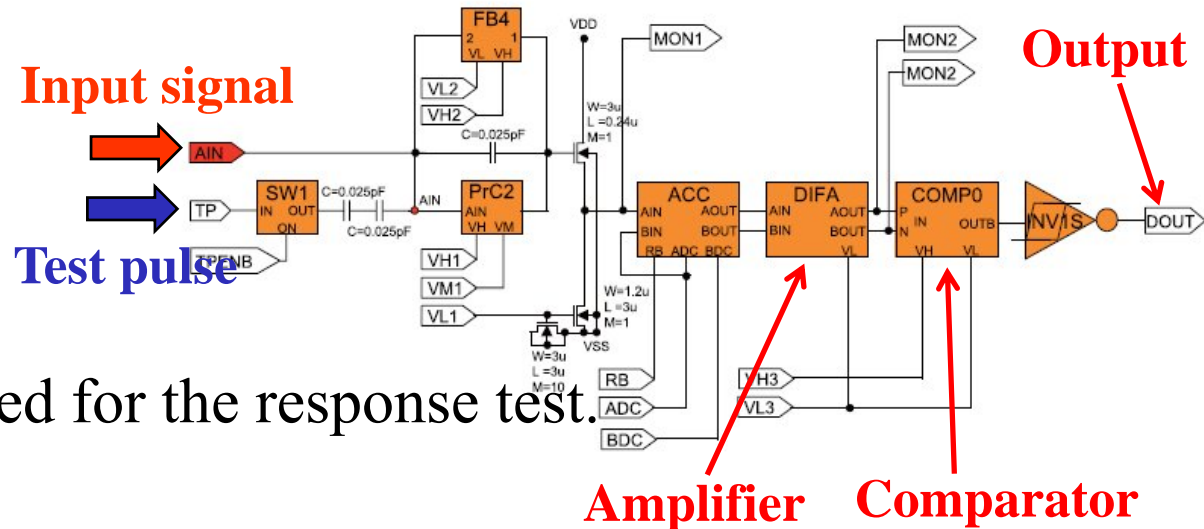


Structure of readout cell is explained.

# Analog part

## Analog part

- Signal input
  - Test pulse can be used for the response test.
- Amplifier
- Comparator
  - B.G. event below threshold is rejected.
- Signal monitoring after and before the amplifier.
  - The readout cell and monitoring part can be specified by the operation signal.
- The digitized signal is sent to the digital part.





## Digital part

- 
- The diagram illustrates a 4-bit parallel adder circuit. It consists of four 74181 ALUs (Arithmetic Logic Units) and one 74160 counter (8-bit counter).
- Inputs:** Four 4-bit input registers (R1, R0, W1, W0) provide the operands. An 8-bit input signal (W3, W2, W1, W0) is used to set the carry-in (CIN) of the counter and the enable (ENB) of the ALUs.
  - ALU Configuration:** Each 74181 ALU is configured to perform addition. The inputs A1, A0, B1, B0 are connected to the 4-bit inputs. The carry-in (CIN) is connected to the carry-out (COUT) of the previous ALU. The output (F) is connected to the 4-bit output registers (F1, F0, F1, F0).
  - Counter:** The 74160 counter is configured to count from 0 to 15. The output (Q0, Q1, Q2, Q3) is connected to the carry-in (CIN) of the ALUs. The enable (ENB) is connected to the input signal.
  - Output:** The 4-bit output registers (F1, F0, F1, F0) provide the final 4-bit sum.
- Annotations in the image:
- Output:** Points to the 4-bit output registers (F1, F0, F1, F0).
  - Count registers:** Points to the 4-bit output registers (F1, F0, F1, F0).
  - Input signal:** Points to the 8-bit input signal (W3, W2, W1, W0).
  - 8-bit counter:** Points to the 74160 counter.