Vertex Summary at LCWS2007

Summary Report on VTX R&D

motivates new directions for R&D on silicon sensors.

- Test Facilities (4 talks)
- Sensor Technology (6 talks)
- Background Simulation (2 talks)
- Integration (3 talks)

outlook

requires silicon sensors which are substantially thinner and more precise than LHC

- close to IP : reduce extrapolation error
- impact parameter resolution:
  $\leq 5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$
- minimal multiple scattering : < 0.1% X_0/layer
- occupancy → small pixel size
  → data sparsification and zero suppression

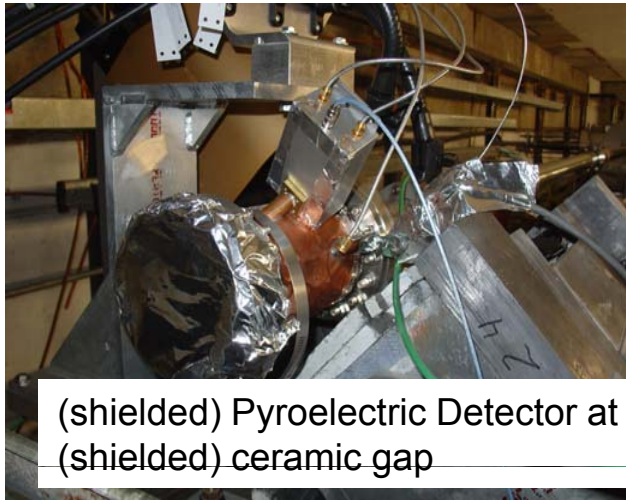
Hwanbae Park (Kyungpook Nat'l Univ.)

Progress on Test Facilities
- SLAC, LBNL, DESY, CERN, FNAL

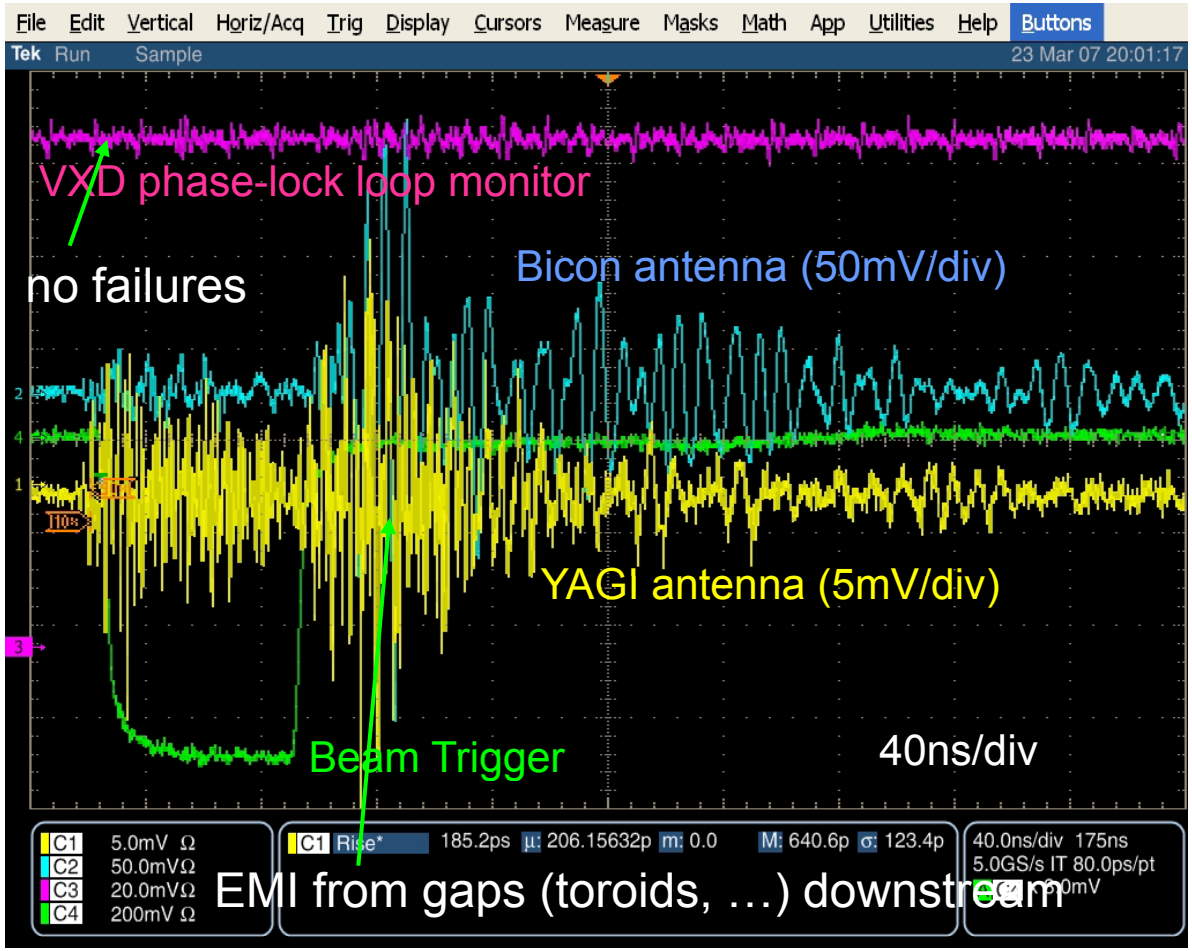
Test Facilities: EMI Studies at SLAC ESA

(by M. Woods)

- Placing just the VXD board inside an aluminum foil shielded box, covering the gap stopped failures
  - failures not due to ground loops or EMI on power/signal cables
  - failures are due to EMI emitted by gap which are camera windows, BPM feedthroughs, toroid gaps, etc.



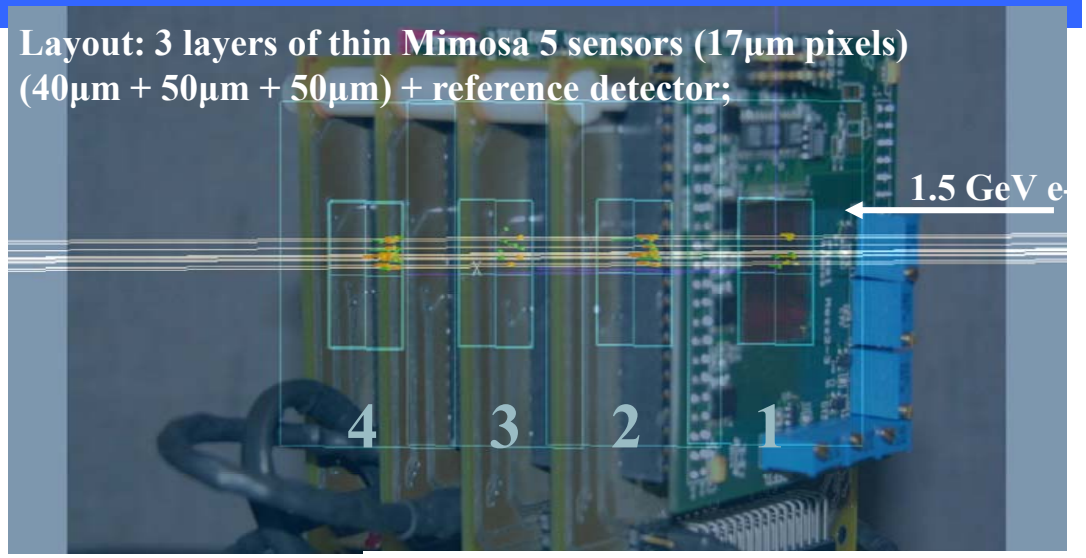
(shielded) Pyroelectric Detector at (shielded) ceramic gap



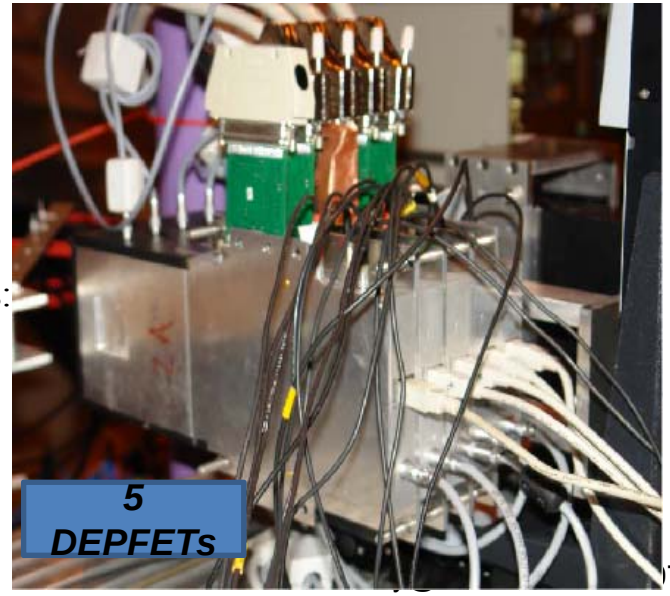
Test Facilities: Telescopes (1)

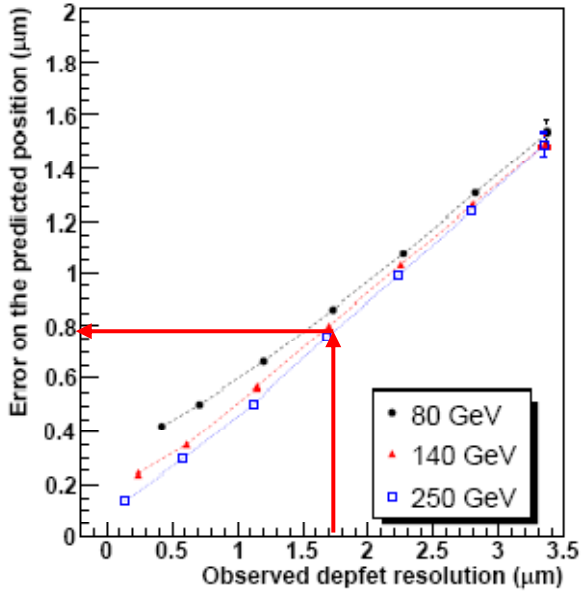
(by M. Battaglia, L. Reuen, D. Haas, A. Besson)

- First beam telescope based on thin CMOS pixel sensors at LBNL
- Prototype for proposed FNAL MBTF telescope & T966
- System test of multi-M pixel detector in realistic conditions



- DEPFET telescope at CERN
  - 4 DEPFET plane telescope + 1 DEPFET DUT
  - confirmed DESY test results: (4 planes of 350 t, 50 um strip, dssd +1 DUT)

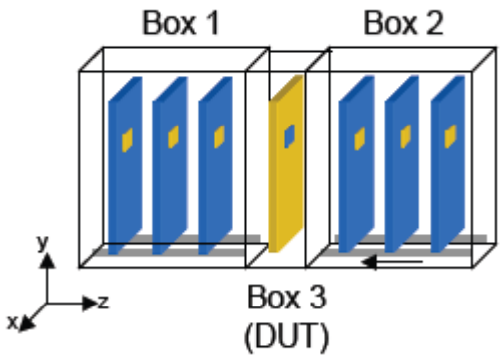


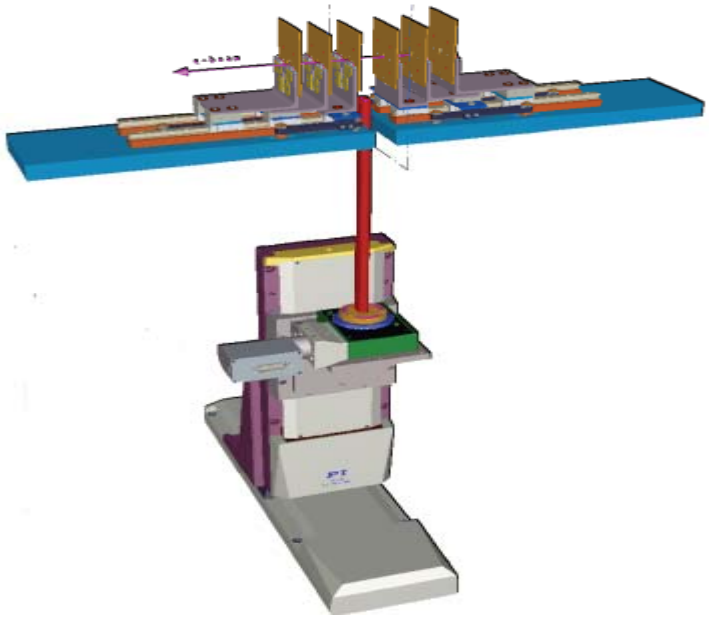


Test Facilities: Telescopes (2)

(by M. Battaglia, L. Reuen, D. Haas, A. Besson)

EUDET Telescope





- pixel beam telescope
  - 4~6 layers of MAPS detectors
  - CCD and DEPFET pixel detectors for validation
- easy-to-use DAQ system including Trigger Logic Unit
- EUDET infrastructure is movable
  - initial test at DESY
  - possible move to CERN, FNAL, etc

Final telescope by the end of 2008

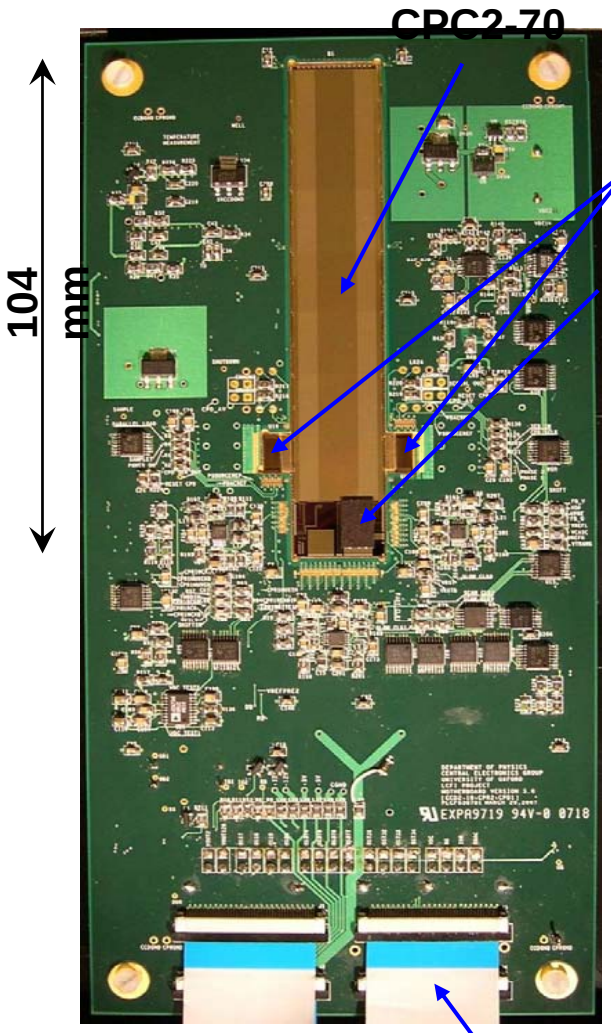
"Demonstrator" is available in this fall

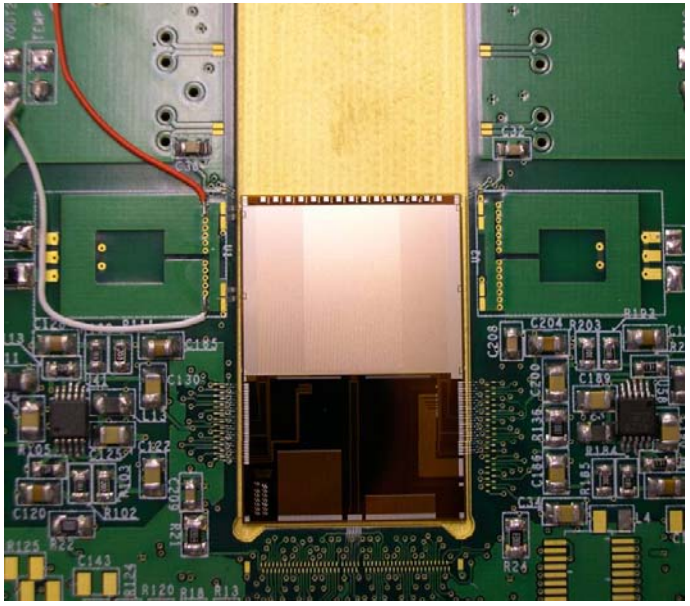
- Only 3 sensor planes
- Mimotel sensors (256x256, 7.6x7.6 mm)
- Testbeam next week (@DESY), to:
  - qualify the concept
  - test the DAQ
  - measure sensor performance

"Come and Use It"

Development on Sensor Technology - CCD, DEPFET. CMOS, SOI&3D

Sensor Technology: CPCCD (by K. Stefanov)

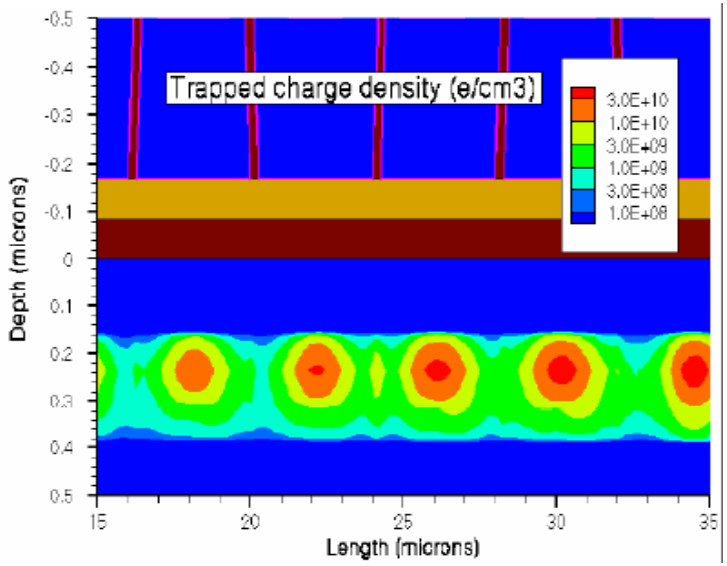


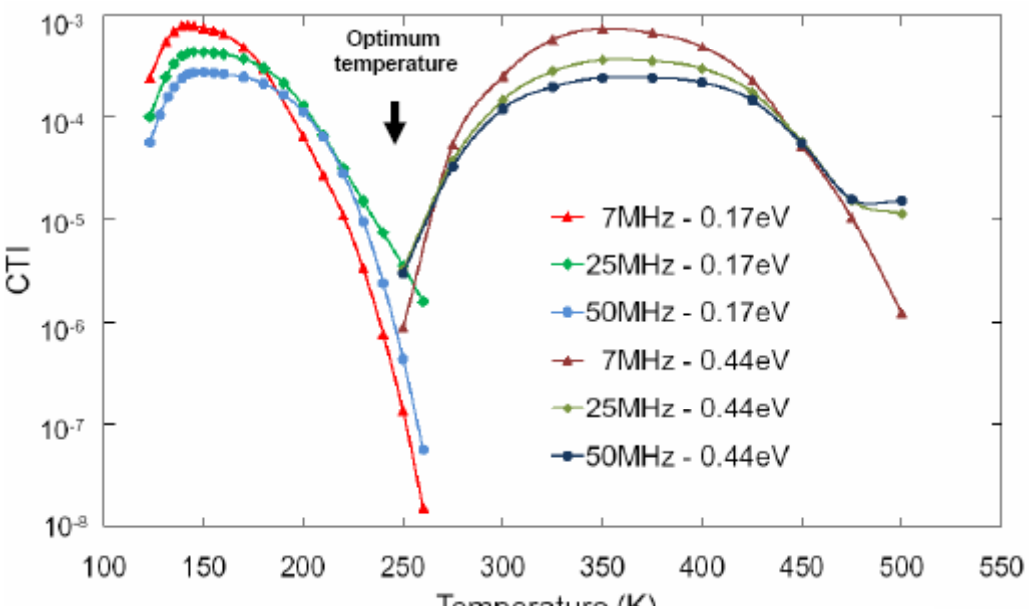


High-speed busline free CPC2 working at 45MHz

- All ingredients are in place – intensive testing ahead in the next months
- Getting closer to prototype ladder
- Third generation CMOS readout chips CPR2A in design stage

Simulation Study of CTI: CCD (by A. Sopczak)





- ISE TCAD simulations and analytical modelling have been applied in order to predict the Charge Transfer Inefficiency (CTI) for a three-phase CCD detector.
- Expected radiation hardness is well understood as a function of temperature and frequency.
- The optimal operation temperature has been determined where the CTI expectation has a minimum.
- Results obtained from ISE TCAD simulation and analytical modelling are compared. Good agreement has been found for the 0.17 eV traps, but not for the 0.44 eV traps.

Sensor Technology: FPCCD (by Y. Sugimoto)

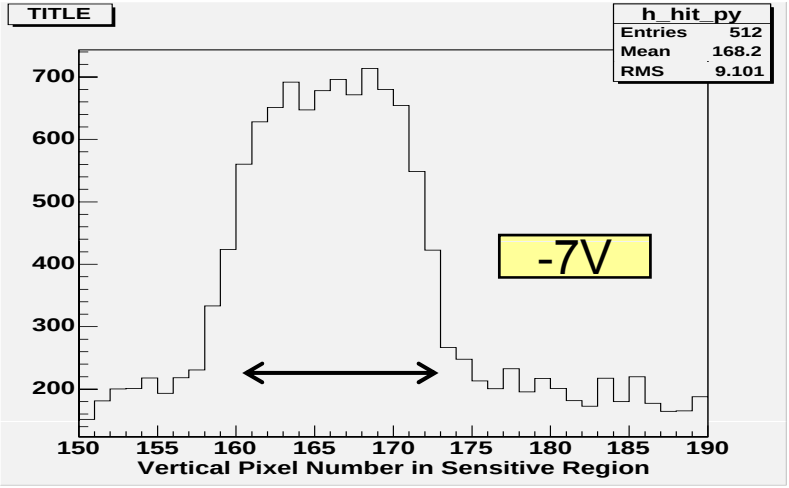
- Accumulate hit signals for one train and read out between trains (200ms) → Completely free from EMI

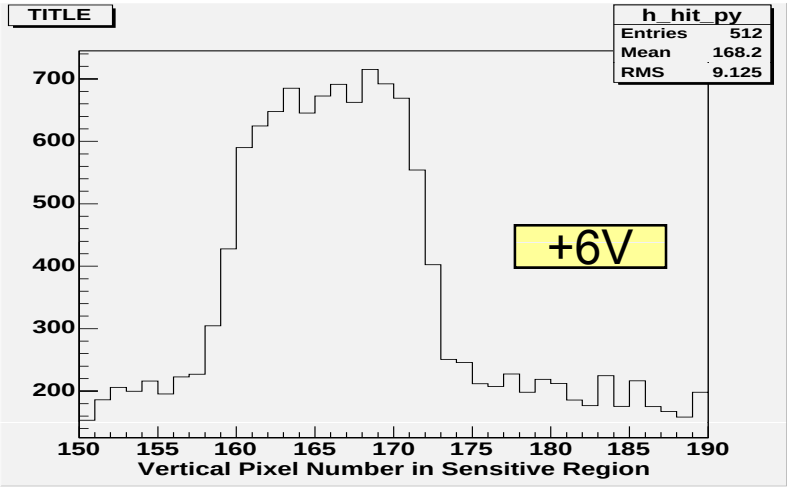
→Fine pixel of ~5μm to keep low pixel occupancy

→Fully depleted epi layer to minimize the number of hit pixels due to charge spread by diffusion

Confirmation of full-depletion using line-focused LASER

Highest resistivity 24um thick epi-layer





- Measurement of Lorentz angle and study of radiation hardness of this CCD are planned in this FY
- Fabrication of smaller pixel, multi-port readout CCD and ASIC for readout of the multi-port CCD are also planned in this FY

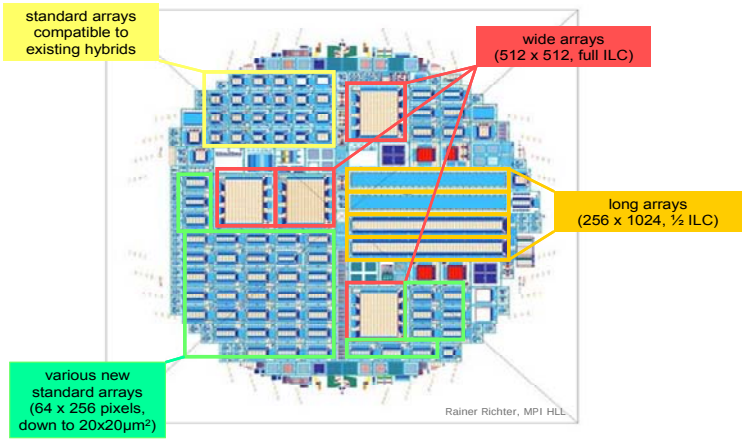
Sensor Technology: DEPFET (by L. Andricek)

- Preparations for the new DEPFET generation are in full swing:
  - New Sensors, larger matrices, with improved gain expected end of June 2007
  - Steering chip Switcher operational and rad. hard
  - New r/o chip submitted
- Radiation tolerance of basic pixel cell proven for fluences far beyond the ones expected at the ILC .

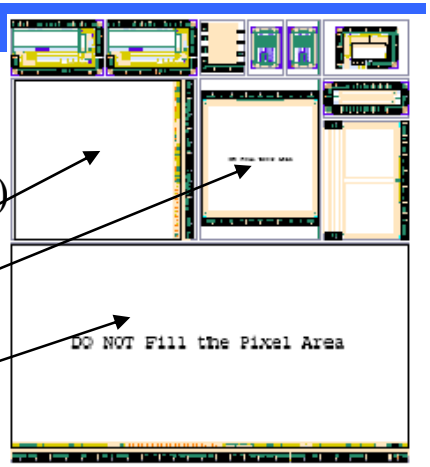
(*) 5..22 fA non irrad.

irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3x10^{12} n/cm^2	~-5V	~ -15%	26 pA

- New generation is almost done
  - very small pixels (20µm x 20µm)
  - increase internal amplification



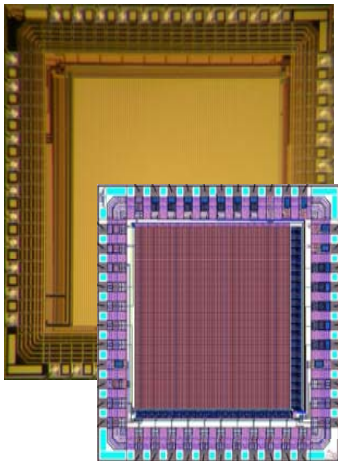
Sensor Technology: CMOS (by A. Besson)



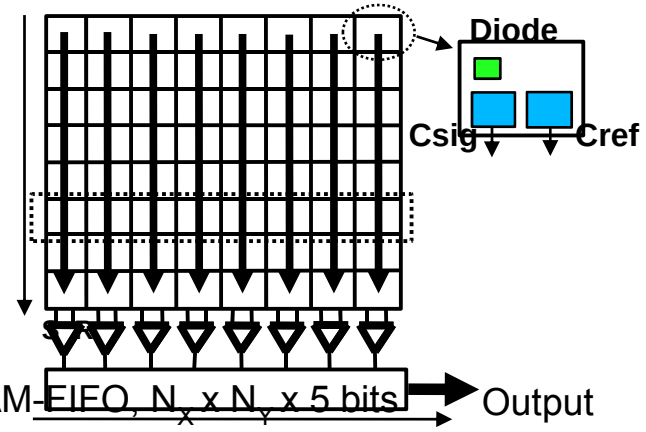
- CMOS sensors developed for running conditions
  - with beam background >> MC simulation (sizeable occupancy uncertainty)
- General performances well established
  - eff., S/N, fake hits, resolution, rad. hardness, moderate cooling
  - AMS 0.35 µm OPTO techno assessed. ⇨Baseline for R & D
  - new generation of full scale sensors underway:
    - real experimental conditions: equip EUDET, STAR, CBM demonstrator in 2007/2008
- Fast read-out sensors progressing steadily
  - column // architecture with integrated discri. operationnal
  - ADCs close to final design
  - ∅ µcircuits: 1st generation close to fabrication
- Milestones
  - EUDET/STAR: final sensors with discri. binary charge encoding (2009 and 2010 resp.)
  - replace discris by ADCs. Increase final read-out frequency
  - find the final fabrication process (~< 0.2 µm)

Sensor Technology: CMOS (by D. Contarato)

- Two prototypes of LDRD family produced and tested, exploring various pixel designs and architectures; submission of next prototype with CP readout and 5-bit ADC in Summer



- second prototype chip in AMS 0.35 µm OPTO process, 14 um epilayer
- 20×20 µm^2 pitch, 3×3 mm^2 and 5×5 mm^2 diodes
- Tests underway; study of performance w.r.t. to clock frequency, up to 25 MHz



Sensor Technology: CMOS (by J. Brau)

- Macro (50 um pitch) for timing
- Micro (5 um pitch) for precise position

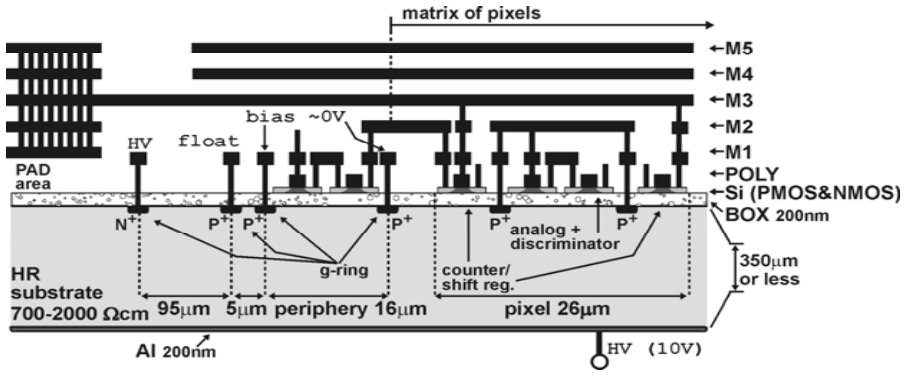
563 transistors, 2 buffer, 50 um pixel (180nm tech)

- Detector sensitivity
  10 µV/e (eq. to 16 fF)
- Detector noise
  25 electrons
- Comparator accuracy
  0.2 mV rms (cal in each pixel)
- Memory/pixel
  2 x 14 (will be 4 x 14)
- Ready for 80 x 80 array submission
- Designed for scalability
  eg. No caps in signal path

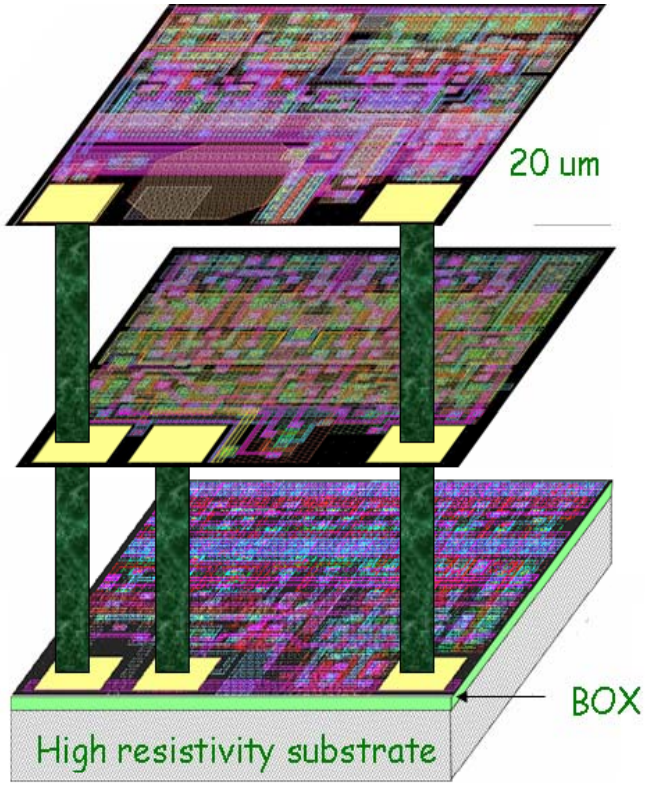
10~15 um pixel (45 nm tech):
Much more tolerant to high background

Emerging Sensor Technology: SOI & 3D
(by S. Cihangir)

- Isolation from the bulk silicon:
  Lower parasitic capacitance and therefore faster switching and lower power consumption…
  Enabling operation at higher temps (250°C)



- OKI 0.15 µm SOI process (Mambo SOI X-Ray Chip)
- Counting pixel detector plus readout circuit
  - max counting rate ~1 MHz
  - 64x64 26 um pitch on 350 um thickness, 12 bit counter
- Just received → tests are underway at Laser test stand.



3D integration (VIP1 chip, fabricated in MIT LL 0.18 µm)

At LBNL (by D. Contarato)

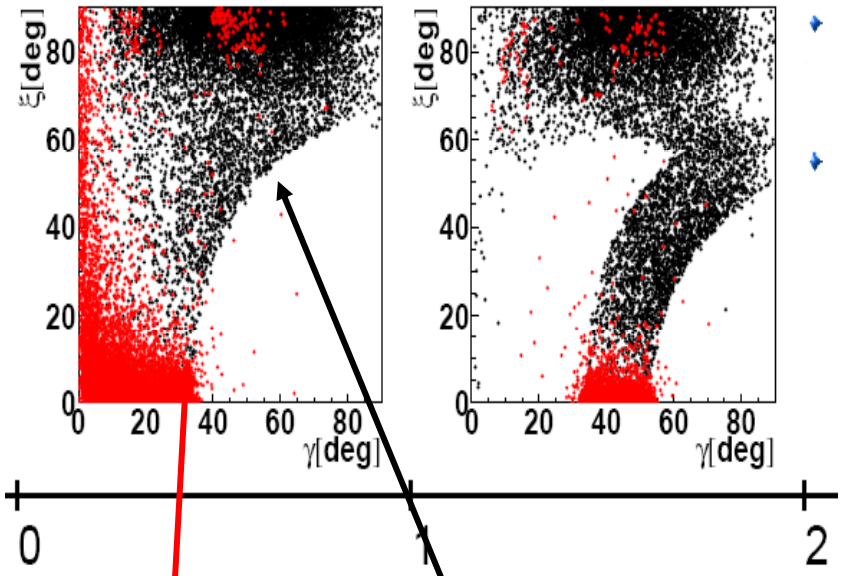
- First prototype in OKI 0.15 um SOI technology (160x150 pixels, 10x10 um2 pixels) just received, tests underway; next prototype submission in Fall '07 with optimized process.

Simulation Study

- Effect of beamstrahhlung on VTX performance
- Pamametrization for MAPS response and Geant4 Simulation

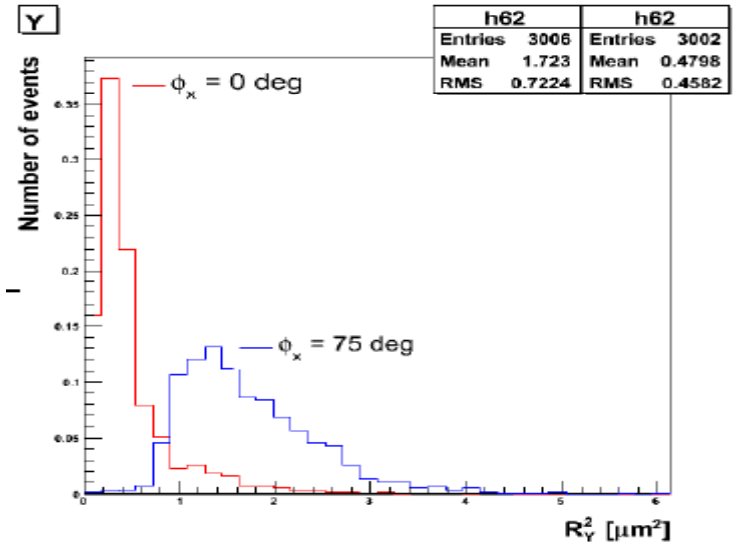
Simulation Study (by P. Luzniak and L. Maczewski)

- 14 mrad crossing angle
- MCS and energy loss
- VTX readout : 20 times per bunch train (1 readout cycle = 131 BX)



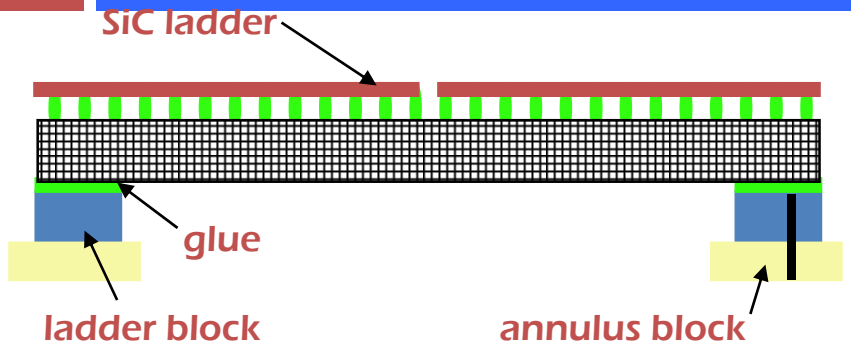
- may possible distinguish between "physics" and "background" hits with help of variables describing hit cluster shape

- Proposed parametrisation of MAPS response describes test data for particles passing detector at $\theta = 0^\circ$
  - Needed measurements with rotated array in order to check how our parametrisation works for $\theta \neq 0^\circ$
- The model presented here can be used to implement detailed detector response description in a Geant4 simulation
- Check possibility to reject beamstrahlung background exploiting cluster shape.



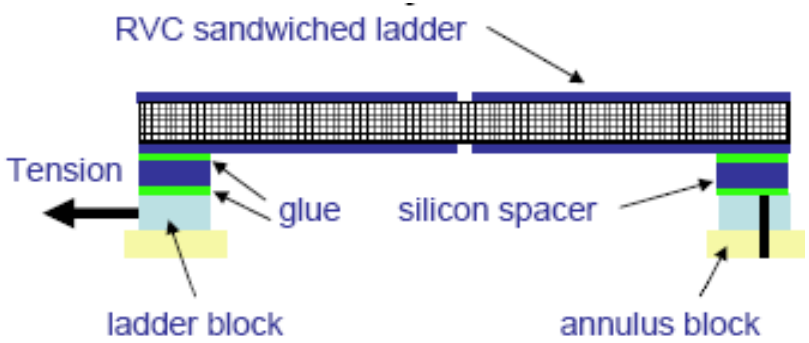
Integration Issue

Integration: (by E. Johnson, M. Battaglia, L. Andricek)



- Silicon Carbide Foam Ladder
  - 20 um thickness silicon
  - 1.5 mm thickness SiC foam
  - Silicone adhesive pads

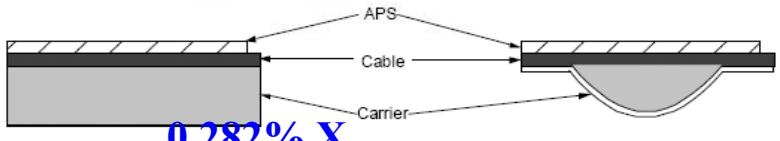
~0.14% X_0



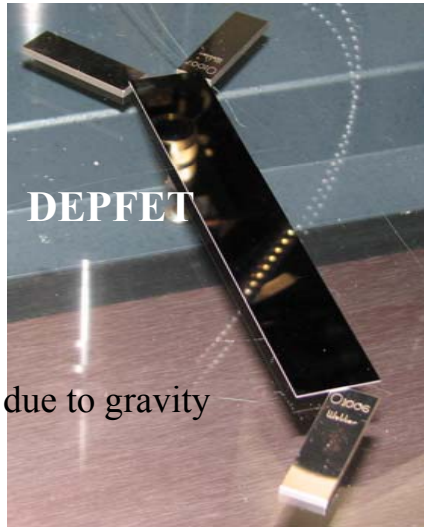
- Reticulated Vitreous Carbon Foam/Silicon Sandwich Ladder
  - 20 um thickness silicon
  - 1.5 mm thickness RVC foam
  - Silicone adhesive pads
  - Tension ~1.5 N

~0.08% X_0

- Continue prototyping foam ladder
- Finite Element Analysis is in progress
- Build and test carbon fibre shell



0.282% X_0



20 µm deflection due to gravity

Outlook

- Advertise: global effort is starting to address integration issue across regions, technologies and concepts (regular phone meetings)
- Oct. 2007 VTX R&D review at FNAL

not later than 2012: complete prototype ladder