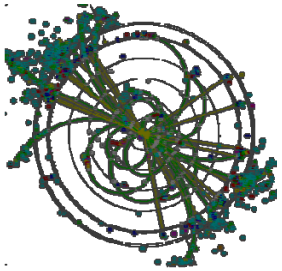
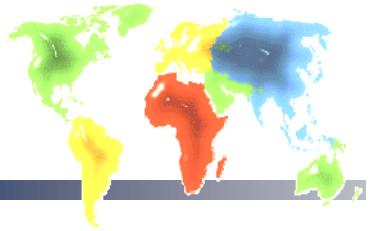


Development of an ILC vertex detector sensor with single bunch crossing tagging



Chronopixel[†] Sensors for the ILC

J. E. Brau, N. B. Sinev, D. M. Strom
University of Oregon, Eugene

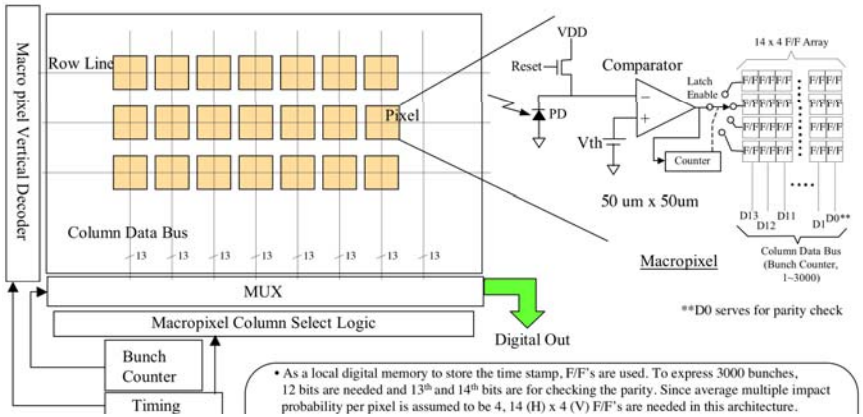
C. Baltay, H. Neal, D. Rabinowitz
Yale University, New Haven

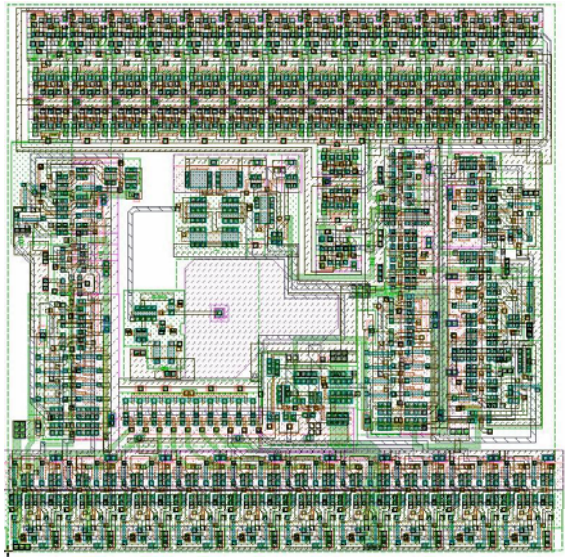
EE work is contracted to Sarnoff Corporation

Chronopixel (CMOS)

Yale/Oregon/Sarnoff

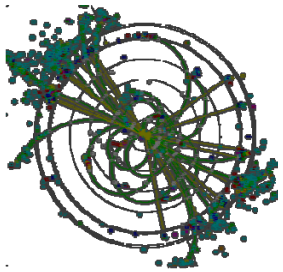
- Completed Macropixel design last year
  - ⇒ Key feature – stored hit times (4 deep)
  - 645 transistors
  - Spice simulation verified design
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Talking to JAZZ (15 μm epi-layer)
  - 90 nm ⇒ 20-25 μm pixel
- January, 2007
  - Completed Chronopixel design
    - **2 buffers, with calibration**
  - Deliverable – tape for foundry
- This year
  - Fab 50 μm Chronopixel array
    - Demonstrate performance
  - Then, 10-15 μm pixel (45 nm tech.)



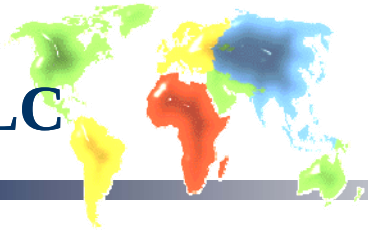


563 Transistors (2 buffers +calibration)

50 μm x 50 μm

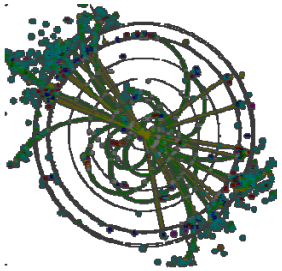


Inner Tracking/Vertex Detection for the ILC

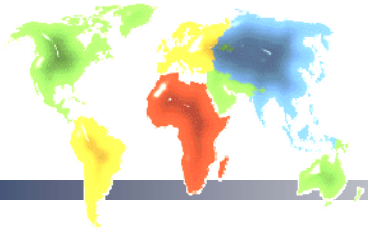


Detector Requirements

- Good angular coverage with many layers close to vertex
- Excellent spacepoint precision (**< 4 microns**)
- Superb impact parameter resolution (**$5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$**)
- Transparency **(~0.1% X_0 per layer**)
- Track reconstruction (**find tracks in VXD alone**)
- Sensitive to acceptable number of bunch crossings (**<150 = 45 μsec**)
- EMI immunity
- Power Constraint **(< 100 Watts**)



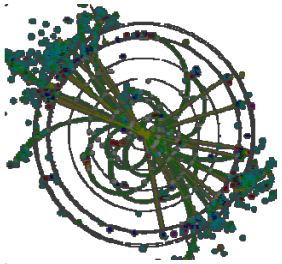
Occupancy



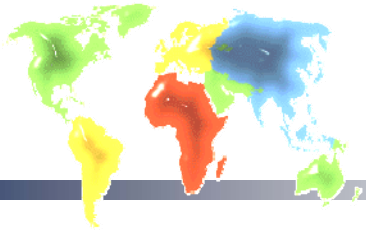
- Baseline occupancy 0.03 hit-clusters/mm^2/bunch,
  but could be higher for some configurations of the ILC.

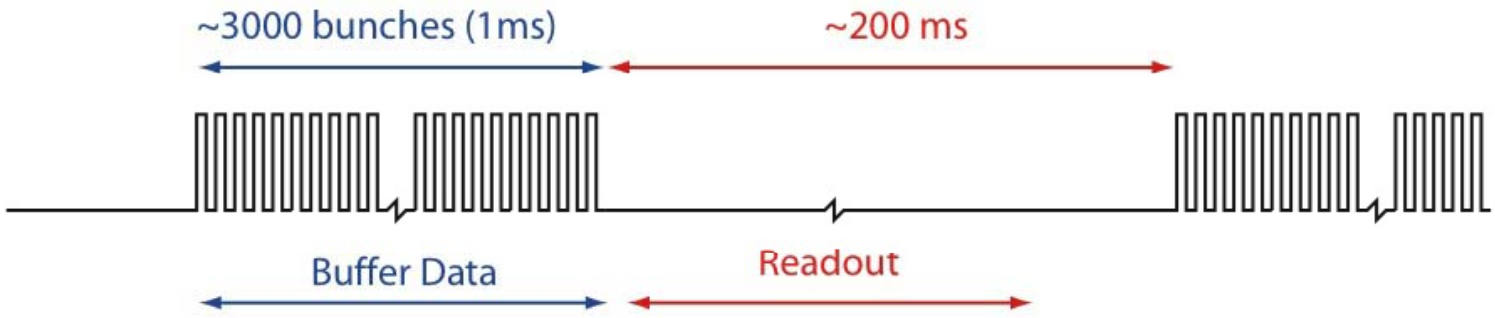
- Ideal situation is to have a bunch-by-bunch time tag for each pixel:
  For 20μm × 20μm pixels the baseline gives an occupancy of
  1.2×10^{-5} /bunch.

  n.b. from the point of view of occupancy, the pixels could be larger.
  For 50μm × 50μm pixels the occupancy is 7.5×10^{-5} /bunch.



Readout Strategy



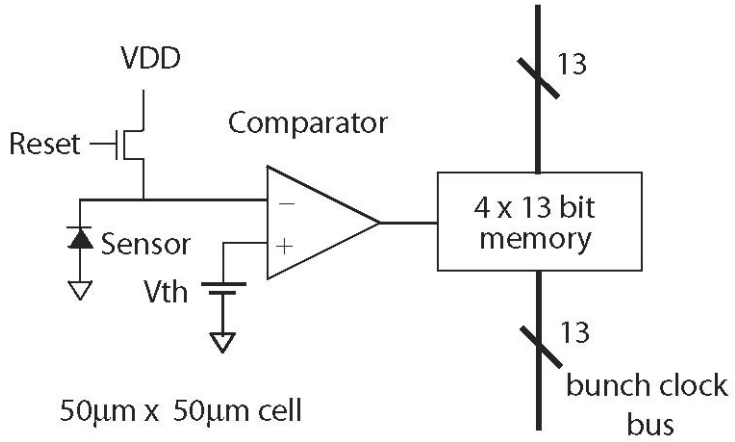


- Buffer data during the 3000 bunches in a train
  and readout between bunch trains

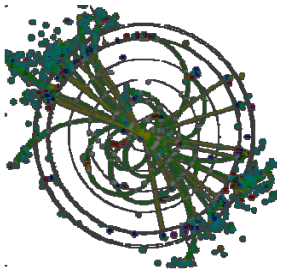
- For 50μm × 50μm pixels 0.03 hit-clusters/mm^2/bunch corresponds
  to a bunch-train occupancy of 22.5%.

- Assume 4 buffers per pixel
  Poisson probability for getting 4 or more hits is 10^{-4}

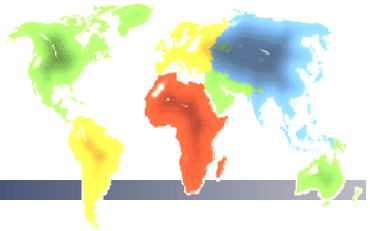
Simplified Chronopixel Schematic



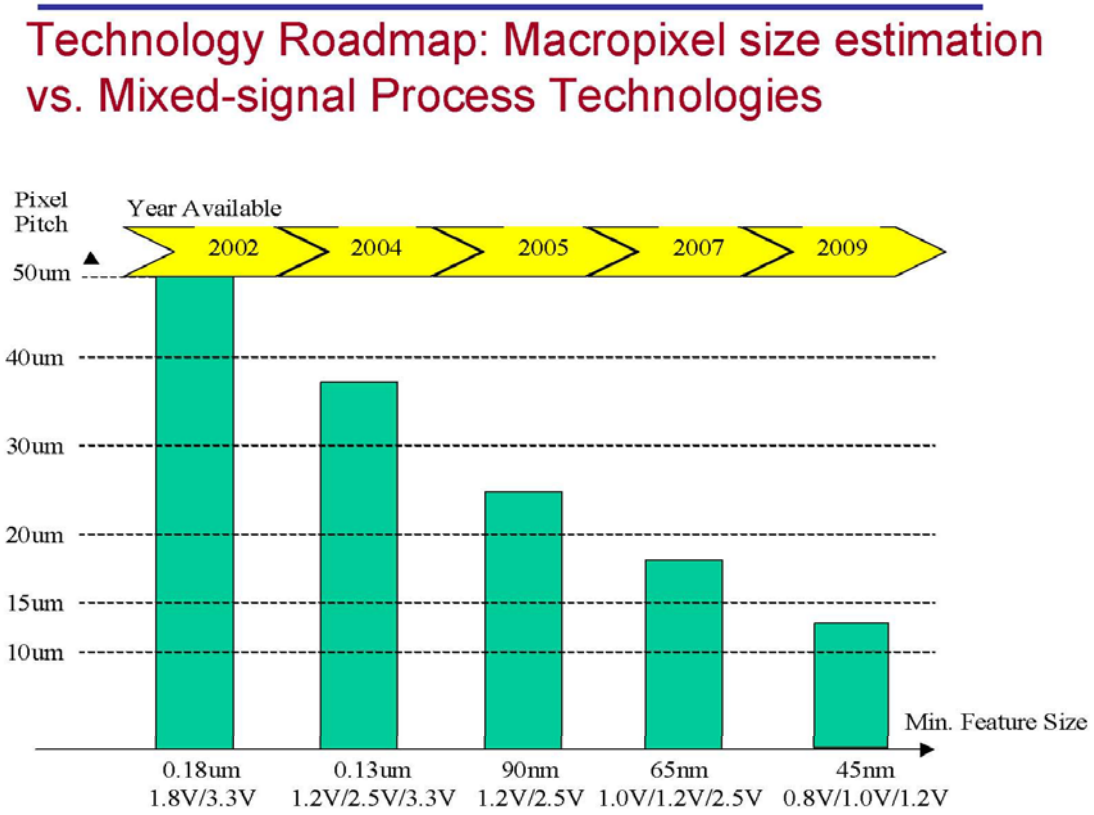
- Bunch number stored for up to 4 samples
- Target 180 nm CMOS and 50 µm x 50 µm pixel for initial R&D
  - Funding limited
- Voltage Vth is set via automatic calibration in each pixel



Technology Roadmap



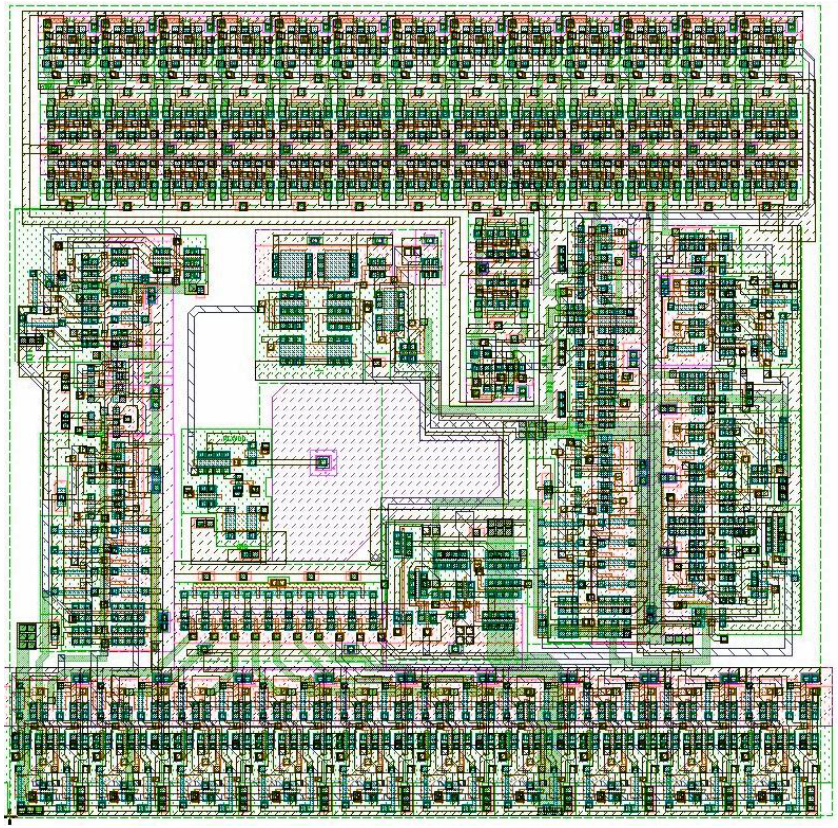
- Pixel size will scale down as technology advances
  - 180 nm -> 45 nm
  - 50 μm pixel -> 20 μm or smaller pixel

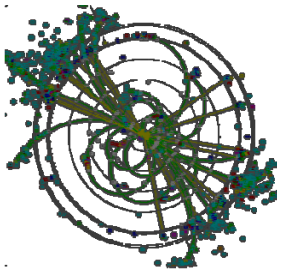


Completed Layout

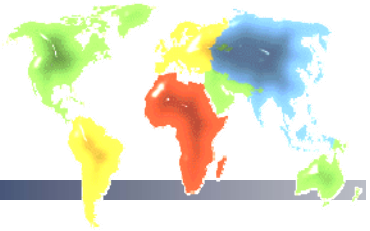
- Completed Layout of Sarnoff fits 2 buffers with 563 transistors
  into 50 μm x 50 μm for 180 nm technology

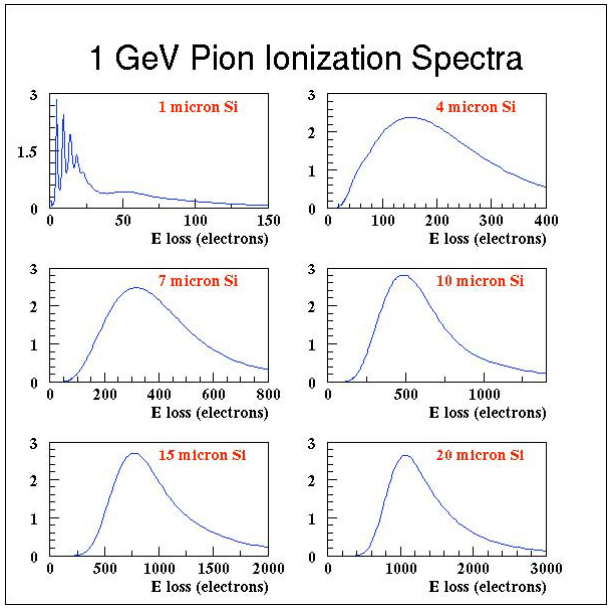
- Detector sensitivity
  10 μV/e (eq. to 16 fF)
- Detector noise
  25 electrons
- Comparator accuracy
  0.2 mV rms (cal in each pixel)
- Memory/pixel
  2 x 14 (will be 4 x 14)
- Ready for 80 x 80 array submission
- Designed for scalability
  eg. No caps in signal path

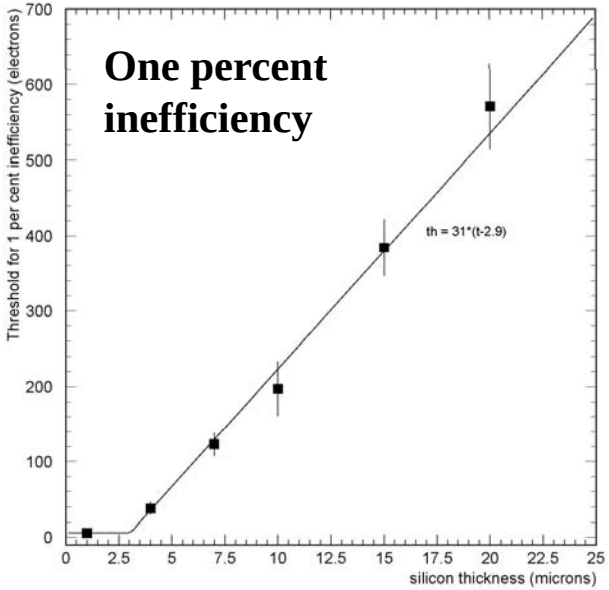




Expected Signal and Efficiency



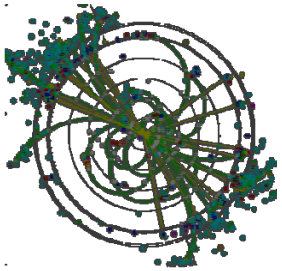




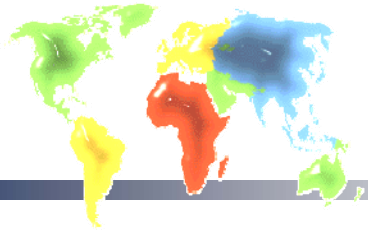
epilayer thickness (μm)	1% ineff. threshold electrons	50% hit sharing electrons	noise electrons
5	65	32	4
7	127	63	16
10	220	110	28
15	**375**	**188**	**47**
20	530	265	66

Target:
15 μm
fully depleted

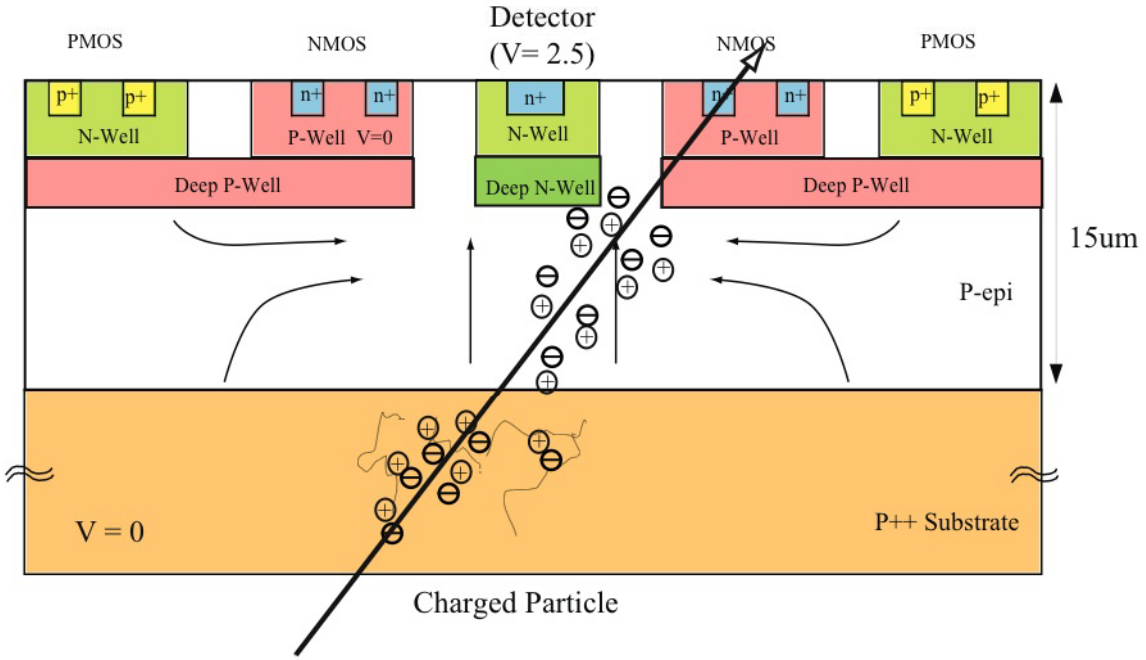
Noise requirement for threshold = 4 * noise

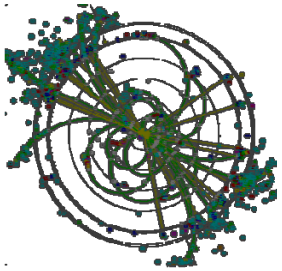


Ultimate Pixel Design

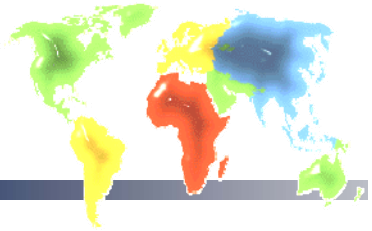


- Small charge collection node for low capacitance
- Deep p-well to direct electrons
- Relatively deep depletion for efficient charge collection
  - Thickness and resistivity of p-epilayer critical
- Detailed field simulations underway



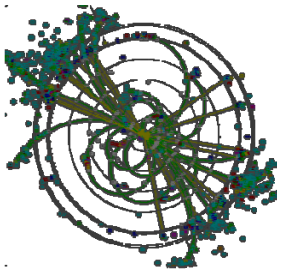


Simulation of Field Lines

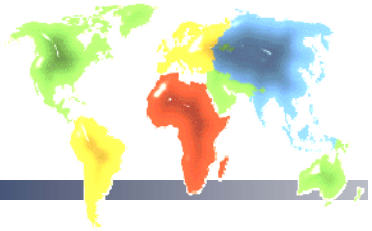


Calculations by Nick Sinev

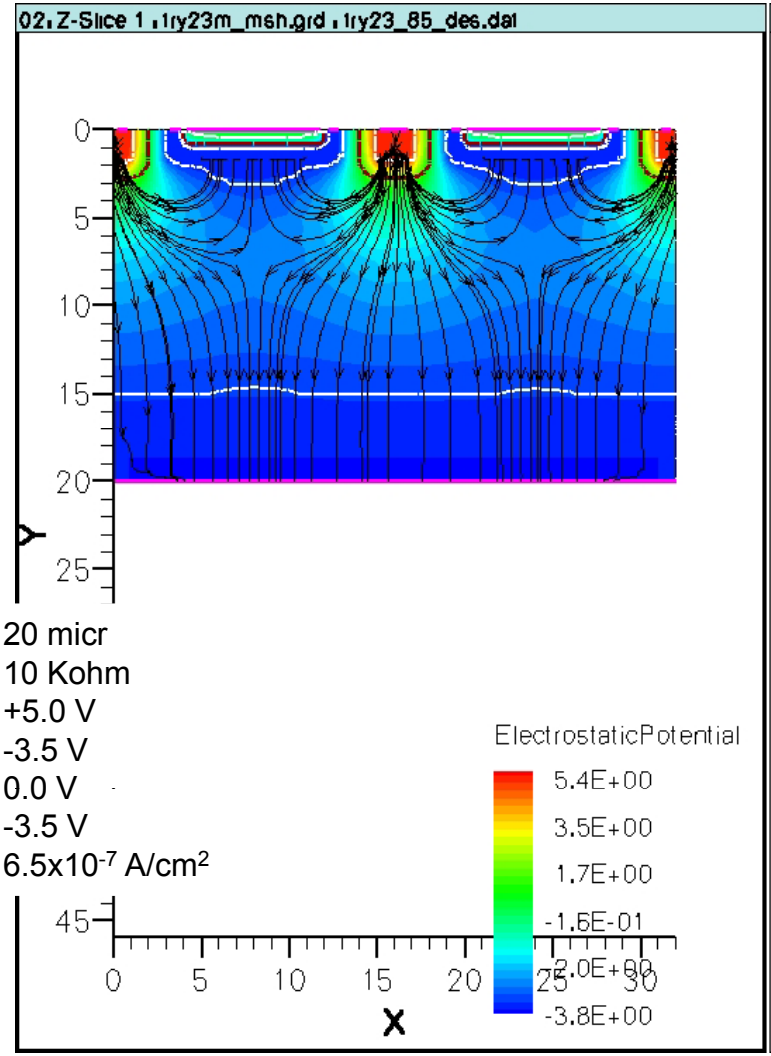
- 3D simulations underway
- Charge collection appears difficult
- 2D simulations not appropriate

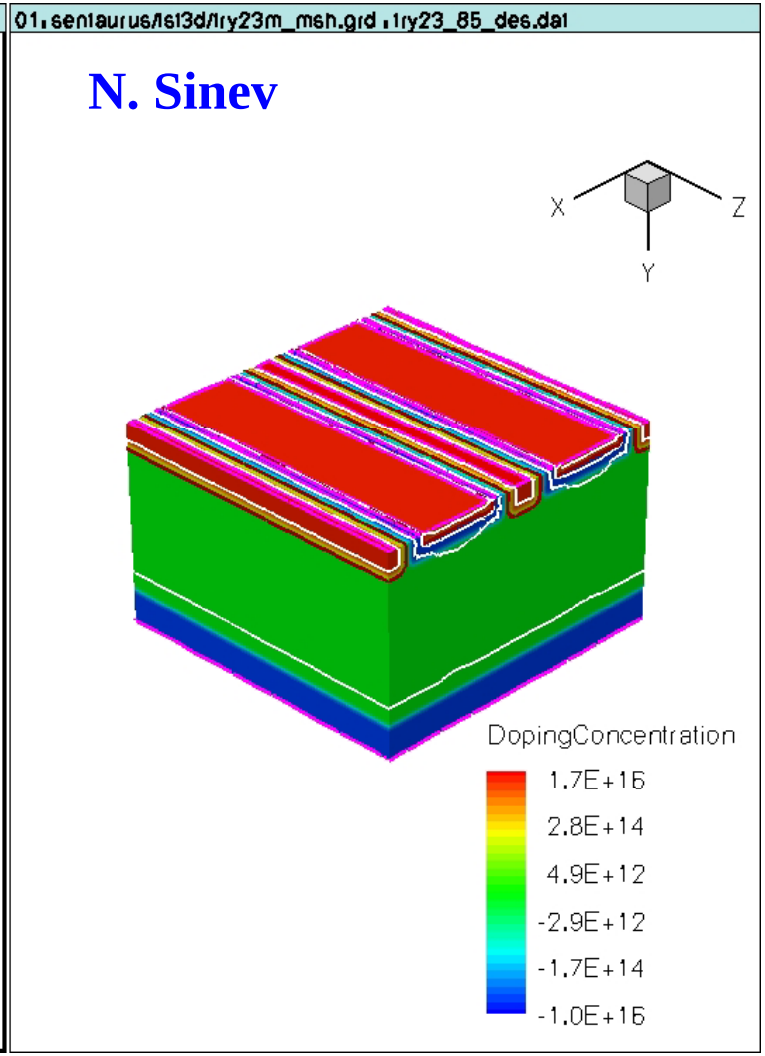


2D Simulation of Field Lines

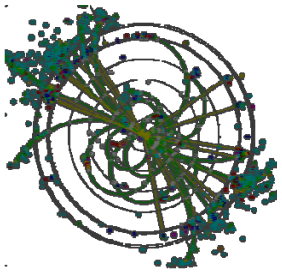


Calculations by Nick Sinev

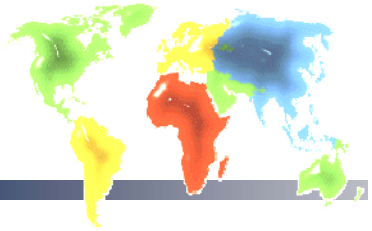




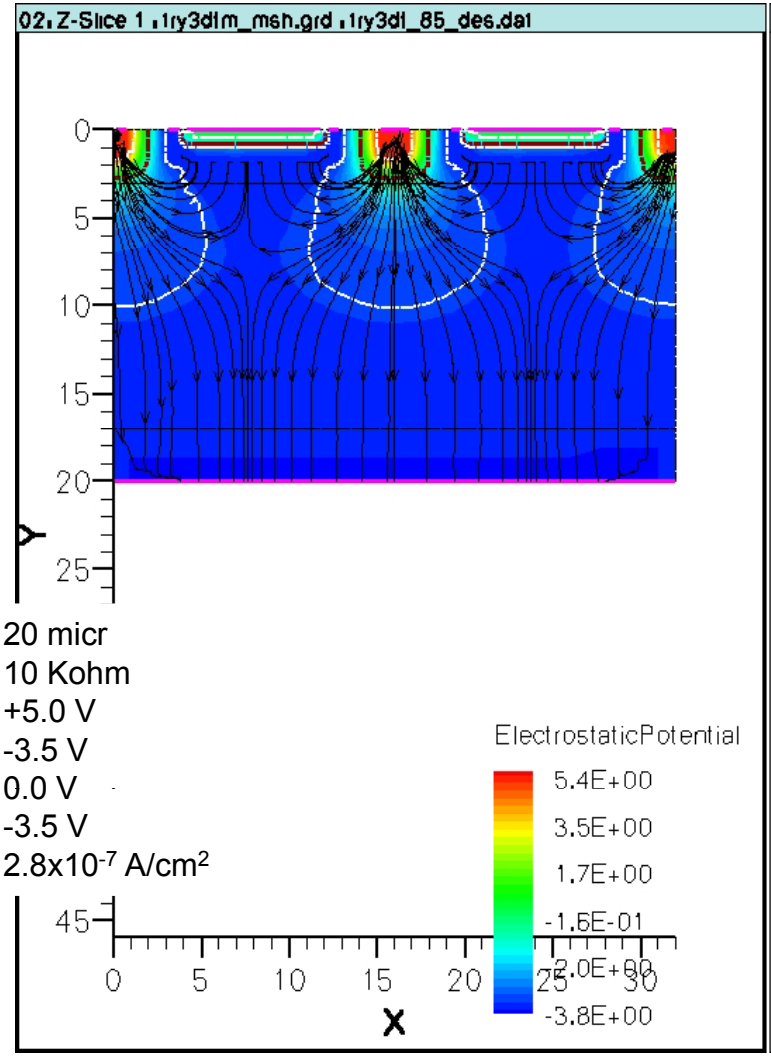
Epi thick.	20 micr
Si resistance	10 Kohm
Charge coll. V	+5.0 V
Deep p-well V	-3.5 V
Digital el. V	0.0 V
Back plane V	-3.5 V
Total leak. cur.	6.5×10^{-7} A/cm^2

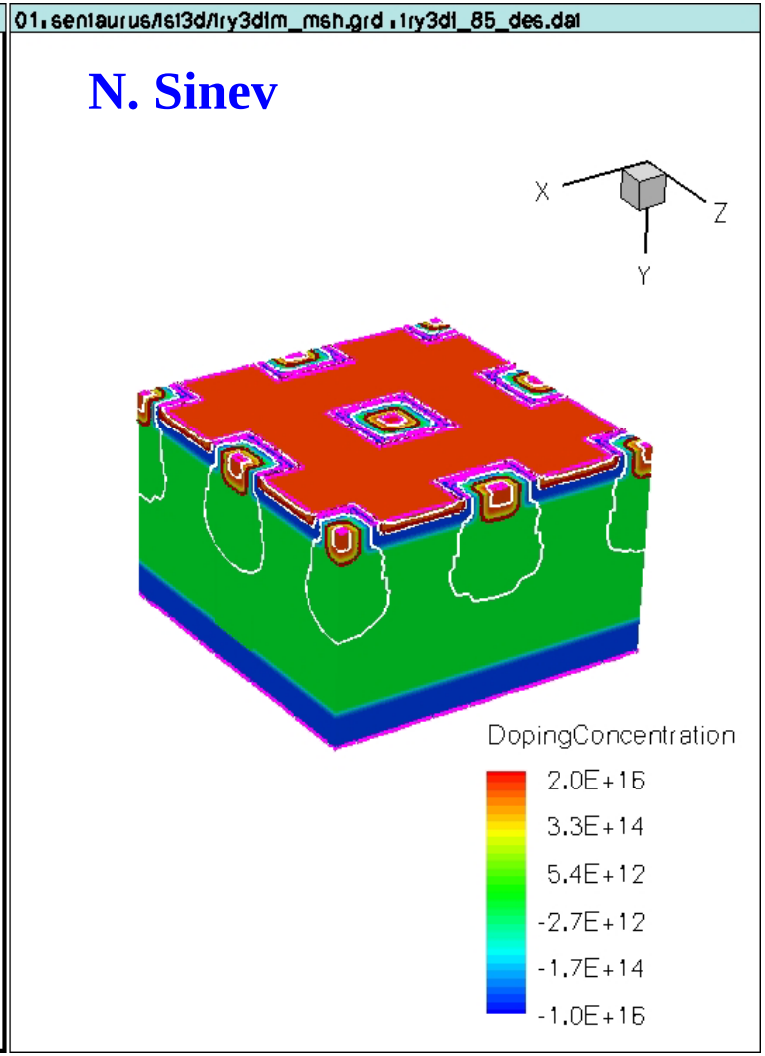


3D Simulation of Field Lines

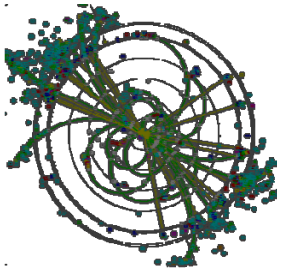


Calculations by Nick Sinev

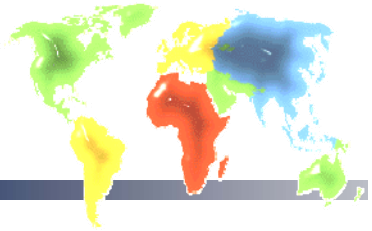




Epi thick.	20 micr
Si resistance	10 Kohm
Charge coll. V	+5.0 V
Deep p-well V	-3.5 V
Digital el. V	0.0 V
Back plane V	-3.5 V
Total leak. cur.	2.8×10^{-7} A/cm^2



Fabrication Roadmap

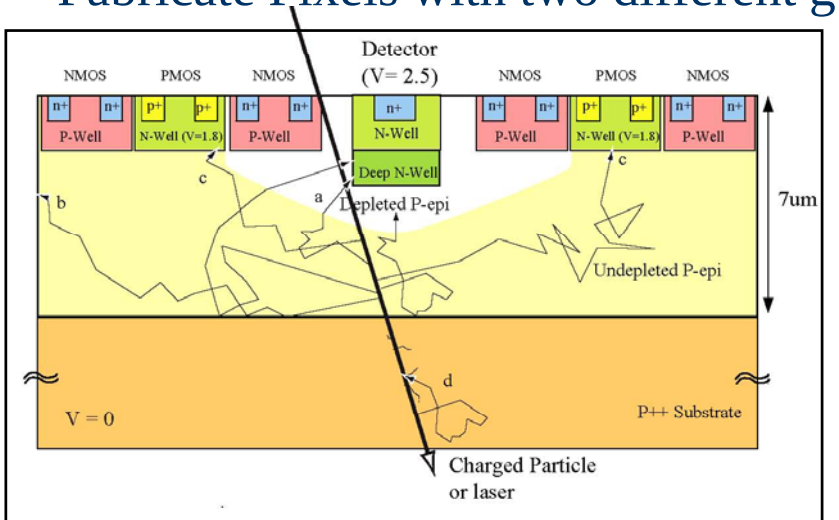


- Epi-layer resistivity and the deep p-well limit foundry choices

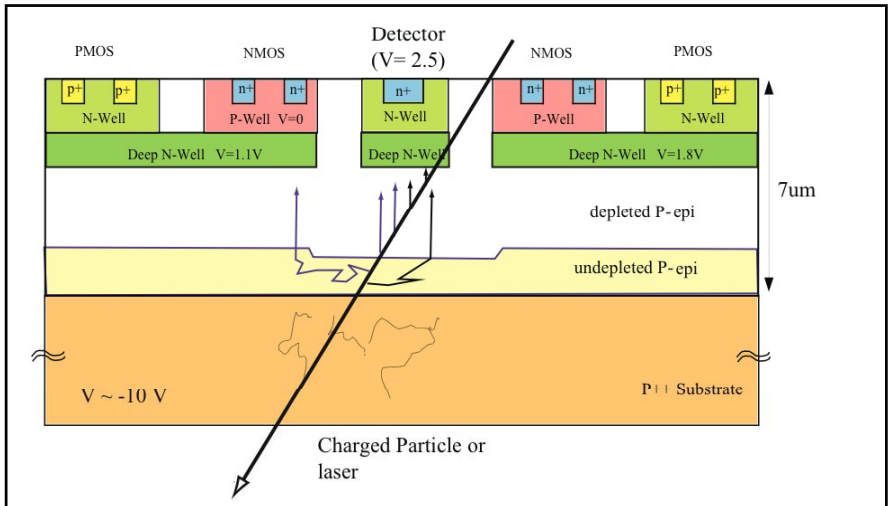
- Most cost effective procedure:
  - Prototype pixel circuit in TSMC 180nm process
    - High yield well characterized process
    - Lowest cost
    - Functionality of pixel circuit can be tested with IR laser and Fe55
    - Lack of deep p-well limits sensitive area of pixel to 5%
  - Model TSMC pixel and final pixel using 2D and 3D simulations
    - Model charge collection efficiency from MIPs as a function of position on the pixel for the deep p-well pixel
    - Model charge collection efficiency of TSMC pixels for Fe55 to establish sensitivity

Two Geometries

Fabricate Pixels with two different geometries to allow for model tests:



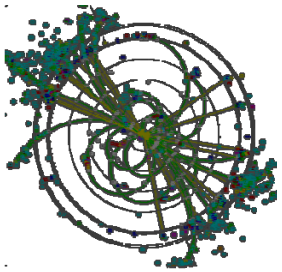
Pixel A – Most charges collected via diffusion



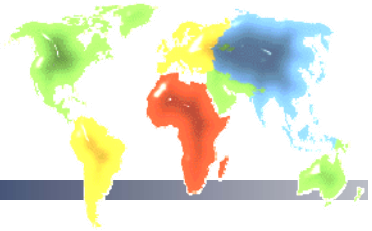
Pixel B – enhanced charge collection due to larger depletion region

The two different configurations will check models of charge collection and verify that the electronics meets the specification.

Simulating charge collection for each geometry



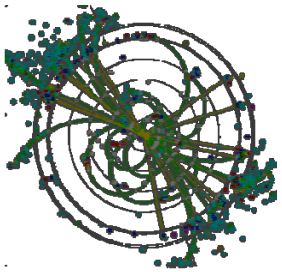
Noise



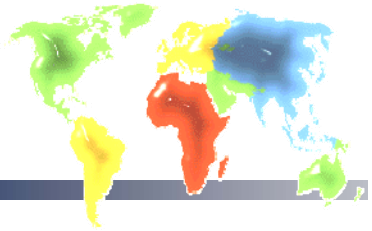
- Almost all noise sources depend critically on pixel capacitance.
- We expect total input capacitance to be about 16 fF.
- Simplest electronics would be reset noise limited:

$$ENC_{reset} = sqrt(kT\ C_{tot}) / e \sim 50 \text{ electrons}$$

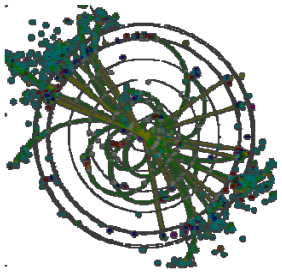
- To beat the reset noise a specially shaped “soft-reset” with feedback is used (reduces by a factor of 2)
- Other sources of noise should be smaller



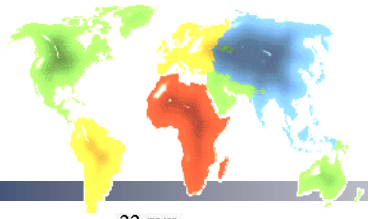
Power



- Sarnoff estimates analog power will be ~ 40 μW × f/channel
  or 16mW/cm^2 for f = 1/100 and 50μm × 50μm pixels.
  This amounts to ~ 0.4 W/ladder. Peak current is ~ 16 A.
  (Including reset noise suppression has not increased power)
- Assuming input FET and pixels capacitance scale by the same factor,
  the fundamental limit on current and power naively scales as
  $C^4_{tot} = w^8$, where w is the pixel width and power/ unit area
  scales as w^6!
- Actual power per channel will decline more slowly
- Speed of digital electronics not critical. Can run at very low voltage (e.g. 1 Volt or less for digital).
- Expect power/area will at least stay constant as pixel
  and feature size are reduced.



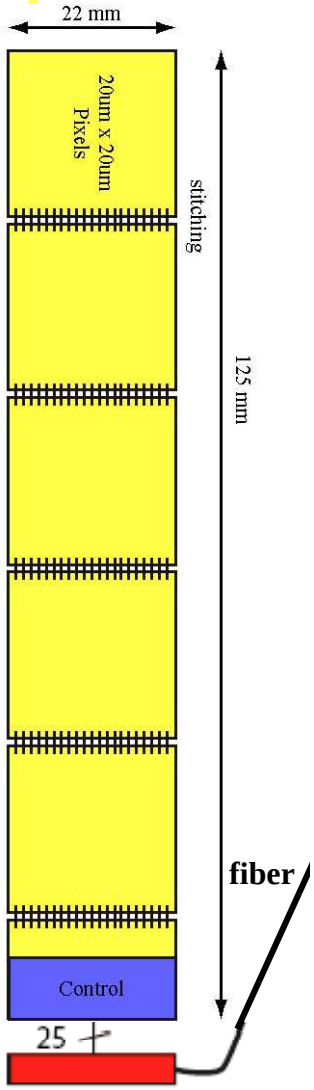
Data Rates

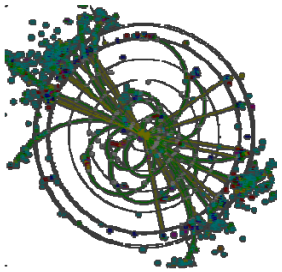


- At baseline occupancy, we expect 250k hitsclusters/ ladder/train, 1.25 M hit-clusters/ladder/sec
- Readout of chip at 50MHz gives factor of 40 safety margin for multiple hits and increased occupancy
- Possible data structure (10μm pixels)

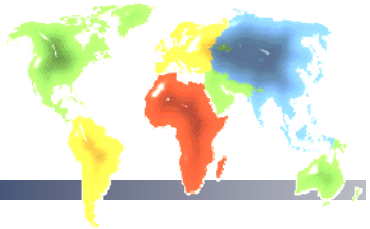
Row & Ladder (25bits)	
Column (12 bits)	Bunch No. (13 bits)
. . .	
Column (12 bits)	Bunch No. (13 bits)
End of Row (25bits)	

- Readout 25 bits in parallel, serialize on optical fiber, 1.25Gbits/s





Plans



Last summer-

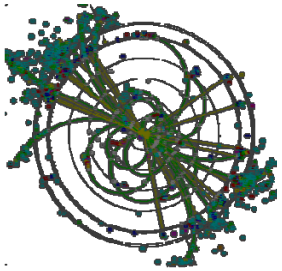
- **Analog design - completed**
- **Digital design of in-pixel circuit - completed**
- **Digital design of readout - completed**

Near term plans as of last summer

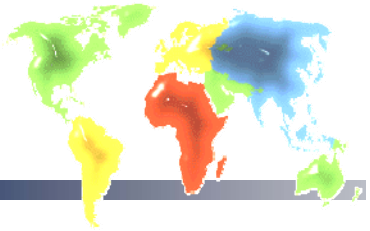
- **Explore alternative pixel designs - now completed**
- **Finish analog design and detailed pixel simulation - now completed**
- **Layout circuit - now completed**

Medium term plan (2007-2008)

- **Fabricate 5mm × 5mm prototype with 50 μm × 50 μm pixels in 180nm CMOS (started)**
- **Fabricate readout board (SLAC)**
- **Test with laser in lab**
- **Test with sources in lab**
- **Simulated charge collection efficiency of TSMC prototype and ultimate device - in progress**



Chronopixel Summary



- Chronopixel approach allows for low occupancy
  in an ILC vertex detector with time stamping by bunch

- Prototype design in 180 nm CMOS allows for test with
  $50\mu m \times 50\mu m$ pixels

- Expect to reach $20\mu m \times 20\mu m$ pixels or better in 45 nm CMOS

- No fundamental barrier to operation at reasonable power
  - can use thicker oxide for crucial analog transistors
  - High speed operation of SRAM memory not needed