Silicon Pixel Tracker for the ILC

(with some thoughts for the forward region)

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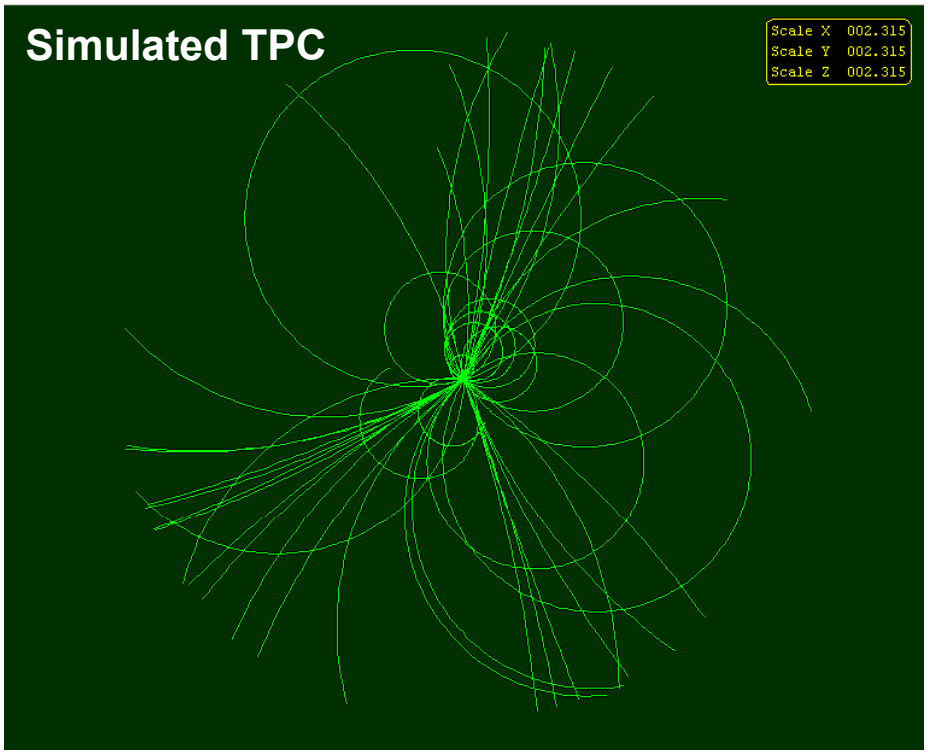
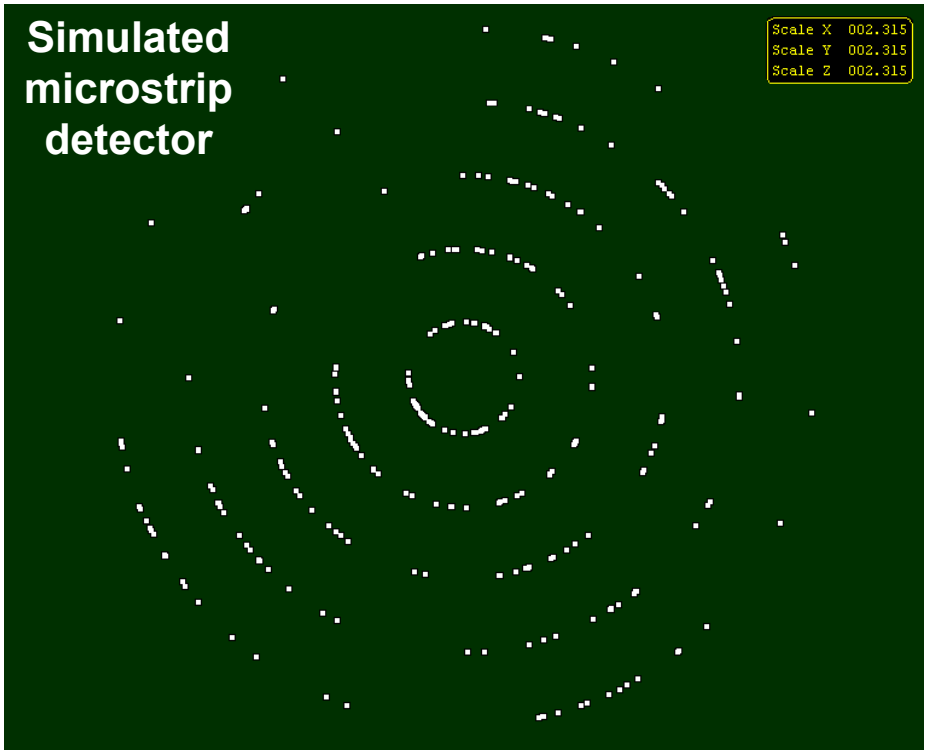
- Introduction
- Considerations for Pixel Tracker at the ILC
  - Parameters
  - CCD-based SPT
  - MAPS-based SPT
- Conclusions

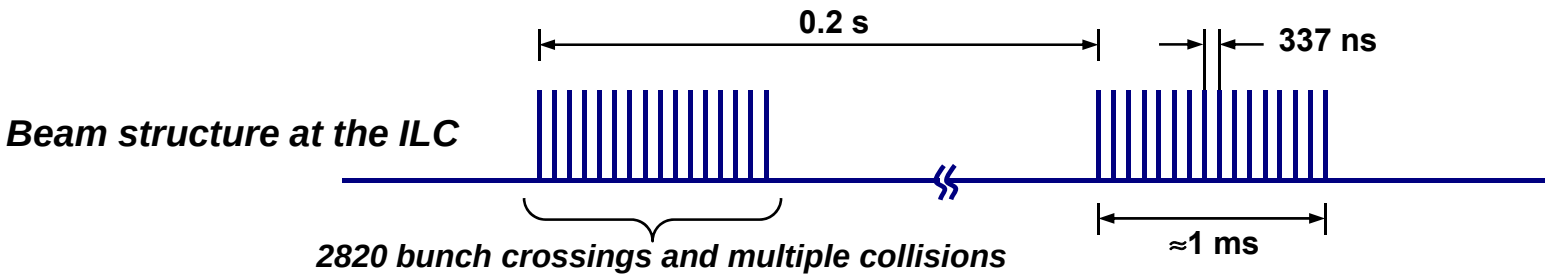
The Tracker at ILD/SiD





- Time Projection Chamber (TPC), in ILD
  - ❖ Measures many rφ coordinates along a track
  - ❖ Point resolution in rφ ≈ 100 μm, resolution in *z* ≈ 0.5 mm
- 5 layers of Si microstrip sensors, 25 μm pitch / 50 μm readout (in SiD)
  - ❖ Measures 5 rφ coordinates
  - ❖ Resolution rφ ≈ 5 μm, resolution in *z* ≈ 5 mm (with charge division)

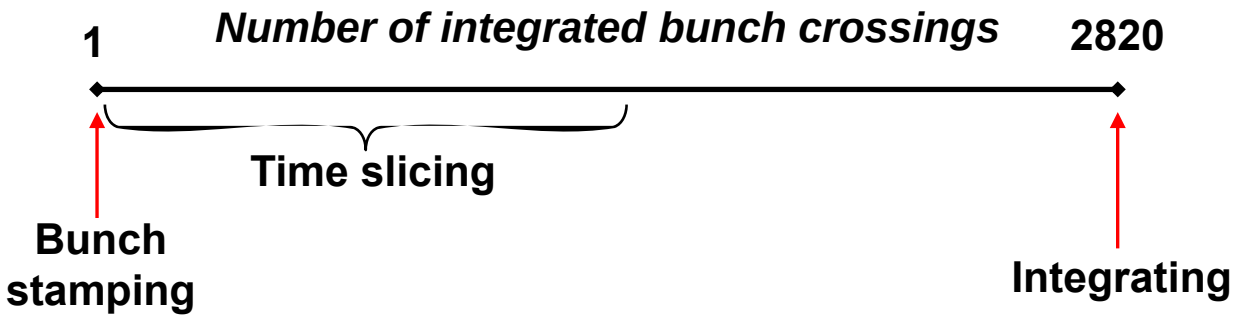
Beam Structure at the ILC and Implications for the Tracker



Considering the barrel:

- **Physics event rate is tiny: 1.5 hits/BX over all of layer 1 (20 cm radius)**
- **Background is photons:**
  - **Converted on 300 μm Si gives 0.002 hits/cm^2.BX, or 6 hits/cm^2 for the train (in the barrel)**
  - **On 100 μm thick Si this is 2 hits/cm^2 for the train**
- **With 50 μm × 50 μm pixels (point resolution ≈14 μm) the occupancy in L1 would be only 0.005% for the whole bunch train!**

Integrating, Time Slicing, Bunch Stamping Options



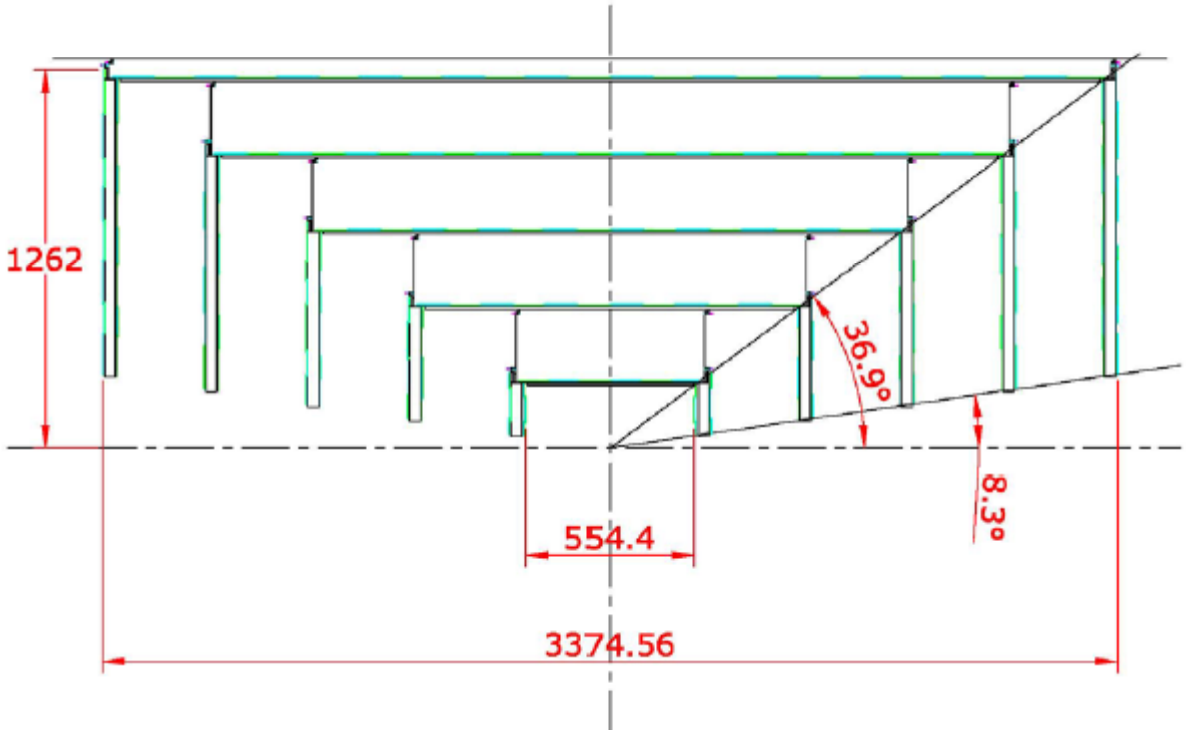
In the barrel:

- It could be possible to integrate all events (and the background) and read in the inter-train gap
- We have to prove that the pattern recognition does not deteriorate
  - Additionally, the detector becomes highly tolerant to beam-induced EMI

In the very forward region:

- Time slicing or bunch stamping could be necessary due to higher backgrounds (e.g. 2-photon processes), needs good knowledge of the backgrounds and more studies

Pixel Tracker Based on the SiD Design



- Barrel and Forward trackers, total area = 70.3 m^2
- With 50 μm × 50 μm pixels – 28.1 Gpix system
- Low mass support, gas cooling
- If each chip is 8 cm × 8 cm (2.6 Mpix): 11,000 sensors is total
- Readout and sparsification scheme to be developed

“Luppino Plot” – Evolution of Focal Plane Sizes for Astronomy with Time

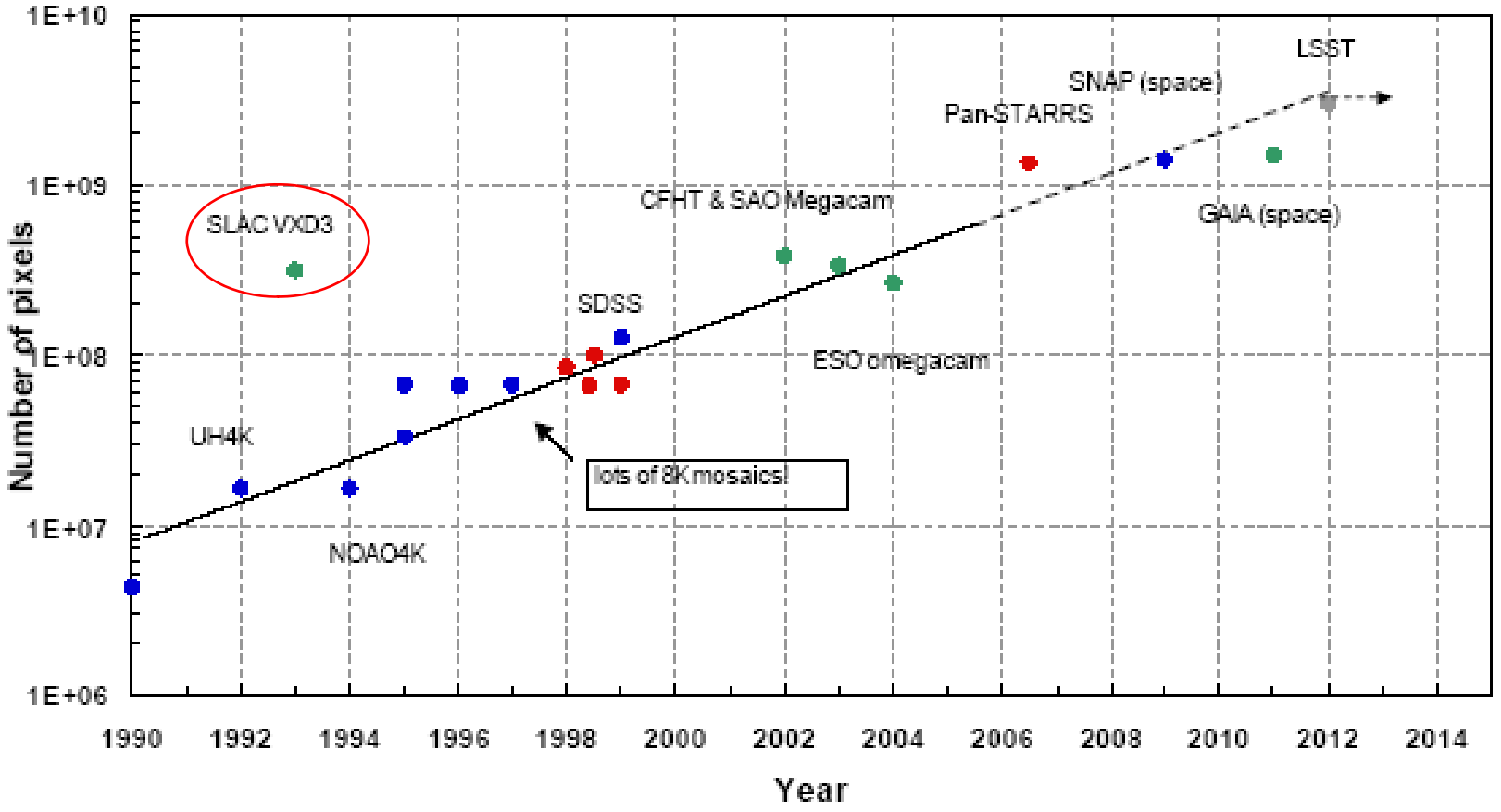


Illustration of focal plane sizes, from Luppino/Burke ‘Moores’ law

Focal plane size doubles every 2.5 years

From: Burke, Jorden, Vu, SDW Taormina 2005

General Considerations for the SPT

- The main challenge is to reduce material and therefore power
- Sensors ≈100 μm thick, low mass support (<1% X_0 per layer in the SiD design)
- Gas cooled, power dissipation ~*O*(100 W), in SiD < 500 W
- Pixel size around 50 μm × 50 μm (point resolution ≈14 μm in binary mode)

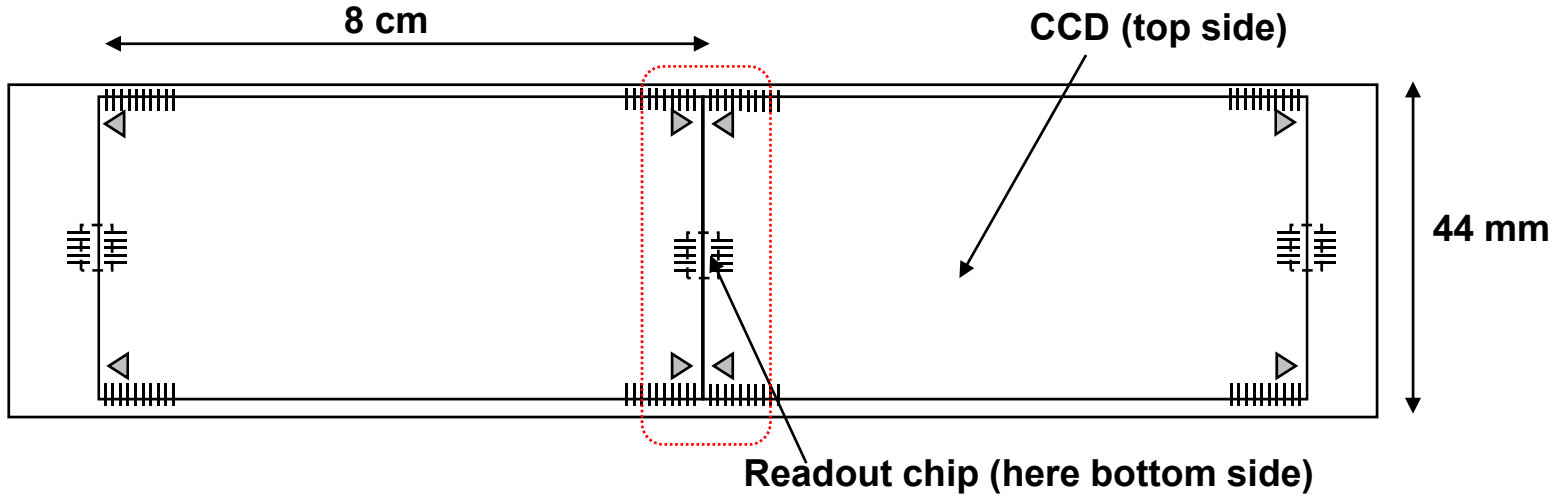
- Bunch stamping/time slicing tracker:
  - ❖ Implies on-pixel intelligence and therefore more power
  - ❖ Binary readout and sparsification most likely, but measurement of charge centroid is not excluded
- Integrating:
  - ❖ Lowest power (due to slow readout) and low mass
  - ❖ Full pixel readout to local readout chip
  - ❖ Resolution likely to improve below 14 μm due to the use of charge centroid
  - ❖ Preferred if track reconstruction is fully efficient
    - ❖ Out-of-time tracks rejected using the ECAL

<u>We have considered two technology solutions:</u>

- Charge Coupled Devices
- Monolithic Active Pixel Sensors

CCD-based Pixel Tracker

- **CCD-based SPT could be an excellent solution**
- **Each CCD is read out from 4 outputs (1 or 2 outputs also possible)**
  - **Here 8 cm × 4 cm CCDs, other sizes (smaller/larger) possible up to 8 cm × 8 cm, with yield and cost implications**
  - **Alternating mounting on top/bottom sides also possible**
- **Readout chip serving 2 adjacent CCDs on the same or other side of the support**
- **All chips thinned to ≈100 μm and glued to the support**
  - **Kapton tape providing all power, clocks and signals;**
- **Material budget:**
  - **0.1% X_0 for CCDs (100 μm thick)**
  - **0.2% X_0 for kapton *(rough estimate)***
  - **0.45% X_0 for mechanical support, e.g. 5 mm-thick SiC ladders (mechanically linked to form a barrel)**



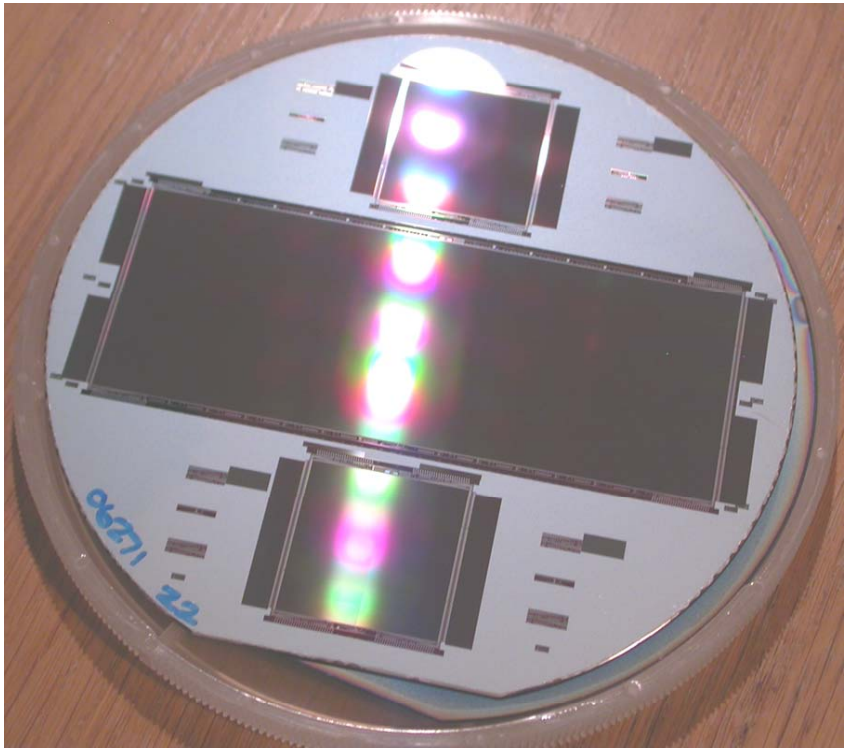
CCD-based Pixel Tracker

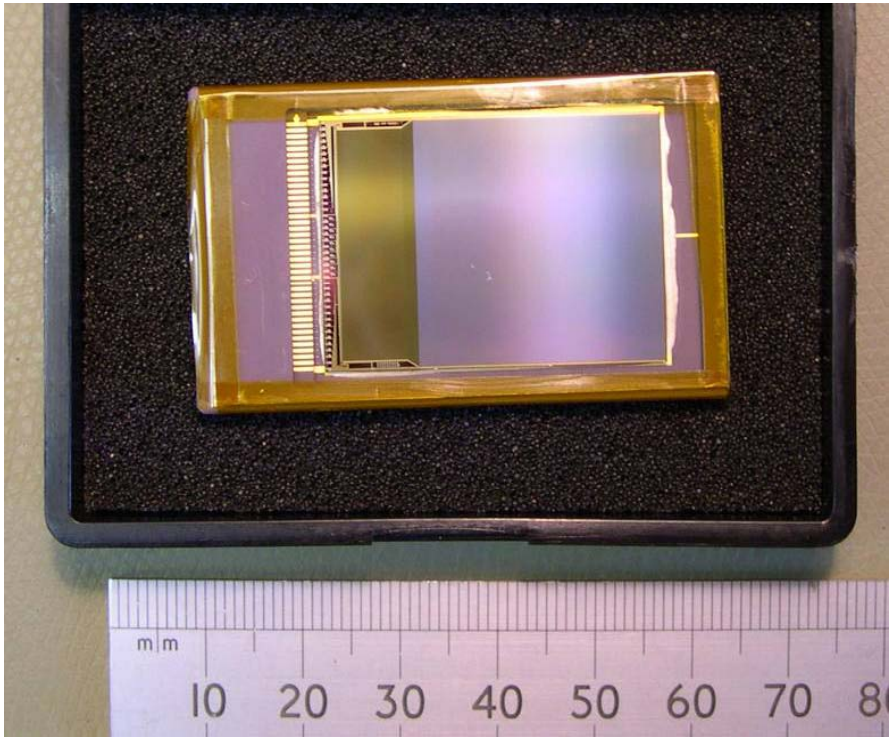
Excellent detection properties:

- 100% fill factor
- Epitaxial layer between 20 μm and 50 μm (signal between 1600-4000e-)
- Well capacity > 10ke-
- Full depletion possible
- Noise below 50 e- @ 10 MHz, S/N > 30
- Efficient charge transfer for small signals despite the large pixel size

- 70 m^2 tracker with 50×50 μm^2 pixels, 28 Gpixel system
- Total power dissipation ≈ 600 W (0.86 mW/cm^2)
- Will need *O*(10,000) 6-inch wafers – within the capabilities of at least one vendor
  - Cost around *O*($10M), strongly depending on size, cost of testing…
  - The technology is available with little R&D
    - CCD with 40 μm × 40 μm pixels for X-ray astronomy has been made in the past
    - We got some samples
  - Possible manufacturers:
    - e2V Technologies (UK)
    - DALSA (Canada)
    - Hamamatsu Photonics (Japan)

Large Existing CCDs





- Wafer scale CCD from e2V
- 6-inch wafers

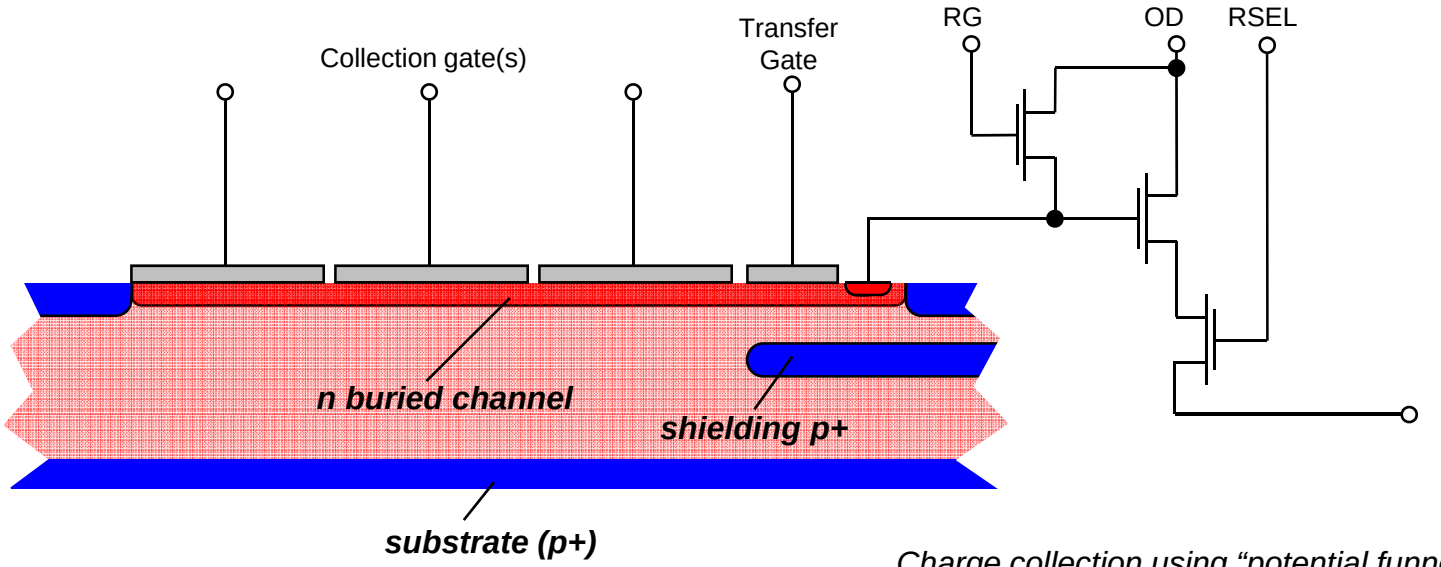
- 40 µm pixel CCDs using advanced charge collection and transport
- Noise = 5e- at 1 MHz
- We have few chips in our hands
- Will be interesting to put in a beam and test

Solution with Monolithic Active Pixel Sensors (MAPS)

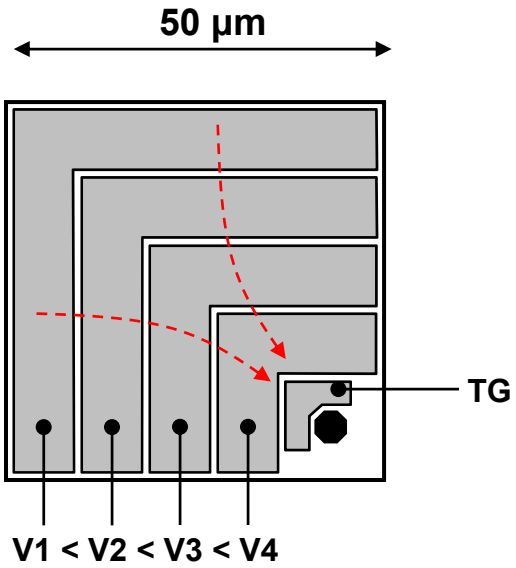
- MAPS can do all 3 readout schemes:
  - Integrating
  - Time slicing
  - Bunch stamping (relevant experience with CALICE ASIC1)
- Integrating tracker
  - Functionally the same as the CCD option
  - Lowest power by elimination of high gain amplifiers, comparators and logic
  - However:
    - Large pixels are not easy to make – small collection area and significant charge sharing are common
    - Single sense node for high sensitivity and low noise is preferable
    - Correlated double sampling on short timescale for effective noise suppression is mandatory
    - Devices are unlikely to be as large as the CCDs due to lower yield

Pixel Designs for Integrating Tracker – Some Ideas

Photogate transfer with Buried Channel CCD storage



Charge collection using "potential funnel", inspired by Grzegorz Deptuch (Fermilab)



- **Charge transfer allows correlated double sampling and low noise (10 e- possible)**
- **LCFI is developing the underpinning technology for the ISIS2**
- **Charge transfer is fast due to the funnel action**
- **Possible problems with inefficient transfer due inter-gate gaps**
- **Buried channel pinned photodiode designs are is available, but only for small pixels**

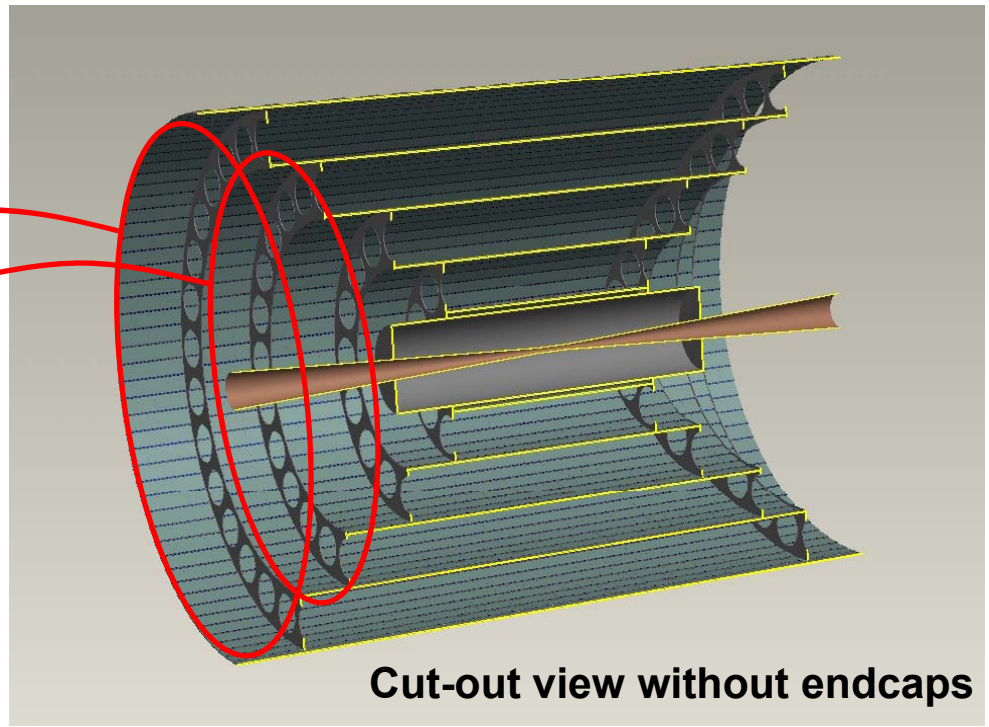
Bunch Stamping Tracker with MAPS

First experience with the CALICE ASIC1 for MAPS-based ECAL (designed at RAL)

- Functionally very close to bunch stamping tracker
- 50 μm × 50 μm pixels on 0.18 μm CMOS process
- 4-diode readout with preamplifier
- Targets S/N > 10, preliminary S/N = 6.5 (worst case), noise = 27e- ENC
- Time stamping at ≥150 ns intervals
- On-chip data storage of up to 3 hits/pixel with 13-bit timestamp
- Binary readout
- ≈10% dead area in strips due to the space needed for data storage

- Presently the power is 7.2 mW/cm^2, including 1% duty factor (i.e. the analogue sections are *ON* for 1% of the time, applicable to the SPT as well)
- SPT with CALICE-like sensors could use 5 kW – can this be air cooled?
- Time stamping implies analogue amplification and discrimination during the bunch train, with peak power ~100 times the average – how is the material budget affected by this?

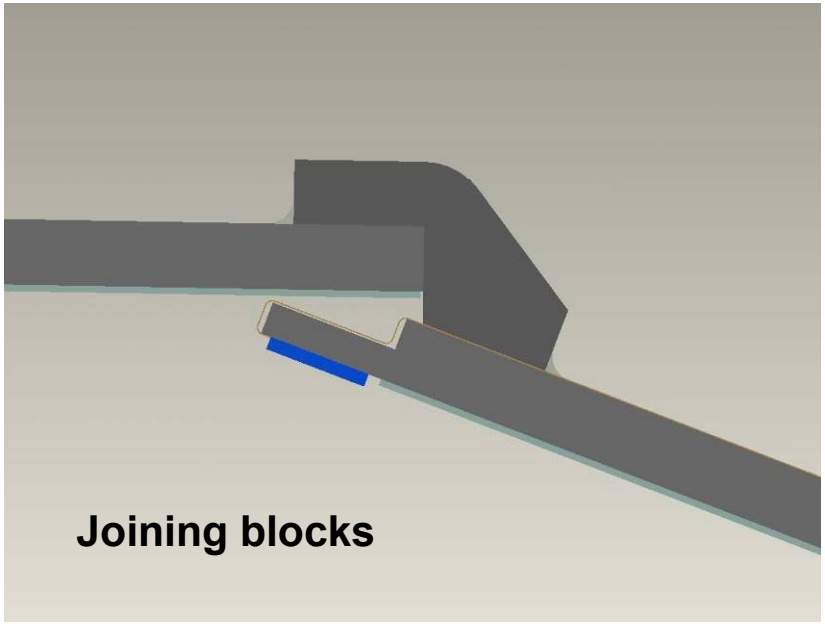
Some Thoughts about the Forward Tracking

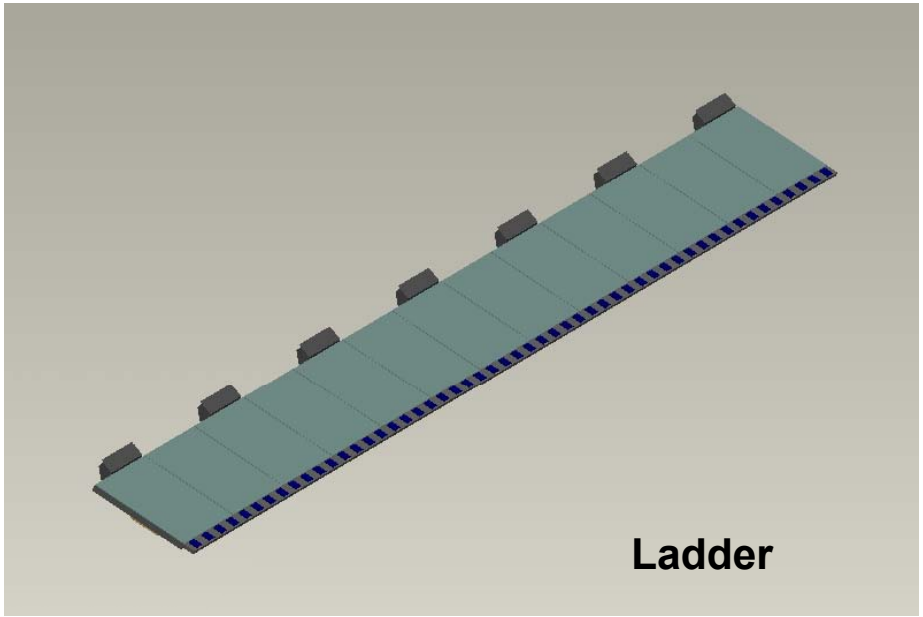


- Mass of cables, connectors and cooling adds up heavily in the forward region
- Pulsed power (microstrips; time slicing or bunch stamping MAPS)
  - ❖ Local energy storage (i.e. mass)
  - ❖ Cables rated for the peak power (i.e. mass again)
- Continuous LOW power (integrating MAPS or CCDs)
  - Thin cables and no energy storage – lowest mass possible
  - Just one cable per layer? Would be great!

Mechanics

- Geometry has been "borrowed" from the SiD design, but we have some new ideas:
  - Long ladders made entirely from 8% SiC foam (5 mm thick = 0.45% X_0)
  - Self-supporting barrel with SiC joining blocks, glued for low mass
  - Additional rings (CF of SiC) and the endcaps keep it stable
  - This is one of many possible implementations…





Conclusions

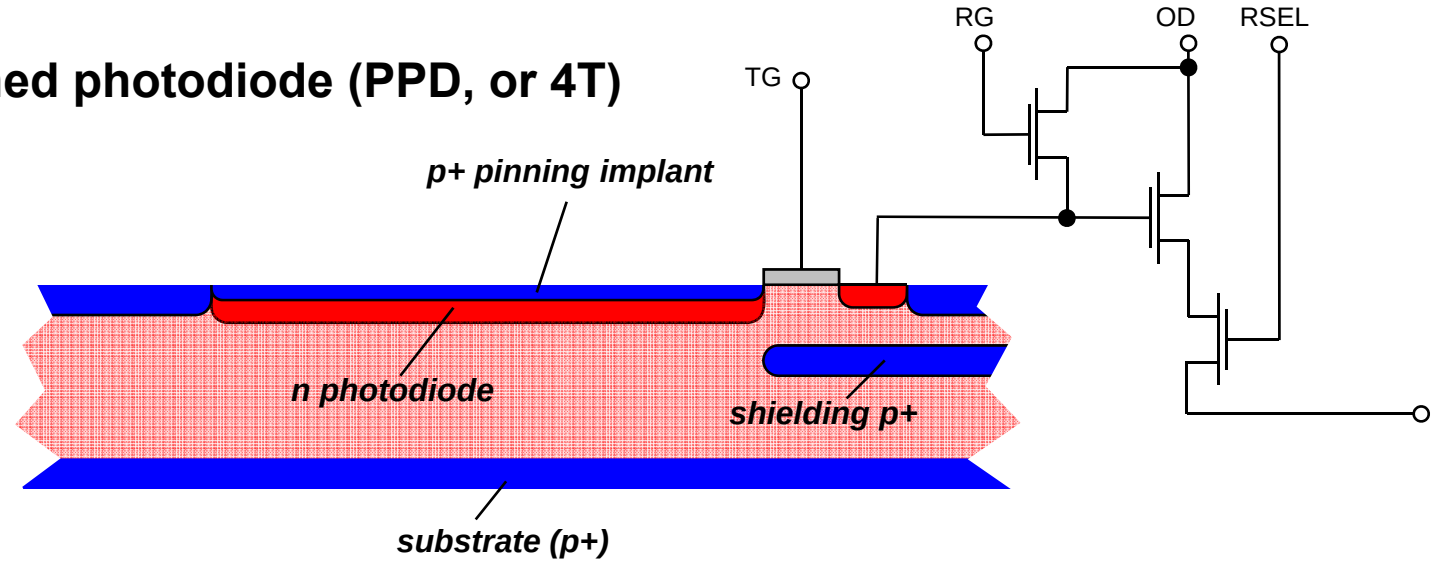
- Silicon Pixel Tracker for the ILC is very attractive and technologically possible
- Integrating tracker is the first option:
  - Benign backgrounds should allow it
  - CCD-based detector is possible now, with little R&D
  - MAPS-based tracker should be possible in the near future, after some R&D
  - Power requirements, mechanics and cost are comparable to the SiD microstrip design
- Bunch stamping or time slicing tracker could also be considered:
  - Power could be much higher
  - Only MAPS-based solution
  - Could be the only option for the forward disks – will need good knowledge of backgrounds
- Pattern recognition with integrating tracker
  - We encourage people with interest and time (LCFI has only the former!) to simulate the pattern recognition in the integrating tracker
  - Time slicing or bunch stamping should be considered if needed to improve the pattern recognition performance

Many thanks to Mike Tyndel, Peter Pool, Andy Lintern and Chris Damerell for their help

Thank you

Pixel Designs for Integrating Tracker (1)

Pinned photodiode (PPD, or 4T)

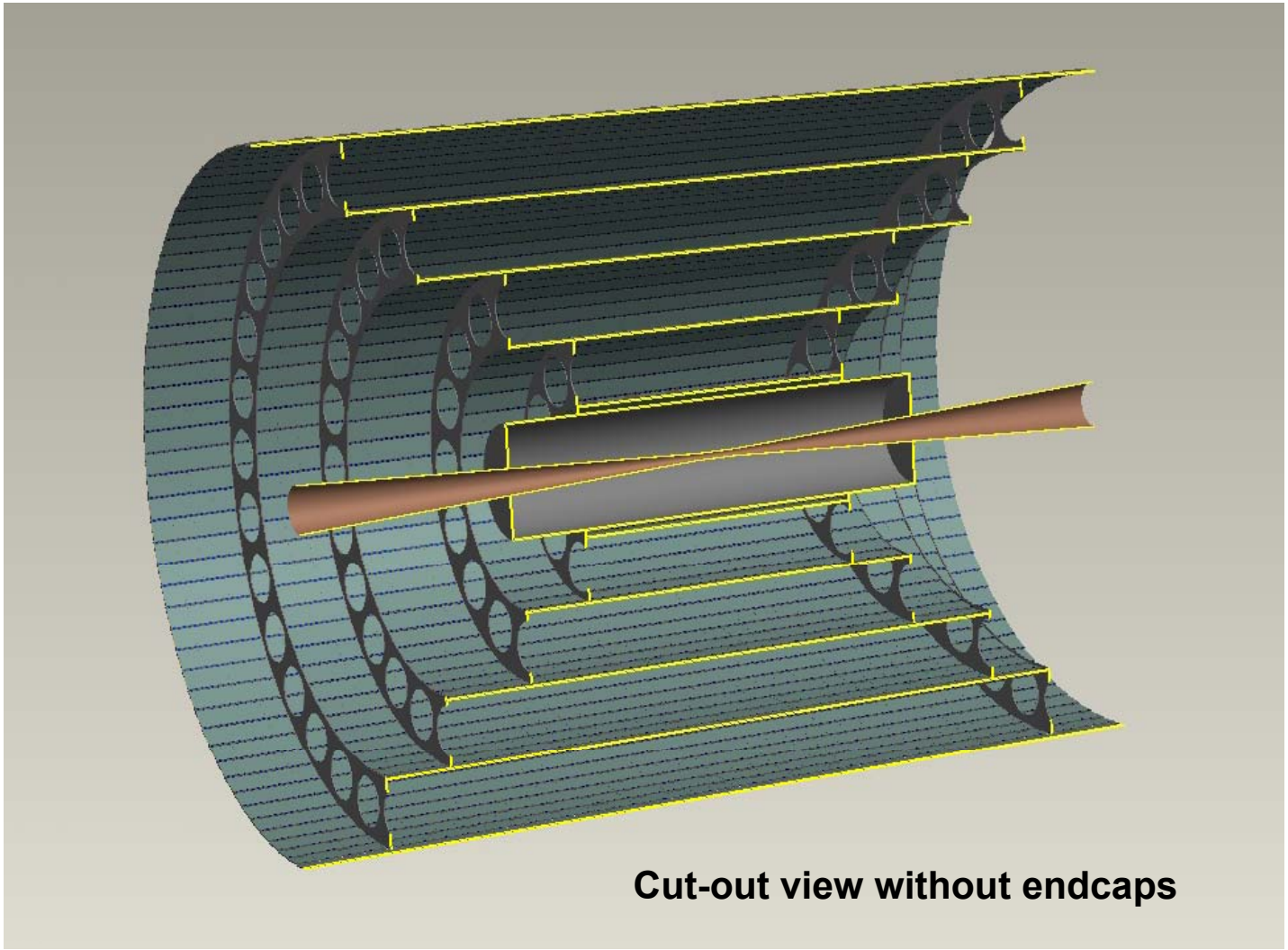


- PPD IP offered by numerous foundries for imaging
- Pinning implant to reduce dark current
- Charge transfer allows correlated double sampling and low noise (10 e- ENC quoted)
- Large area PPD pixels will have to be developed
- Charge transfer is slow (~100 ns)
- Possible problems with inefficient transfer due to small potential fluctuations in the photodiode area
- Dynamic range is small, but should not be a problem

CCD-based Pixel Tracker : Power

- Full pixel readout in the inter-train gaps
- CCD details:
  - Readout time ≈ 180 ms (at 6 MHz serial rate if one output per 1 Mpix)
  - 3-phase image area, capacitance = 30 nF/phase
  - 2-phase serial register, capacitance = 40 pF/phase
  - Will use the knowledge within LCFI on low power CCD operation
- Power dissipation (approximate):
  - 130 W for parallel clocking (@ 3 V clocks)
  - 120 W for serial clocks (@ 3 V clocks)
  - Source follower power ≈ 210 W
  - Readout chip power ≈ 140 W
  - Total = 600 W (0.86 mW/cm^2)

Mechanics (2)



Cut-out view without endcaps

Mechanics (3)