Readout ASIC for Pair Monitor

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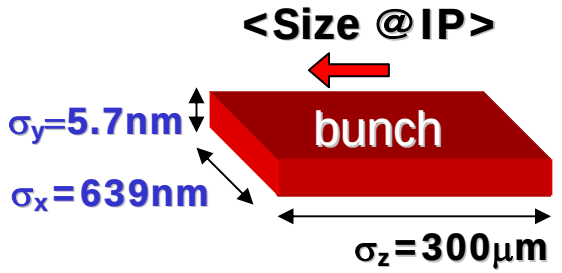
- Development of readout ASIC
- Test for shift register
- Test for amplifier

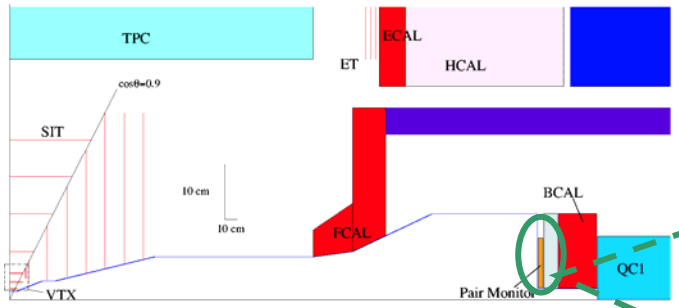
Pair Monitor

Beam Profile Monitor : Using information of pair background

- Position : 400cm from IP
- Accuracy of Beam Profile : ~nm at IP

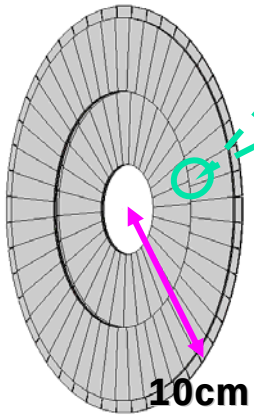


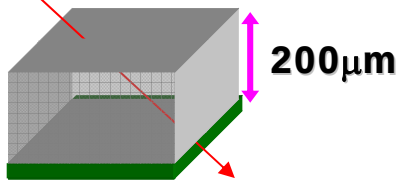
(Position of Pair Monitor @ GLD)



IP 400cm

(Pair Monitor)



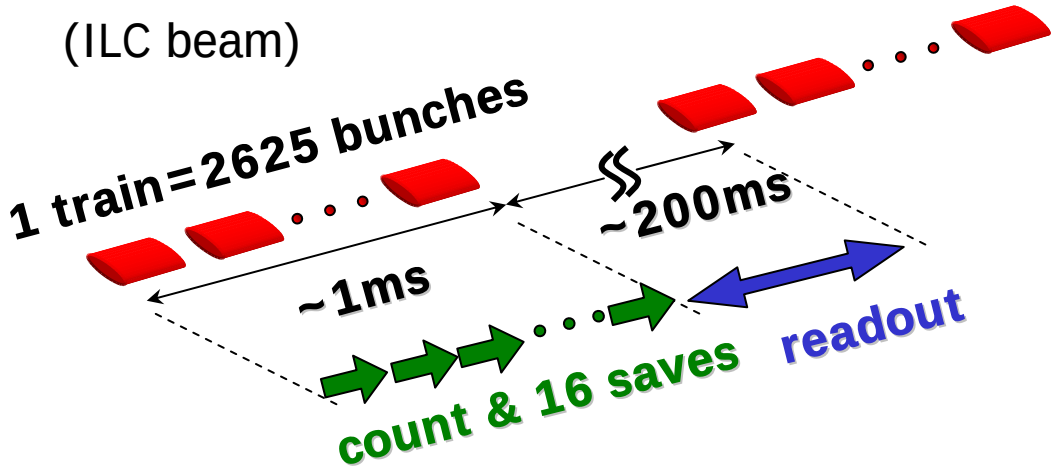


Development of readout ASIC

Performance requirement for readout chip

- Hit distribution of pair background } 2-dimentional pixel
- Hit count depending on time
- Less than 10% accuracy of measurement } Count & save every 1/16 train
- Completion of readout by the time the next beam train comes } Readout for 200ms
- Radiation tolerance : 2 Mrad / year

(ILC beam)

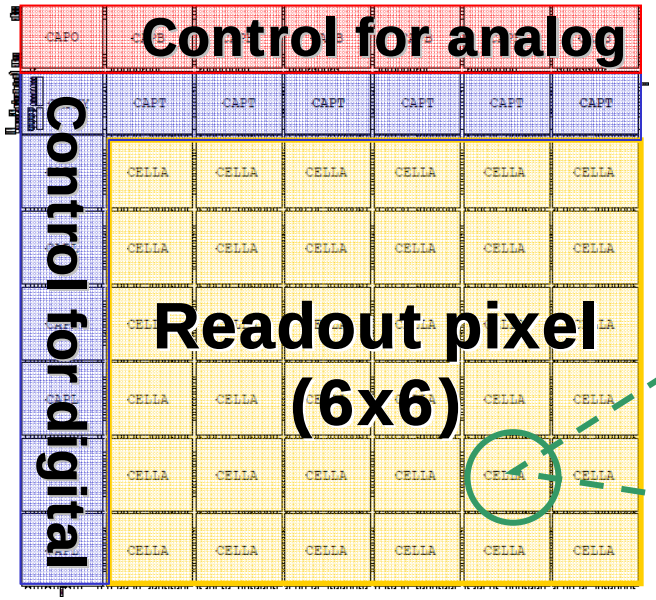


We designed the chip based on them.

Design for readout chip

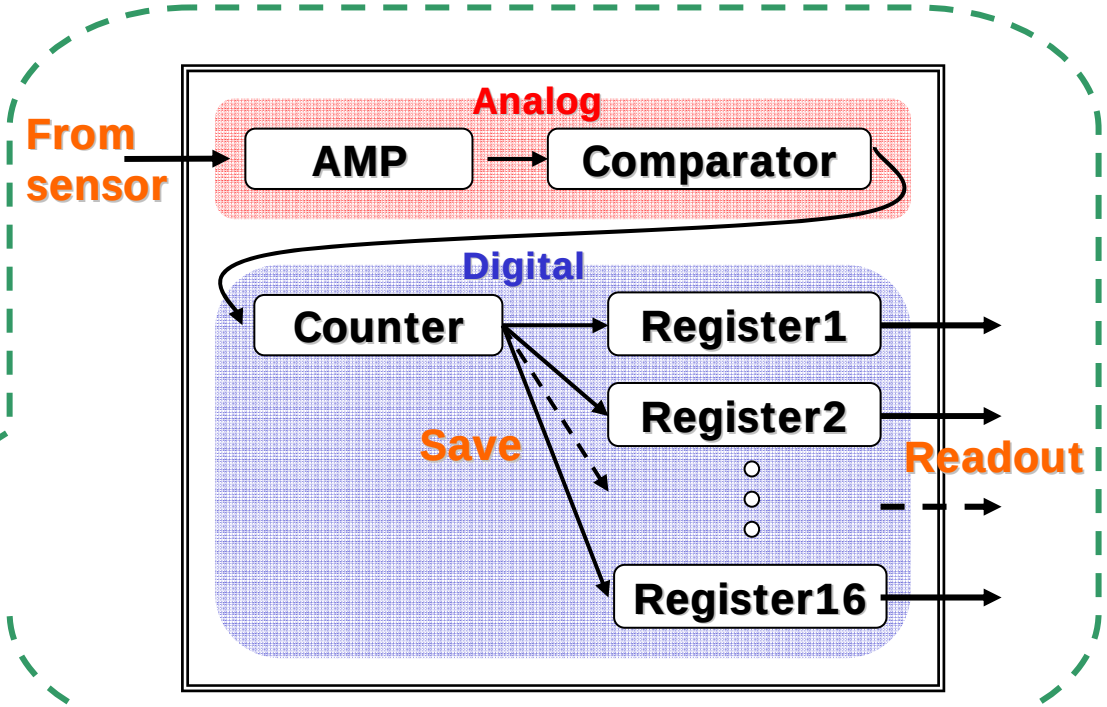
<Overall structure>

- ASIC with analog & digital
- Readout pixel : 6x6=36



<Readout pixel>

- Register : 16

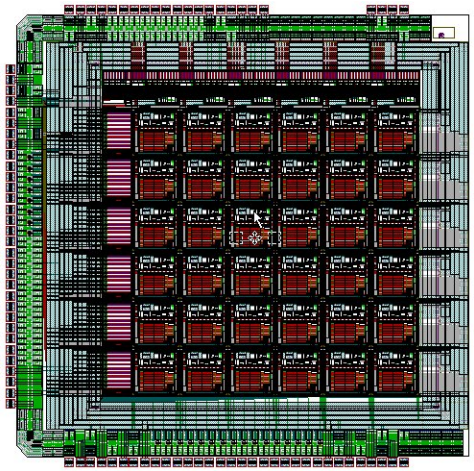


We produced the chip based on them.

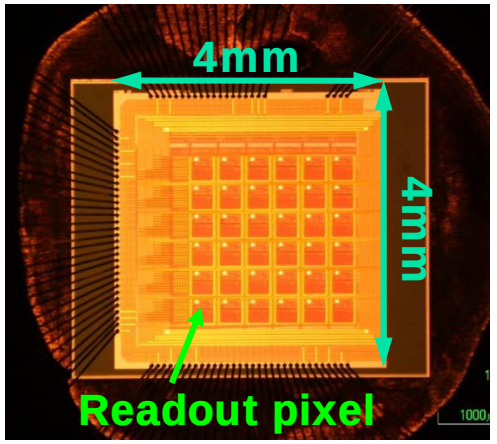
Prototype of readout chip

- Produced by MOSIS
- CMOS 0.25 μm process by TSMC
- Size of chip：4x4 mm^2
- Size of readout pixel：400x400 μm^2

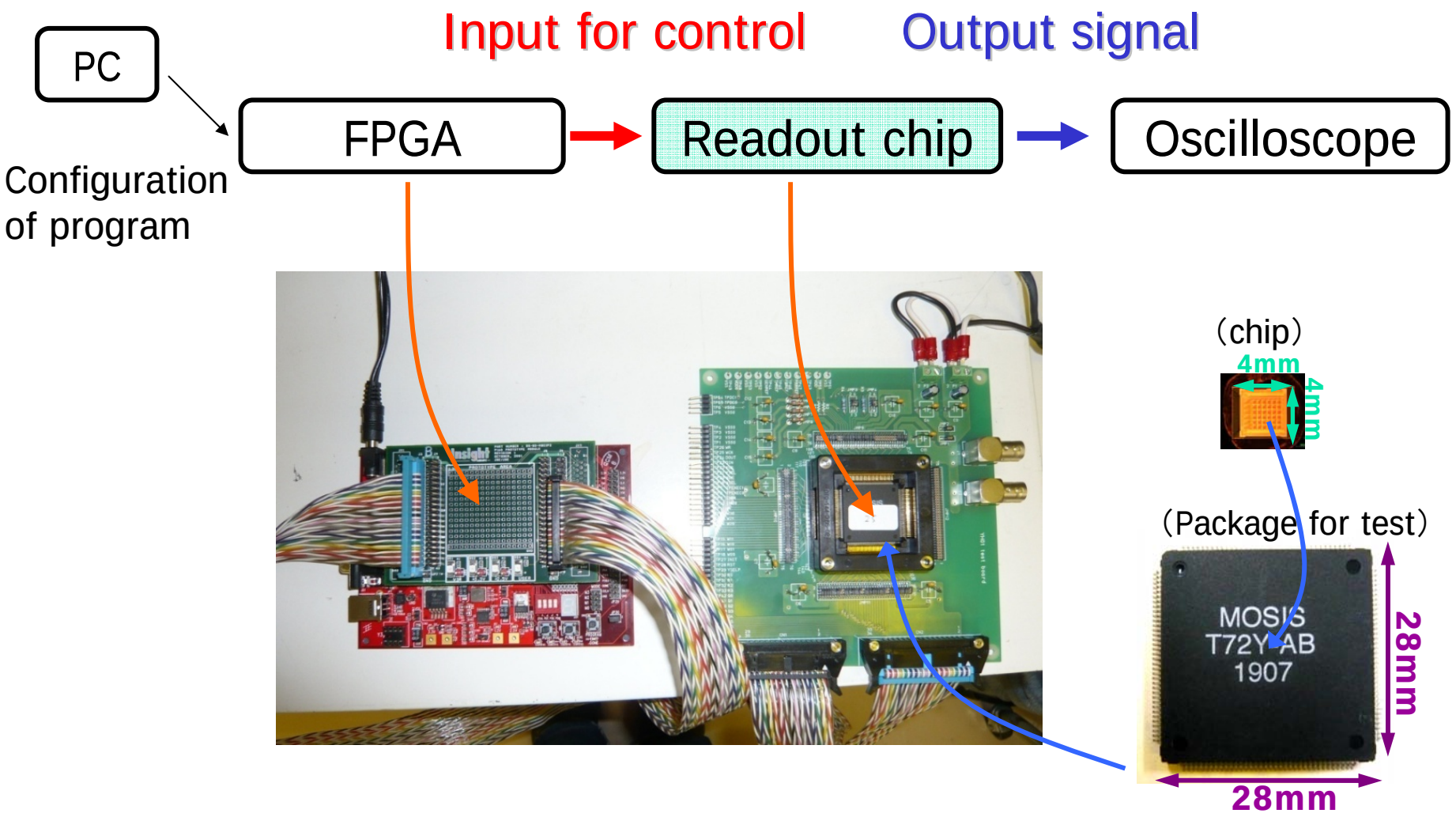
(Design of chip)



(Picture of chip)



Setup for test

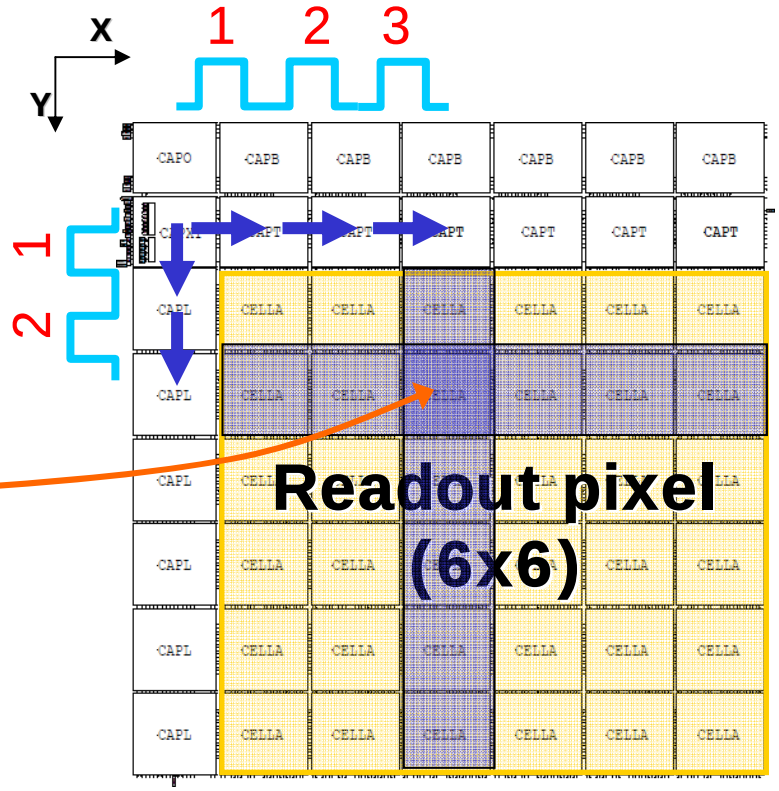


Shift register

For example…

When we make { 3 X_shift_clock, 2 Y_shift_clock,

we can select (X,Y)=(3,2).

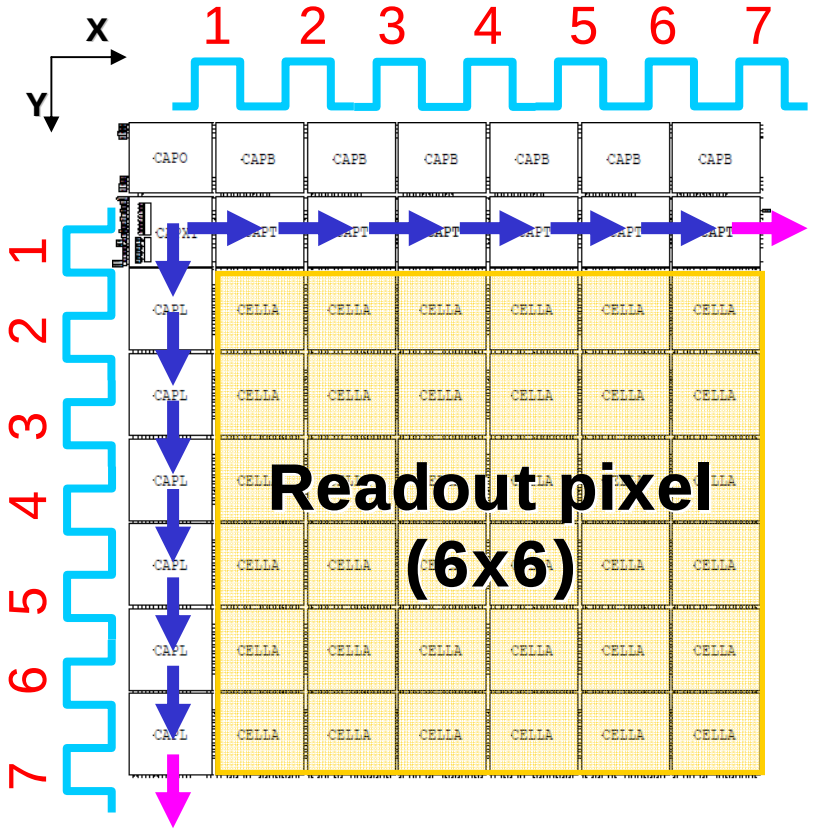


It is possible to select all readout pixels.

Test for shift register

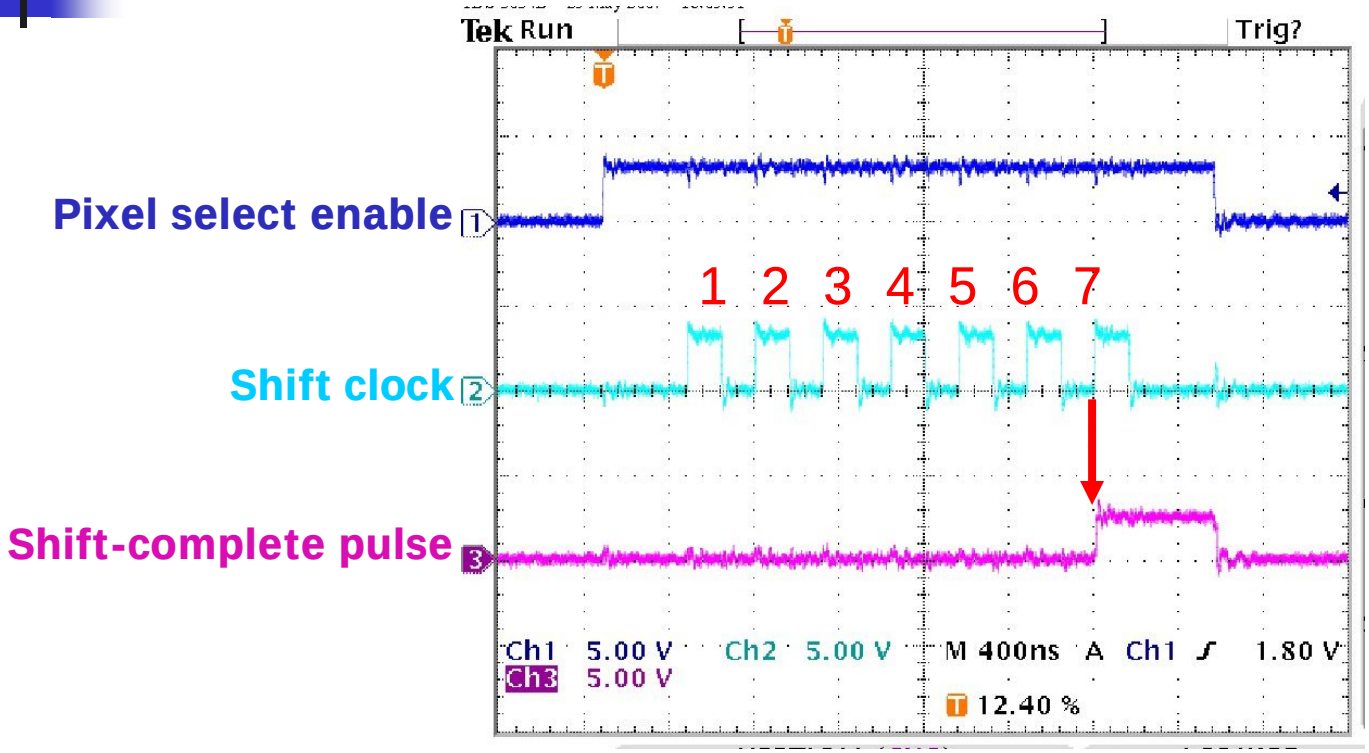
Select signal goes outside chip after the **7th** shift clock.

X (or Y) shift-complete pulse



Test for shift register by using X shift clock

Test result of shift register



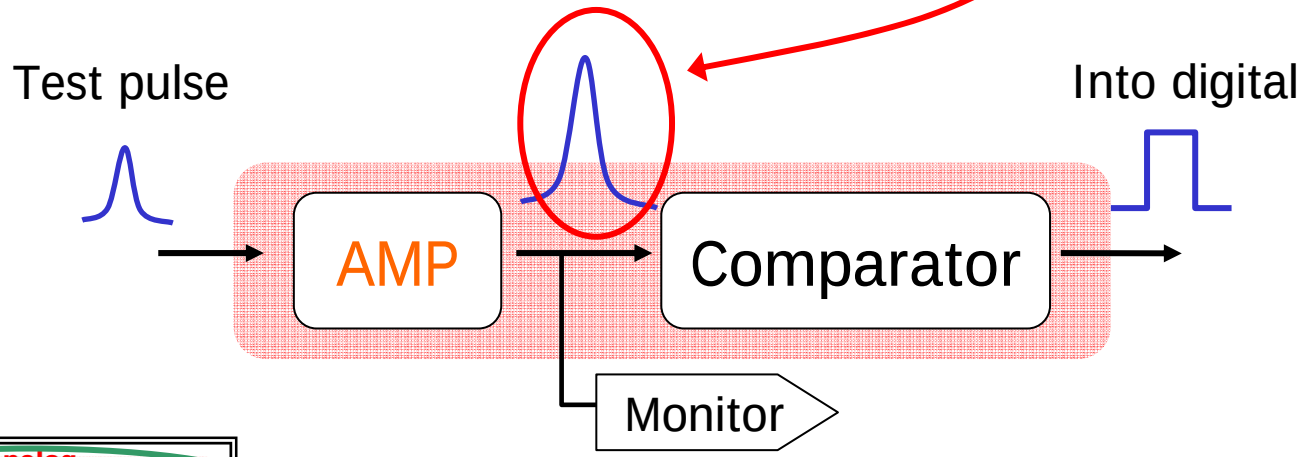
Shift-complete pulse is rising after the 7th shift clock.

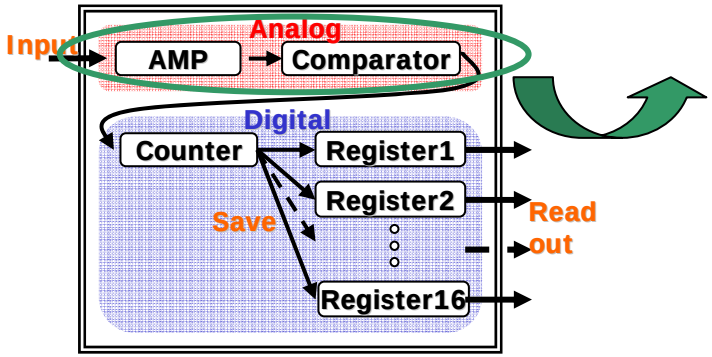
(same as Y direction)

Shift register is correctly working!

Test for amplifier

1. Input of test pulse
2. Amplification of test pulse (x 3.5) ← Monitor
3. Output of digital pulse



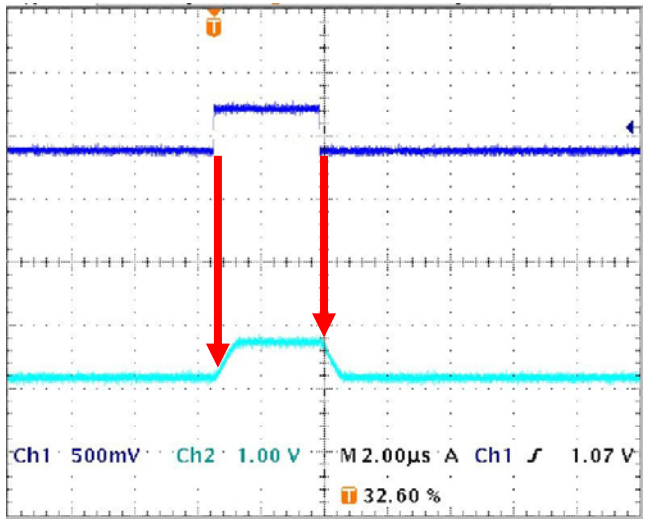


Test for AMP by monitoring

Test result of amplifier

Trigger of test pulse

Monitor



- Amplification starts at trigger's rising.
- Amplification finishes at trigger's falling.

- Voltage of input : 0.2V
- Voltage of output : 0.7V

× 3.5

Amplifier is correctly working!

Conclusion & plan

<Conclusion>

- We designed the chip based on the requirement.
- We made prototypes of readout chip.
- Shift register and amplifier are correctly working.

<Plan>

- Test for counter and register
- Test for radiation tolerance