A Brief Summary of the Talks in the Vertex/Tracker Parallel Sessions

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TILC08 at Sendai
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7 Talks on TPC

1. **(Update on) Silicon Pixel Readout for a TPC at NIKHEF / Jan TIMMERMANS (NIKHEF)**

2. **Performance study of a GEM-TPC prototype using cosmic-ray / Prof. Yulan LI/Tsinghua University**
3. **CF4 gas test for GEM-TPC / Ryo YONAMINE (GUAS)**

4. **The LCTPC Large Prototype at the DESY Test beam / Klaus DEHMELT (DESY FLC)**
5. **Status of Marlin-TPC / Klaus DEHMELT (DESY FLC)**

6. **Ions in the ILC-TPC / Vincent LEPELTIER (LAL-CNRS)**
7. **Electron transmission measurement of GEM gate / Hirotoshi Kuroiwa (Sag University)**

Silicon Pixel Readout for a TPC at NIKHEF

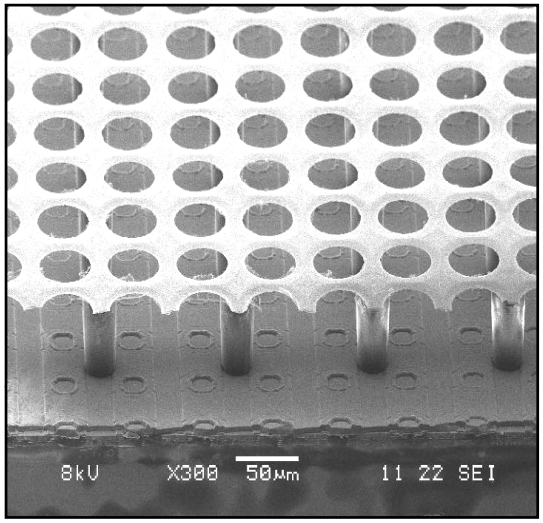
Idea: Use 'naked' CMOS pixel readout chip as anode of MPGD.

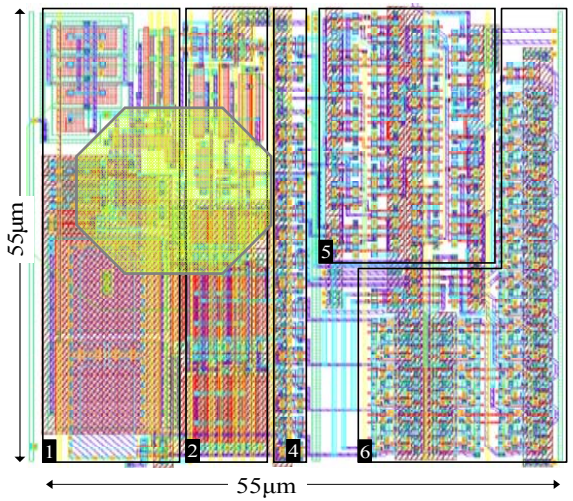
(1) Fabricated "Timepx" in 2006 (CERN): 256x256 pixels of 55x55μm2 with a preamp, a discriminator and a counter. The counter measures hit time in one of its three modes.

(2) It is most interesting (for me) to use it with MicroMEGAS because the chip measure position and arrival timing of each primary electron, thus function as a digital TPC.

(3) The digital TPC is very attractive because of it beautiful graphical capability. In the ILC TPC application, it has an potential advantage to avoid the gas gain fluctuation providing the possibility to improve the resolution of position measurement of charged track.

(4) With "ingrid" (the integrated grid: MicroMEGAS mesh), it became an integrated detector.





Silicon Pixel Readout for a TPC at NIKHEF

(5) To prevent discharge (in particular in Ar-based gases) to kill chip, the discharge protection of high-resistive (~1011) Ω·cm amorphous Si layer (20 μm thick) on top of CMOS chip was processed.

(6) With the protection, even the killers are captured!

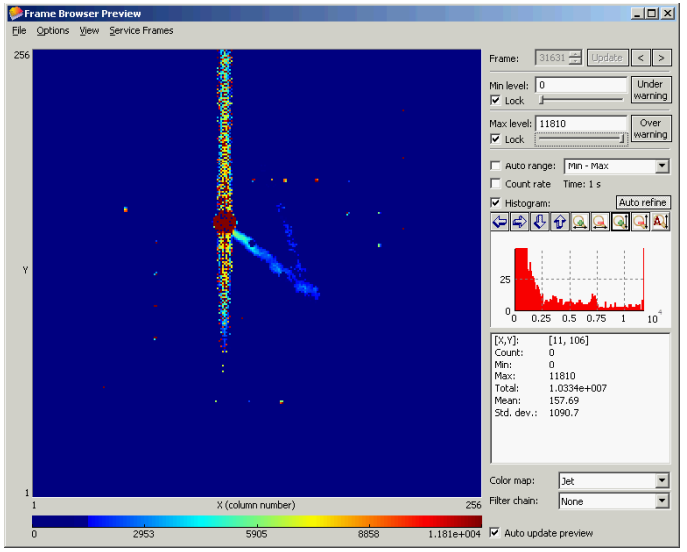
(7) A TPC with Timepix , though still very small, is working measuring the beautifully curing tracks from in a magnetic filed!

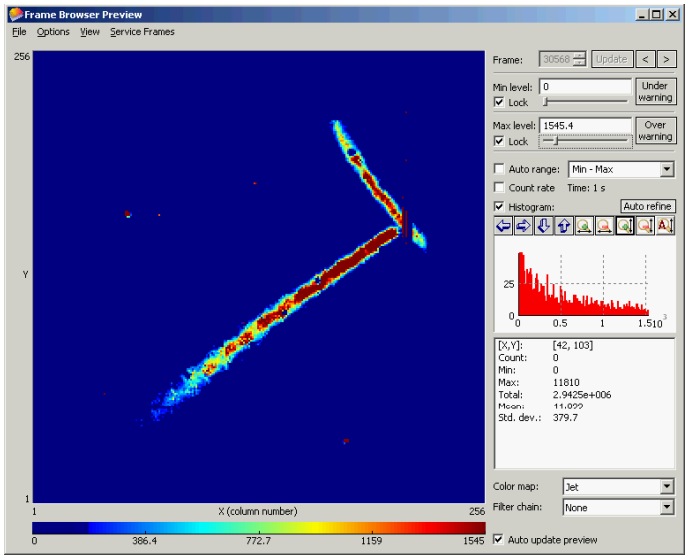
(8) Timepix with GEM has been shown very robust.

(9) Conclusion: Part of the technology is ready:
- Very good energy resolution for Ingrid devices
- Ion backflow at the few per-mil level at high field ratio. Discharge protection seems working for Ingrid (and Micromegas) devices

(10) Plans: Build larger multi-chip detector systems with fast readout.

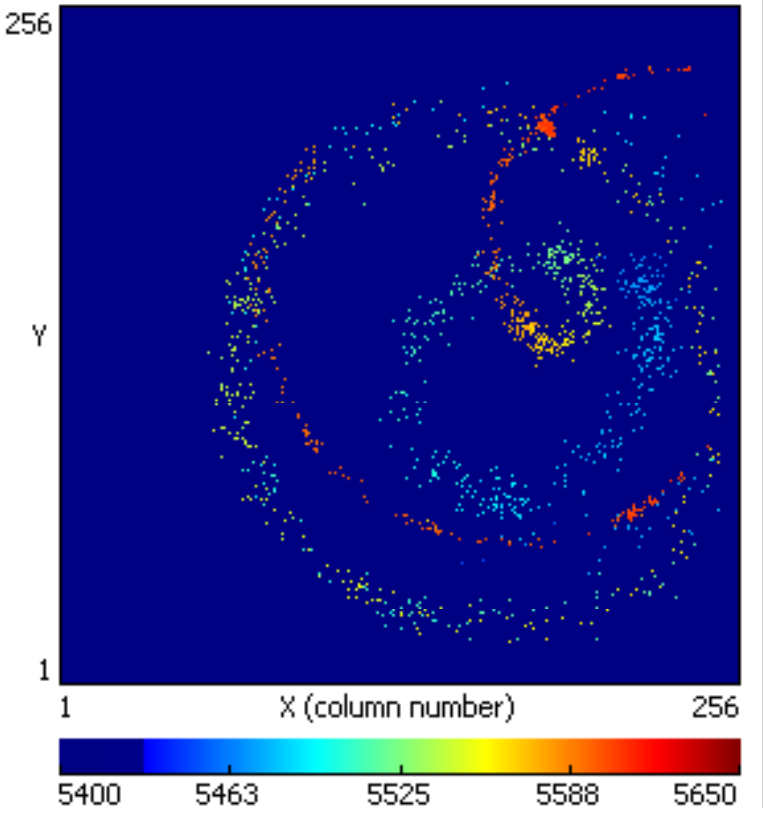
With Thorium in the Ar gas

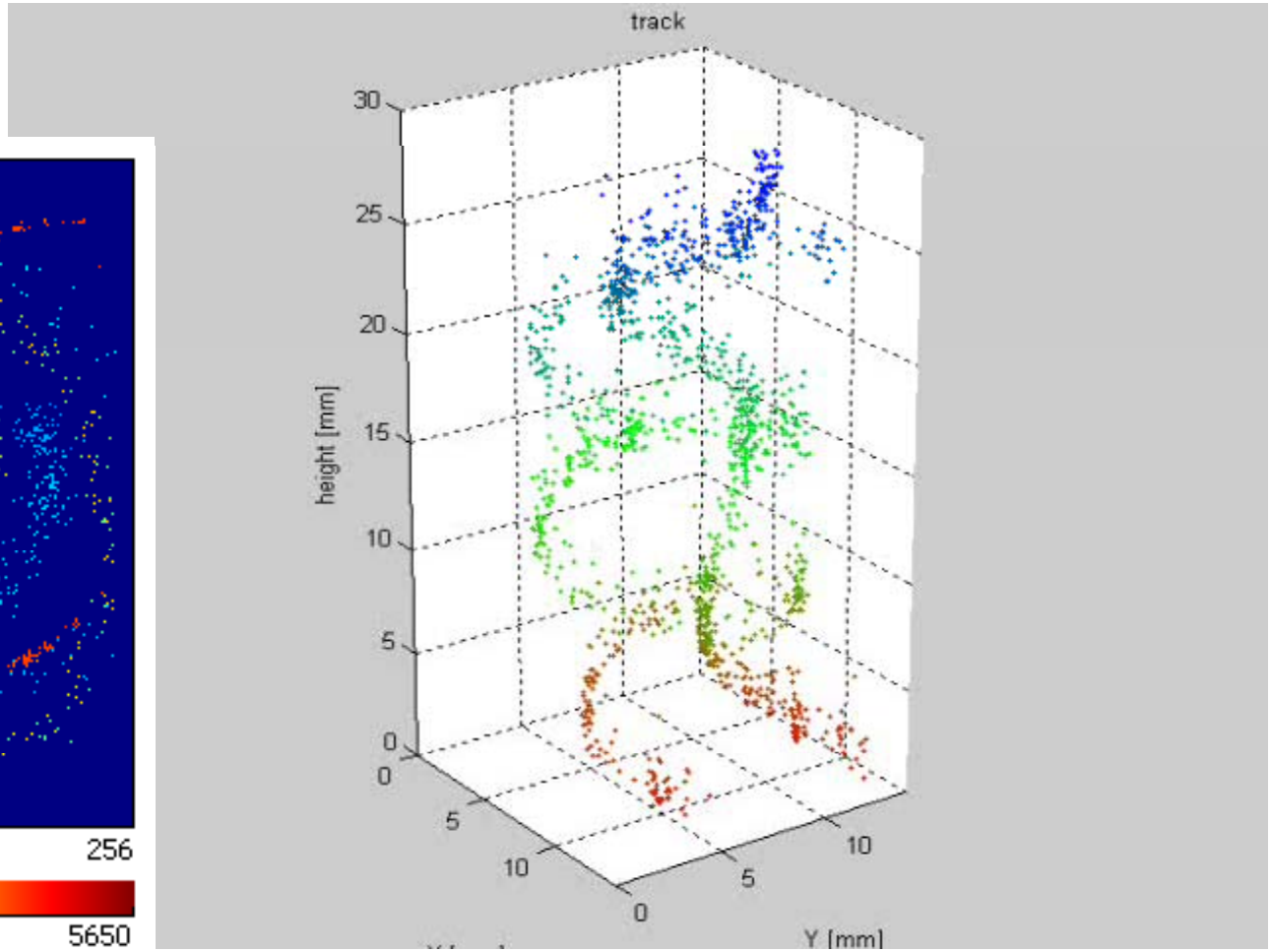




A 5 cm^3 TPC (two electron tracks from ^{90}Sr source)

B = 0.2 T





Performance study of a GEM-TPC prototype using cosmic-ray & CF4 gas test for GEM-TPC.

(1) Reaming issues of the ILC/ILD TPC include the choice of good gases: small diffusion high magnetic filed, sufficient primary electrons, reasonable drift velocity, small electron attachment and stable MPGD operation, gating condition etc.

(2) The Asian groups, under collaboration and cooperation with other LC TPC groups, have been working using small prototype TPCs.

(3) One of the good candidate gas is Ar-CF4-Isobutene mixture providing small diffusion at high magnetic filed according to the Magboltz simulation.

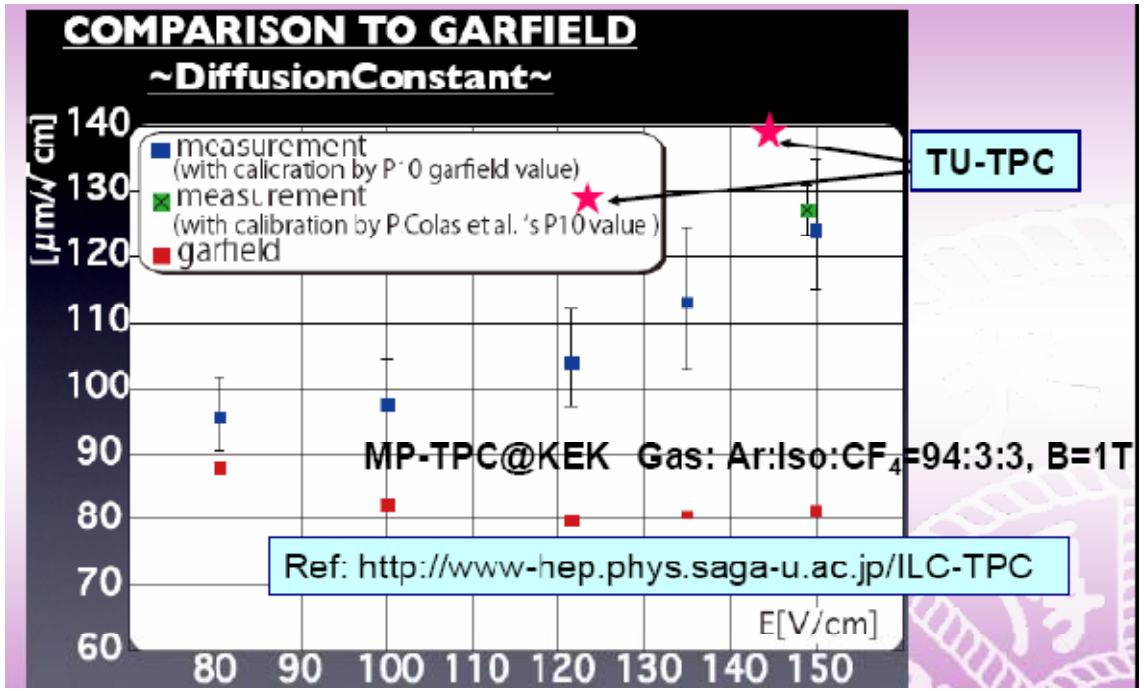
(4) Both groups have tested Ar-Cf4(3%)-isoButene(3%) gas in the TU TPC and MP-TPC in 0 - 1T magnetic field at the KEK cryogenic center.

(5) The 3-layer GEM systems of the two TPC prototypes work fine with the gas although CF4 gas has a high electron attachment at higher electric filed. The measured resolutions for selected cosmic rays agree well with the analytic formula (FK) and provide the numbers of effective electrons Neff closed to our expectation (around 22 for 6 mm long pad).

Performance study of a GEM-TPC prototype using cosmic-ray. & CF4 gas test for GEM-TPC.

(6) Measured diffusion constants of the Ar-CF4(3%)-isoButene mixture are sistematically higher than those given by the Magboltz simulation, in particular, in higher drift filed, although for P10 they agree.

(7) The groups continue the systematic measurement. When the disagreement is confirmed, the results should be feed back to the Magboltz simulation.

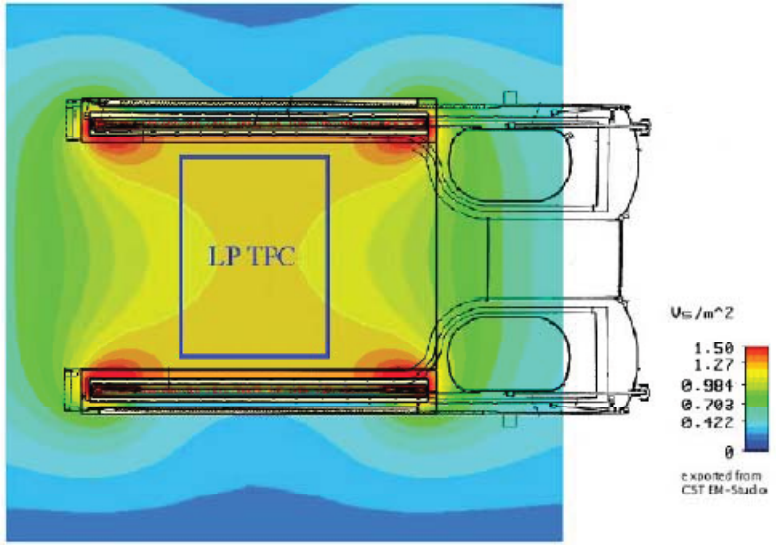


The LCTPC Large Prototype at the DESY Test Beam

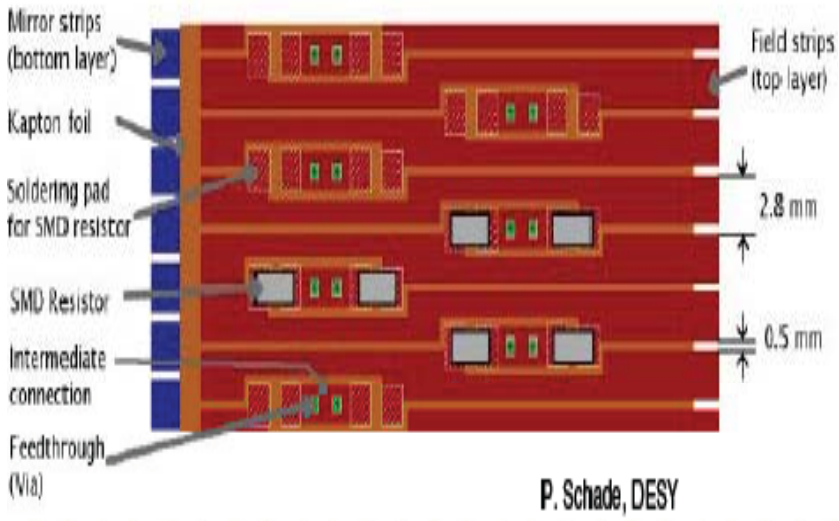
(1) **LC TPC collaboration is preparing the TPC Large prototype beam test from summer 2008 at DESY using the 1T solenoid magnet (PCMAG).**

(2) **A filed cage, 2k channels (later 10K channels) TPC readout electronics based on the ALTRO chips, Si-envelope and support structures are being built as a part of the EUDET project. Under a cooperation with the LC TPC collaboration.**

(3) **Detector modules with MicroMEGAS, GEM and SiTPC, and a common endplate which mounts these detector modules are being designed and fabricated by groups of the LC TPC collaboration.**



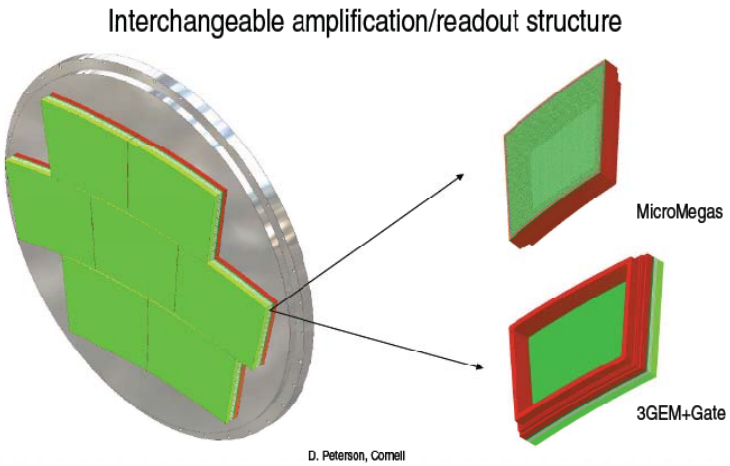
P. Schade, DESY

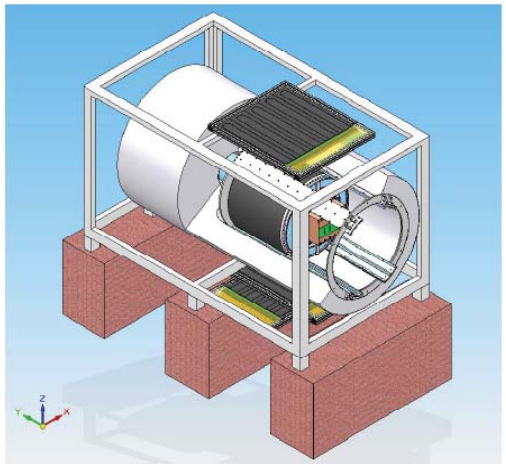


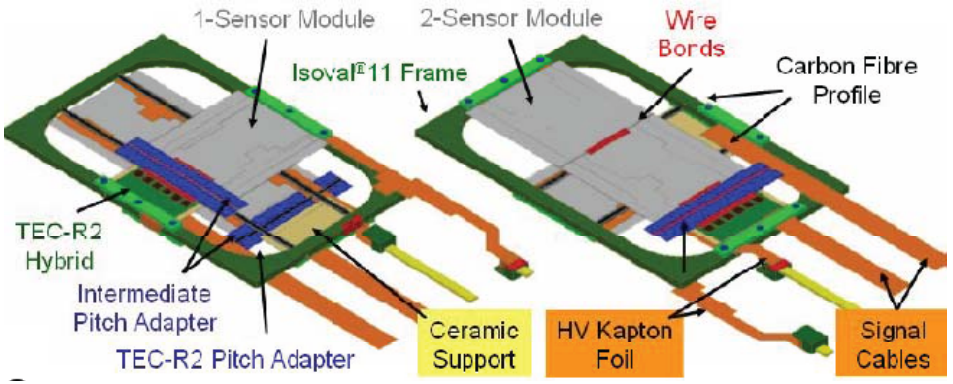
The LCTPC Large Prototype at the DESY Test Beam

(4) Schedule:

- Components are being collected and assembled
- FC – Cathode – Anode expected in April
- First amplification panel (MicroMegas) expected in April
- Commissioning will start in April/May
- Commissioning / Calibration with Cosmic Muon Trigger Setup
- ALTRO electronics available in May
- GEM amplification panel(s) available in August
- DESY II testbeam available in September 2008
- LP is under way







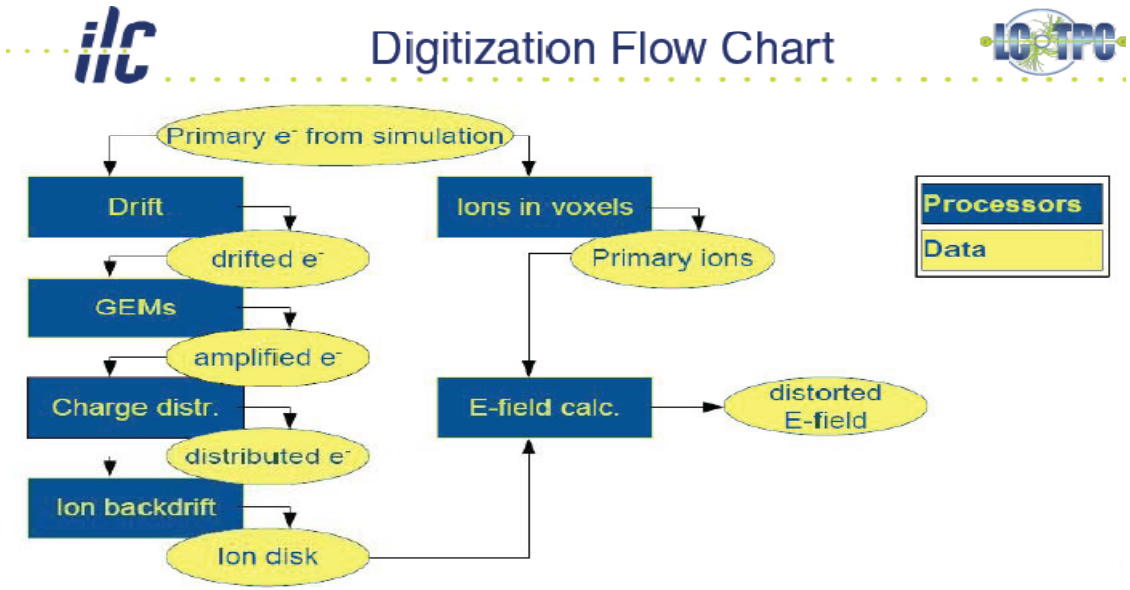
Status of Marlin-TPC

(1) A software package, Marlin TPC is rapidly developed as a common frame work of simulation, digitization, reconstruction and analysis for the LCTPC based on the LCIO, aiming at the advantages of easy comparison, easy transfer from prototype TPC to a full size TPC.

(2) Marlin TPC provides tools to handle different TPC readouts form the standard pad readout to the pixel readout and deal different readout electronics.

(3) Presently 33 processors from different categories in truck. In les than one year in last year there were more than 800 commits and 13 people are working on this project.

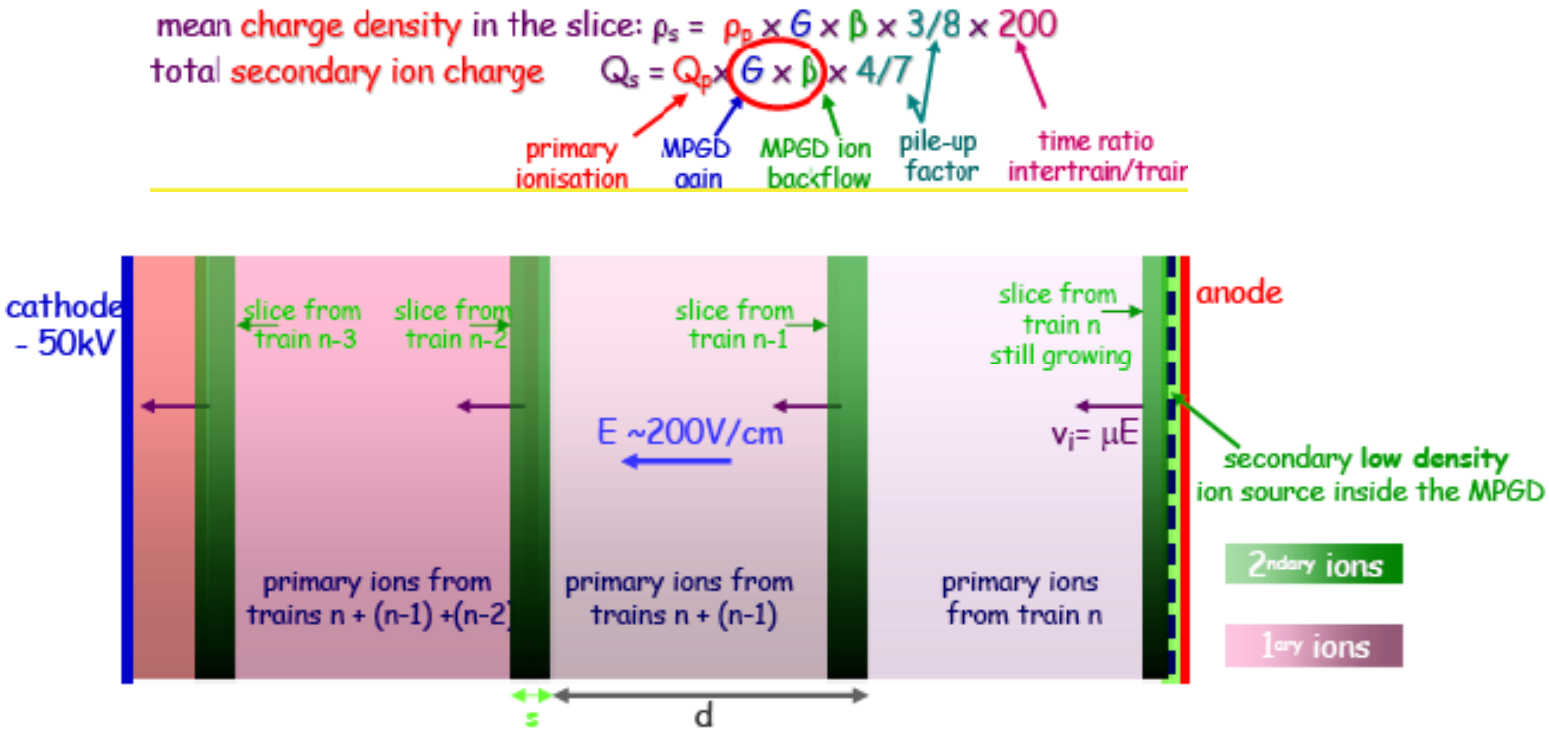
(4) Marlin TPC is now integrated in ilcinstall providing an easy installation.



Ions in the ILC-TPC

(1) Ions in the TPC drift volume, if its density is high, introduce the distortion.

(2) There are two sources of ions; primarily ions and feed back ions from the amplification region.
(3) The collection time of ions is slow: 600ms for the drift filed of 200V/cm compared to the electron drift time of about 40 micro sec.
(4) If the ion feedback ration from the amplification is height, the feed back ions build up the a few ion slices in the TPC drift volume.
(5) G x β is the key factor for the secondary ions. If > 1, we need an ion gating device.



Ions in the ILC-TPC

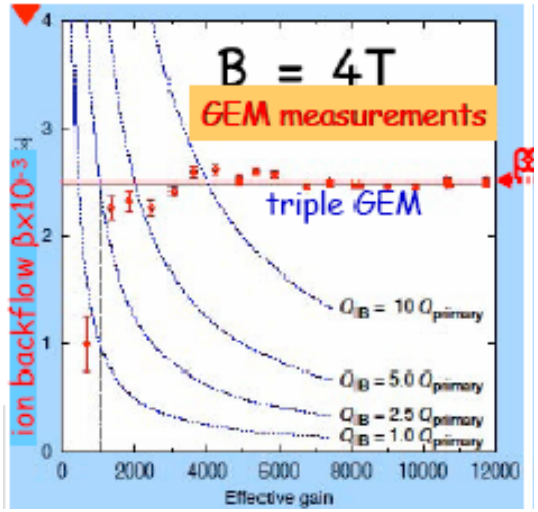
(5) G for the standard MPGD such as MicroMEGAS and 3-layer GEM is 2-3 %. If the gas gain of the MPGD system is say 1,000, the total charge of the feed back ions is about the same order of the primary ions and the mean charge density in the slice may be as high as of about 200 times of that of primary ions.

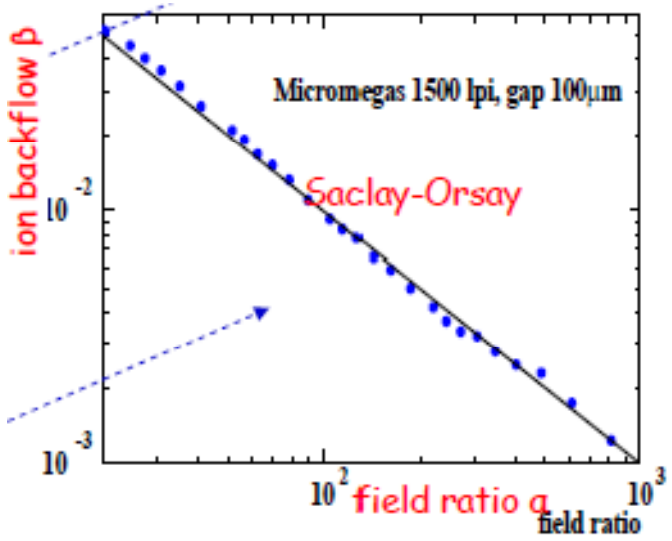
(6) There are few gating scheme to stop the secondary ions. The wire gating is very efficient to stop the feed back ions, easy to implement and no degradation of the electron transmission. But it introduce a mechanical complication to stretch wires and introduce small distortion. Gem gating also stop the feed back ions but the electron transmission may be 70 % at the best and thus introduces some degradation of the position resolution. There are also other new ideas.

(7) Conclusion:

Work the MOGD with low gas gain (500) and try to work with a gas mixture with a large ion mobility. There are a few possible gating scheme which have to be fully studied.

(Need a full investigation by simulation.)





Electron Transmission Measurement of GEM gate

(1) The electron transmission are measured for different types of gating GEM and compared to the simulation with Maxwell 3D and Garfield.

(2) The GEM gate stops the feed back ions almost completely (< 10-4).

(3) Measured the electron transmission of three different gating GEM.

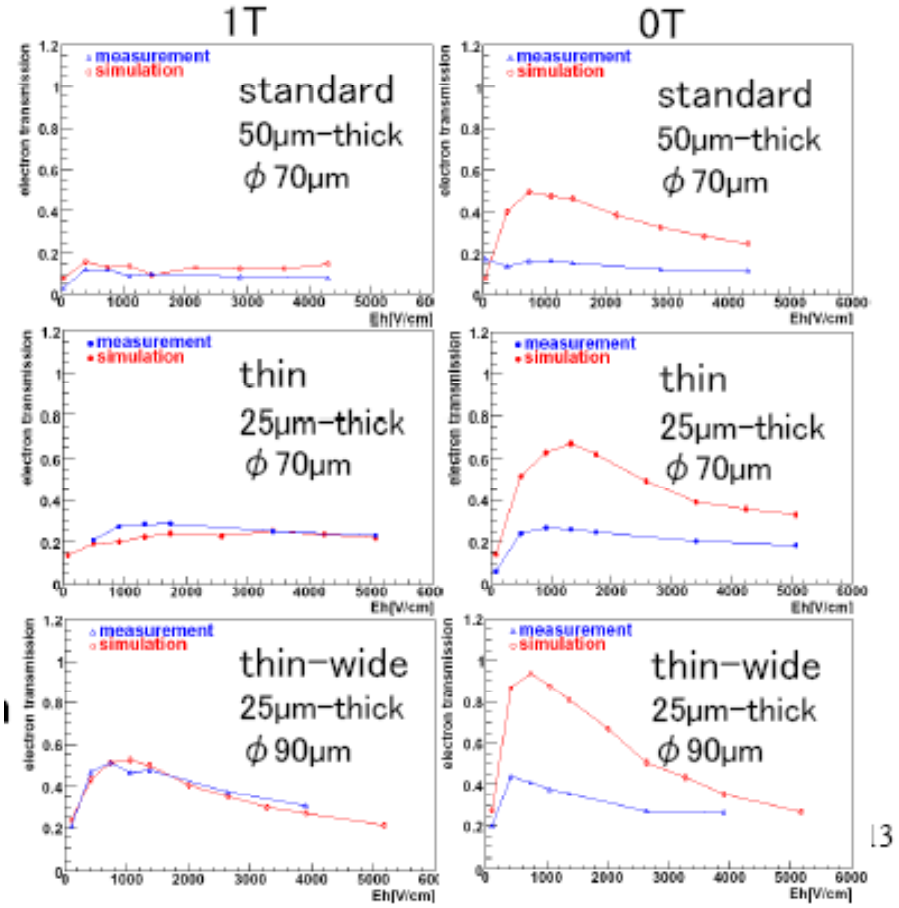
(4) The electron transmission is measured to be better for thinner GEM with larger holes (25μm-thick, φ90μm). The best transmission efficiency was around 50 % at B = 1T.

(5) The measurement results agree well with the simulation at 1T but not at 0T.

(6) The best transmission obtained by the simulation is about 70% for 12.5μm-thick GEM with 90μm holes for Ar-CF4(5%)-isoButene(1%) at 3T. The GEM is under fabrication for test.

Gate GEM	Standard	Thin	Thin – Wide
Insulator Thickness	50[μm]	25[μm]	25[μm]
Hole diameter	70[μm]	70[μm]	90[μm]
Cu thickness	5[μm]		
Hole pitch	140[μm]		
Insulator	polyimide		

Electron transmission measurement of GEM gate



Ar:isoC$_4$H$_{10}$ (90:10)

B = 0 and 1T (at KEK C.C.)

7 Talks on Pixel Detectors

1. **First test beam result of the ISIS1 by Dr. Jaap VELTHUIS (University of Bristol)**
2. **A CCD-based Vertex Detector for the ILC by Dr. Konstantin STEFANOV (RAL)**

3. **FPCCD vertex detector for ILC by Dr. Yasuhiro SUGIMOTO (KEK)**
4. **4. Development of FPCCD Readout ASIC by Dr. Yosuke TAKUBO (Tohoku University)**

5. DEPFET ILC VTC by Dr. Marcel VOS (IFIC Valencia)

6. Recent developments on MIMOSA CMOS sensors by Marc WINTER (Institut de Recherches Subatomiques (IReS))

7. Silicon Pixel Tracker for the ILC by Dr. Konstantin STEFANOV (RAL)

First test beam result of the ISIS1

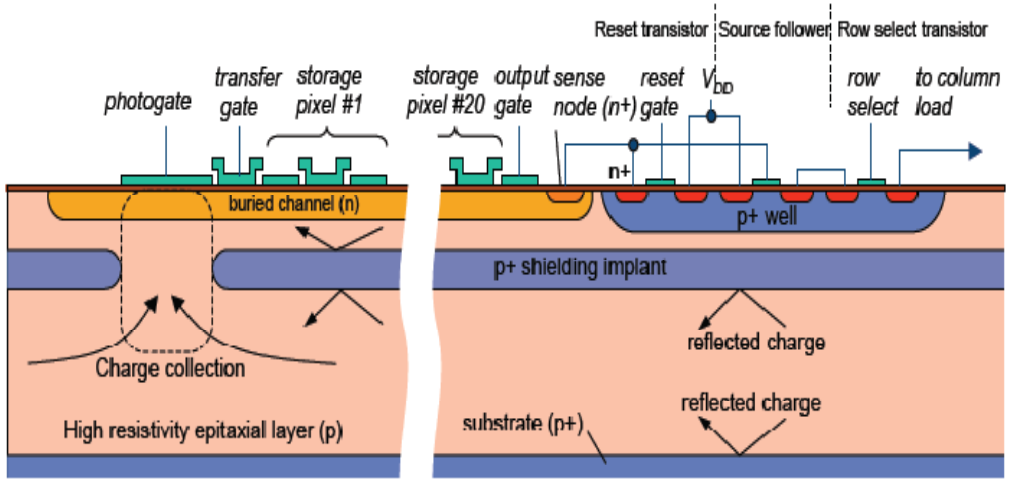
(1) A beam test of ISIS1, the proof of principle device of In-Situ Image Sensor, was performed successful, and demonstrated that ISIS works as a sensor.

(2) Results are: S/N=37.3±0.2, σ = 10.8± 0.4 μm and they were homogeneous over memory cells.

(3)The lower signal peak is due to local charge loss. This should be improved in newer ISIS design (p-well&ISIS2).

(4) Thinning the detector to the ILC thickness does not affect S/N, however the pixels size is still large.

(5) ISIS2 is being designed.



- **Every pixel has mini CCD to store charge**
- **Transfer red to storage pixel during bunch train**
- **20 transfers per 1ms bunch train**
- **Readout during 200ms quiet period after bunch train**

ISIS1: 16 x 16 channels, Cell: 40 μm × 160 μm and with 5 pixels

A CCD-based Vertex Detector for the ILC

(1) CPCCD programme:

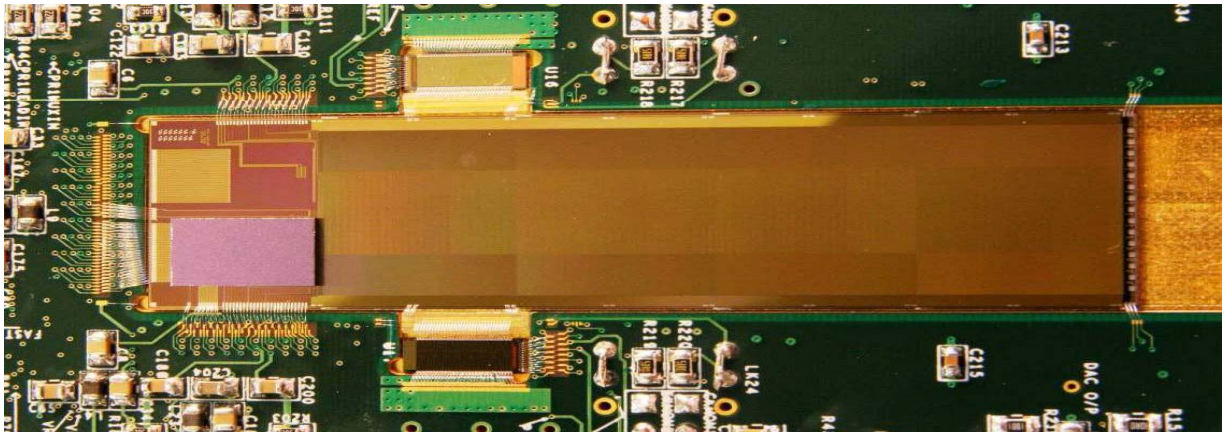
- **Bump-bonded assemblies CPC2-40/CPR2 reach 9 MHz**
- **Programme for capacitance and clock amplitude reduction underway**
- **Driver system with CMOS ASICs or transformers**
- **Third generation readout chip CPR2A to be delivered in April**

(2) ISIS development:

- **ISIS1 with p-well shows good protection from parasitic charge collection**
- **Now designing ISIS2 in CMOS process**

(3) Mechanical support aims at ≤ 0.1% X0 using modern materials:

- **Silicon(25μ）-RVC foam sandwich (~ 3% density): Achieves 0.09% X0**
- **Silicon on SiC foam (~ 8% density)**



Bump-bonded assemblies CPC2-40/CPR2

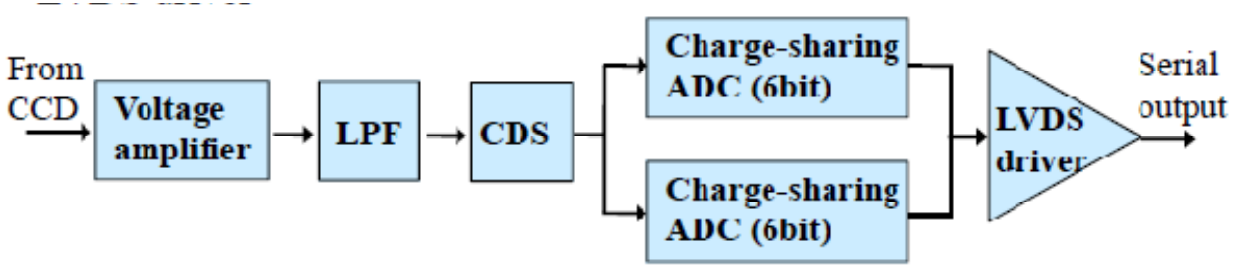
FPCCD vertex detector for ILC
Development of FPCCD Readout ASIC

(1) The first prototype FPCCDs have been made by HPK and will be delivered soon
- **Pixel size: 12mm**
- **H-register same size as pixels in image area**
- **4ch/chip**
- **Several types of output circuit**
- **Two different epitaxial layer thickness (15 / 24 mm)**
- **Two different gate oxide thickness for output transistors**

(2) Detailed study on the prototype FPCCDs will be done in FY2008.

(3) Radius of innermost layer Rin of VTX was studied for 3, 3.5, and 4T magnetic field, and Rin=17.5, 16, and 15 mm are proposed, respectively to keep reasonable clearance between pair-background core and beam pipe, and between beam pipe and ladder.

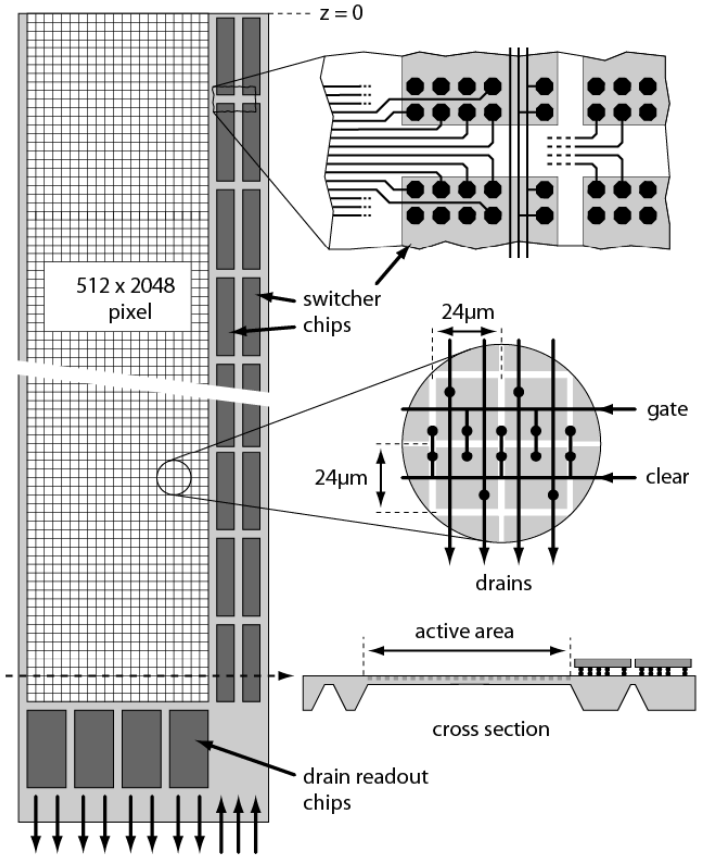
(4) The readout ASIC has been developed for the FPCCD:
- **10Mpixel/sec, noise < 30e, <6mW/ch,**



DEPFET ILC VTC by Dr. Marcel VOS (IFIC Valencia)

1. **ILC VDX Prototype System with DEPFETs (450µm), CURO and Switcher.**
2. **Test beam @ CERN:**
   - **S/N≈110 @ 450 µm while the goal S/N ≈ 20-40 @ 50 µm**
   - **Sample-clear-sample 320 ns while the goal 50 ns**
   - **Space resolution of 1.3 µm @ 450 µm while the goal ≈ 4 µm @ 50 µm**
3. **Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)**
4. **Radiation tolerance tested with single pixel structures up to 1 Mrad and ~1012 neq/cm2**
5. **Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.**
6. **Preparations for the new DEPFET generation are in full swing:**
7. **Thinning technology at the door step to migrate to the production line. Excellent results using a commercial supplier for the engineered SOI wafers.**

ILC VXD baseline design

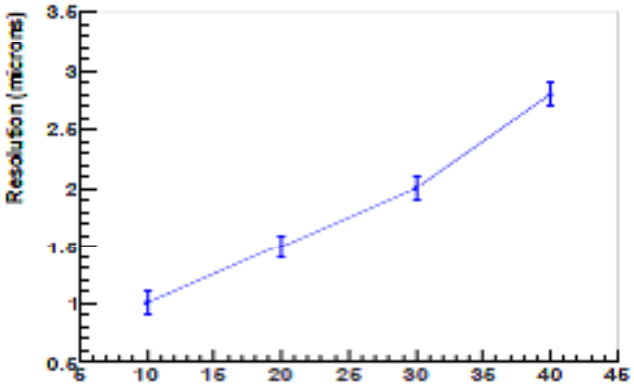


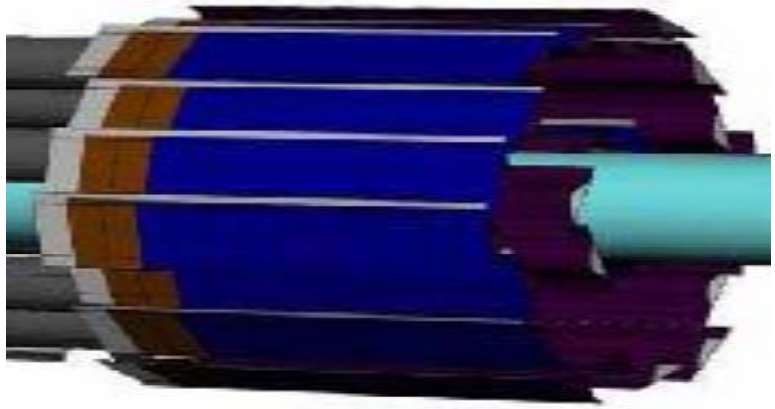
Recent developments on MIMOSA CMOS sensors

(1) Commissioning and Use of a MIMOSA Telescope
New beam telescope operated at DESY and CERN-SPS:

(2) Beam test Results:
Single point resolution versus pixel pitch:
Response to inclined tracks
Thinning of Diced Sensors:
(50 µm on a good track)

(3) Vertexing Applications of MIMOSA Chips: Short & Mid-Term
Vertex Detector upgrade for STAR experiment at RHIC
2 cylindrical layers : 1600 cm2
160 million pixels (30 µmpitch)
3 steps : 2007: telescope (3 MIMO-14) BG meast, no pick-up !
2008/09: digital outputs without Ø (640 µs)
2010/11: digital outputs with integrated Ø (200 µs)
Beam telescope (FP6 project EUDET)





Recent developments on MIMOSA CMOS sensors

5) Integration of Signal Processing:

MIMOSA-16 beam test

Zero Suppression Micro-Circuit : SUZE-01 Fabrication & Tests

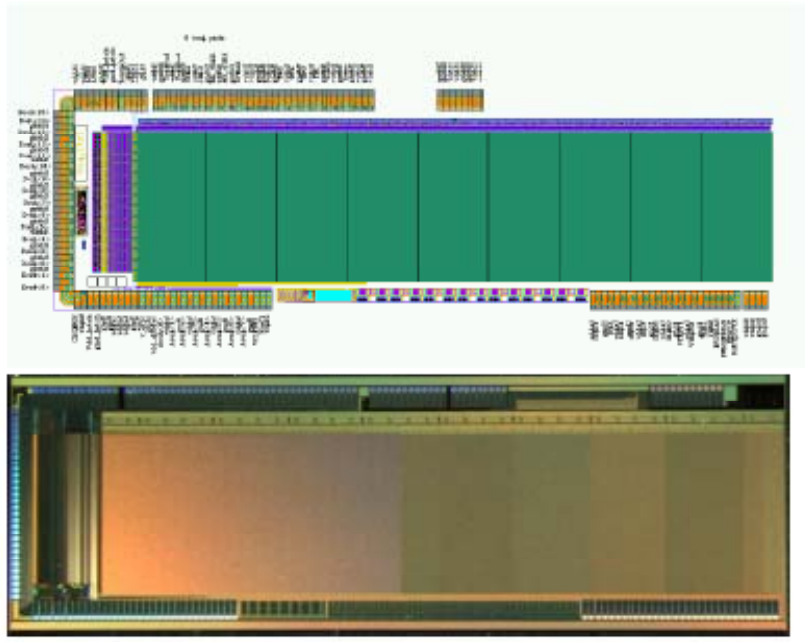
Final prototype with column // architecture : MIMOSA-22

Pixel characteristics (*optimal charge coll. diode size ?*) :

- pitch : 18.4 μm (compromise resolution/pixel layout)
- diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- 128 columns ended with discriminator
- 8 columns with analog output for test purposes
- 9 sub-matrices of 64 rows :

  17 pixel designs w/o ionising rad. tol. diode

  $\Rightarrow$ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)
- read-out time $\sim$ 100 μs



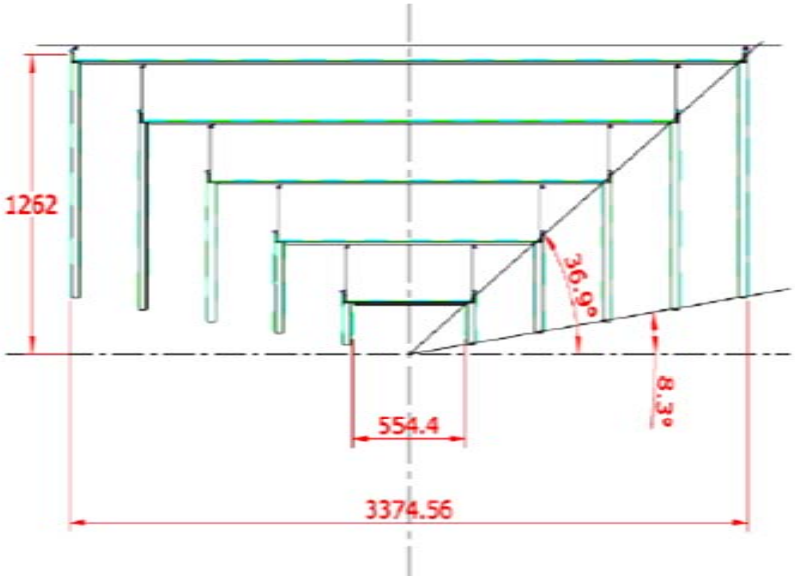
Silicon Pixel Tracker for the ILC

In the barrel:

- **It could be possible to integrate all events (and the background) and read in the inter-train gap**
- **We have to prove that the pattern recognition does not deteriorate**
  - **Additionally, the detector becomes highly tolerant to beam-induced EMI**

In the very forward region:

- **Time slicing or bunch stamping could be necessary due to higher backgrounds (e.g. 2-photon processes), needs good knowledge of the backgrounds and more studies**



- Barrel and Forward trackers, total area = 70.3 m^2
- With 50 μm x 50 μm pixels – 28.1 Gpix system
- Low mass support, gas cooling
- If each chip is 8 cm x 8 cm (2.6 Mpix): 11,000 sensors is total
- Readout and sparsification scheme to be developed

With CCD or MAPS (time stamping)

4 Talks on Silicon Detector

1. **The latest developments of the SiLC collaboration by Dr. Aurore SAVOY NAVARRO (LPNHE-UPMC/CNRS-IN2P3)**

2. **A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips readout by Dr. Aurore SAVOY-NAVARRO (LPNHE-UPMC/CNRS-IN2P3)**

3. **Alignment System for Silicon Tracking by Alberto RUIZ JIMENO (Universidad de Cantabria)**

4. **Silicon sensor new developments by Dr. Winfried MITAROFF (Austrian Academy of Sciences / Inst. of High Energy Physics)**

The latest developments of the SiLC collaboration

(1) R&D on sensors:

μstrips:

New HPK detector:

3D Planar μstrips: provide edgeless (hermetic), low V, thinner, faster and rad hard device.

Develping new routing and inline pitch Technology with HPK for FE chip onto the strips:

Also consider pixel:

Pixels for the very forward zone nearby the vertex detector

Pixels in the overall internal region both central barrel and all very forward disk:

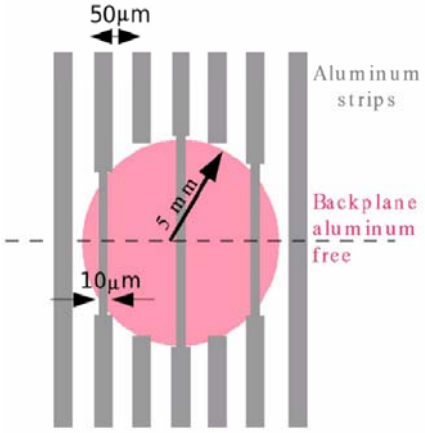
(2) R&D on electronics:

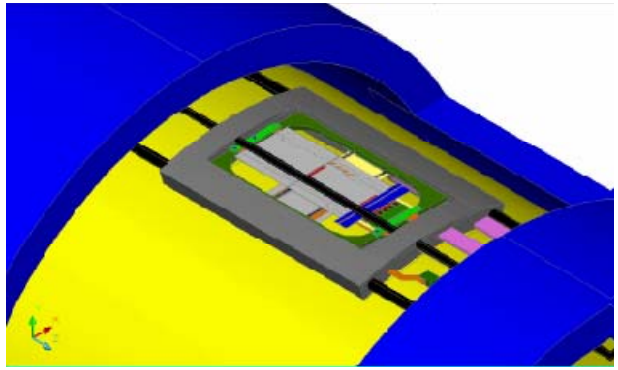
(3) Mechanics developments

Alignment by 2-fold approach

Test with of the Silicon Envelope with LCTPC in 2008 at DESY: Modules(HEPHY), structures(IEKP) final electronics (LPNHE)

(4) Test beam activities:





A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips readout

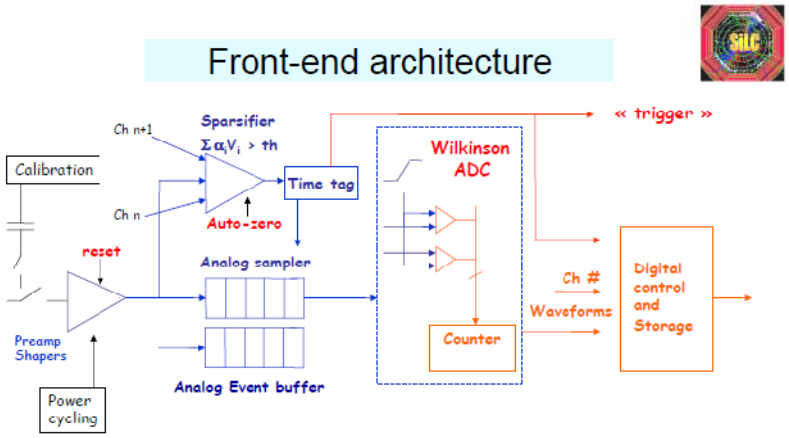
(1) The goal: Full readout chain integration in a single chip, 512 or 1024 ch in 90nmCMOS

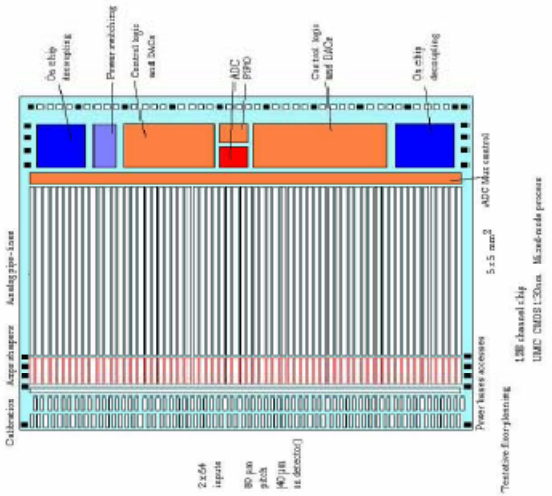
(2) The first step: the 4-channel chip,SiTR-130_V1&2: Test Amplifier, Shaper, Sparsifier, Analog sampler & ADC.

(3) SiTR-130_V1 test-beam response demonstrates the feasibility of a highly integrated front-end for Silicon strips.

(4) New 96ch version: SiTR-130_96 with a complete FE and readout chain on detector, higher multiplexing to be submitted in April 15. The simulation underway.

(5) Attempt of bump-bonding the chip onto the detector (HPK).





The latest developments of the SiLC collaboration

Perspectives cont'd

- SiLC is a **transversal R&D activity**
- It intends to play a major role not only on the development of novel technologies needed to overcome the challenges ahead of us,
- But also **to study and compare the tracking alternatives** proposed for the ILC **with a joint optimization task force**.

  This workshop played an important role in reinforcing the will some people from the 3 proposed ILC detectors have to collaborate with a joint simulation tracking effort. Sharing tools and expertise (see discussion at the SiLC meeting yesterday).

  It will be benefitial to help in the processus of validation, Loi's etc…in front of us.
- Same for **combined test beams** especially those at FNAL next year.
- SiLC intends also to **further exploit the synergy with other machines and HEP domains**, especially the LHC and its upgrades.