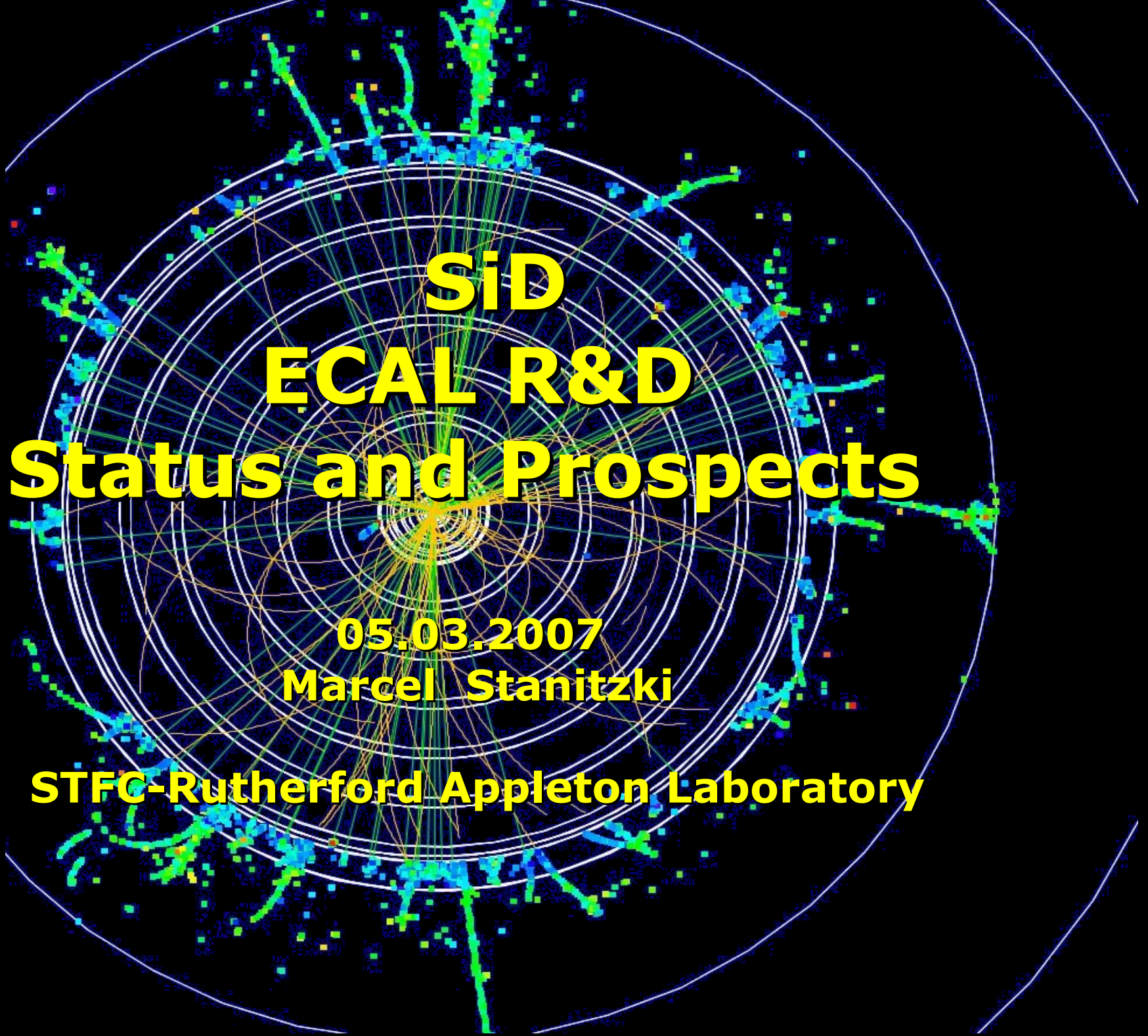


# SiD ECAL R&D Status and Prospects

05.03.2007

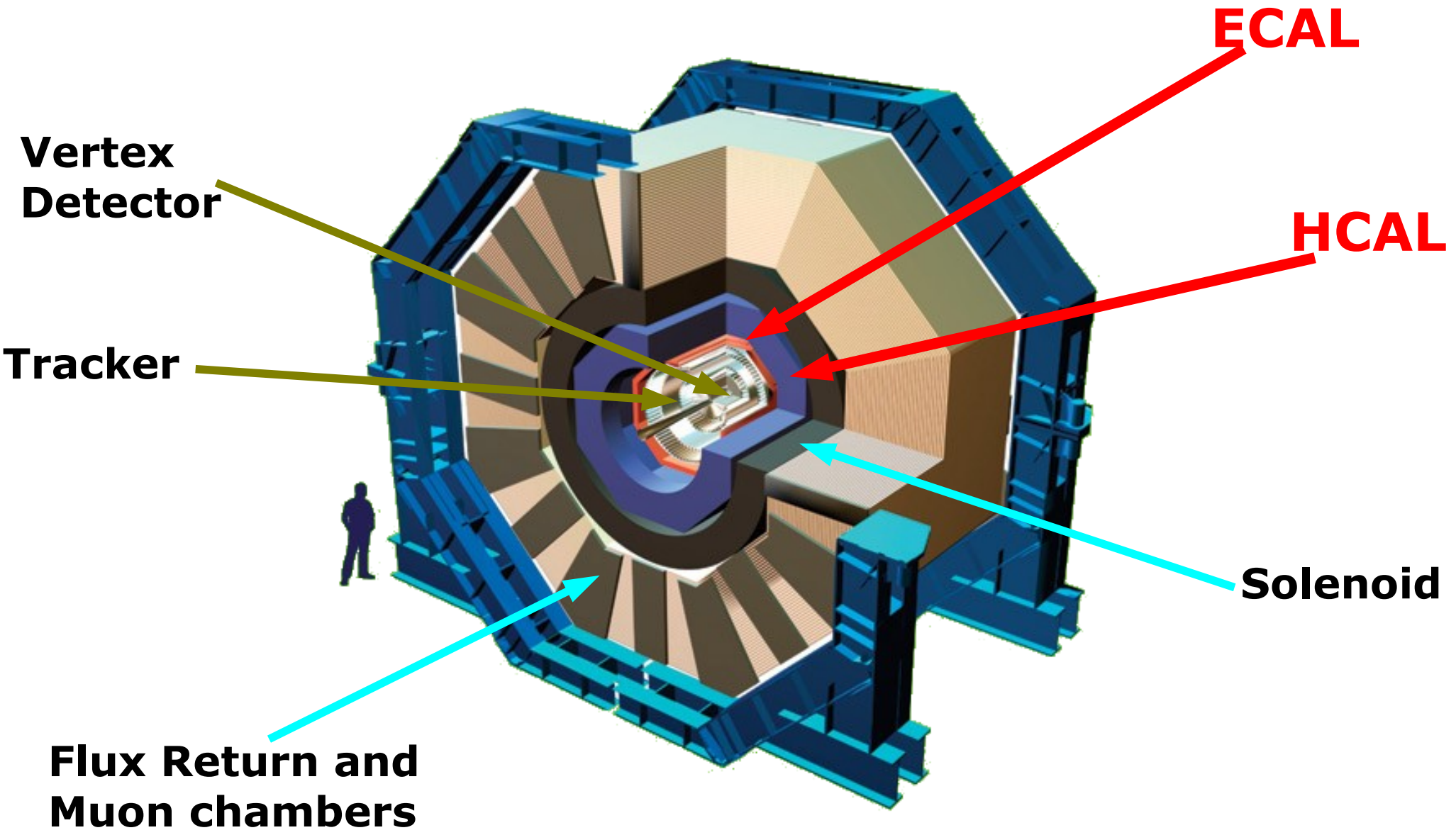
Marcel Stanitzki

STFC-Rutherford Appleton Laboratory

# Introduction

- The SiD Calorimetry System is build around the Particle Flow paradigm
  - High granularity
  - Located inside the solenoid
  - Well integrated with Tracking
- The ECAL is designed as ***Imaging ECAL***
  - Material of choice is Si+W
  - Sampling calorimeter
  - Good energy resolution
  - Compact
  - Segmentation smaller than $r_{Moliere}$

# SiD – a PFA detector

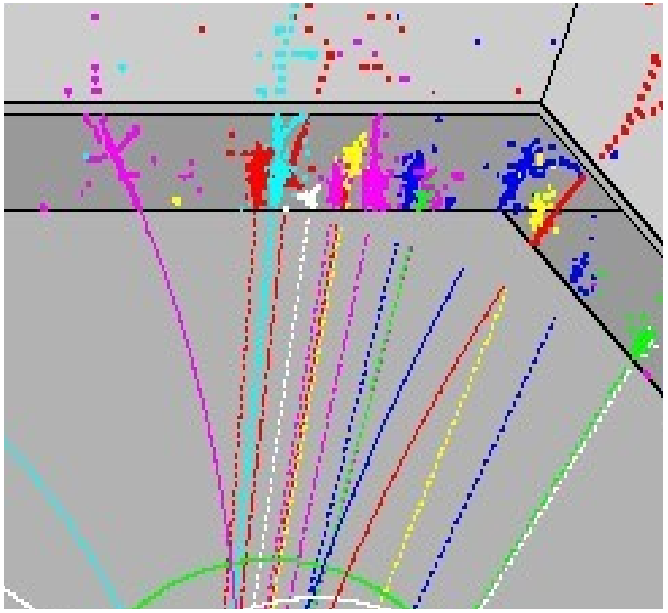


# Physics with the ECAL

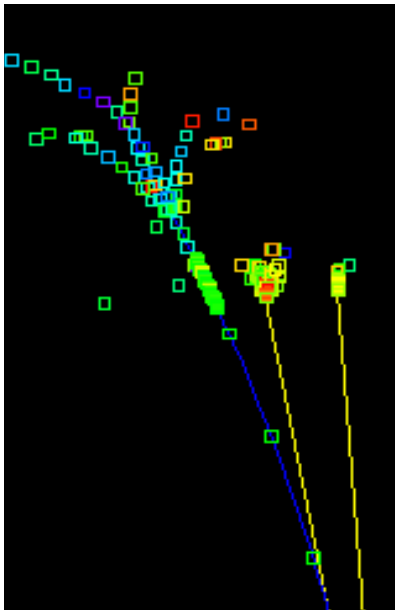
- Multi-jet final states (Higgs, Top ..)
  - $\pi^\circ$ measurement should not limit jet resolution
  - identify and measure hadronic showers
  - track charged particles
- $\tau$ id and analyses
- Photons
  - Energy resolution, e.g. $h \rightarrow \gamma\gamma$
  - Vertexing of photons ( $\sigma_b \sim 1$ cm ), e.g. for SUSY studies
- Electron ID
- Bhabhas and Bhabha acollinearity
- Hermiticity

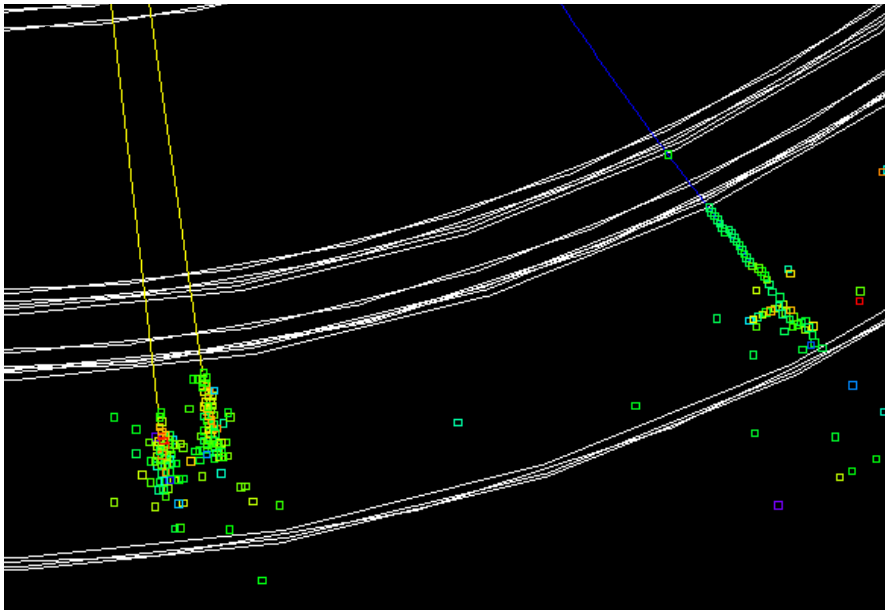
$\Rightarrow$ Imaging ECAL can do all this

# Some Examples



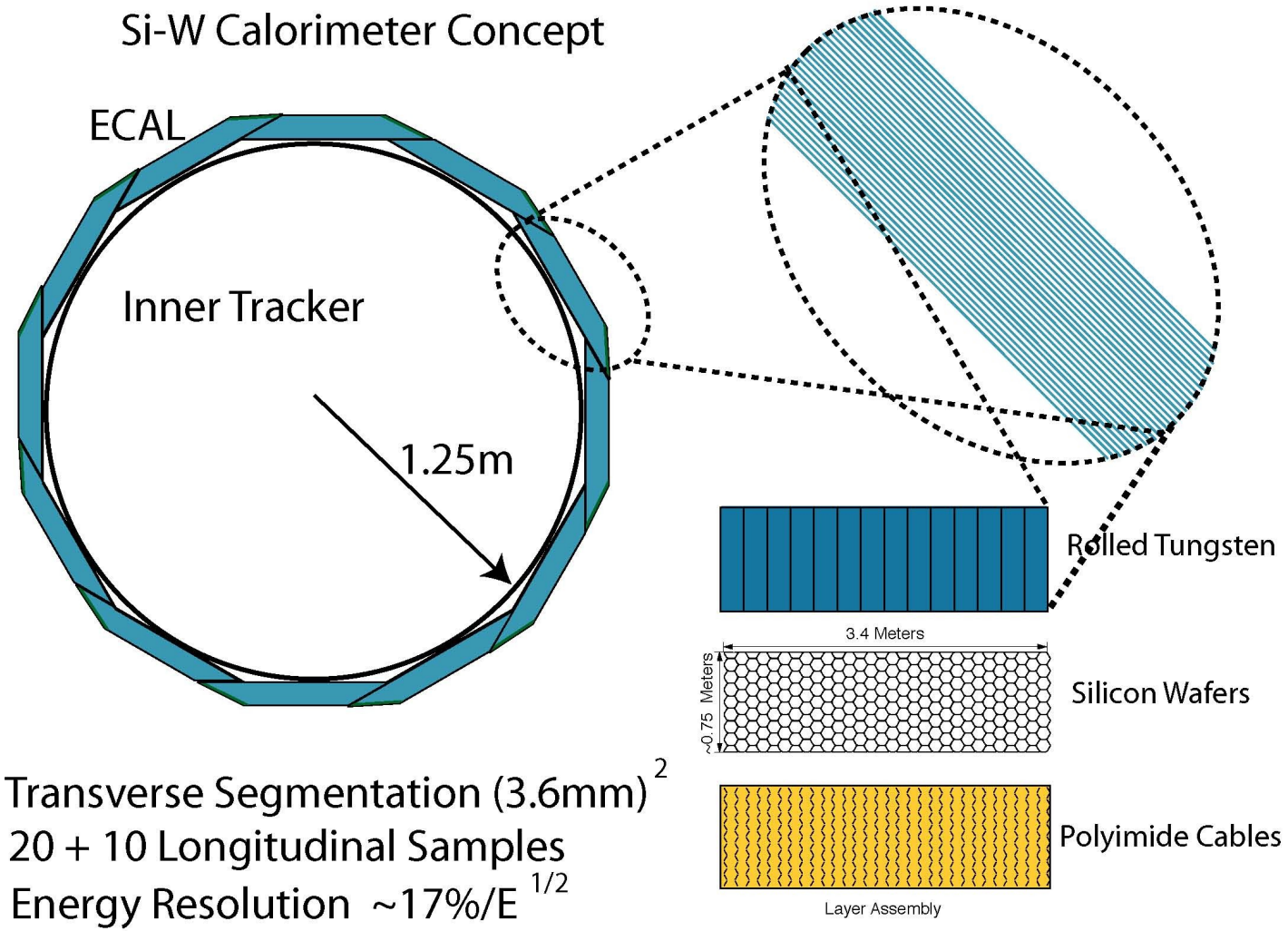
**Jet Environment**





$\tau^+ \rightarrow \rho^+\nu \quad (\pi^+\pi^o\nu)$

# Mechanical layout




Transverse Segmentation $(3.6mm)^2$

20 + 10 Longitudinal Samples

Energy Resolution $\sim 17\%/E^{1/2}$

**Baseline configuration:**

- longitudinal: $(20 \times 5/7\ X_0) + (10 \times 10/7\ X_0) \Rightarrow 17\%/\sqrt{E}$
- 1 mm readout gaps $\Rightarrow$ 13 mm effective $r_{Moliere}$

# Two ECAL options

**Si+W**

**Common Mechanical Design**

## Traditional Silicon Diodes

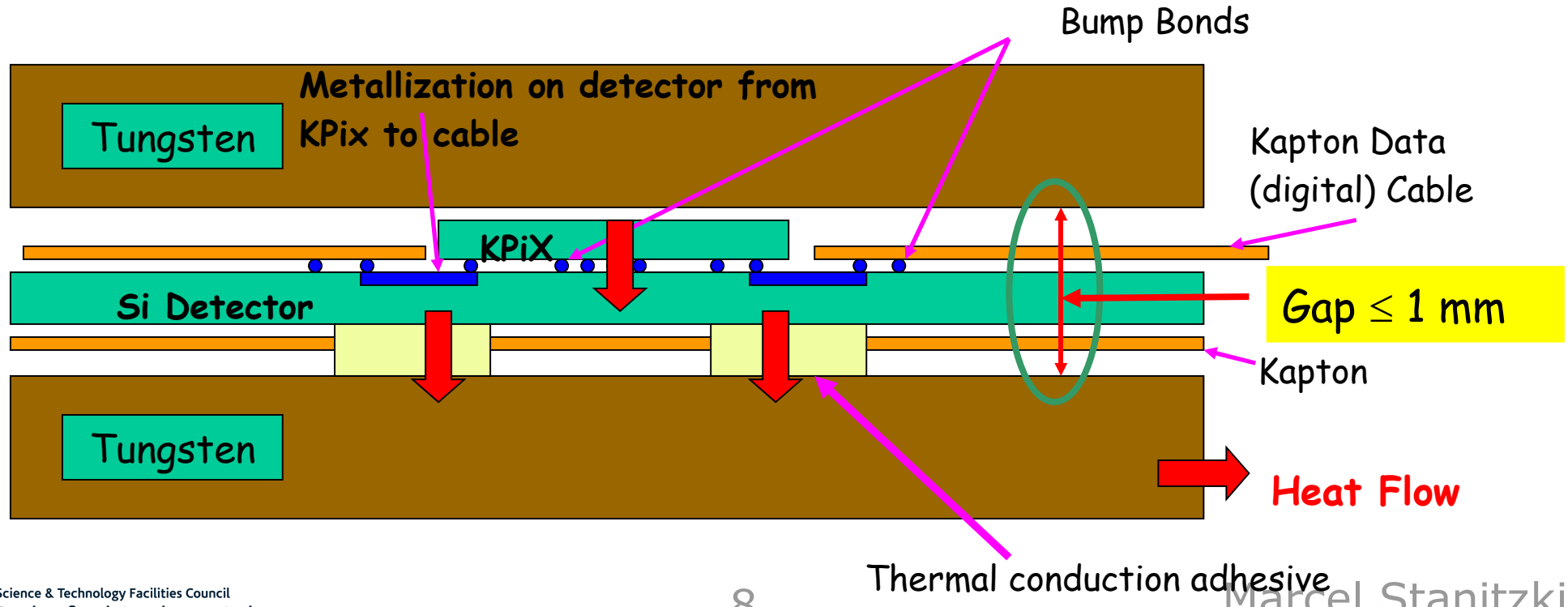
- HEP-style silicon
- 16 mm$^2$ hexagons
- Analog readout
- KPiX readout chip
- SiD *baseline*

## TeraPixel

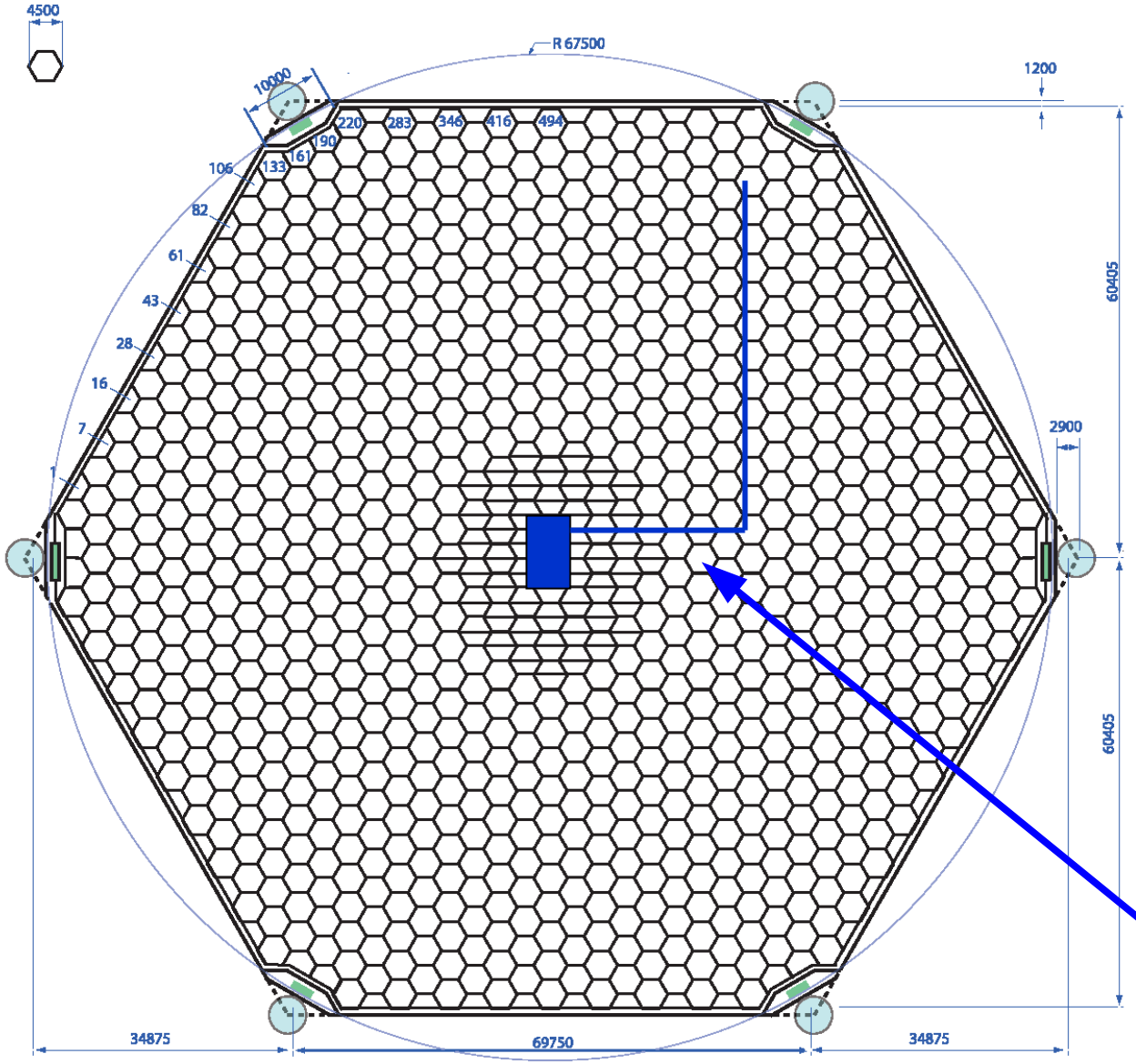
- CMOS MAPS
- 50 μ pixel size
- Digital readout
- readout integrated in pixel
- *Alternate* option

# SiD Requirements

- Fit in common mechanical structure
- Power pulsing (1 % duty cycle)
  - passive cooling
  - Requires < 40 mW/channel
- Single Bunch Time stamping



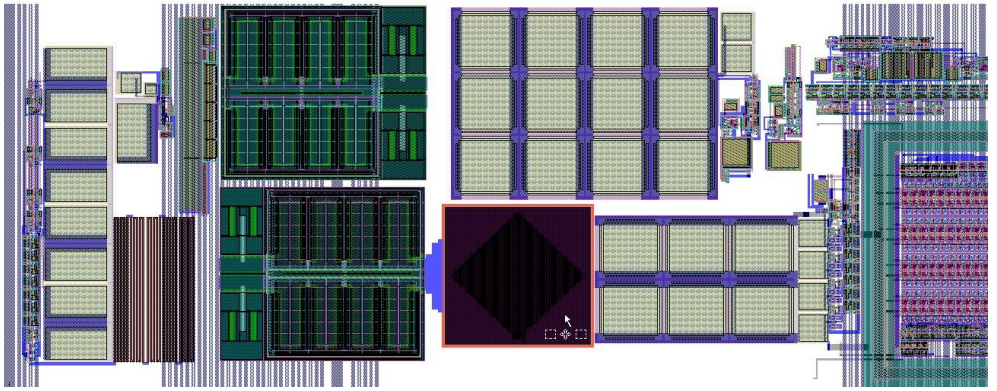
# The "traditional" approach



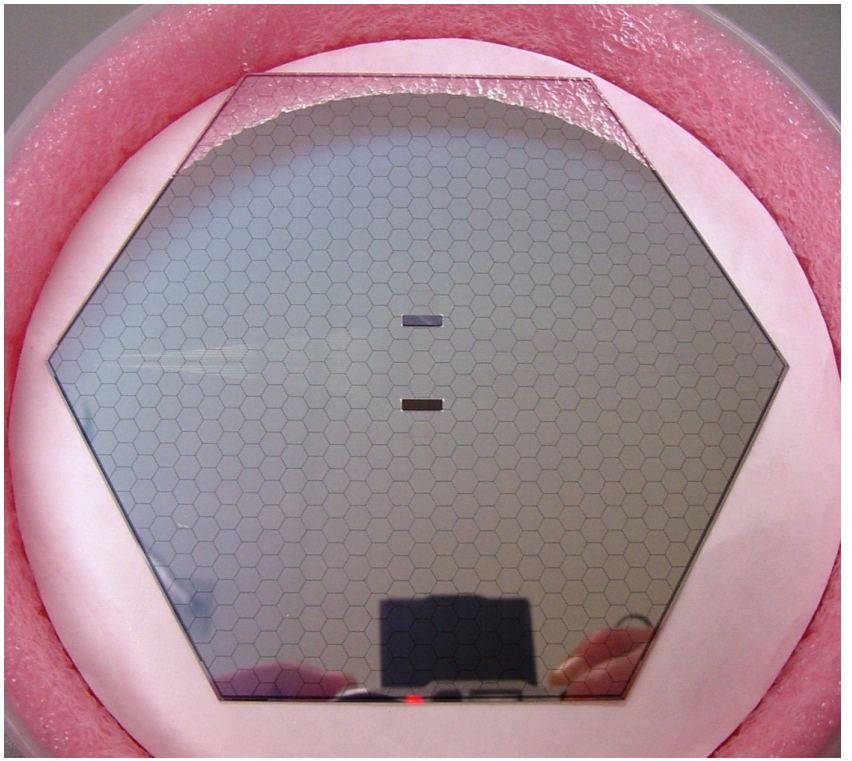

- 6 inch wafers
- 1024 13 mm$^2$ pixels
- improved trace layout near KPiX to reduce capacitance
- procurement in progress , 40 wafers from Hamamatsu

KPiX ASIC and sample trace

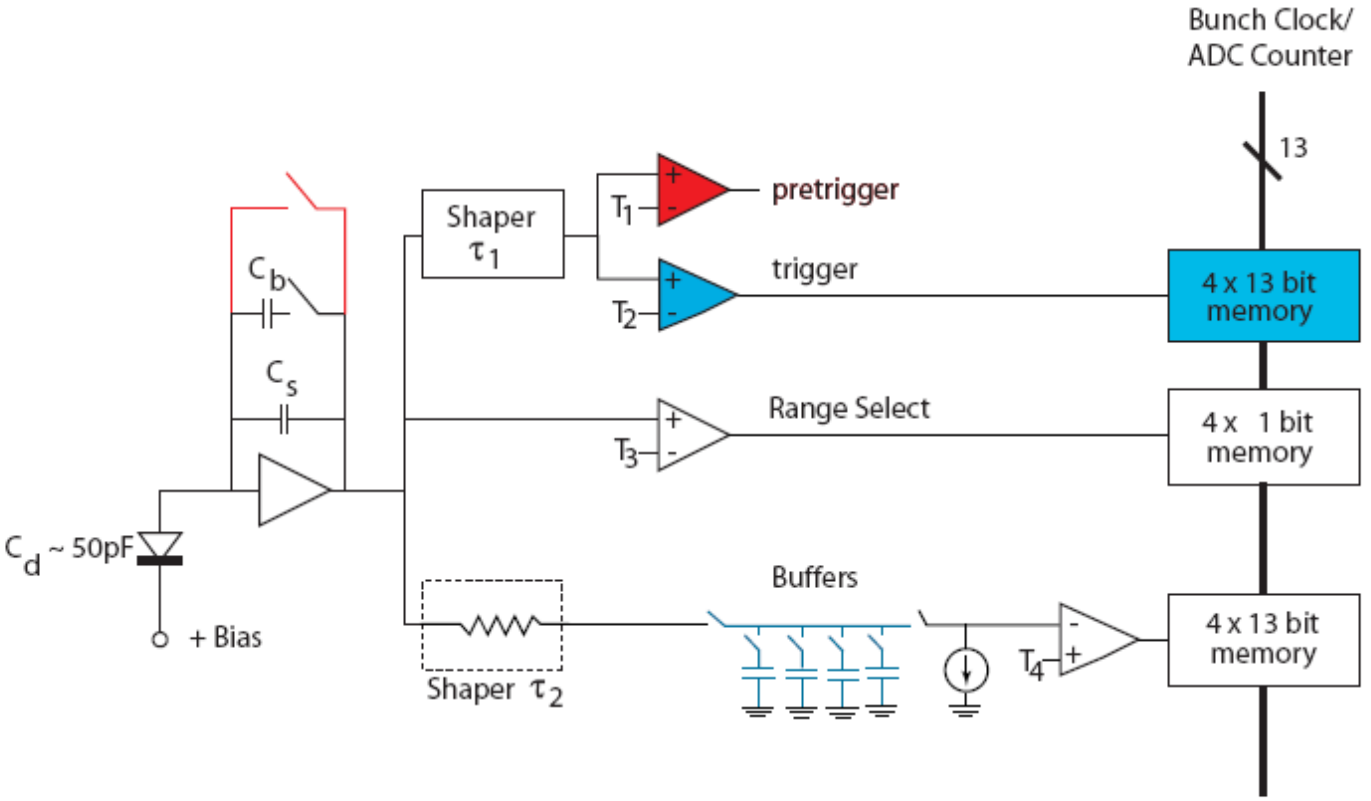
# KPix readout chip



- 1024 channels
  - prototypes have 64 channels
- bump-bondable
- 13 bit ADC and Dynamic Gain selection
- 0.25 micron CMOS
- ~ 20 mW/channel
- KPiX is also foreseen to be used in
  - Tracker
  - HCAL
  - Muon chambers



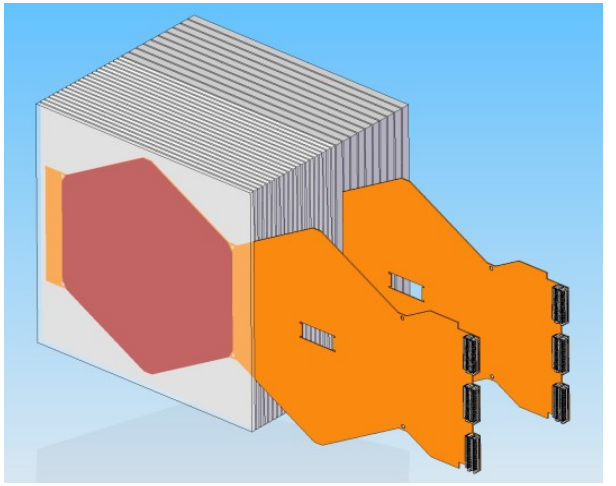
# KPiX in Detail




- Threshold $T_1$ is used to inhibit resets (set at 2 × noise)
- Threshold $T_2$ is used to enable data storage (set at 4 × noise)
- Bunch clock (time) is stored in SRAM (13 bit precision)
- Analog charge is stored on capacitors (13 bit precision)

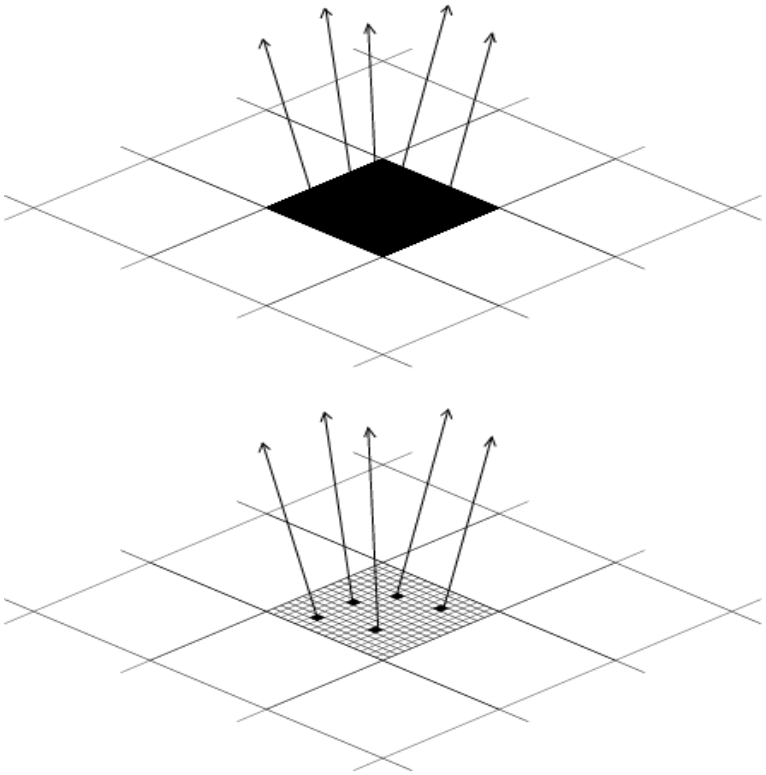
# Current Status

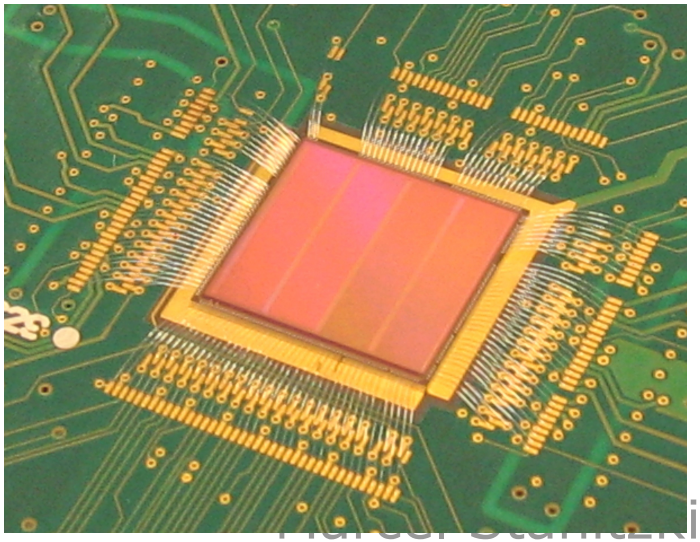
- Working on first 1024 channel version
  - 64 channel protypes are tested extensively
  - 6th generation prototype available
  - Design work on 7th generation
  - One intermediate 256/512 channel version
- Demonstrate Bump-bonding of KPiX
- Build Test beam module (30 layers)
- Start on a real mechanical design



# TeraPixel Option

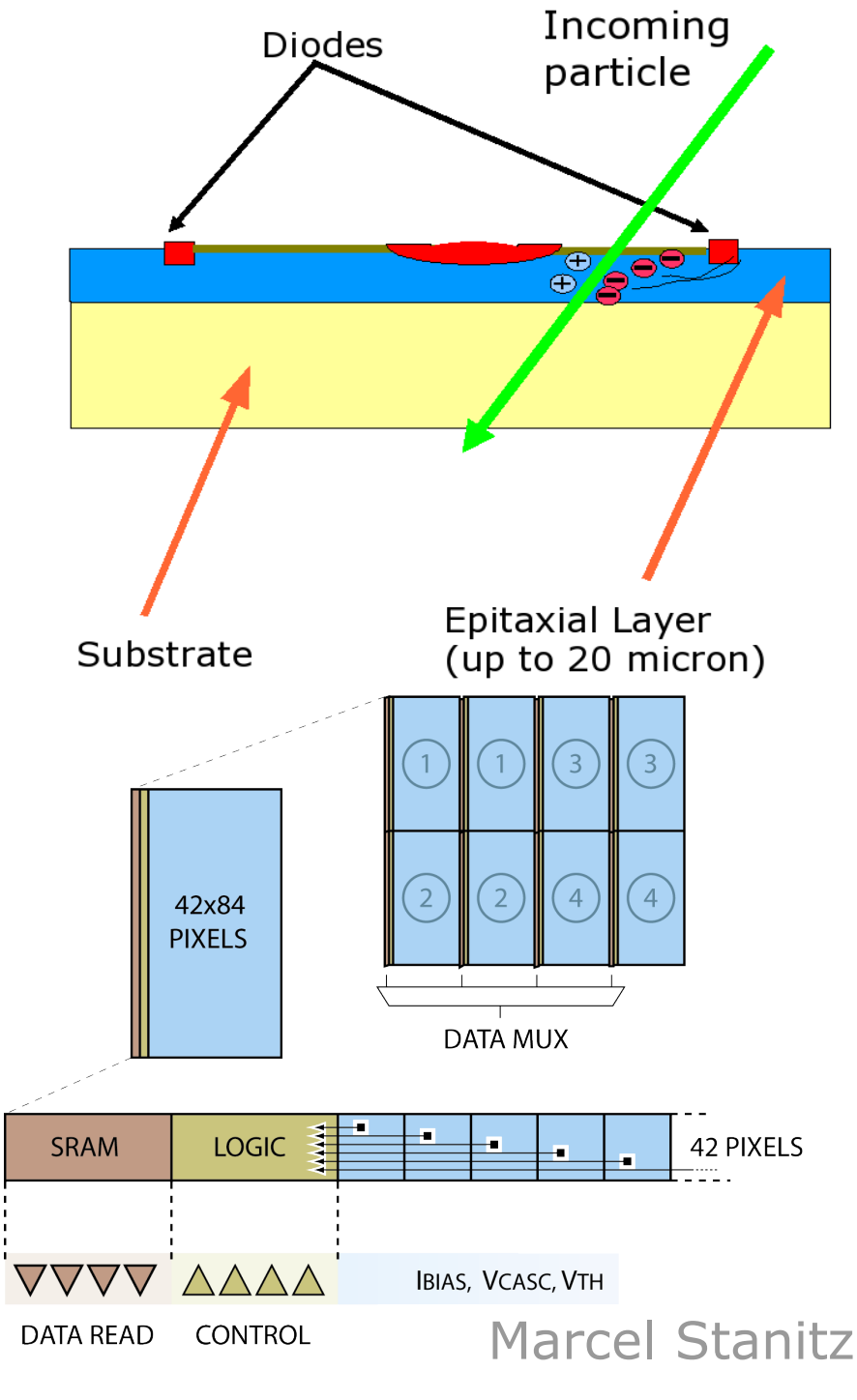
- Build on MAPS technology
  - Using Deep p-well process
- 50 x50 micron pixels
- Digital  ECAL
  - Operates as a shower particle counter
- First generation sensor has been manufactured
- 168x168 pixels, 8.2 million transistors





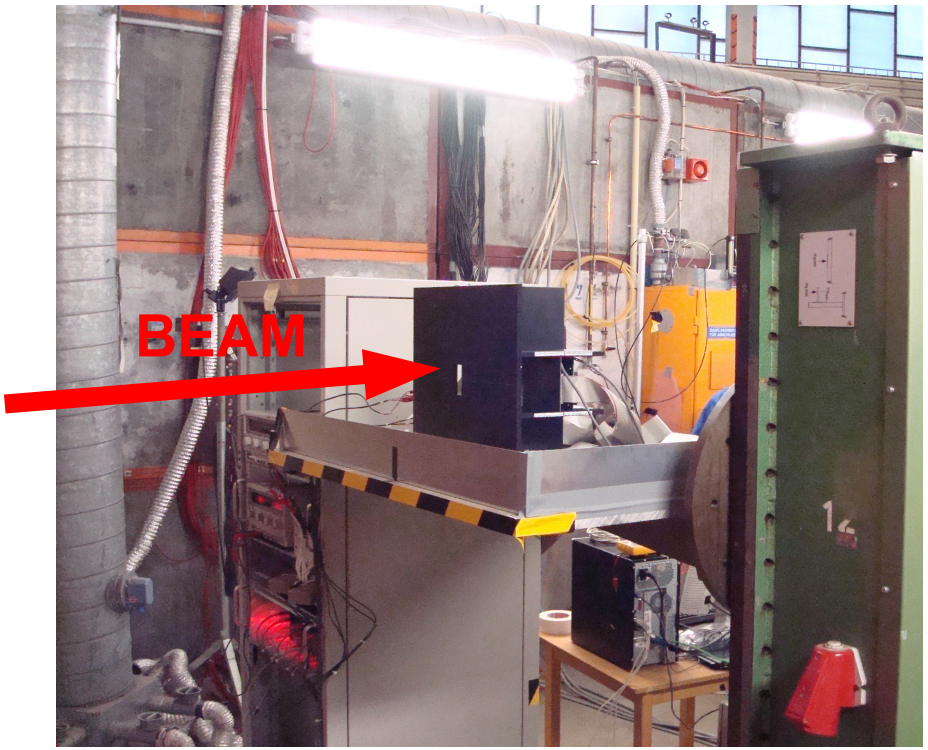
# Integrated Readout

- 28000 pixels
- Each pixel has
  - Amplifier
  - Comparator
  - Mask/Trim
- 42 pixels share (1 row)
  - SRAM memory
  - Logic
- Power pulsing



# Current Status

- First generation chip delivered
  - A technology demonstrator
- Testing has started
- Put in DESY Testbeam Dec 2007
- Started working on second iteration
  - using all input from 1st generation
  - design a more real world prototype



# The people involved

**ECAL Contacts**
**Ray Frey & David Strom**

**Traditional Silicon Diodes**

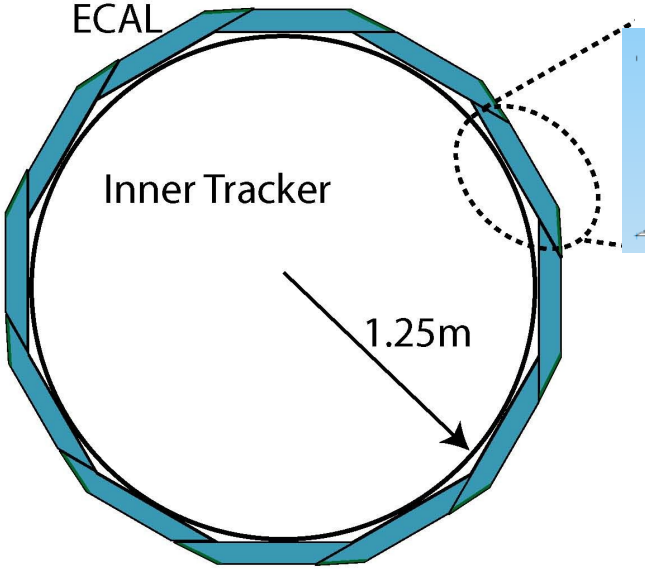
- U Oregon
- SLAC
- UC Davis
- Brookhaven
- LAPP Annecy

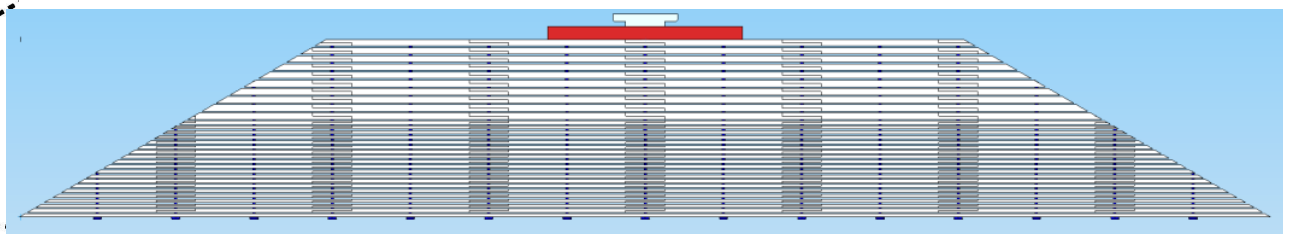
**TeraPixel**

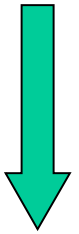
- RAL
- Imperial College
- U. Birmingham

# First mechanical design

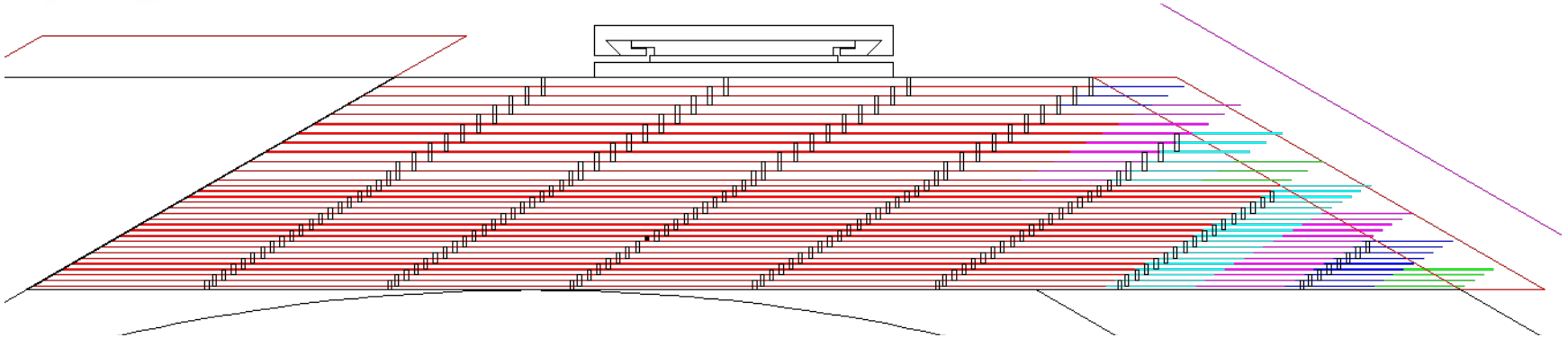
Si-W Calorimeter Concept





Marco Oriunno, SLAC



Only 2 Si sensor mask-sets required

# Where to contribute ?

- Hardware projects always welcome more interested parties
- Clearly have a lot of detector optimization to do as well
  - Needed for the LoI
- Two key areas where we severely lack effort
  - Optimize Detector Layout
  - Physics studies and benchmarks

# Detector Optimization

- Segmentation
  - How small
  - Use for Tracking
- Layers
  - How many layers
  - thickness ?
- Calorimeter depth (How many $X_0$)
- Hybrid Designs
  - 10 layers MAPS + 20 layers diodes
  - Benefits

# Physics

- What performance do we need for e.g.
  - Photon ID
  - $\tau$ id and analysis
  - Flavor tagging
  - Particle Flow
- Do physics studies to test ECAL performance
  - stau studies
  - $h \rightarrow \gamma\gamma$
  - $\tau$ polarization
  - more ideas ...

# How to get involved ?

- Talk to us during TILC08
- Contact the ECAL coordinators
  - Ray Frey and David Strom
- Come to our phone meetings
  - 2 pm (PST) / 10 pm (GMT)
- Come to the next SiD Workshop
  - 14-16. April , RAL http://hepwww.rl.ac.uk/SiDmeetingUK/
- Everyone is welcome !

# Summary

- From Ray Frey:
  - *The recent political choices in the U.S. and U.K. have thrown a monkey wrench in the works.*
- But still making good steady progress ...
- Still going strong for the LoI
- Always open for interested people
- Thanks to Ray Frey, John Jaros, David Strom, Mani Tripathi for comments & material