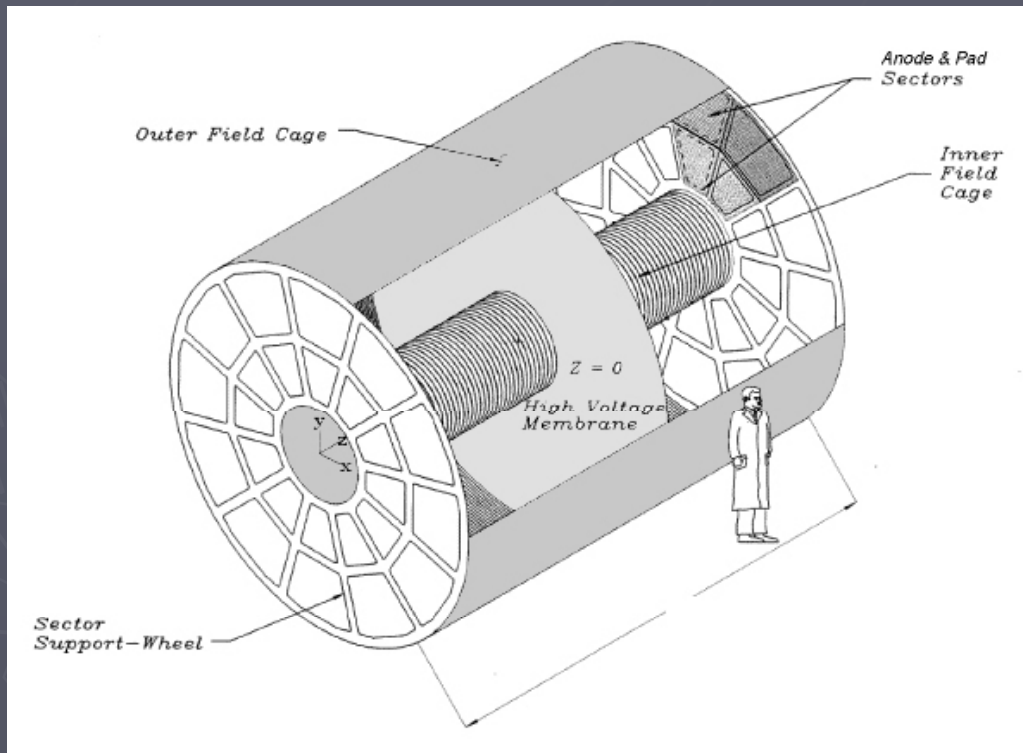


TPC Endcap Materials

Takeshi Matsuda
LC TPC Collaboration
IPNS/KEK
@TILC08
March 5, 2008

TPC: Basic Structure

Materials (and space) in the forward region

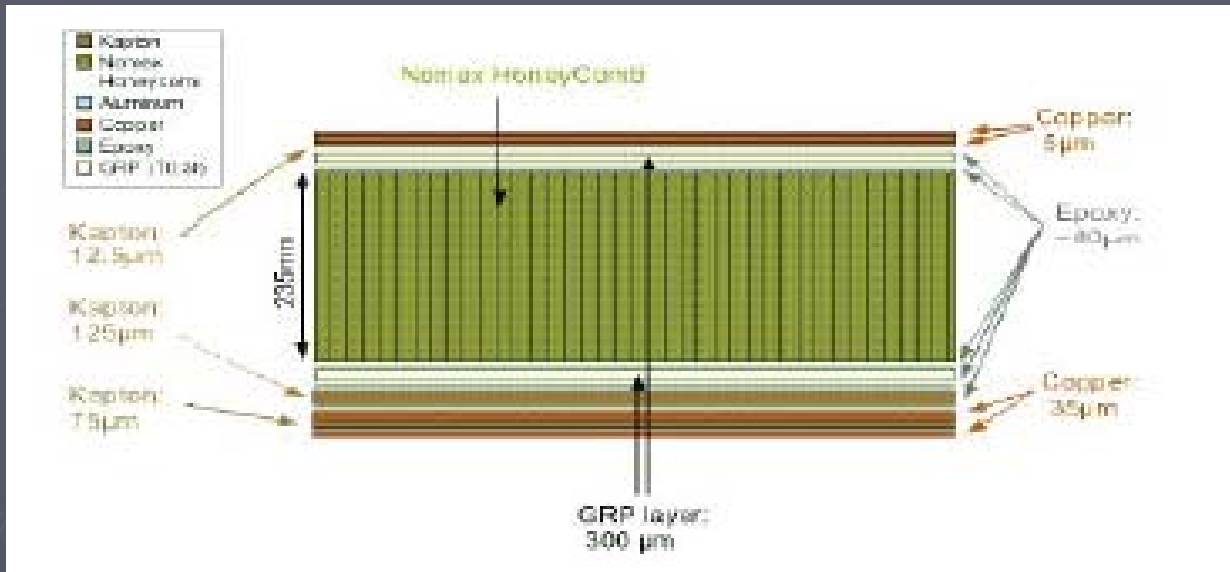


Field cage with the enforcement at the ends
Sector support structure (or End-cap)
Sector (or Detector module)
Front-end electronics
DAQ optical fibers
Power cables
Elements of cooling system
Devices for alignment
Support structures

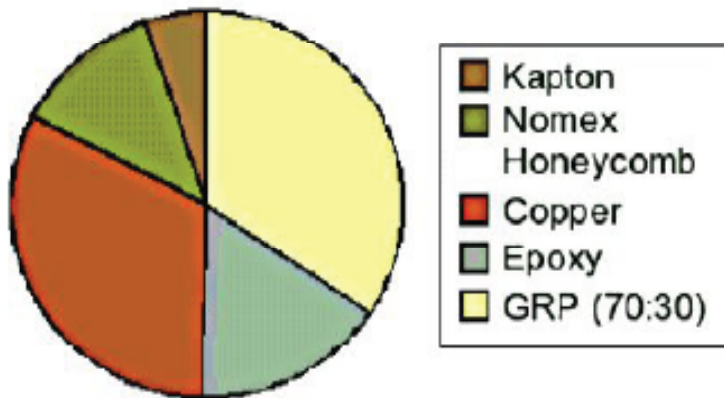
Warning: The numbers appear in this presentation are of a quick estimation by naïve physicists. Urgent to start engineering studies for each TPC elements.

Field cage

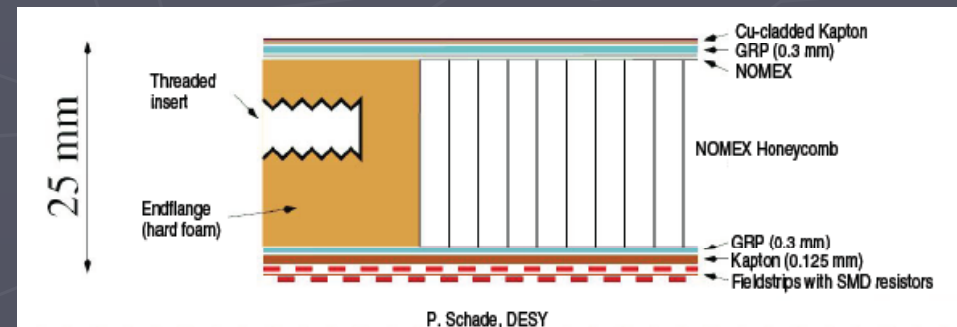
Field cage for TPC Large Prototype: Outer diameter = 770 mm
(May be a reference for the inner field cage of the LC TPC)



Radiation Length: 1.31% of X_0



Reinforcement at the ends

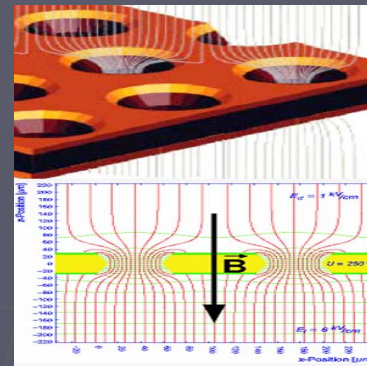
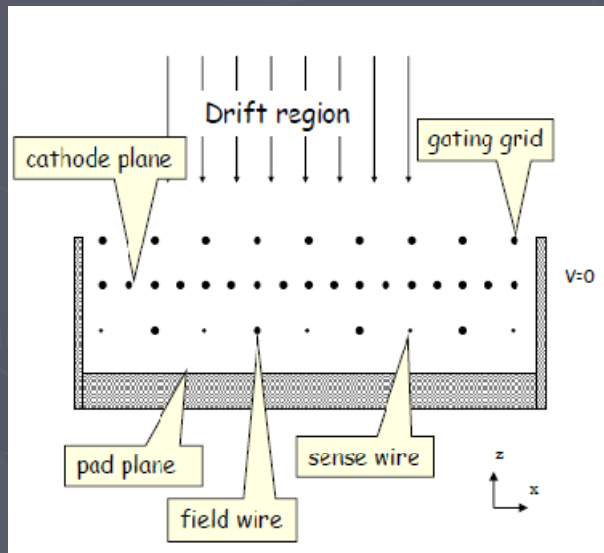


(Klaus Dehmelt at TILC08)

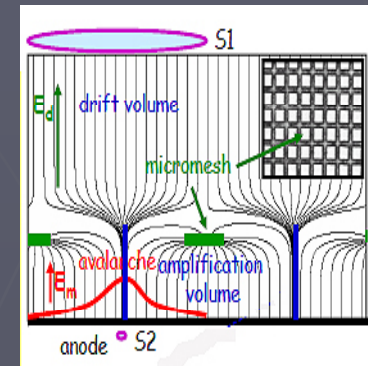
“Sector” (or Detector Module) at ILC

From the MWPC TPC to MPGD TPCs or Pixel TPC (SiTPC) at LC TPC

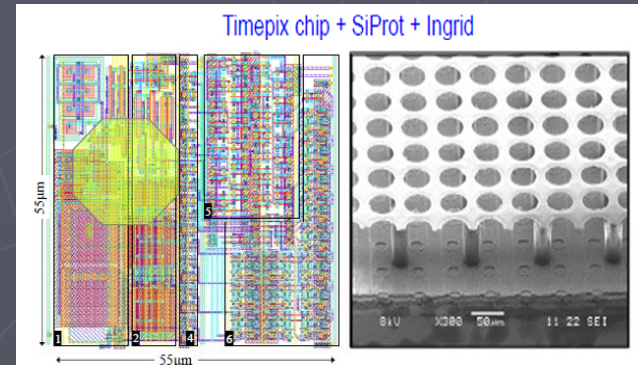
MWPC TPC



Multilayer GEM
with narrow pads



MicroMegas with
resistive anode

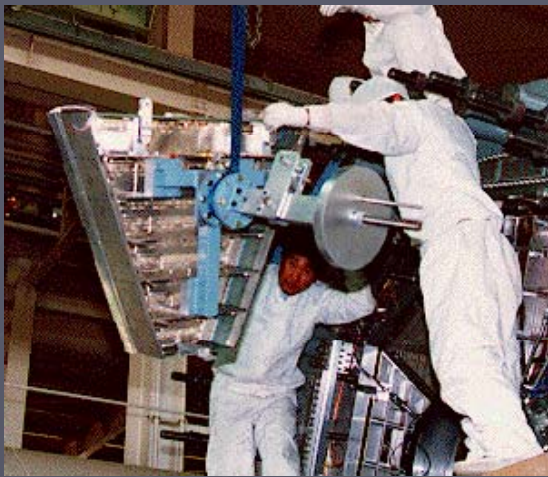


SiTPC

Not stretching wires

→ Lighter detector module with the new MPGD/SiTPC in principle.

Some Images of MWPC TPC in 80s and 90s



1980s (TOPAZ TPC sector)



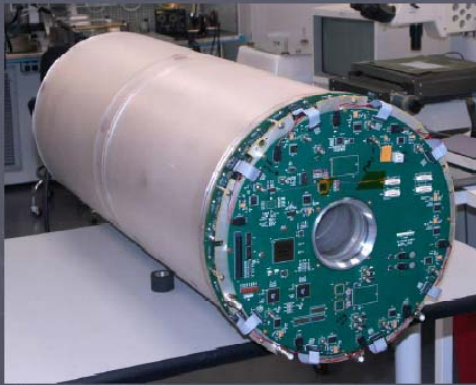
1990s (STAR TPC sectors)



Also cables (ALEPH)

Small but New MPGD TPC

LEGS TPC



Digital readout and control board

End-detector:

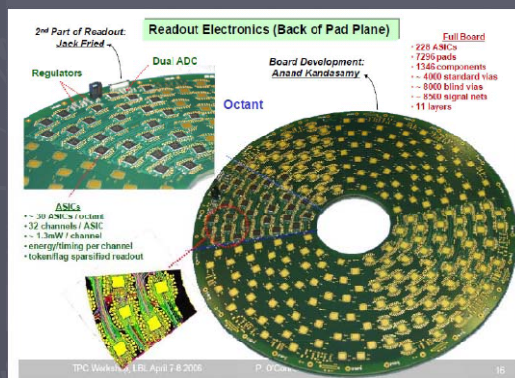
MWPC → MPGD (& SiTPC)

Electronics:

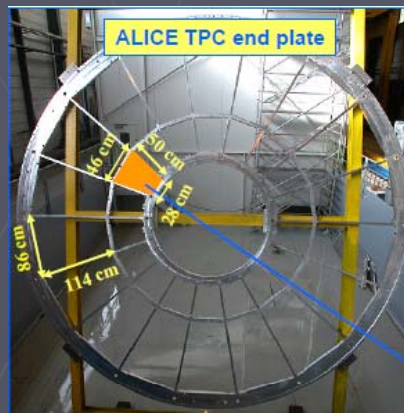
- Custom mixed-analog-digital chips of finer rule.
- Surface mounting on the back of the pad plane
- High speed optical link

LEGS TPC

Direct Mount of Front-end Chips on the Back of the Pad Plane



Geronimo, J. Fried, A. Kandasamy, V. Radeka, & Bo Yu, TPC Application Workshop, LBL, 2006



But still the “old” issues:

Power cables

Cooling

Endplate structure (Mechanical)

Wire bonding @LEGS TPC
→ Bump bonding @ ILD TPC

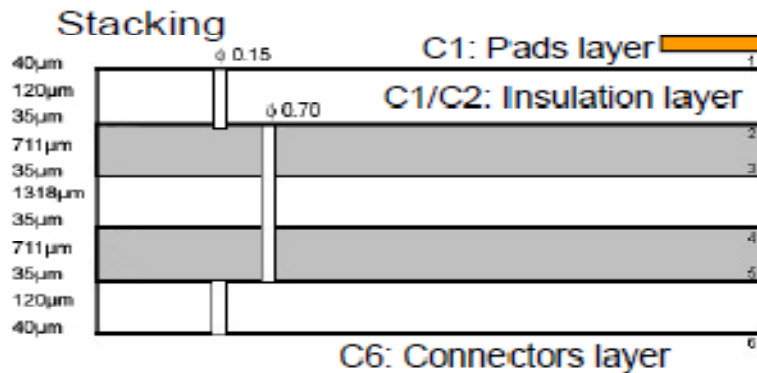
Al → Be, CFRP or a lighter material @ILD TPC

MicroMEGAS Panel for LP1 Test

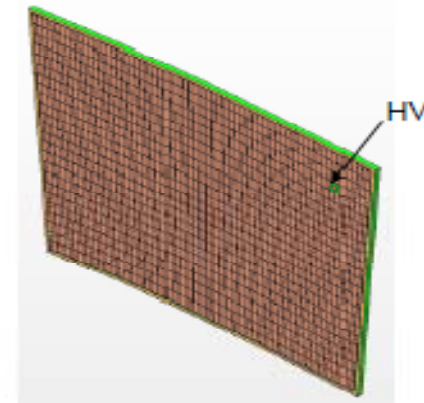
Cu: 220 μm
 G10: 2980 μm
 +
MicroMEGAS
 +
Resistive anode

(Signal routing
 Should be simpler
 for the
 flip-chip mount)

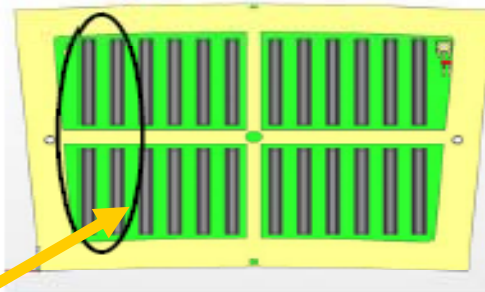
Micromegas Panel: PCB



24 lines of 72 pads: 1728 pads with 2 used for supplier the HV to the grid.
 Routing in progress.



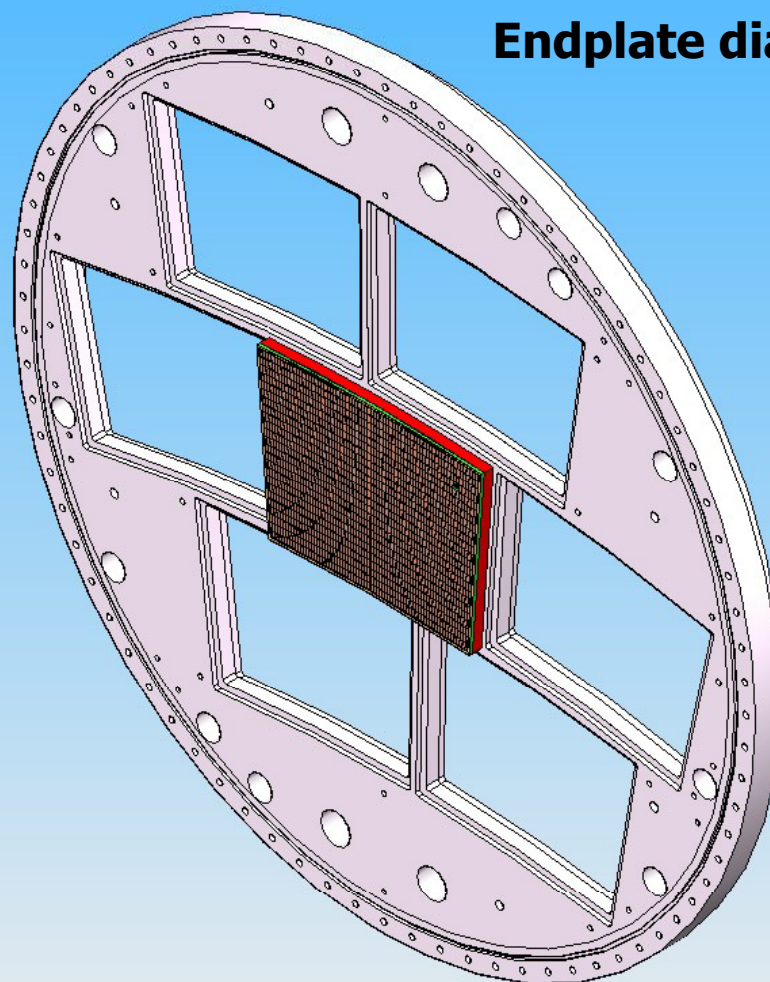
18 connectors of 80 pins: 4 are used by FEC



The layers of insulation are Nelco 7000 (Polyimide:Glass Transition Temperature = 260°C): necessary for the resistive layer

(The connectors and the front-end cards should be replaced by the direct mounting of readout electronics for the LC TPC. But then the material for cooling such as a special metal layer for in the PCB may become needed.)

MicroMEGAS Panel Mounted on the LP1 Endplate

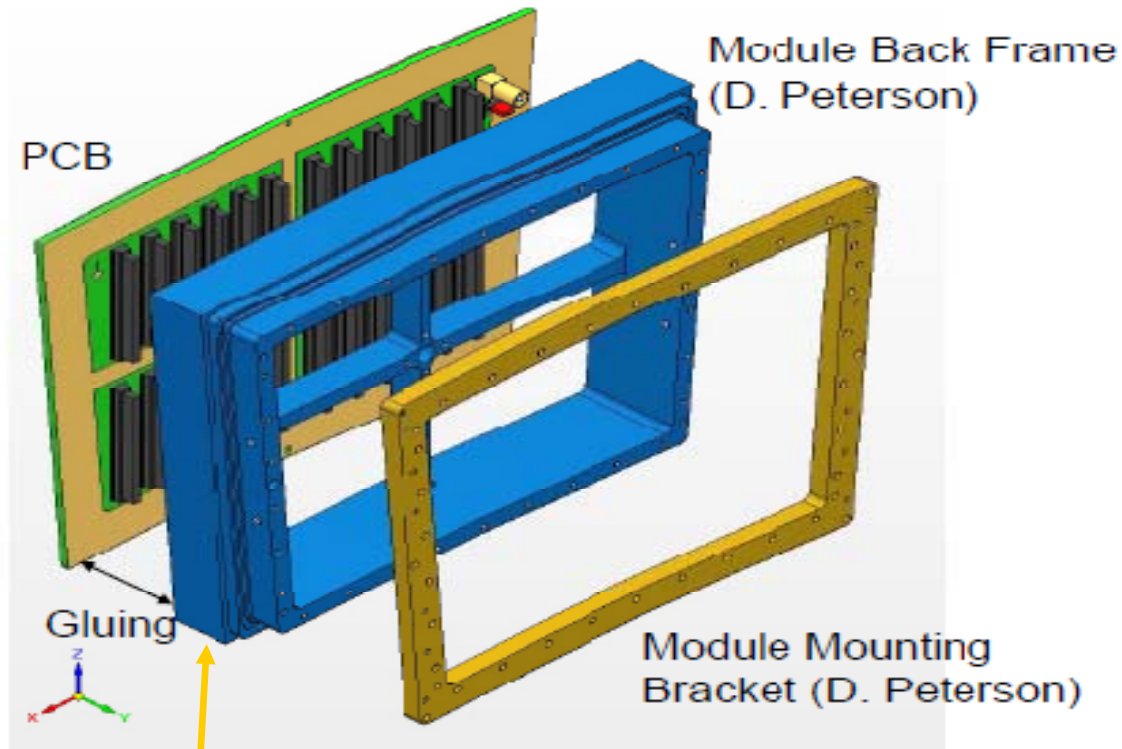


Endplate diameter: 76 cm

No real consideration to thinning the endplate

MicroMEGAS detector module: LP1

Micromegas Panel: Mechanical group



(The blue back frame is intestinally thick to adjust the height to the GEM module with the gating GEM. No real effort to minimize material for LP1 test.)

LC TPC

After the Larger Prototype test of the new TPCs at DESY (LP1 test: 2008-2009), some of the important issues may still remain:

- **TPC sector (detector module) readout by mixed-analog-digital electronics by finer design rule directly mounted on the back surface of the pad plane.**
- **Electronics cooling and power delivery**
- **Optimum design of the endcap with light material.**
- **Overall engineering design of LC TPC**

Need to start the studies urgently, getting resources, to start the studies urgently, getting resources, then,

ALEPH/TESLA: 30% X_0 (material) & 25 cm (the distance to the forward detector)

→ ILC TPC: 15 (→ 10) % X_0 & 15 (→ 10) cm ?

Surface-mounting Electronics for LC TPC

The area (die size) of mixed-analog-digital chip, extrapolated from a general purpose amplifier chip prototype and the ALTRO chip, is expected to be small enough for 1- 3 mm x 4-6 mm pads of the GEM TPC and the MicroMEGAS TPC.

Considerations on readout plane

IC Area (die size)

Luciano Musa

- 1-2 mm² /channel
 - Shaping amplifier 0.2 mm²
 - ADC 0.6 mm² (estimate)
 - Digital processor 0.6 mm² (estimate)
- in the following we consider the case of 1.5mm² / channel
- 64 ch / chip ➔ ~ 100 mm²

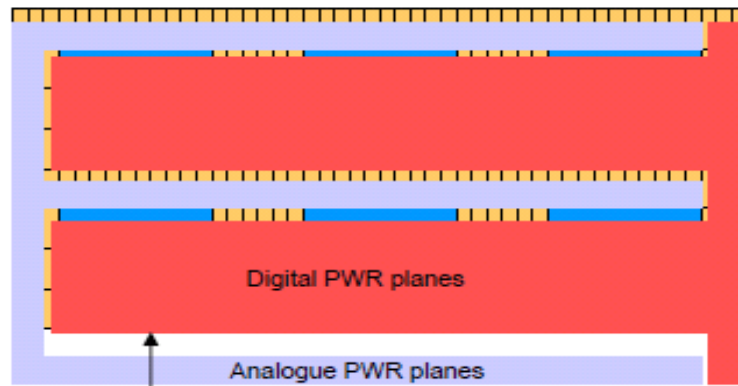
Area of the chip on the PCB: 14 x 14 mm² / chip ⇔ ~ 3 mm² / pad

PCB dimensions < 40 x 40 cm² ⇔ ~53000 pads, ~800 FE chips / board

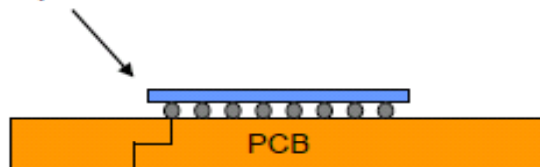
MPGD Pad Plane with Flip-chip Mounted Electronics

Considerations on readout plane

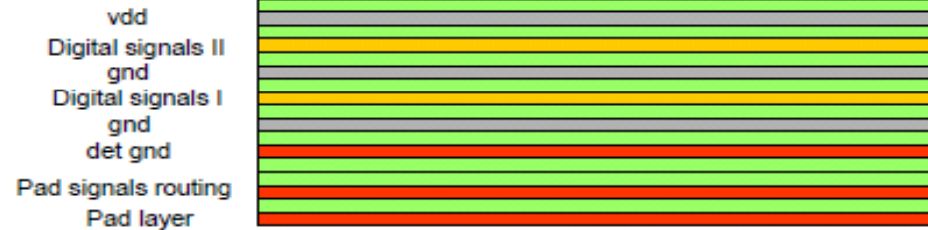
PCB topology and layer stack-up



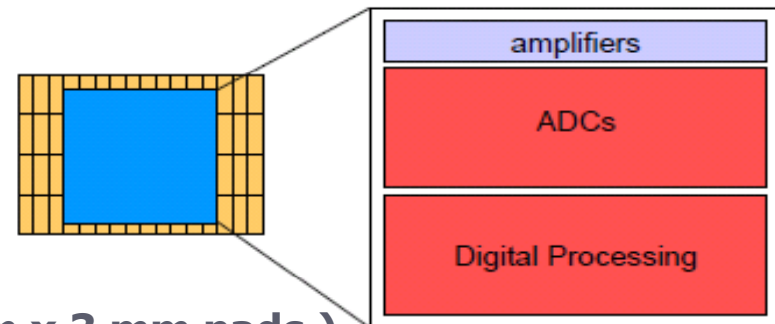
Flip-chip mounted



8-layer PCB



Chip floorplan



(Note that this is an extreme case with 1 mm x 3 mm pads.)

Surface-mounting Electronics

Need to get a complete scheme of LC TPC electronics:

- **The signal processing on board (the endplate or in TPC) has to be defined, and**
- **The data link between the chips and the optical link from TPC have to be integrated in the designs.**

-> Need more space on the endplate, or we may have another idea (3D chip). The power of the fast optical link may be an issue.

Surface-mounting Electronics

Considerations on readout plane

Luciano Musa

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1% ← power switching/power delivery
- average power / channel ~ 0.5 mW / channel
- average power / m² 167 W ← cooling

- **The power delivery network with capacitors** has to be examined to avoid the large transient spikes to destroy the front-end electronics (See the slides by Luciano).
- **The cooling:** May need special cooling method of the PCB board to prevent the heat to go into the TPC gas volume via bumps. Need to prepare for accidents such as the failure of the power cycling, latch up etc).

Material Thickness: TPC Endplate with the surface mounting electronics (Almost Pure Guess!)

Thickness (radiation thickness)

MicroMEGAS Mesh	$X_0 = 1.76\text{cm}$	0.002cm	→ negligible	
Pad plane:				
G10	$X_0 = 19.4\text{cm}$	0.4cm	→ 2 %	
Cu	$X_0 = 1.43\text{ cm}$	0.03cm (8 layers)	→ 2 %	
Chips (Si)	$X_0 = 9.36\text{cm}$	0.05x2 cm x 1/3	→ 0.3 %	
Bumps			→ ?	
<u>Subtotal</u>				<u>5 %</u>
Power cables/buses and large electronics components			→	<u>?</u>
Endplate (mechanical) : Scaled from ALEPH (Al)	$= 13\%X_0$			
Be	$X_0 (\text{Be/Al}) = 4$			
	Strength (Be/Al) = 4		→ ~ 1%	
CFRP	$X_0 (\text{CFRP/Al}) = 1.5$			
	Strength (CFRP/Al) = 2		→ ~ 4%	
				<u>5 %</u>
Cooling (piping)	$X_0 (\text{Al}) = 8.9\text{cm}$	0.2cm	→ 0.2%	<u>1%</u>
Others				<u>?</u>
<u>Total</u>				<u>15 %</u>

(*) Including the additional cooling layers.

Conclusion

A Slide from the LC TPC meeting at ALCPG07

Advanced Endplate

My conclusion and proposals

A systematic R&D of the PCB pad plane with flip-chips electronics is urgent.

A basic design of the whole readout electronics including data transfer.

**A design of the pad PCB plane with the flip-chip assembly.
Simulations of power delivery, cooling and thermo mechanical features, and**

Tests of pad PCB plane models mounted with dummy chips.

**We need a group of electronics/mechanics experts together with some LC TPC physicists to work on the R&D systematically.
(Luciano seems to be too busy to lead this task by himself, which is unfortunate for us) (*)**

Also urgent is the mechanical design of the TPC and TPC endplate.