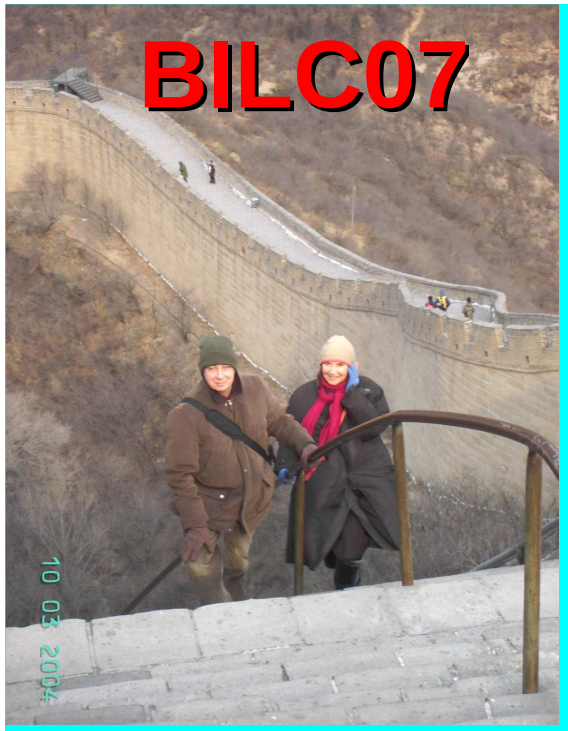


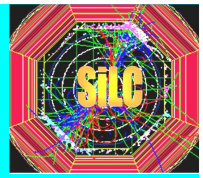
SiLC: What's new?

Progress since BILC07

on behalf of SiLC Collaboration

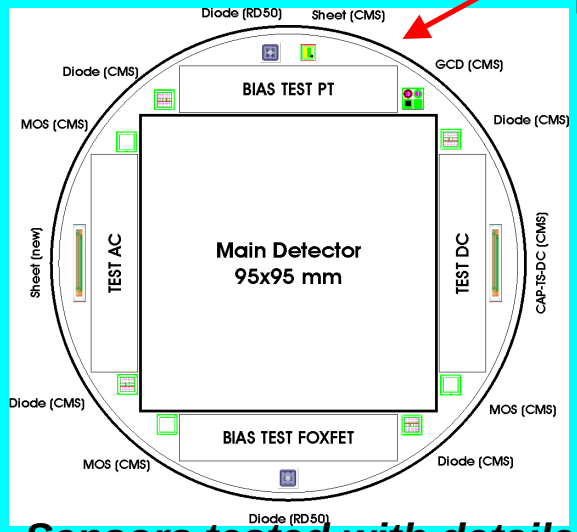
R&D sensors
R&D Electronics
Mechanics
Tests
What's next

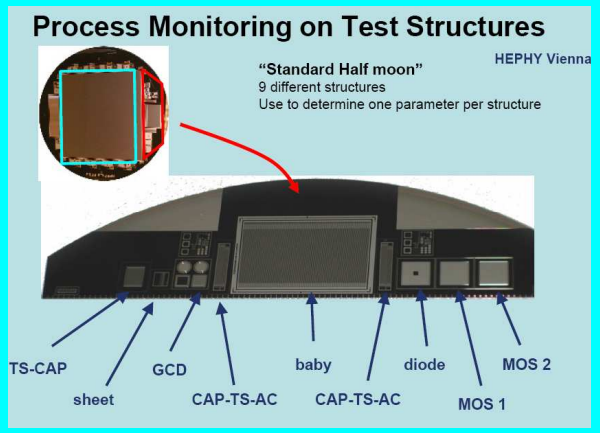
Aurore Savoy-Navarro, LPNHE/CNRS-IN2P3

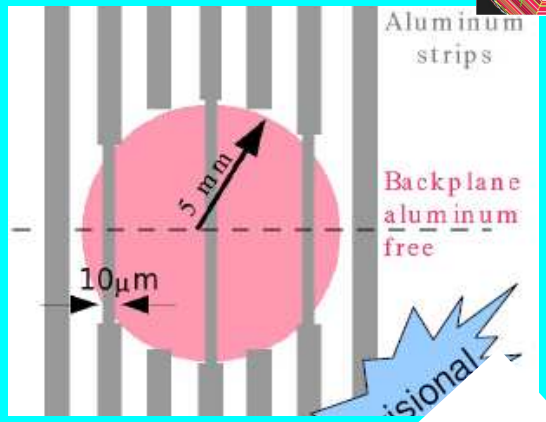


- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beam

Presently new: HPK μstrips, **6'' wafer, but:**
pitch=50μm; thickness: 320μm; Length: 9.15cm,





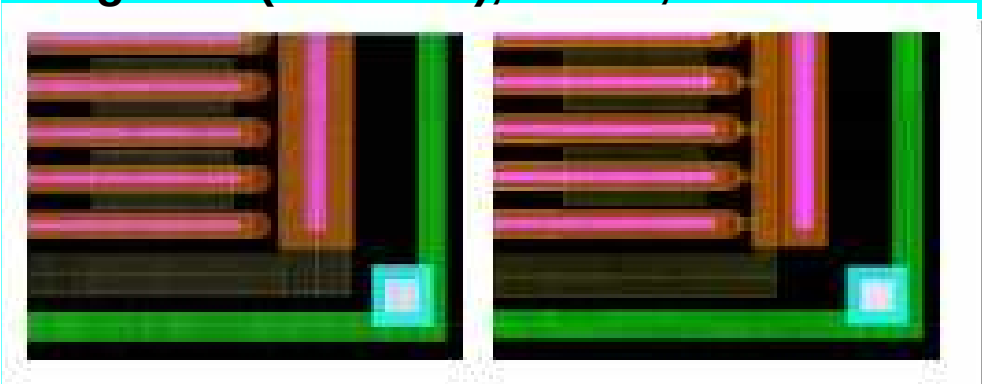


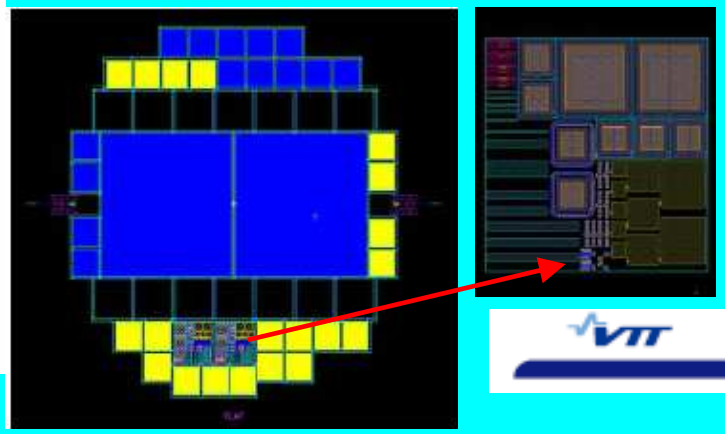
Test structures

5 sensors specially treated for laser alignment

Sensors tested with detailed QA control (HEPHY+IEKP)

New technological approach: 3D Planar μstrips:
Edgeless (hermetic), Low V, Lower Thickness, Faster, Rad hard, expected 03/08





The biaising schemes for the ILC tracker's edge active strip Detector (left) punch through, and (right) FOXFET The detector Is biaised from one corner of the active edge (green)

And also pixels:

SiLC has been proponing since its start to let open the possibility to use pixels in certain region:
Presently considered

1) Pixels for the very forward zone nearby the vertex detector
2) Pixels in the overall internal region both central barrel and all very forward disks meaning an extension of the vertex region
3) Further on??? (see C. Damerell and Stepanov)

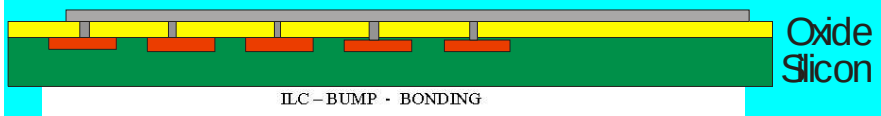
The developments are done within the present vertex detector R&D collaboration.
The main emphasis is on DEPFET because of the people from SiLC collaborating also this R&D activity (IFIC-Valencia and CU Prague mostly)
There is also a growing interest on the 3D pixel technology, starting from the expertise at CNM-IMB/CSIC and VTT and other teams now joining.

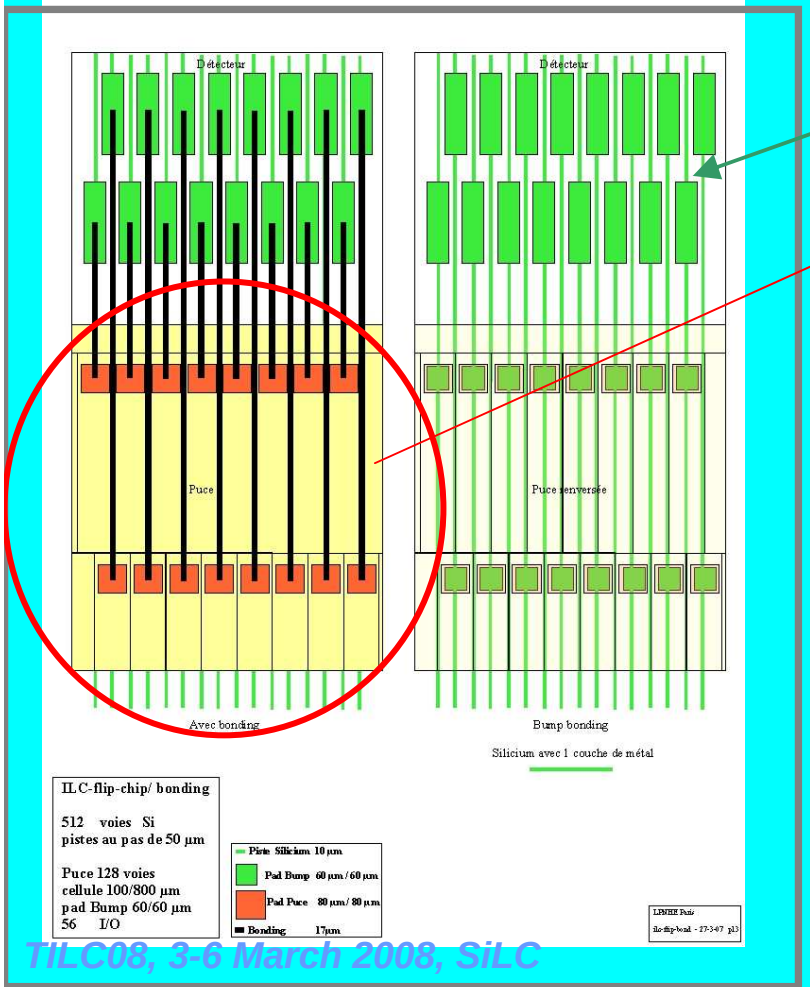
The possible use of pixels will be also an important factor to be taken into account in the optimization studies.

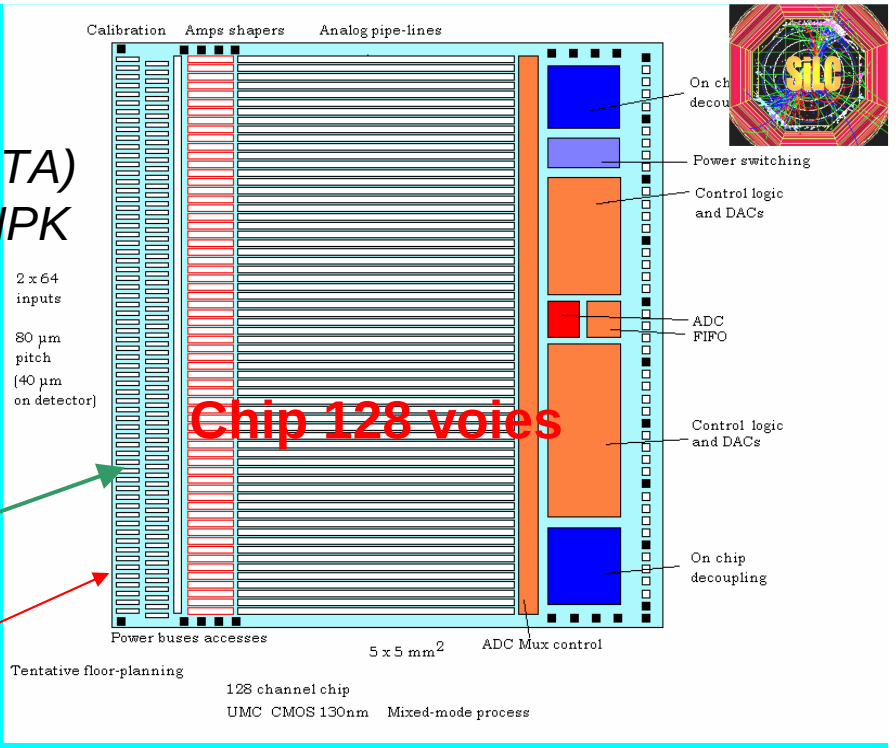
COLLABORATION HPK/LPNHE-IN2P3

Goal: develping new routing and inline pitch Technology for FE chip onto the strips(NdA + MTA)

1st try: SiTR_130-128 chip and presently new HPK sensors







Decrease %X_0: NO hybride & pitch adpater

1st approach (2008-2009):

Chip directly routed onto the strips by bump bonding

HPK: sensor + bonding of the chip

IN2P3: chip 128 voies

performance tests comparing

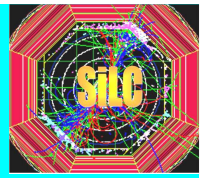
new connection wrt hybrid

Demonstrator: 2008, production 2009

Chip bonded sensors at the price of usual sensors

Futur: Technologie 3D for µstrips &/or connection chip/µstrips

First step: I/O layout

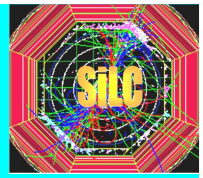


- R&D on sensors
- R&D on electronics:

HEAD ON THE NEW SiTR-130_96

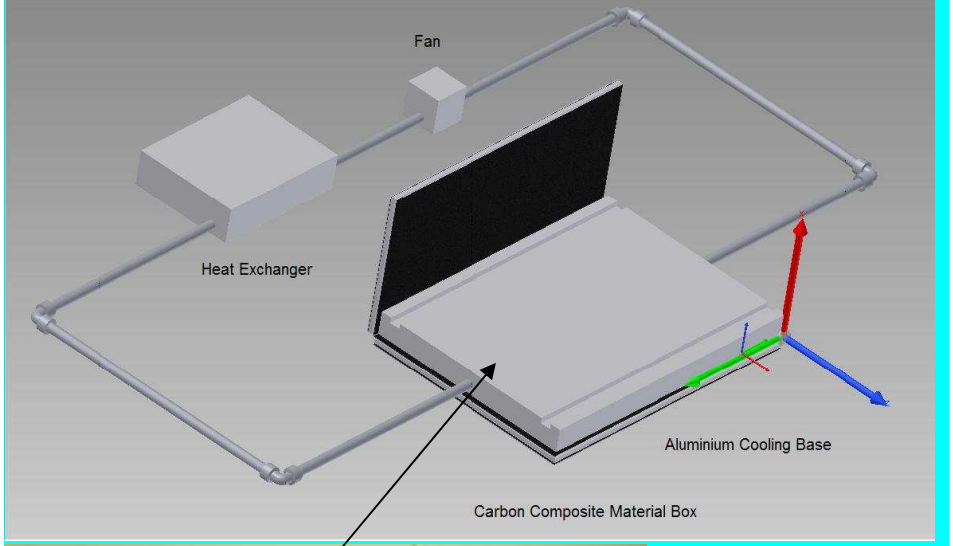
- Mechanics developments
- Test beams

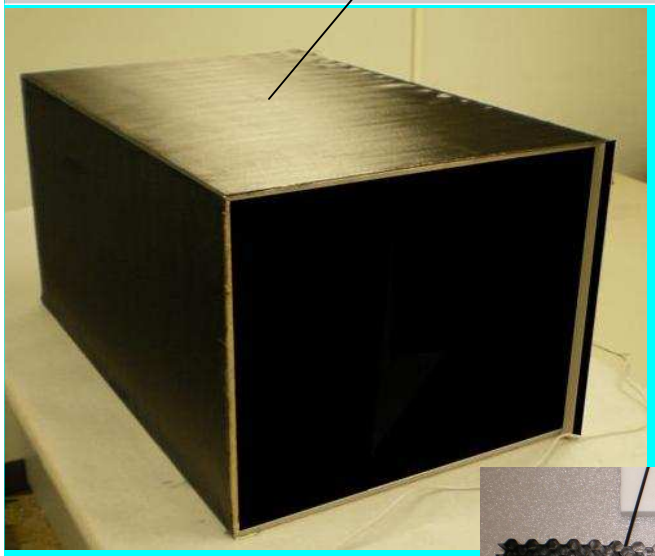
(See next talk on Electronics)



- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beams

Air dry cooling system (OSU) or just an insulating frame



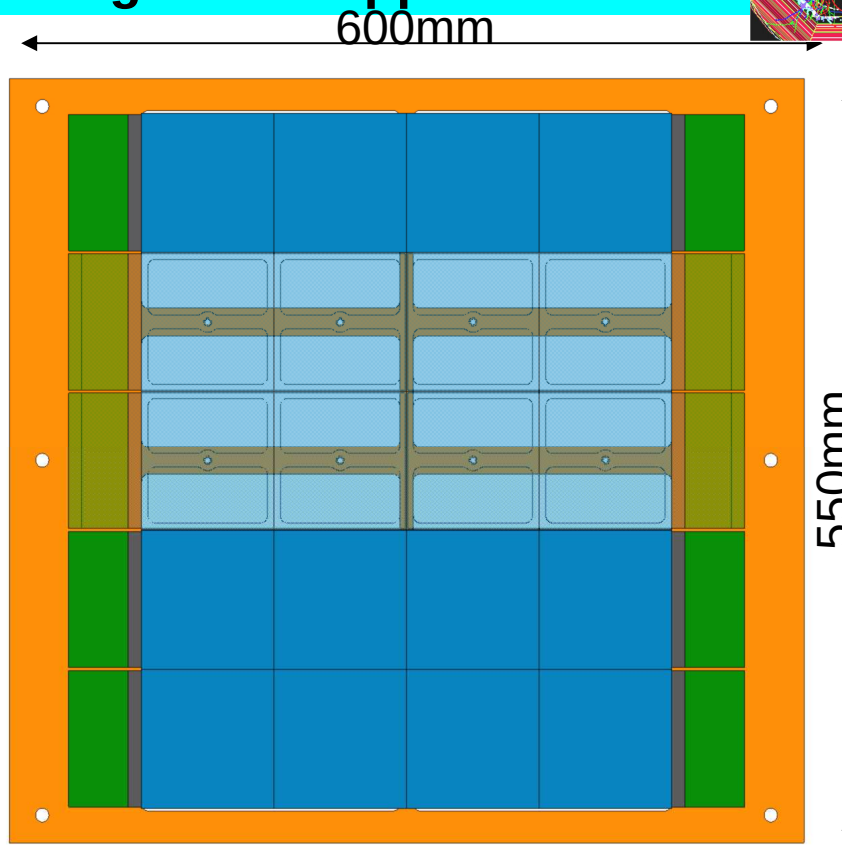


C composite material insulating box

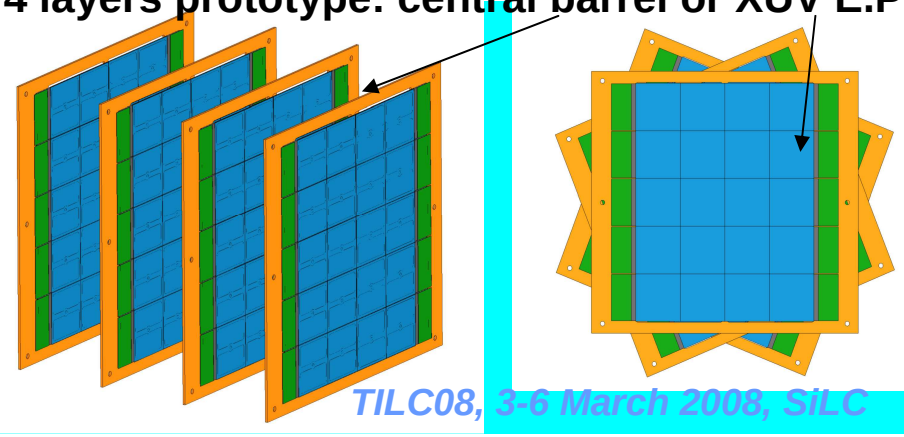
Double-sided honey-comb Carbon composite material

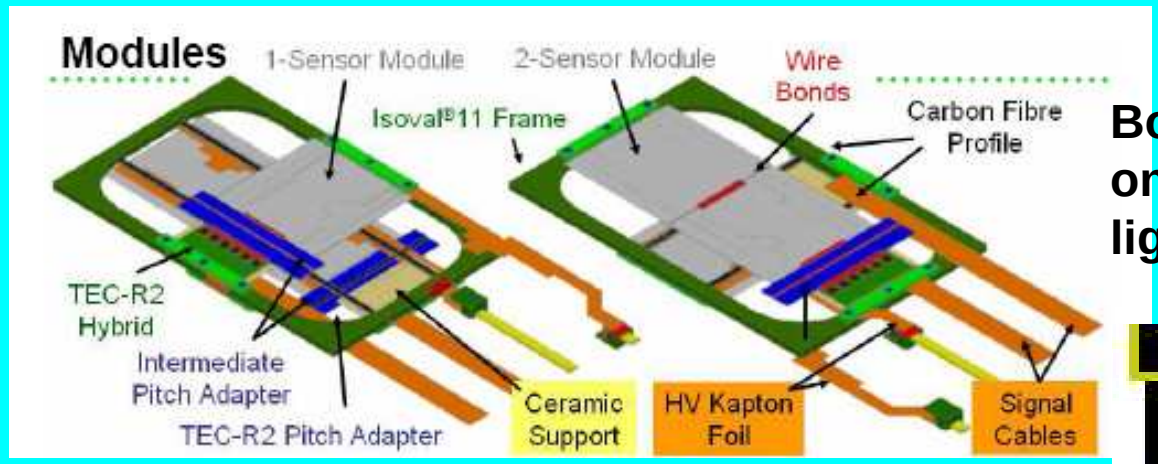
Prototypes for test beams:

- **Large size support structure**

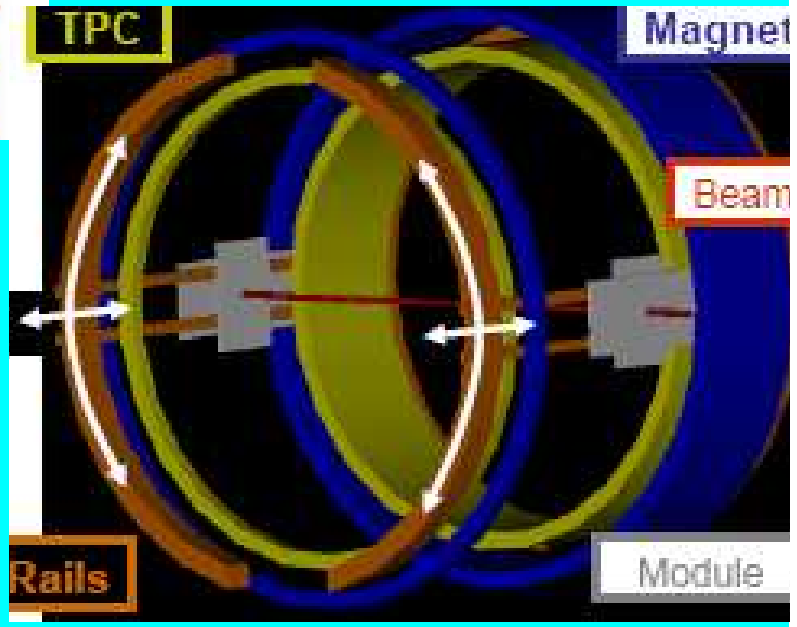


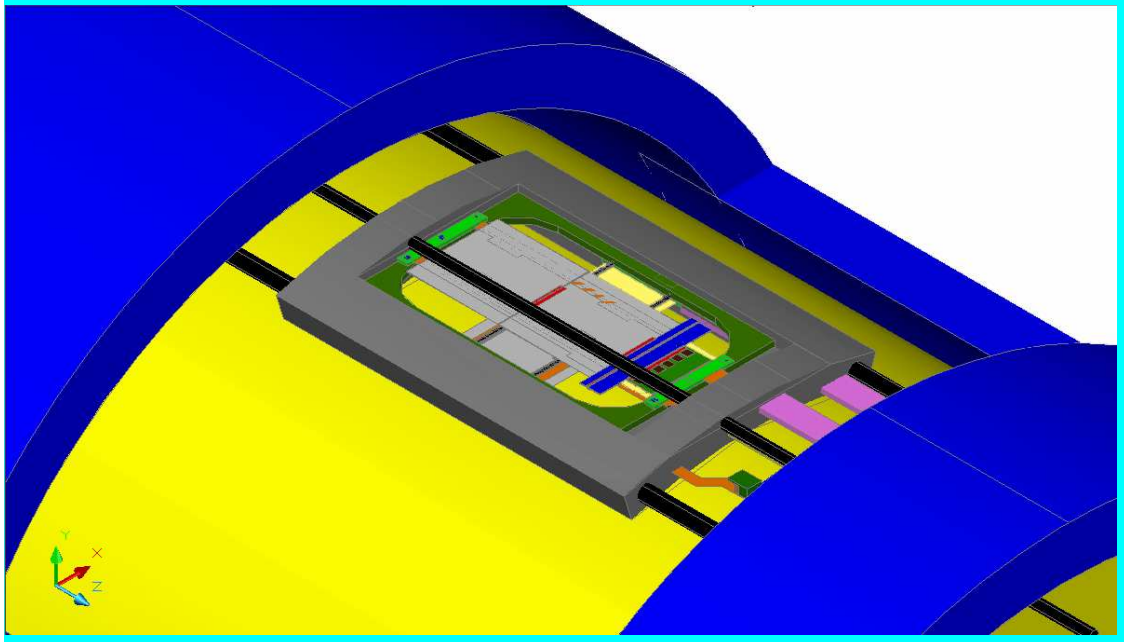
4 layers prototype: central barrel or XUV E.P.





Both prototypes include working on new modules starting with lighter module structure at first .





Test with of the Silicon Envelope with LCTPC in 2008 at DESY: Modules(HEPHY), structures(IEKP) final electronics (LPNHE)

Alignment: 2-fold approach

(see A. Ruiz's presentation

Instituto de Física de Cantabria

and CNM/CSIC

AMS-like approach:

baseline version: Minimum set of changes for any SiLC sensors

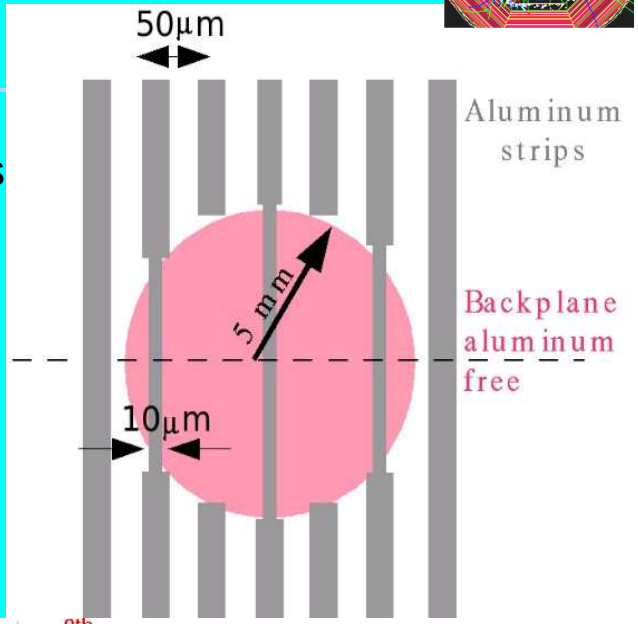
For instance, for the new HPK sensors

Implemented:

- ∅~10 mm window where Al back-metalization has been removed

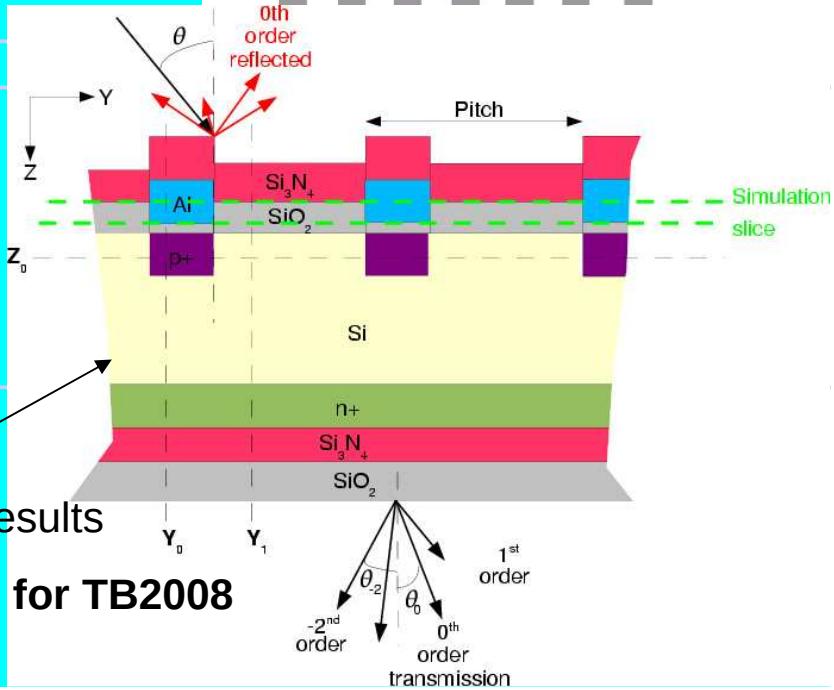
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)



R&D on transparent Silicon µstrip sensors:

- Together with IMB-CNM (Barcelona) design, build and test new IR-transparent Silicon microstrip detectors.
- Consider option of aluminum electrodes or transparent electrodes

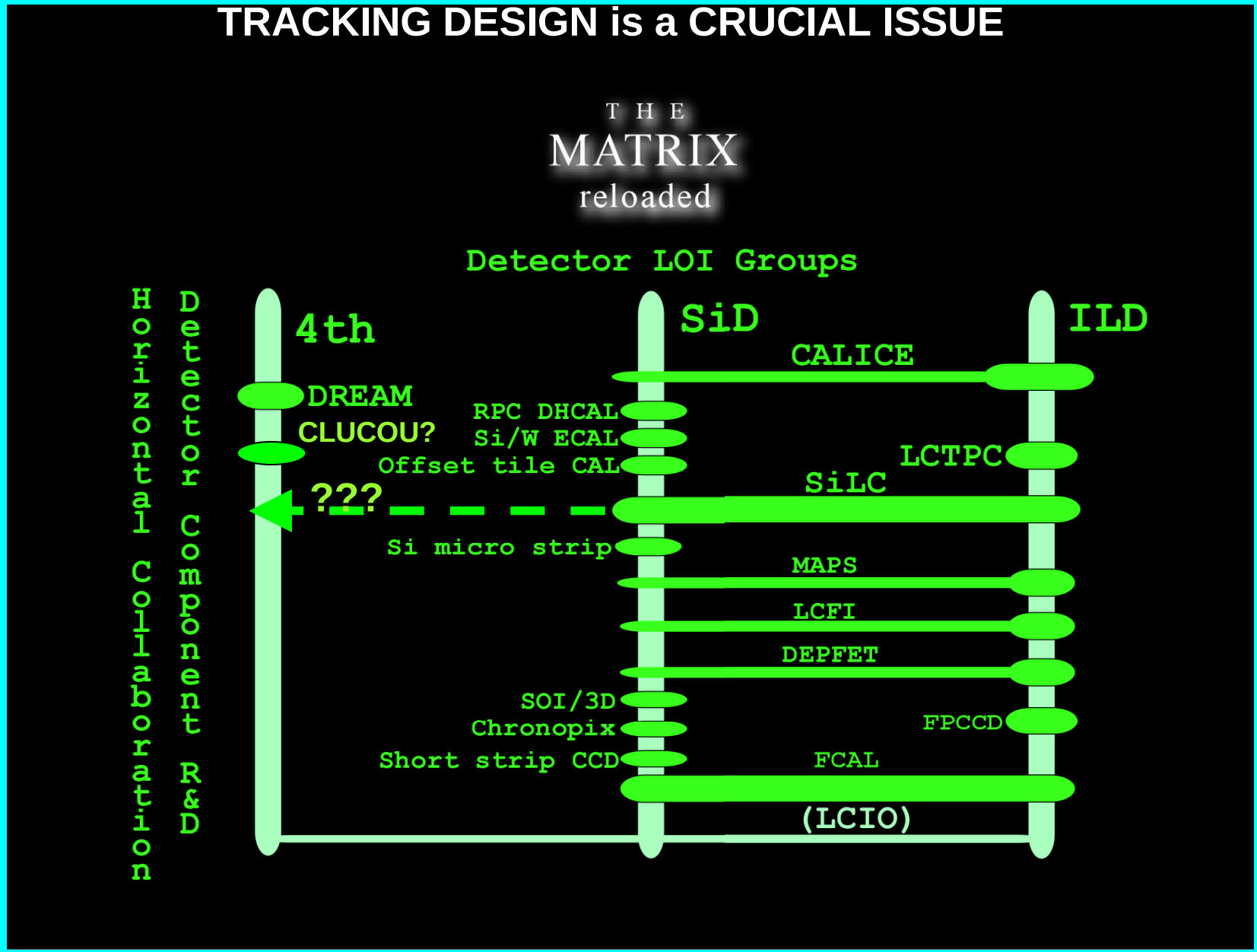


Realistic sensor simulations: very interesting studies/results

Test bench in development and alignment prototype for TB2008

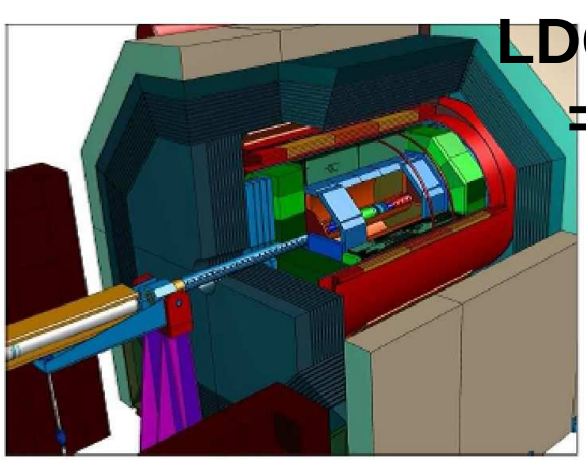
INTEGRATION & OPTIMIZATION:

TRACKING DESIGN is a CRUCIAL ISSUE

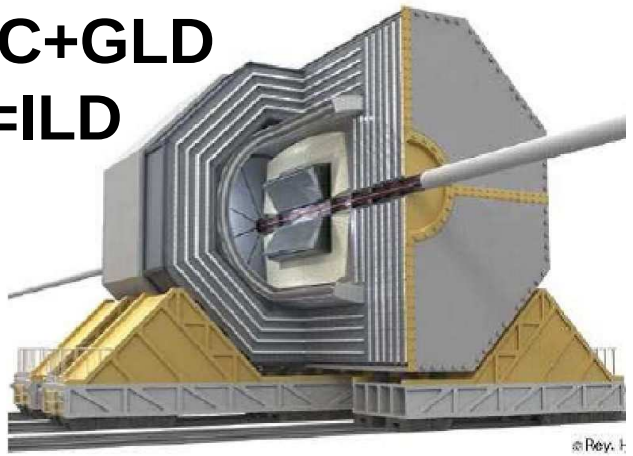


By courtesy Yasuhiro Sujimoto

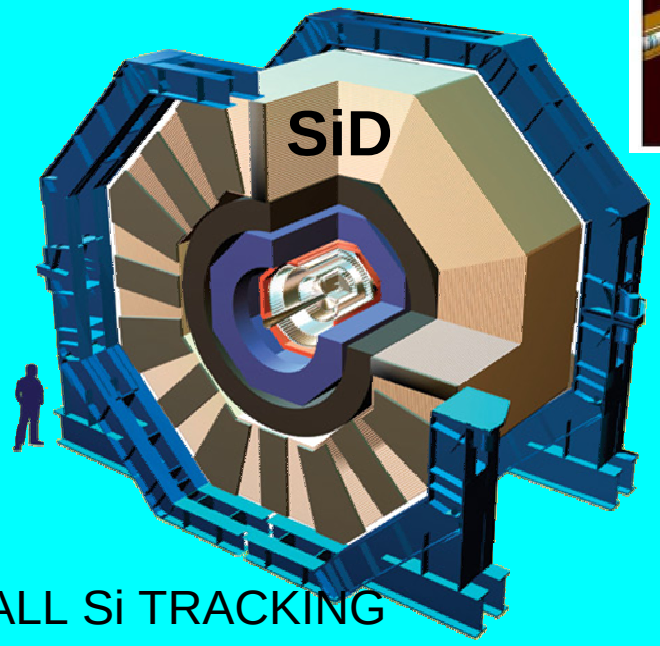
ALL (MOST) DETECTOR CONCEPTS INCLUDE SILICON TRACKING



LDC+GLD =ILD

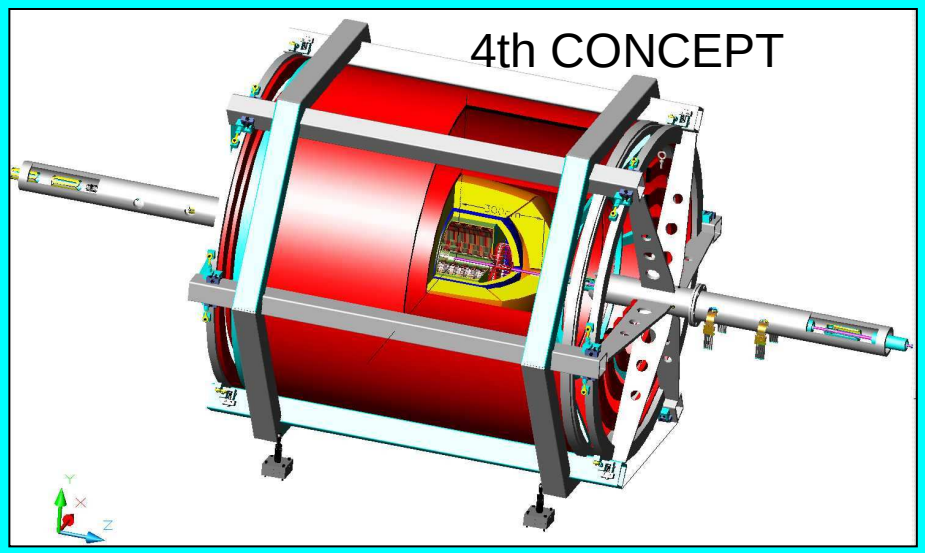


TPC+ Si TRACKING



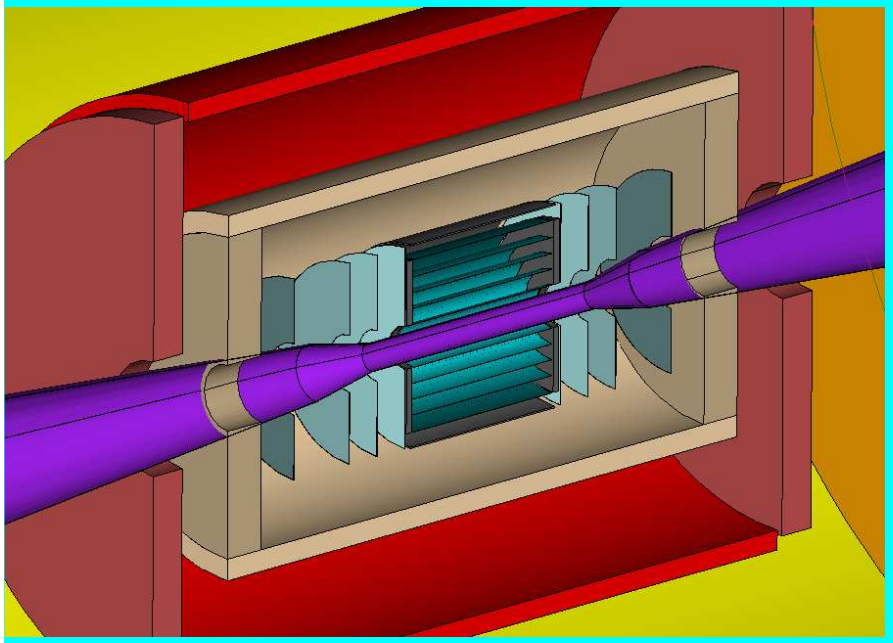
ALL Si TRACKING

Main goals:
Best performances and
Lowest %X0 everywhere
(or quasi everywhere)

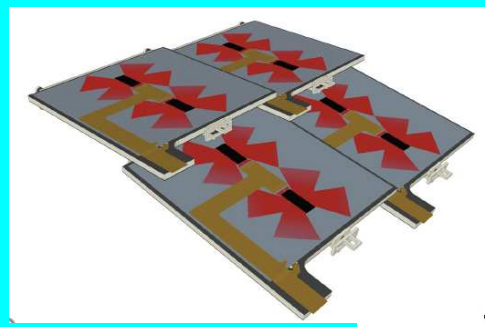


GASEOUS CENTRAL TRACKER?
(+ Si tracking? What Si tracking)
ALL SILICON TRACKING ?

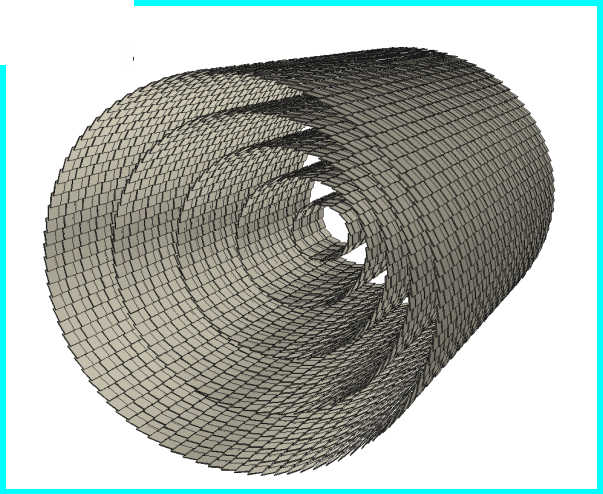
Q1: all silicon versus hybride gaseous + Silicon

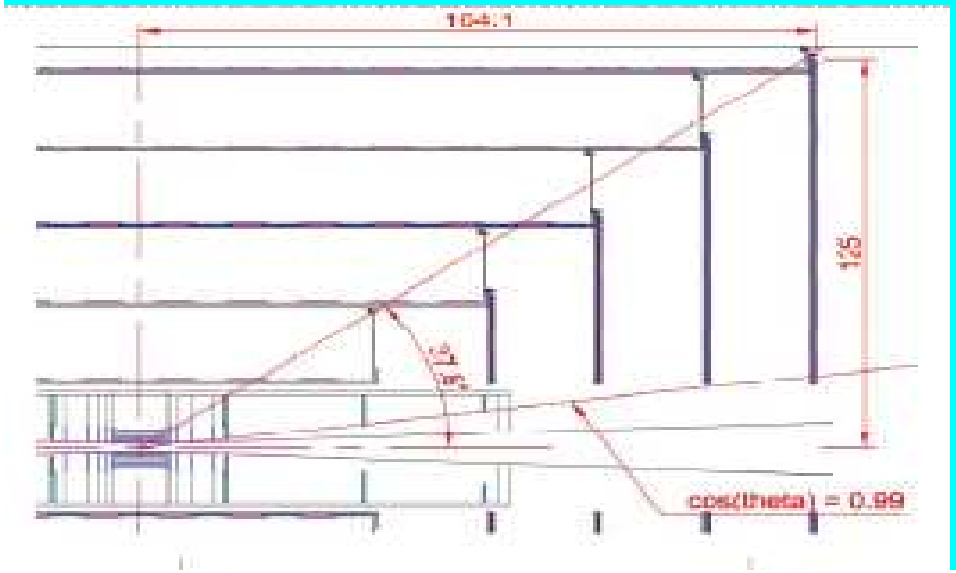


The SiD tracking integrated concept

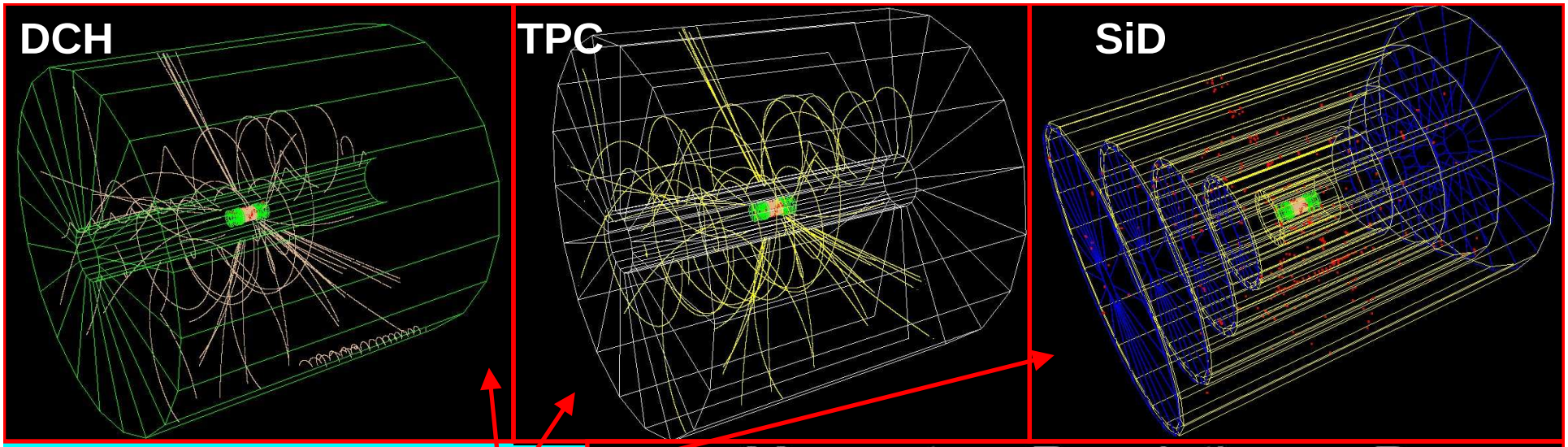


From microstrips tiles
to the all-pixel variante





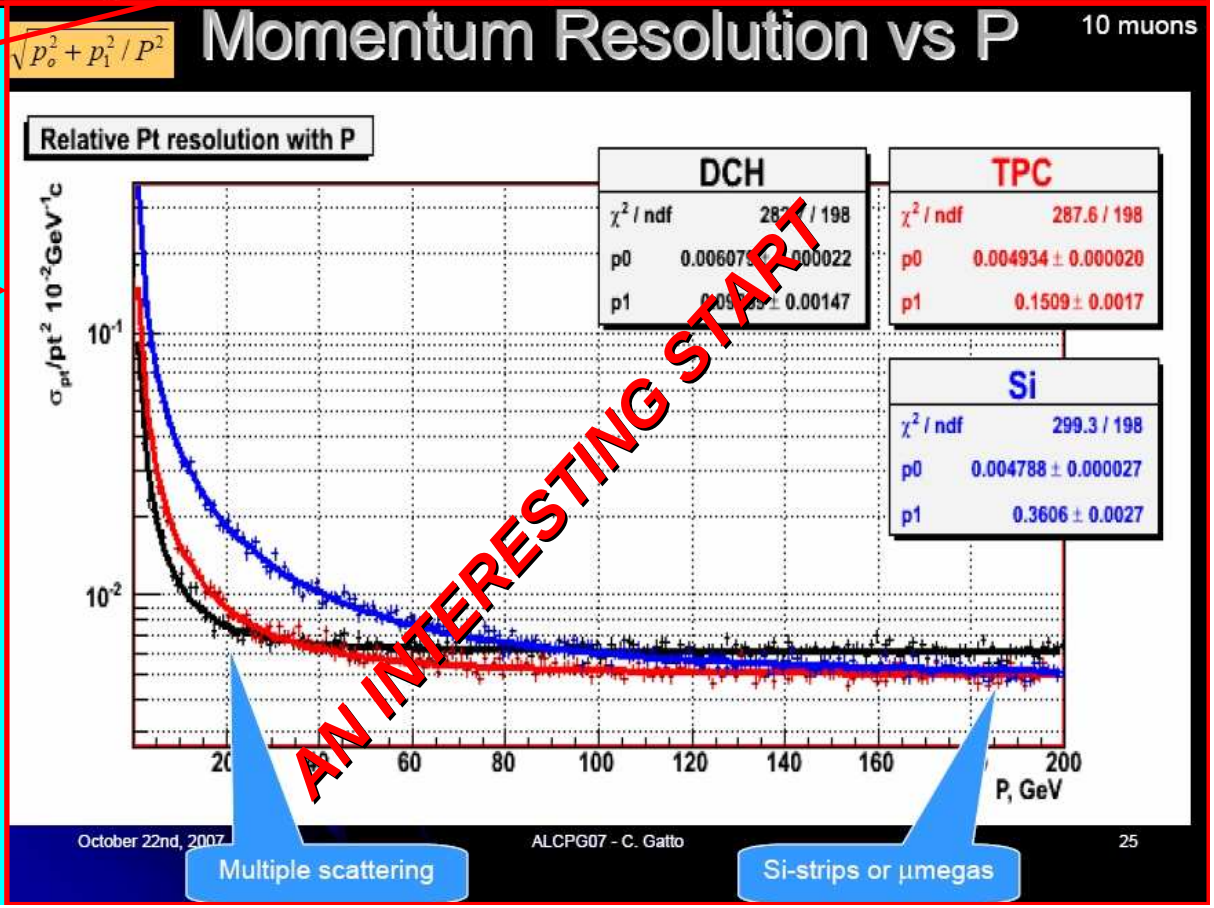
How they compare in the various tracking
Regions, especially:
Who wins at large angles?
Pros and cons of each one and how to
Improve them.
What technogical choices?



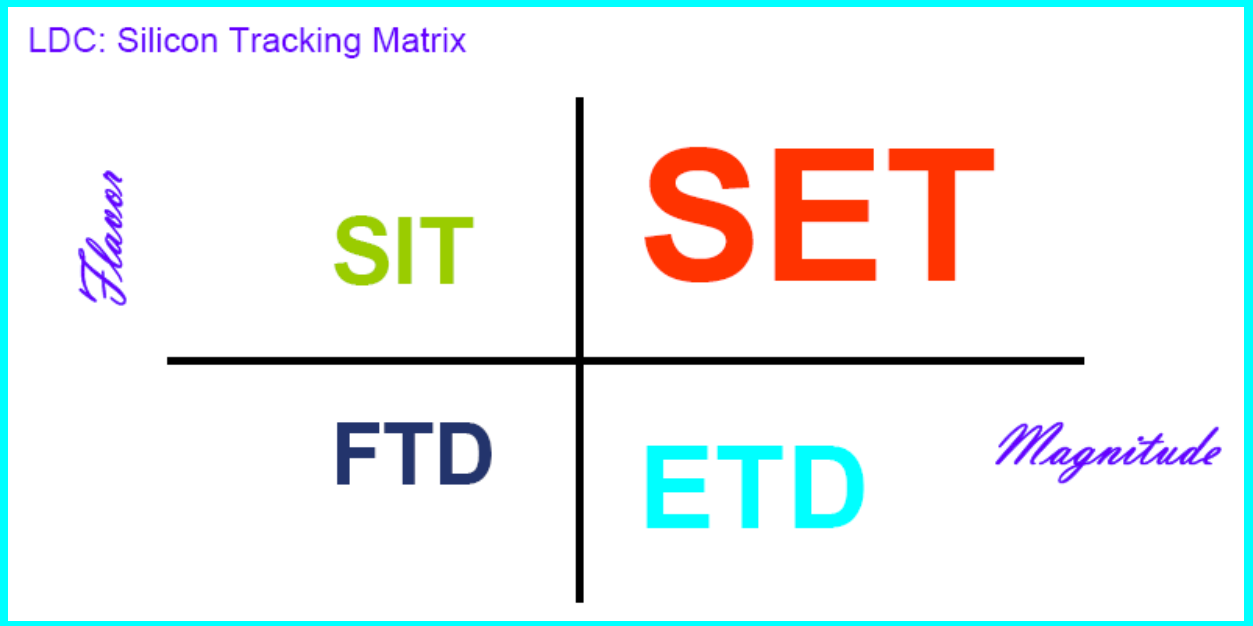
The comparison of tracking performances between gaseous & Silicon tracking has started (see results from C.Gatto & al with ILCROOT)

This effort is being pursued with full simulation and more detailed and mixed scenarios:
-> DCH + Si track. components
-> TPC + Si track. Components
-> All Silicon with various cases

Also various technological possibilities.



Q2: Roles of Si components in the hybride tracking case

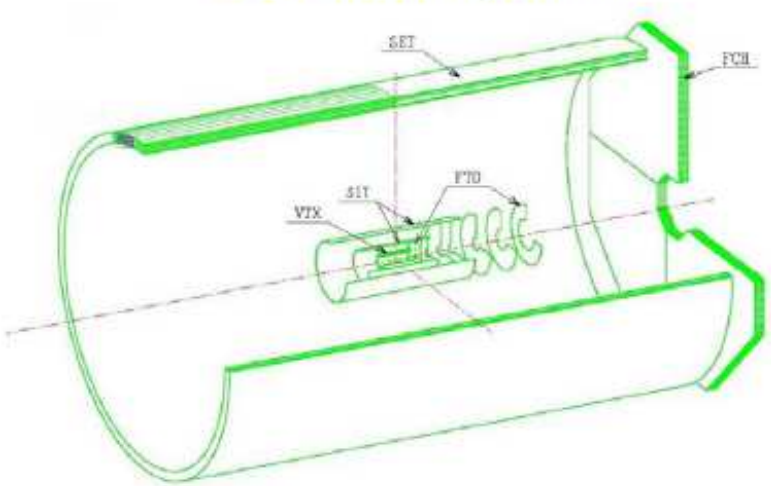


Discuss several times and a lot of simulations studies already done; see:
SiLC proposal to the ILCSC R&D Tracking panel in BILC07
http://lpnhe-lc.in2p3.fr/DOCS/beijing.pdf
and references therein
See also presentation of Valeri Saveliev at ILD Meeting in Zeuthen 0108 and presentations by Marcel Vos and W. Mitaroff, at this workshop

Q3: Comparison between hybride scenarios;

GLD/LDC or some hybride scenarios of 4th concept

LDC Silicon system:

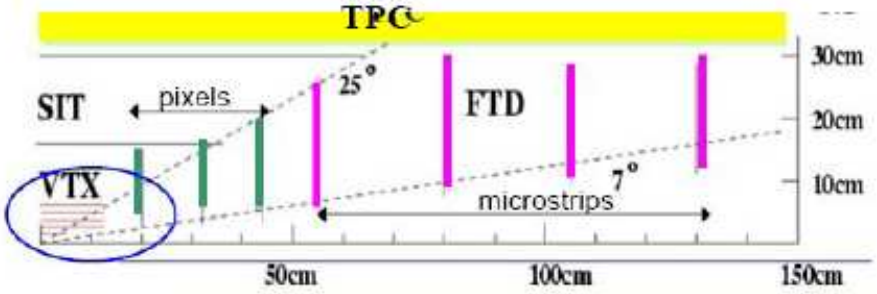


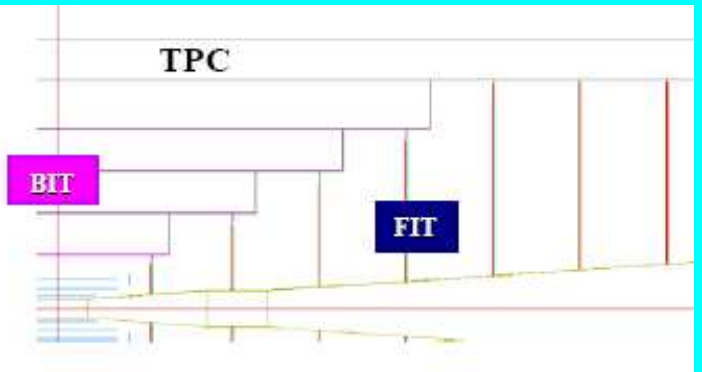
Silicon teams from LDC and GLD are participating in the SiLC R&D Collaboration.
As a result, the Silicon tracking systems in both concepts have evolved jointly; the only main difference is SIT vs IT

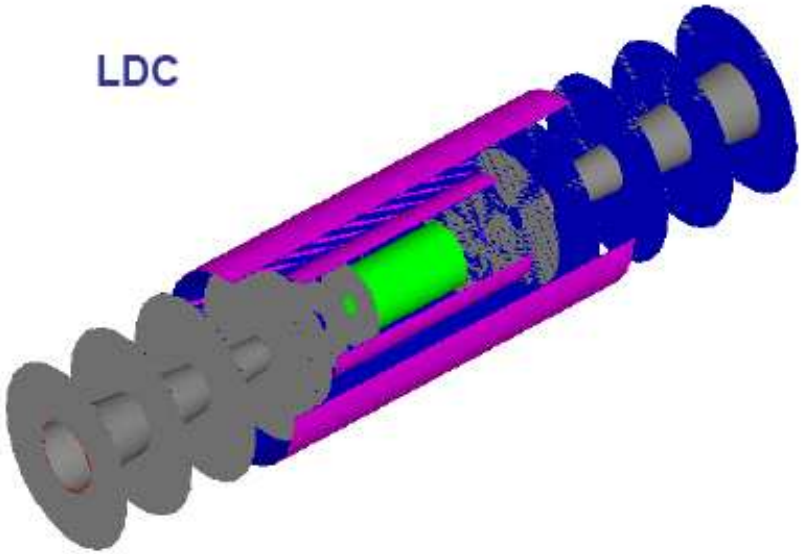
July 18, 2007,Yasuhiro Sugimoto,KEK

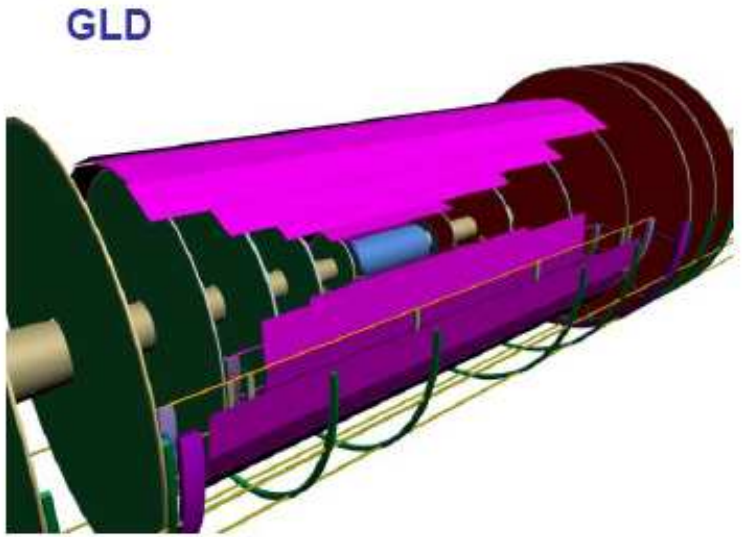
Sub-detector	GLD	LDC
Vertex det.	FP CCD	CPCCD/CMOS/DEPFET/ISIS/SOI/...
Si inner tracker	Si strip (4-layers)	Si strip (2-layers)
Si forward trk.	Si strip/pixel (?)	Si strip/pixel (?)
Main trk.	TPC	TPC
Additional trk.	Si endcap/ outer trk. (option)	Si endcap/ external trk.

Q4: The internal region in the hybride gaseous + Silicon case, *how many layers, resolutions, technology…*

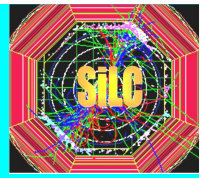








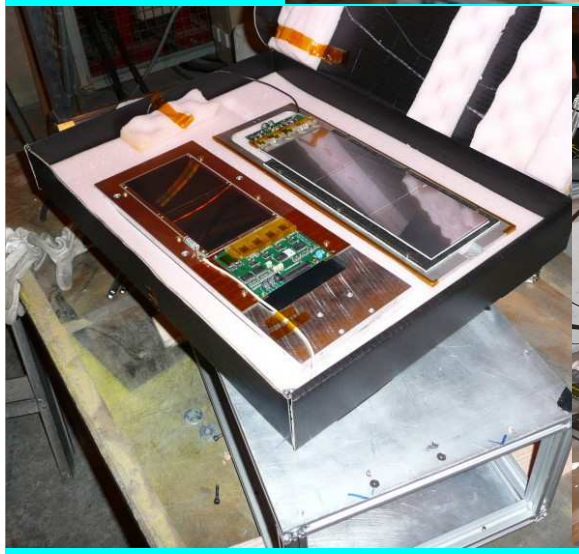
Decision yesterday at the SiLC meeting at this conference:
A joint task force to compare the different cases identified as the most relevant (benchmarks) and work jointly even if not with the same tools (to start with).

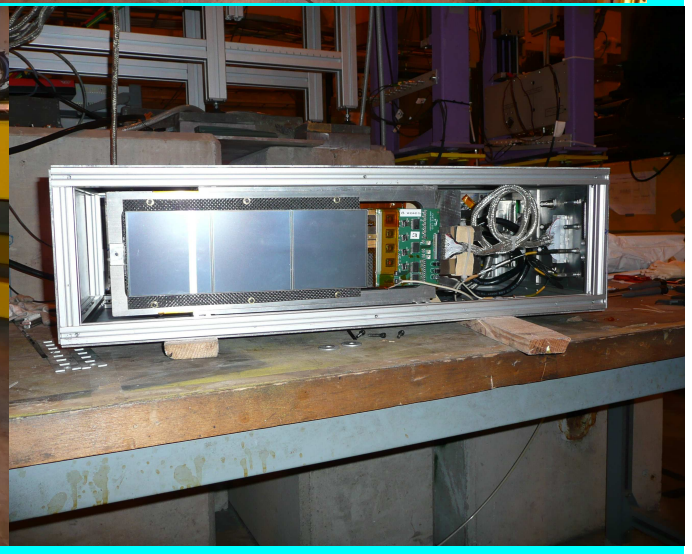


- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beams

SiLC: IEKP Karlsruhe, LPNHE Paris, CU Prague, IFCA Santander, Torino INFN & Uni, and collaboration with Maps telescope: DESY & Geneva U. and CERN support (Silicon Lab)

Arrival and setting up of the test at SPS West area, October 10-22, 2007



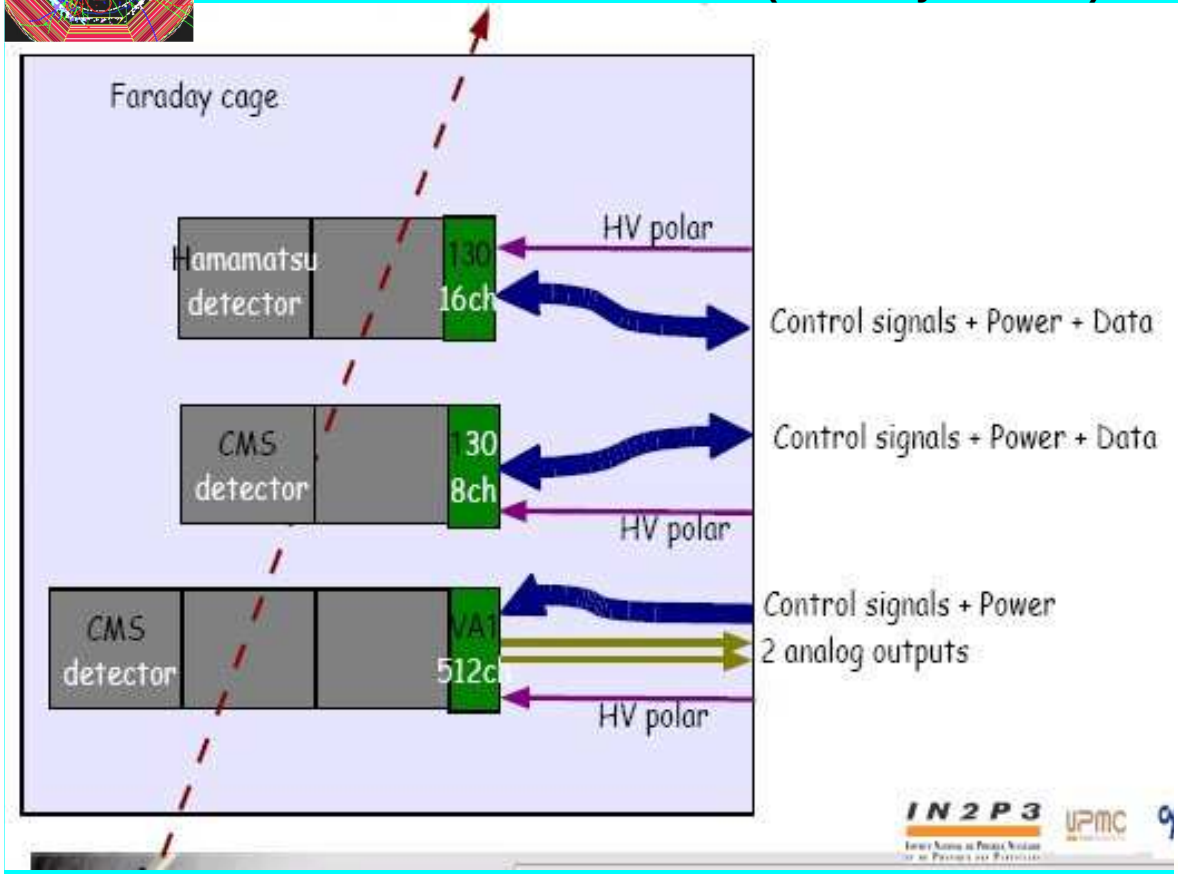


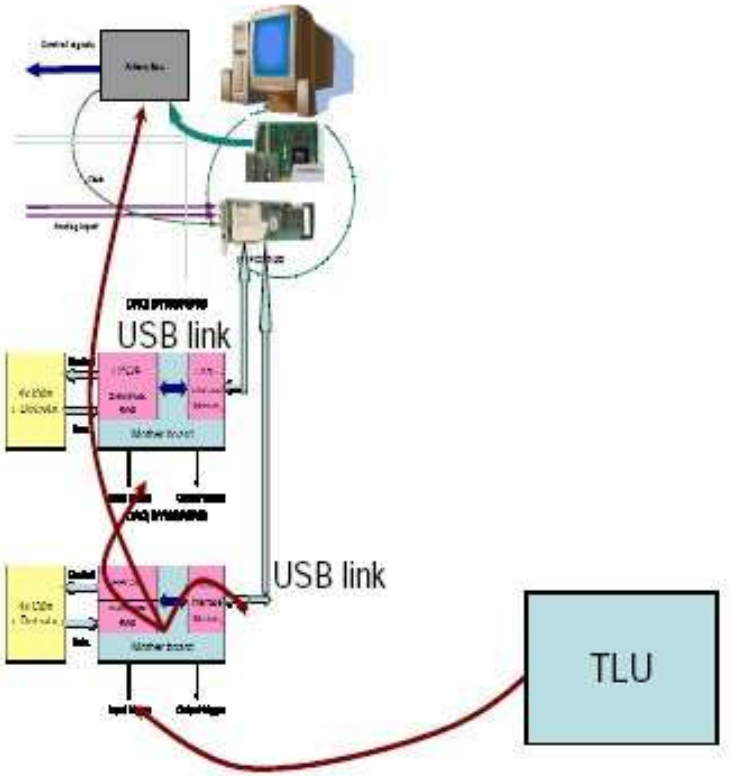
Photographs by F. Kapusta

Inside the Faraday cage

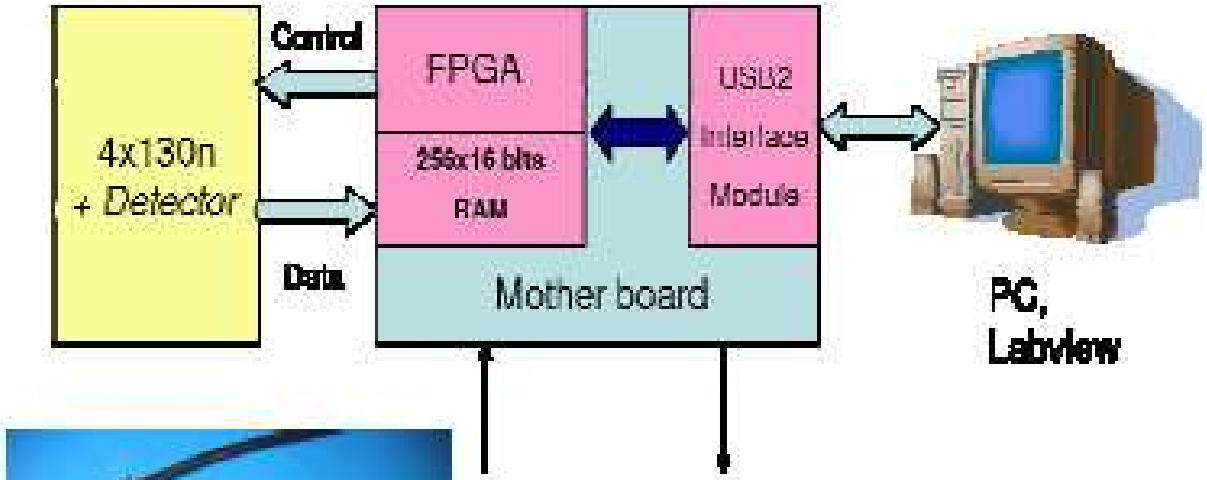
(slides by J. David)

The trigger: TLU



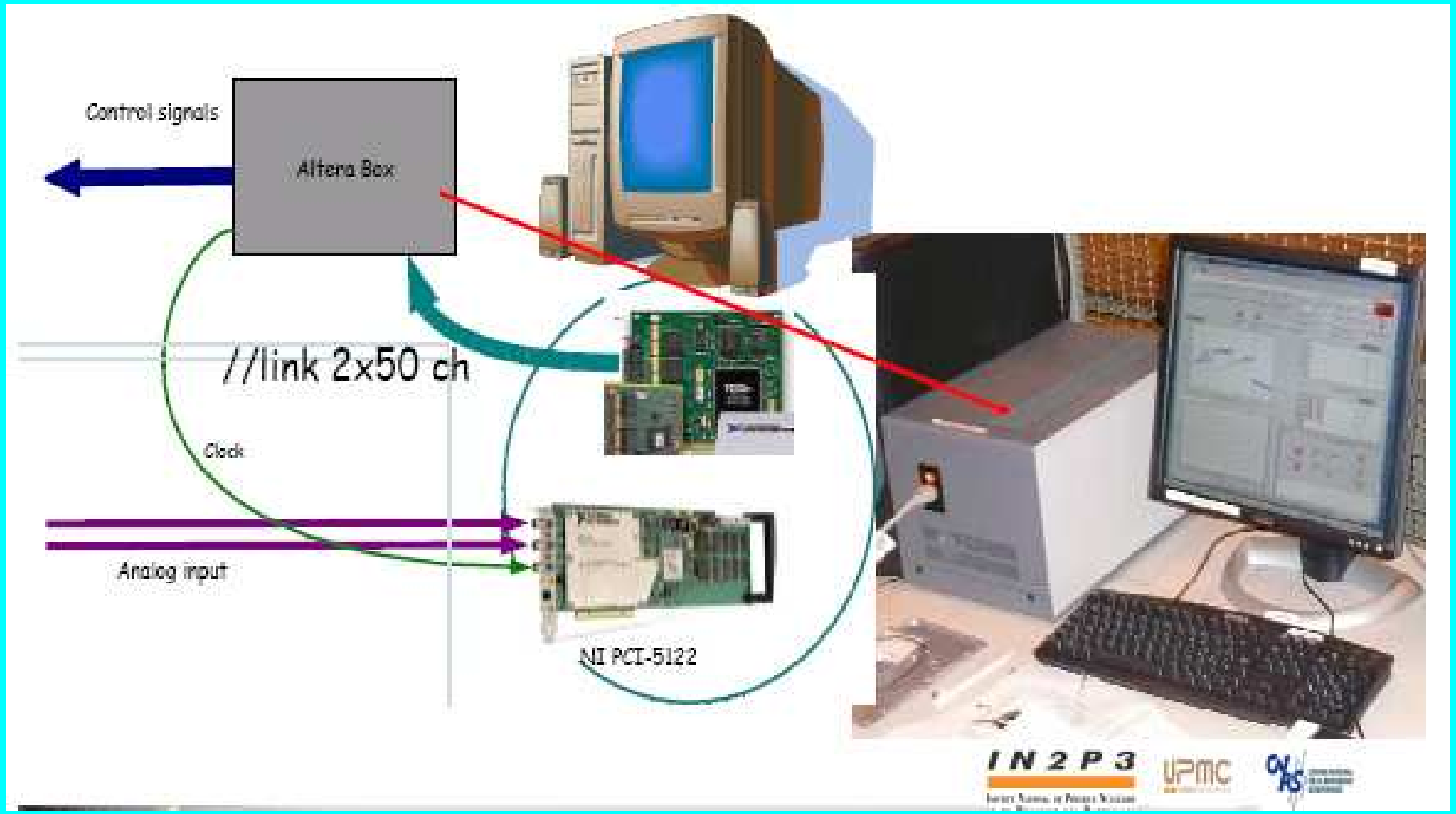


The DAQ for the 130 nm

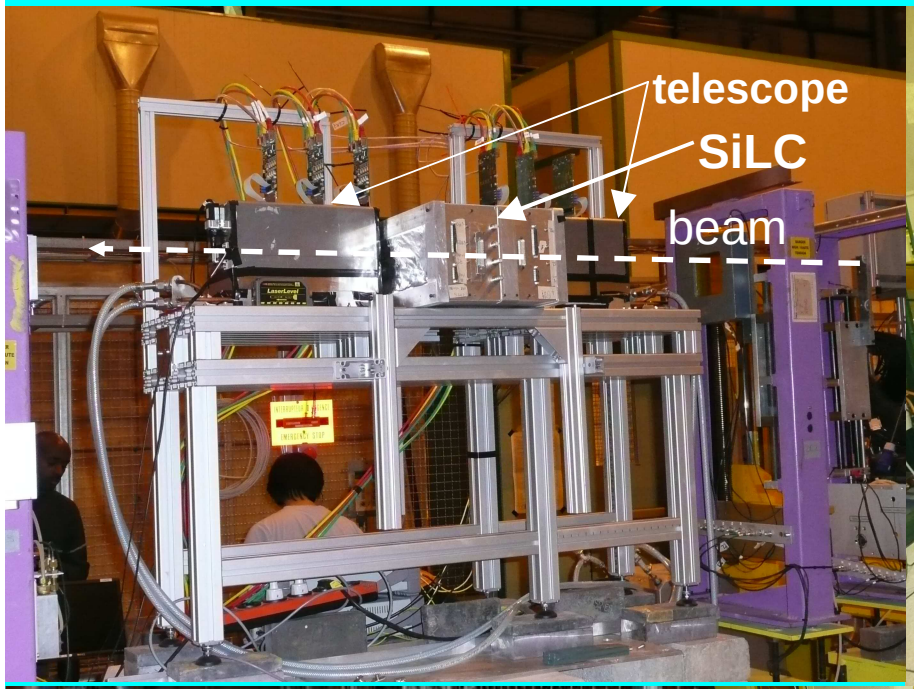


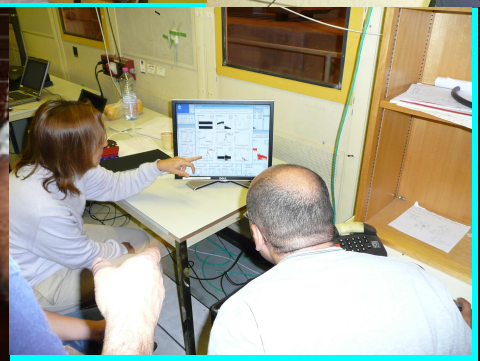
This card was duplicated
for the two 130 nm modules

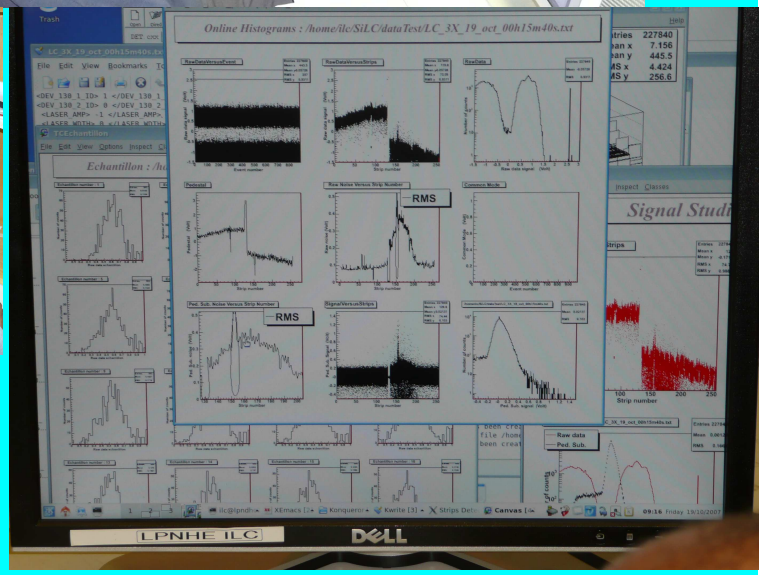
The DAQ for the VA1



Test running and data taking

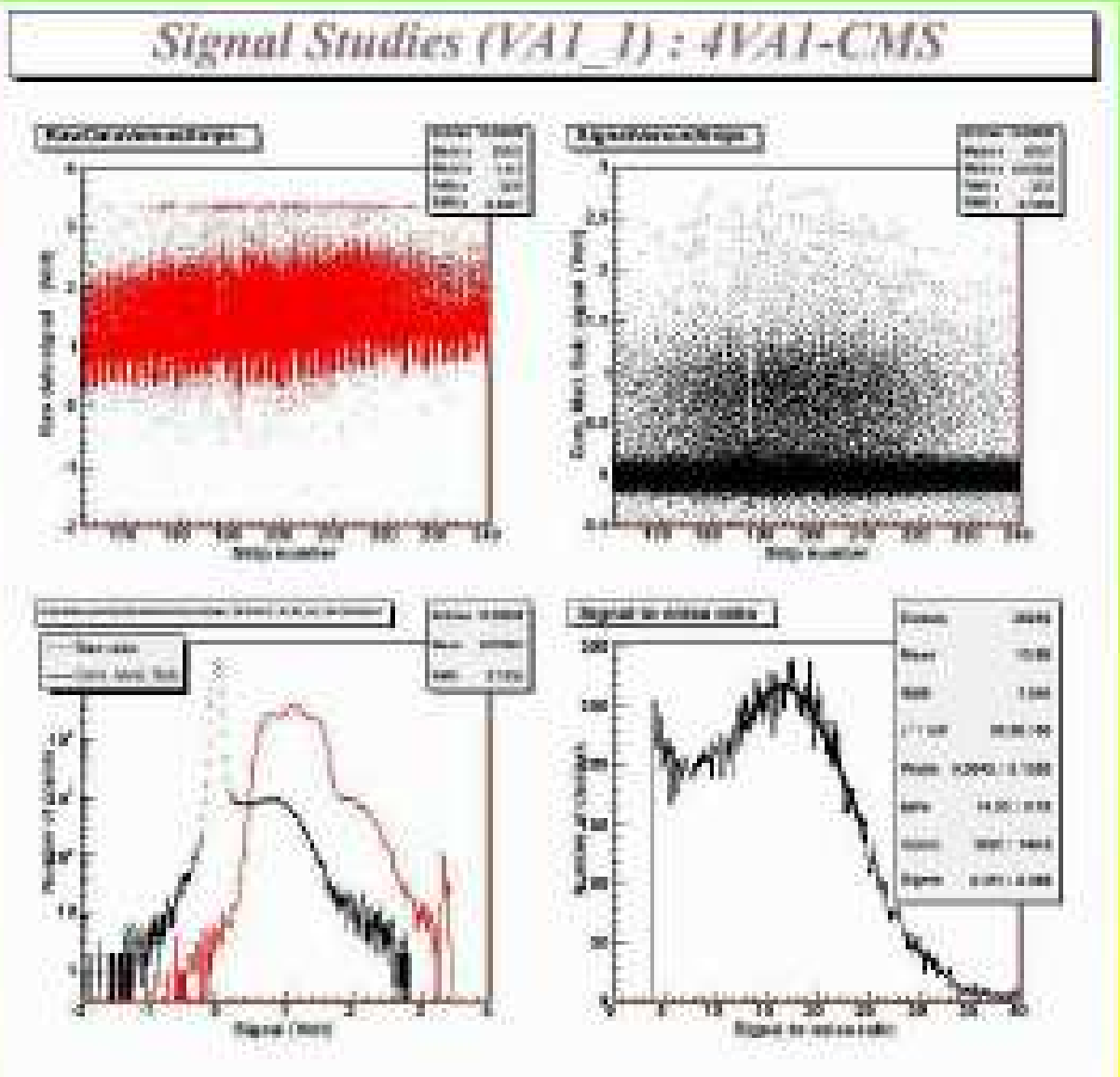






Photographs by F. Kapusta

The beam is on : the VA1-3CMS is responding S/N $\simeq$ 15

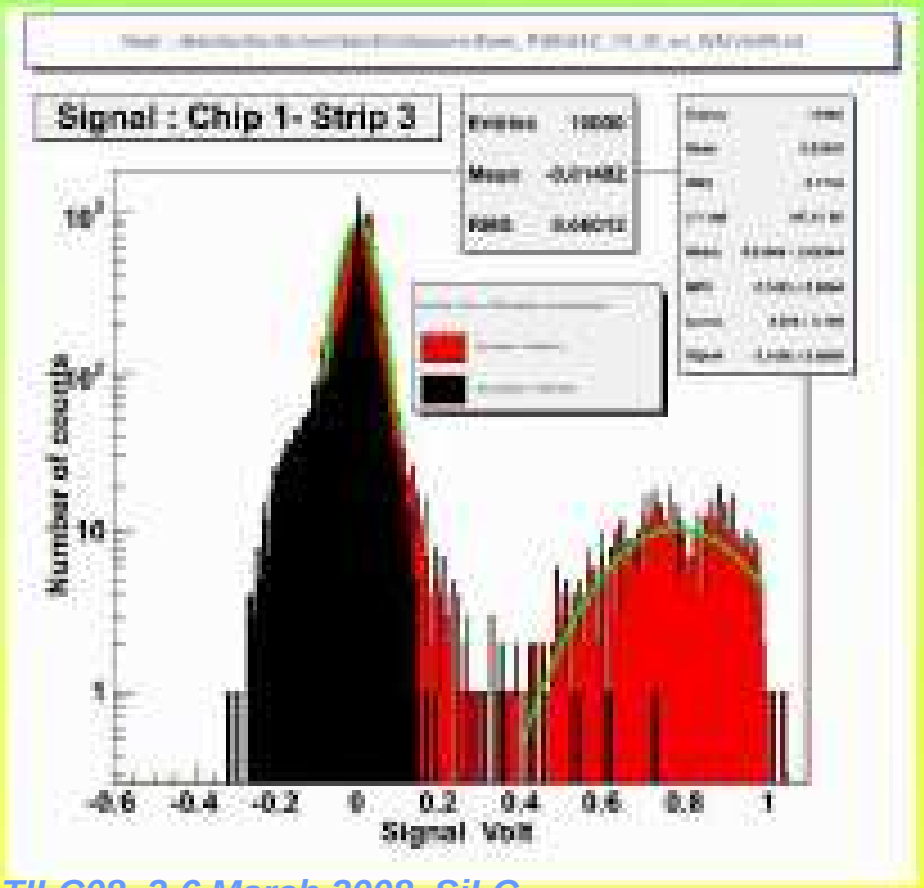


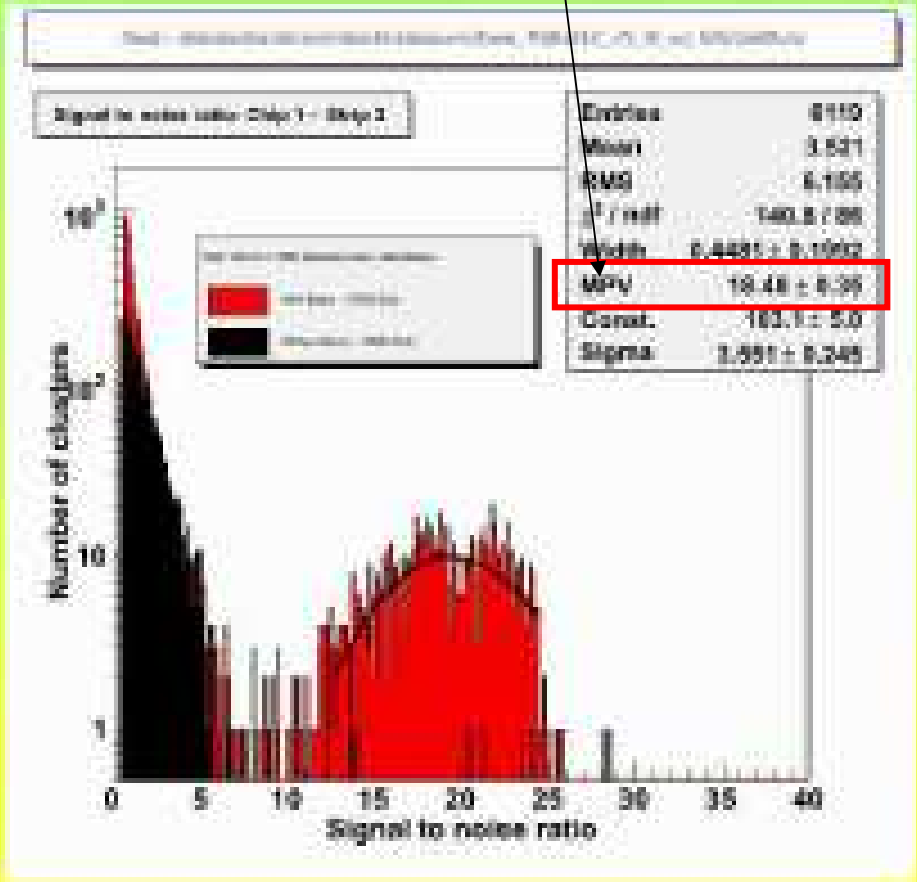
Analysis by W. Dasilva and F. Kapusta

Results with the new HPK + SiTR-130

HPK 130 nm procedure results for a good responding strip

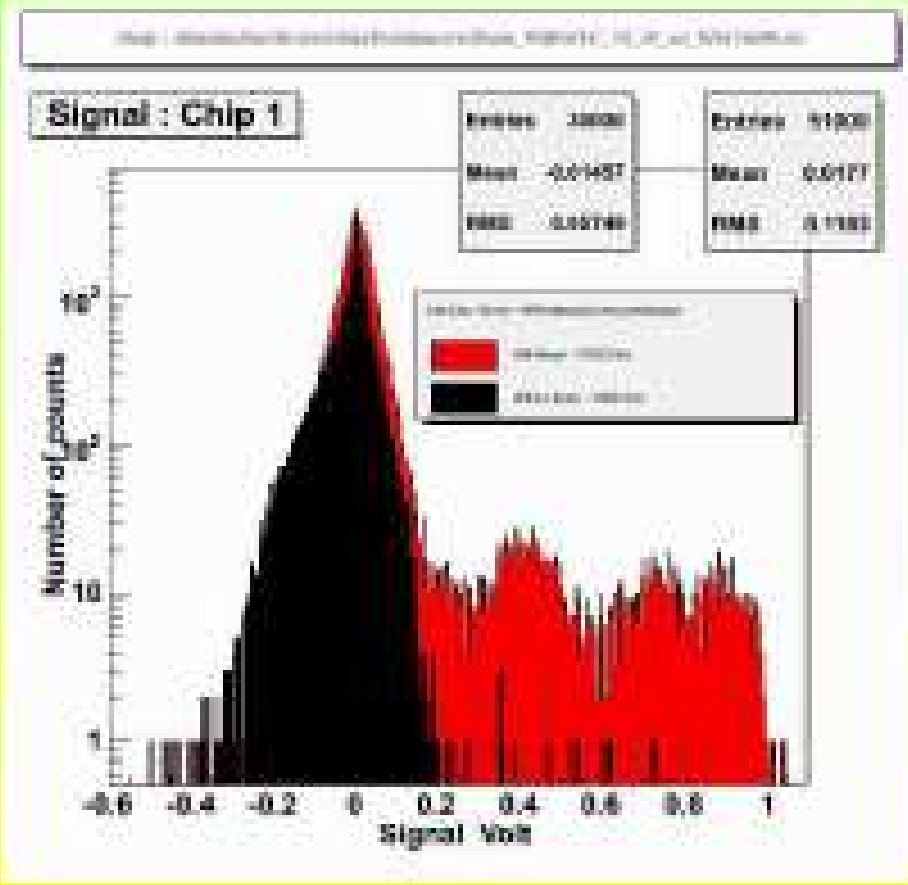
Black : Beam Off - Red : Beam On - S/N ~ 18

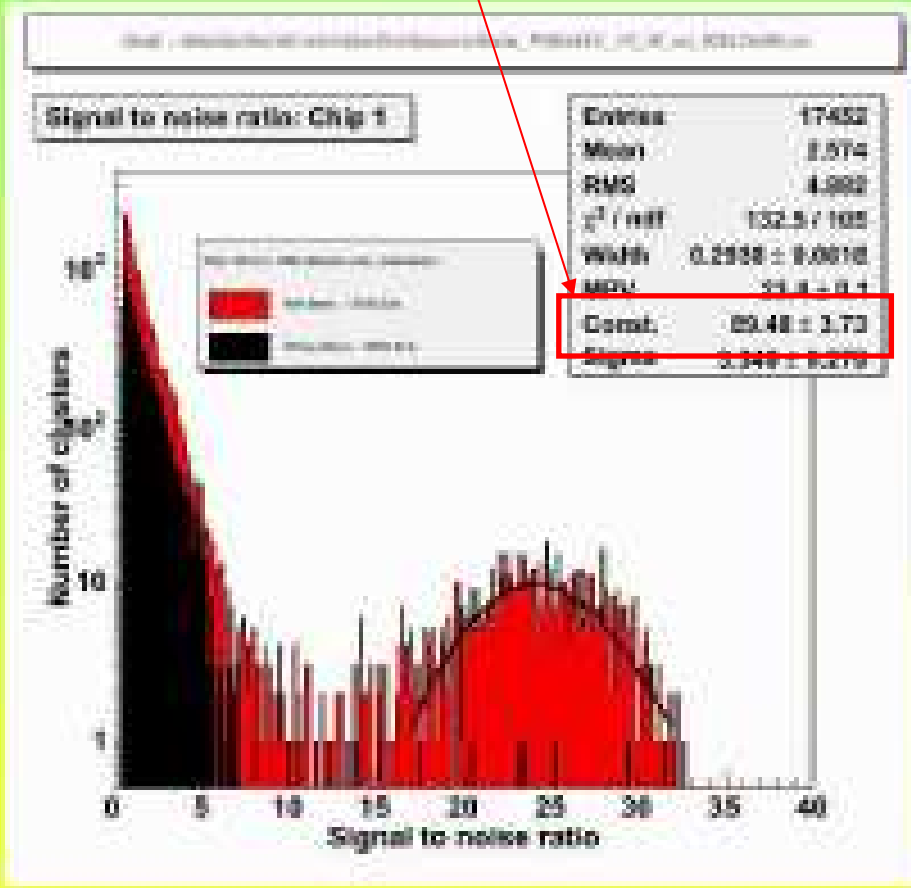




Results with the new HPK + SiTR-130

HPK 130 nm : 2 strip clustering - S/N ~ 23





Perspectives

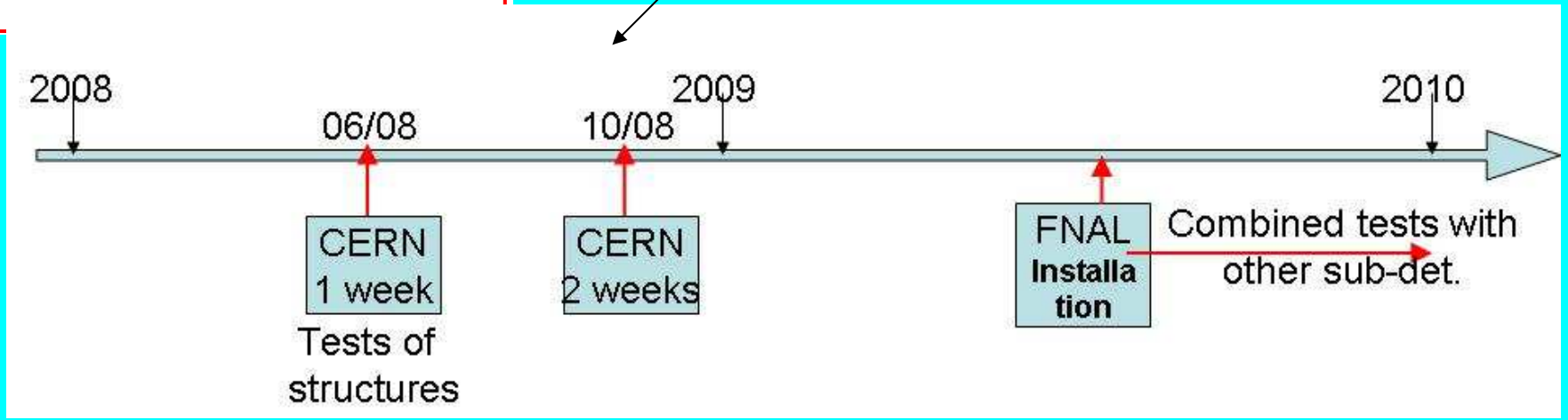
Proposal submitted to the CERN SPS Committee for
A beam test at the CERN-SPS in 2008 by:
SiLC R&D Collaboration

Abstract: *The SiLC R&D collaboration* is requesting a total of three weeks beam test at the SPS at CERN in 2008, in order to pursue the work started at the beam test H6 at CERN SPS, from October 16 to October 22, 2007. This collaboration is aiming to develop the new generation of large area Silicon systems in synergy with the work achieved for constructing the present LHC Silicon trackers and also in view of their upgrades for sLHC and the future trackers for the Future Linear Collider. It is also part of the EUDET JP-P6 European Project.*

*Members of the SiLC R&D collaboration are: University of Michigan-Ann Arbor (USA), LAPP-Annecy (France), University of Barcelona and University Ramon Llull in Barcelona (Spain), IMB/CNM-CSIC in Bellatera (Spain) Helsinki Institute of Physics (Finland) and VTT Technical Research Center of Finland-Helsinki (Finland), IEKP Karlsruhe (Germany), Liverpool University in Liverpool (UK), Moscow State University-Moscow Russia), Obninsk State University – Obninsk (Russia), LPNHE-University Pierre et Marie Curie/CNRS-IN2P3 (France), Charles University in Prague (Czech Republic), ICIPP and University of California in Santa Cruz (USA), IFCA-University of Cantabria and CSIC-Santander (Spain), Yonsei University, Seoul National University and SungKyunKwan University all in Seoul, and Kyungpook National University in Daegu (Korea), INFN-Torino and University of Torino in Torino (Italy), IFIC, University of Valencia and CSIC- Valencia (Spain), HEPHY, Austrian Academy of Sciences in Vienna (Austria), Hamamatsu Photonics in Hamamatsu City (Japan)

SiLC test beam coordinator: Aurore Savoy-Navarro
aurore@lpnhe.in2p3.fr
SiLC contact person at CERN: Marcos Fernandez Garcia
Marcos.fernandez@cern.ch

Proposal submitted to the SPSC-CERN Nov 16,2008



Perspectives cont'd

- SiLC is a **transversal R&D activity**
- It intends to play a major role not only on the development of novel technologies needed to overcome the challenges ahead of us,
- But also **to study and compare the tracking alternatives** proposed for the ILC **with a joint optimization task force**.

  This workshop played an important role in reinforcing the will some people from the 3 proposed ILC detectors have to collaborate with a joint simulation tracking effort. Sharing tools and expertise (see discussion at the SiLC meeting yesterday).

  It will be benefitial to help in the processus of validation, Loi's etc…in front of us.
- Same for **combined test beams** especially those at FNAL next year.
- SiLC intends also to **further exploit the synergy with other machines and HEP domains**, especially the LHC and its upgrades.

SiLC R&D Collaboration

U.S.A

Michigan U.
SCIPP-UCSC

Connections with:
- FNAL (DOE prop 05 funded)UCSC, FNAL, LPNHE
- SLAC (DOE prop 03: funded): UCSC, SLAC Michigan U, LPNHE and meetings SiD
- CERN (collab of bonding Lab+TB infrastructures)

Europe

IMB-CNM/CSIC, Barcelone (SP)
(eudet ass.)
U.Barcelona (SP)
Helsinki U.(Fi) *(eudet)*
VTT-Finland (Fi)
IEKP, Karlsuhe U. (D)
Liverpool U.
Moscow St. U. , Moscou(Ru)
(eudet ass.)
Obninsk St. U., Obninsk (Ru)
(eudet ass.)
LPNHE, Paris (Fr) *(eudet)*
Charles U. , Prague (CZ) *(eudet)*
IFCA/CSIC, Santander(Sp) *(eudet)*
Torino U., INFN-Torino (It)
IFIC-CSIC Valencia (Sp) *(eudet ass.)*
HEPHY, Academy Sci., Vienna (Au)

Asia

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
HAMAMATSU (Japan)

Launched January 2002, Proposal to the PRC May 2003, Report Status May 2005, ILC tracking R&D Panel at BILCW07 February 2007, next PRC Status report April 08

This brief review is an attempt to present all the SiLC collaborators hard work results: Many thanks to all of them!