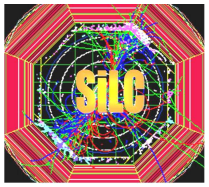
A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips Readout at the ILC



On behalf of

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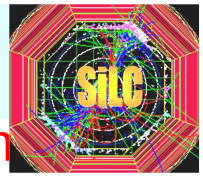
Work in the framework of the SiLC (Silicon trackin for the Linear Collider) R&D Collaboration and the EUDET I3-FP6 European Project

TILC08, March 3 to 6, 2008, Sendai, Japan

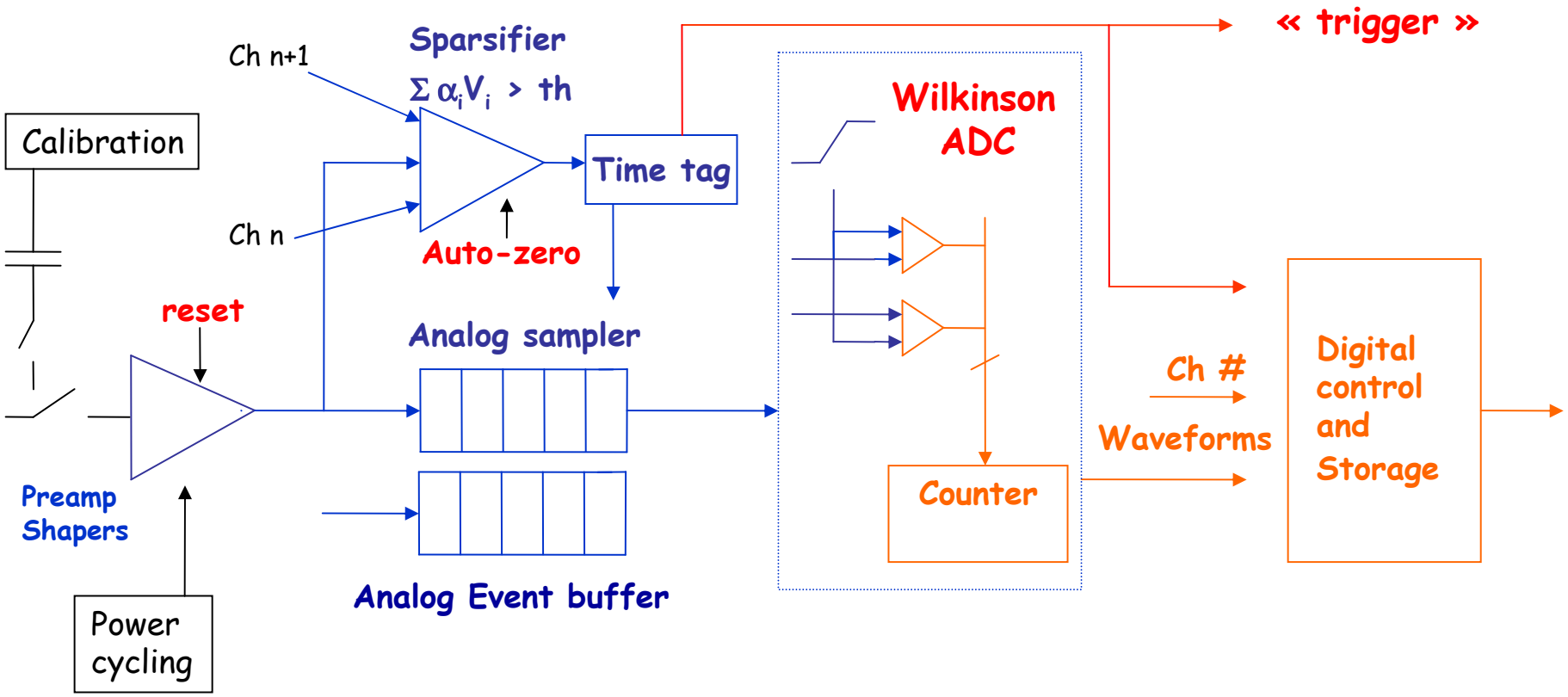
Functionalities to be integrated



- Full readout chain integration in a single chip, 512 or 1024 ch in 90nm
  - Preamp-shaper
  - Sparsification — Trigger decision on analog sums
  - Sampling — 8-deep sampling analog pipe-line
  - Analog event buffering: — Occupancy: 8-16 deep event buffer
  - On-chip digitization — 10-bit ADC
  - Buffering and pre-processing: Centroids, χ2 fits, lossless compression&error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

Amplifiers: - 30 mV/MIP over 30 MIP range
Shapers: - Two ranges: 500ns–1μs, 1μs-3μs
Sparsifier: - Threshold the sum of 3-5 adjacent channels
Samplers: - 8 samples at 80ns sampling clock period
- Event buffer 8 deep
Noise baseline: Measured with 180nm CMOS:
375 + 10.5 e-/pF @ 3 μs shaping, 210μW power dissipation
ADC: - 10 bits
Buffering, digital pre-processing
Calibration
Power switching can save a factor up to about 100

Front-end architecture



Charge 1-30 MIP, Time resolution: BC tagging 150-300ns
80ns analog pulse sampling

Technology: Deep Sub-Micron CMOS 130-90nm

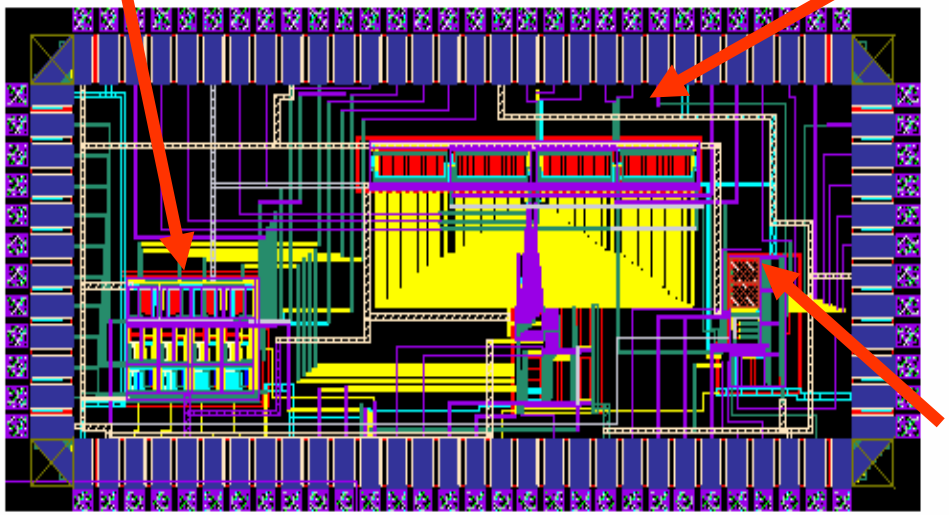
1 step: the 4-channel chip,SiTR-130_V1&2

(LPNHE-LAPP)

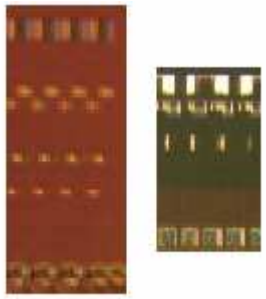
Amplifier, Shaper, Sparsifier 90*350 µm²

Analog sampler 250*100 µm²

layout



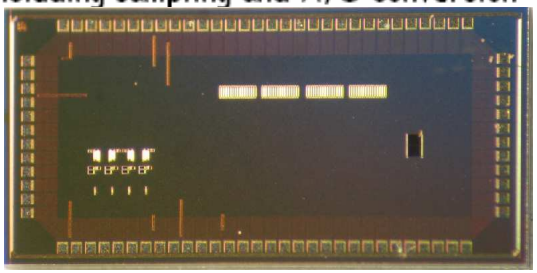
A/D 90*200 µm²



180nm 130nm

Layout of the 130nm chip including sampling and A/D conversion

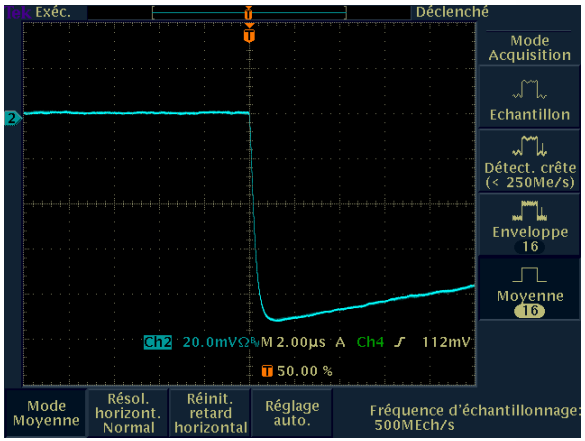
Photo



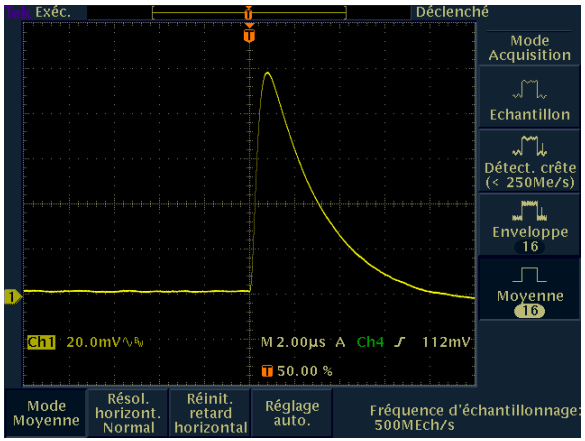
Preamplifier-shaper performances

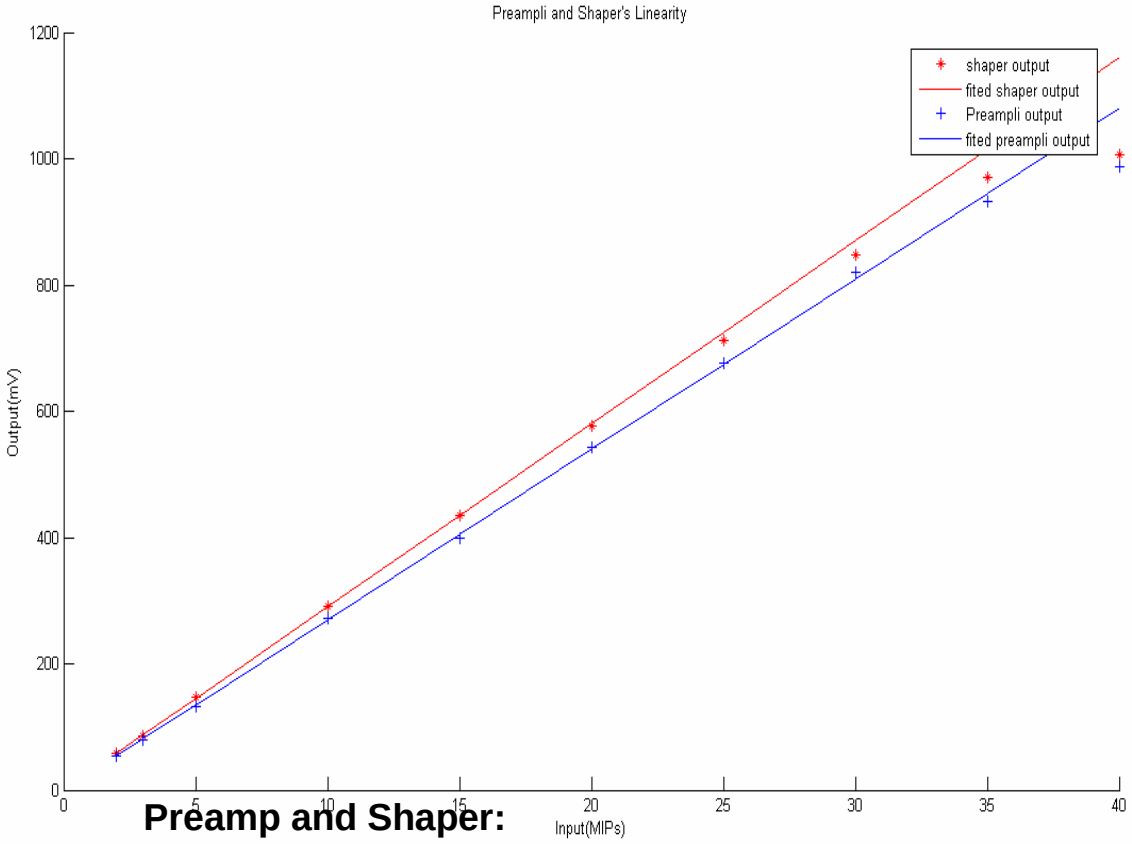
Measured gain - linearities

Preamp output



Shaper output





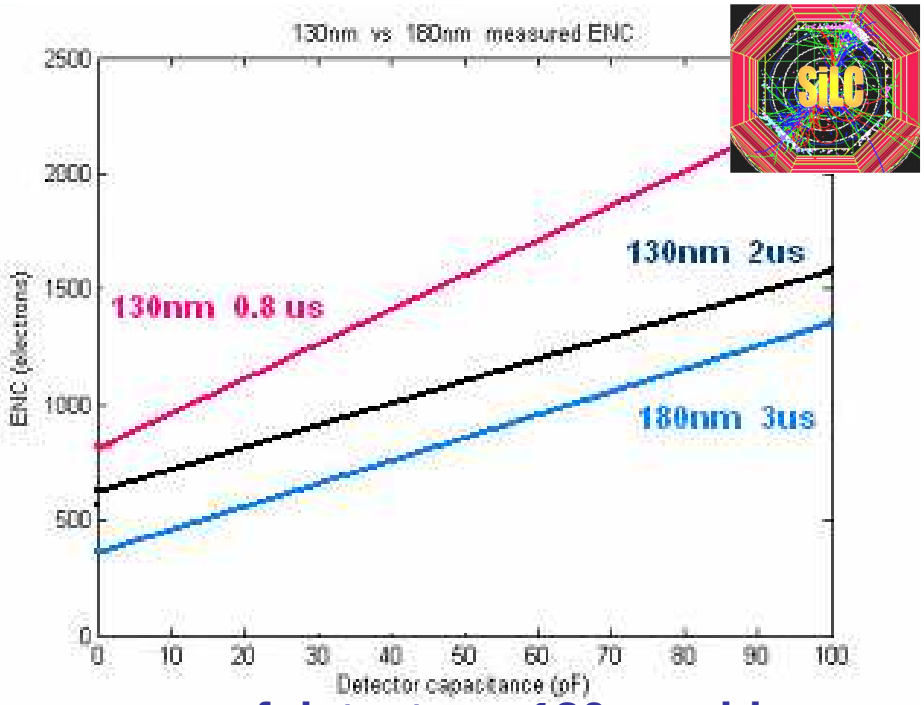
Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

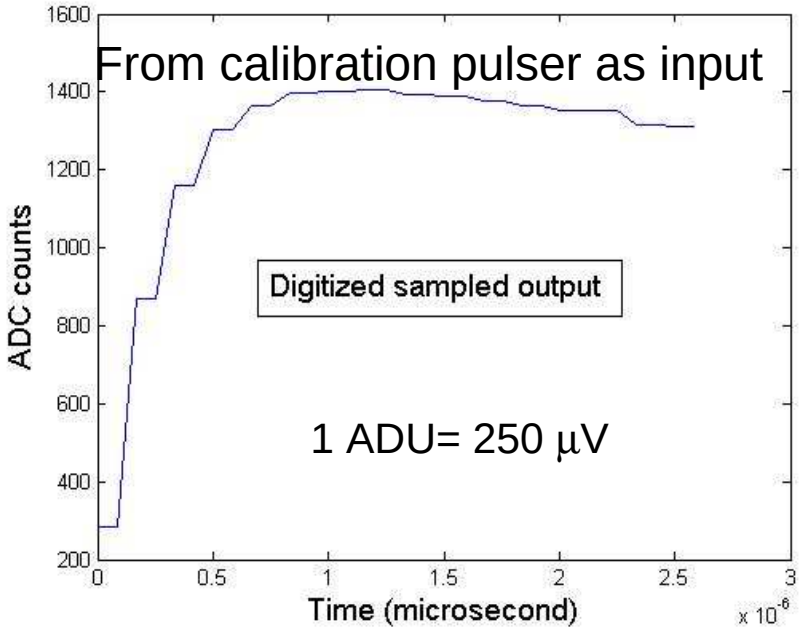
Measured Performances

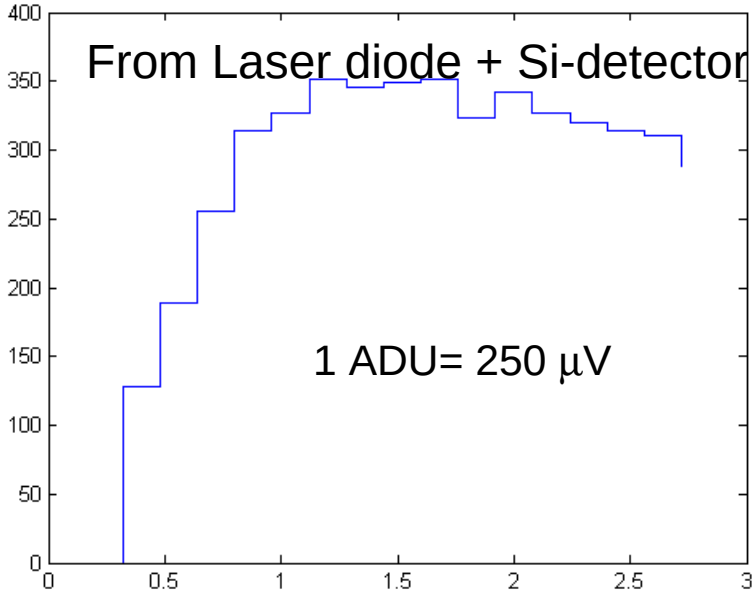
Noise:
130nm @ 0.8 µs: 850 + 14 e-/pF
130nm @ 2 µs : 625 + 9 e-/pF
180nm @ 3 µs : 375 + 10.5 e-/pF

Power (Preamp+ Shaper)
130 nm: 150+90= 245 µW
180 nm: 70+140= 210 **µW**

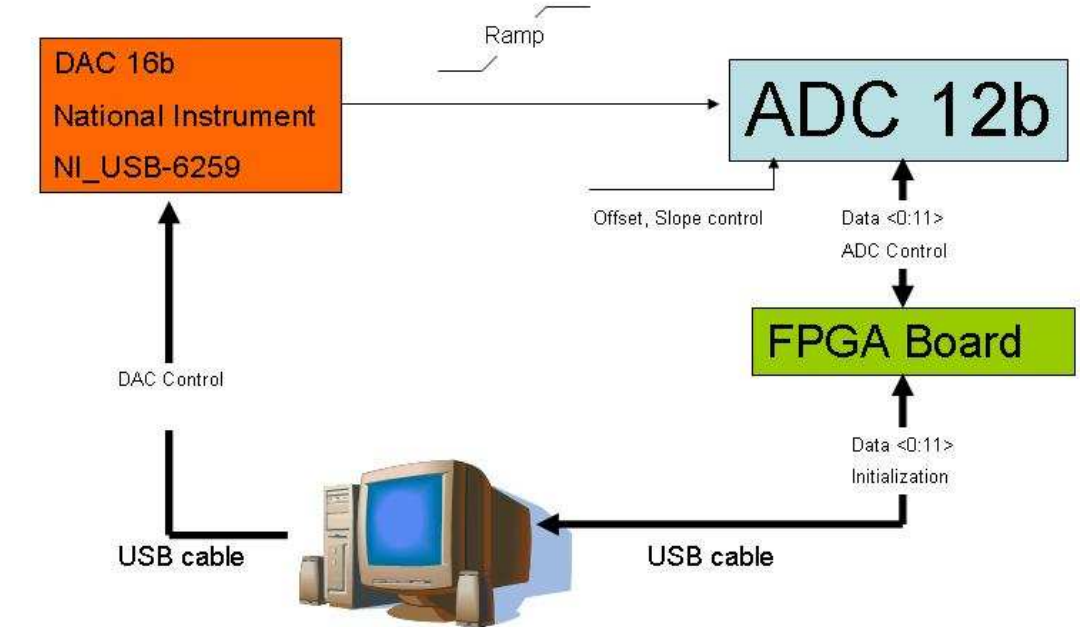


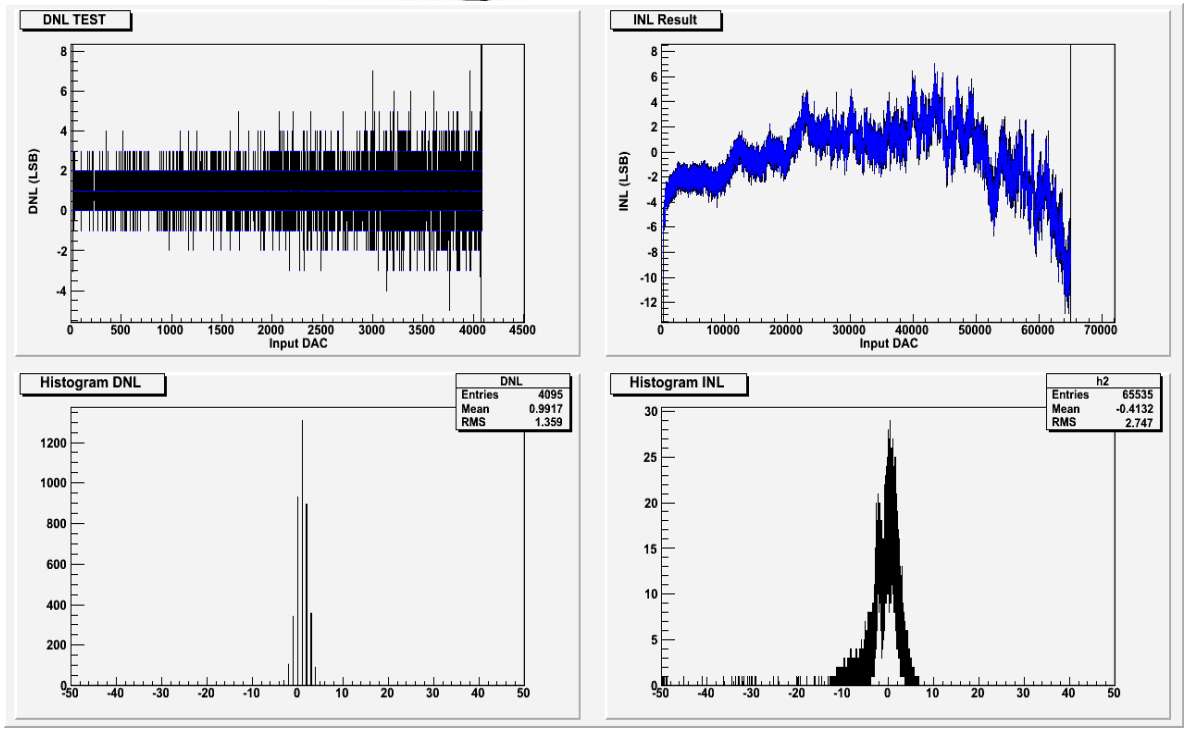
Digitized analog pipeline output Laser response of detector + 130nm chip





Sampling rate = 12 MHz; Readout rate = 10 KHz





ADC TEST

DAC Input :

Dynamic : 0 – 1V

Offset : ~1V

ADC Output :

From 50 bin to 3780 bin:

+INLmax = 7 LSB

+INLrms = 2.74

LSB

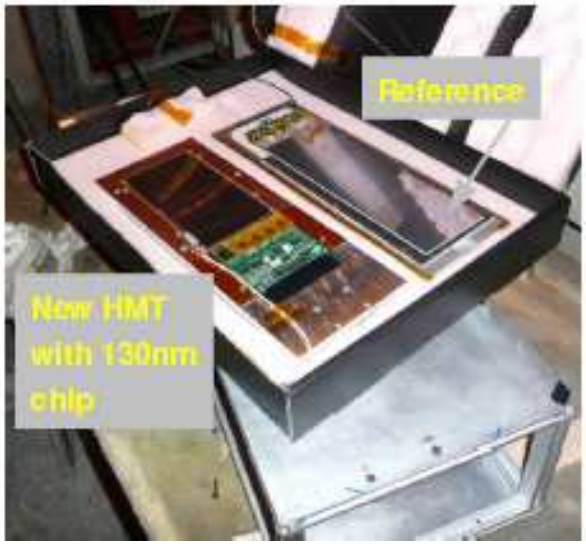
+DNLmax = 7 LSB

+DNLrms = 1.36

LSB

→ ~ 9bit effective in the worst case

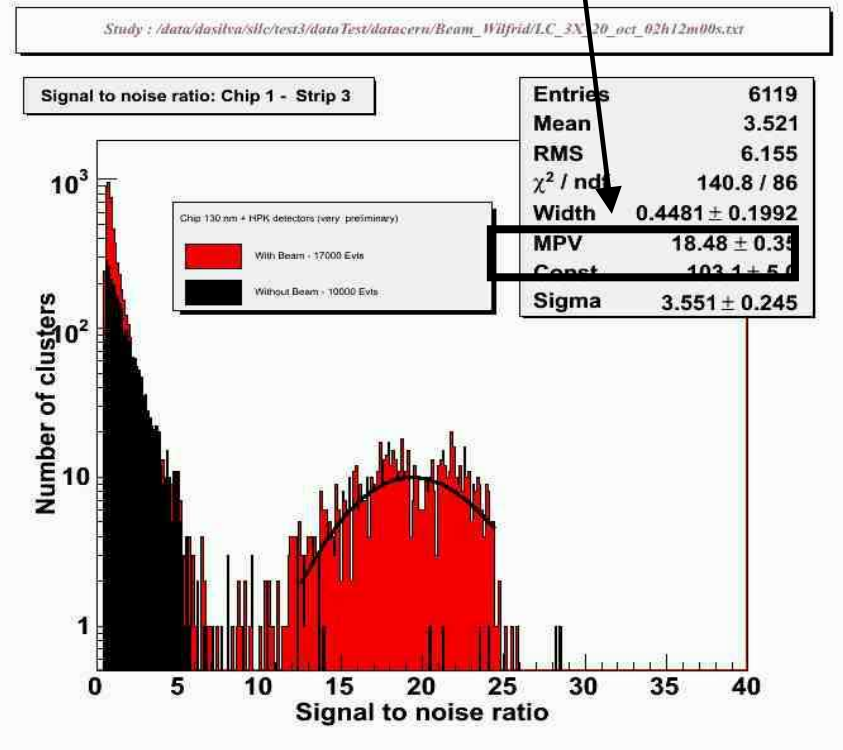
SiTR-130_V1 test-beam response



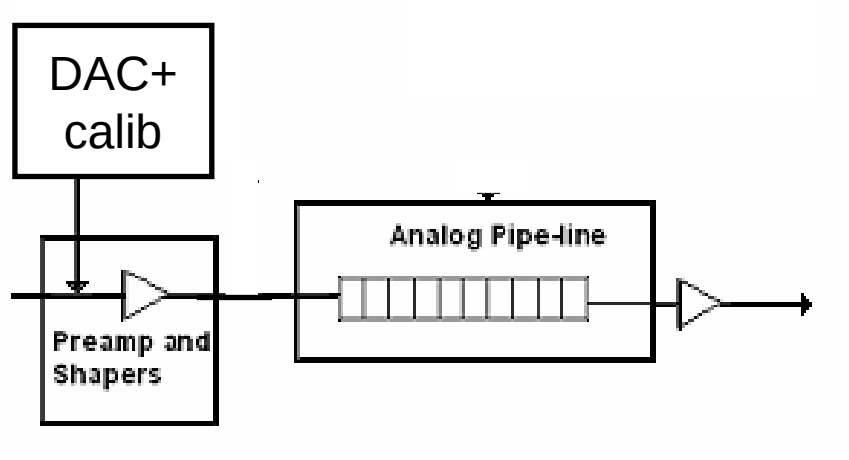
This CMOS 130nm design and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels) with

- DC power under 600μW/ch
- Silicon area under 100 x 500 μ²/ch

Signal to Noise ratio from beam-tests



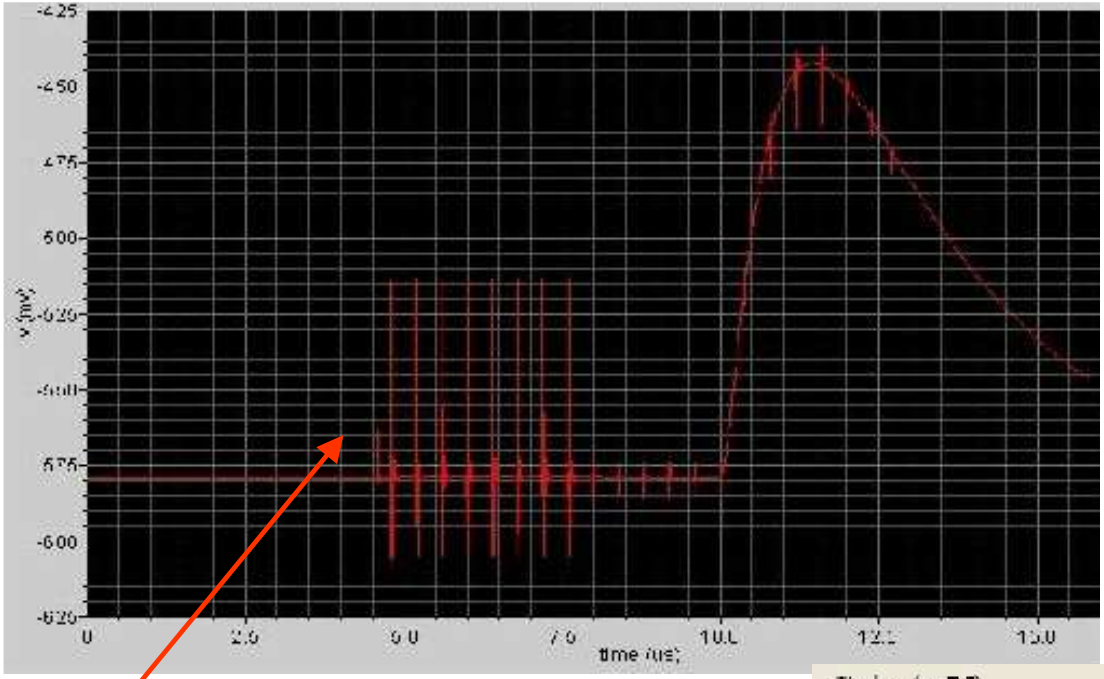
Test of the pipeline and integrated test pulse calibration (LAPP + LPNHE)



New version of the pipeline + calib system

Last block to be tested (in progress).
This the new pipeline developed by LAPP with an output buffer to isolate the pipeline output from parasitic capacitive effects.
The calibration scheme is included also In this new version and is being tested as well.

This new pipeline and calibration schemes are included in the new chip design, in replacement of the previous pipeline version (with no buffer included).
The calibration was not included in the chip itself but in the hybrid.



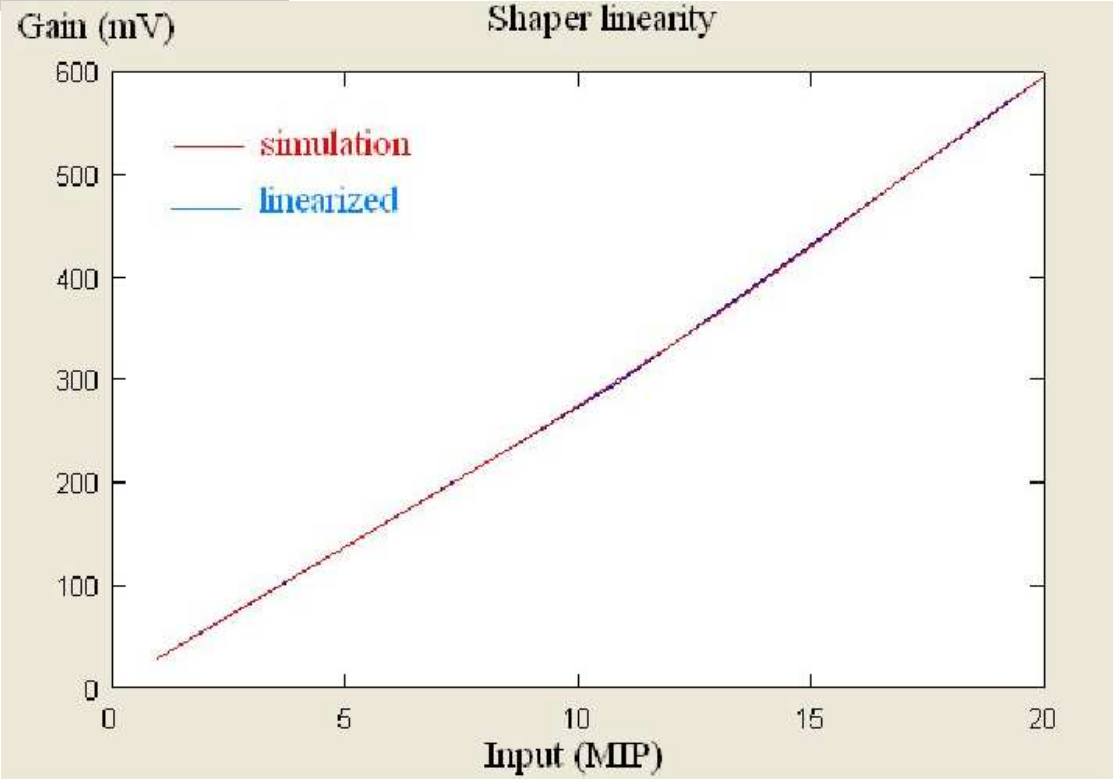
Improved signal shaping in this new version

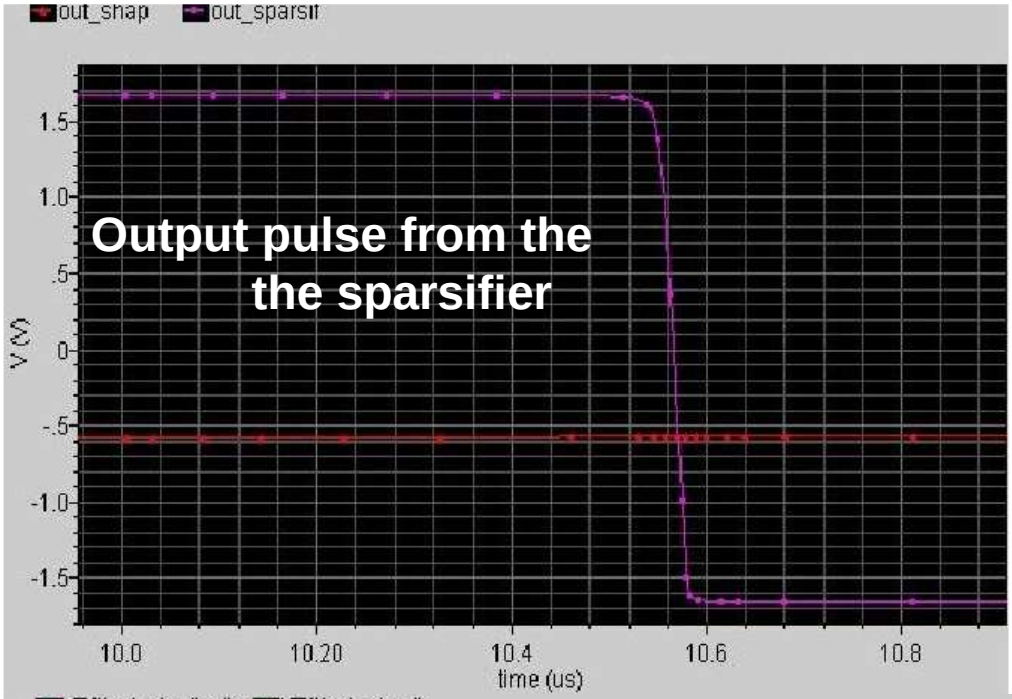
Preampliflier-Shaper (Simulation)

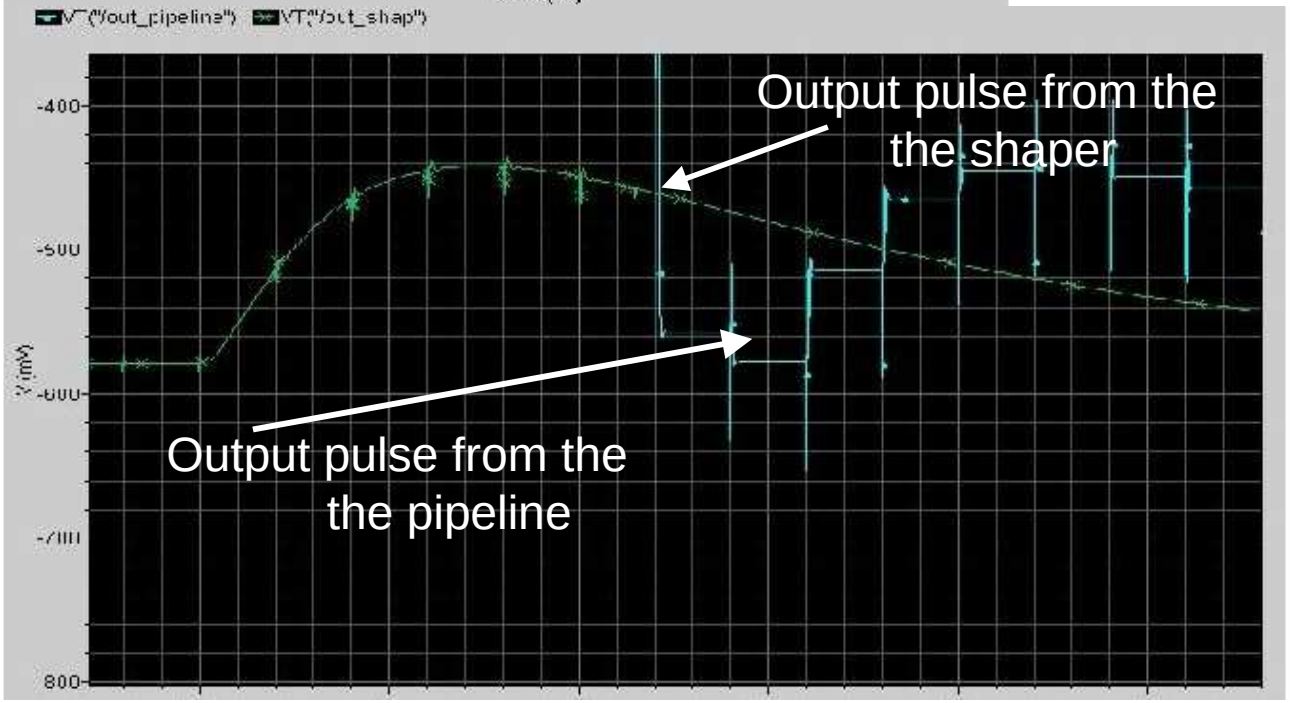
Gain: 2 ranges
28.5mV/MIP (1-10MIPS)
32mV/MIP (11-20MIPs

Dissipation 200µW/channel

Noise 428+63 e-/pF (UMC Models)
Shaping time: programmable from 0.5µs to 2 µS.







Sparsifier

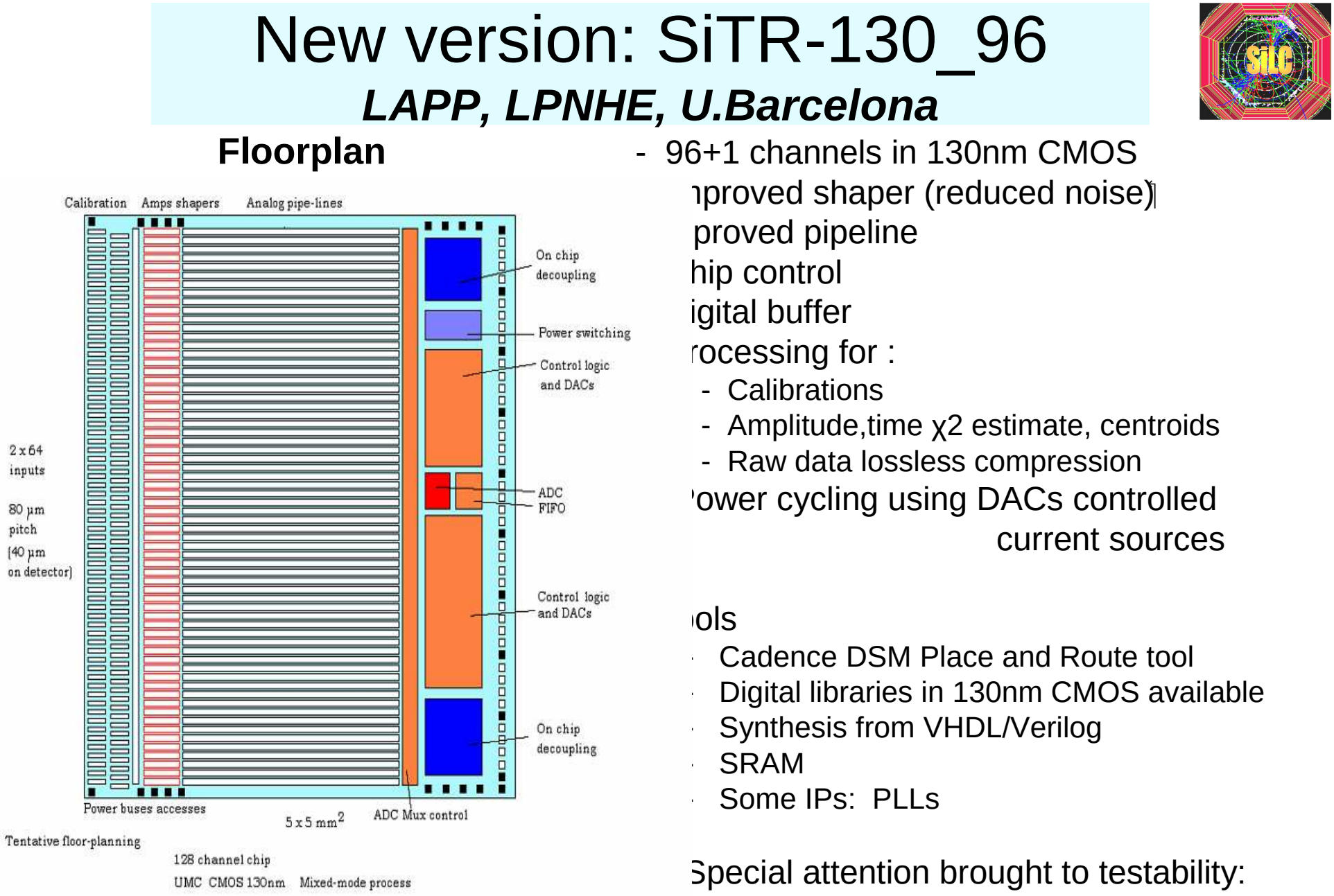
Dissipation~200µW
Response Time~170-570ns
(1 MIP to 20MIP)

Pipeline

avec output à 330ns de période d'échantillonage

New version: SiTR-130_96

LAPP, LPNHE, U.Barcelona



Floorplan

- 96+1 channels in 130nm CMOS
  - ıproved shaper (reduced noise)
  - proved pipeline
  - hip control
  - igital buffer
  - rocessing for :
    - Calibrations
    - Amplitude,time χ2 estimate, centroids
    - Raw data lossless compression
  - ower cycling using DACs controlled current sources

- ols
  - Cadence DSM Place and Route tool
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs

Special attention brought to testability:

Include mixed-mode simulator

AMS designer under installation at LPNHE

I/O PADS


97 CHANNELS CHIP – LPNHE
SIZE = 4898x4942 um2
PAD INPUT : 97x2 STAGGERED TYPE
PITCH = 45um (90um double pitch)
BONDING PAD : 60x60 um2 AL
OTHERS : 133 IN-LINE TYPE
PITCH = 90um
BONDING PAD : 60x60 um2 AL

Concluding remarks

- ***HEAD ON THE NEW SiTR-130_96 with a complete FE and readout chain on detector, higher multiplxing***
- ***with first attempt of bump-bonding the chip onto the detector (HPK),***
- ***Goal in 2008-2009 of EUDET and SiLC projects***
- ***It must equip all the modules in the beam tests starting end 2008 and will be pursued the years after.***
- ***At least one more foundry before end08/beg09***
- ***If chip sent to foundry on April 15, it will be tight in time for the beam tests on Fall this year and in time for the schedule with HPK on bump bonding tests.***

à suivre…..