Devt of CMOS Sensors for an ILC Vertex Detector:

Progress since Summer '07 — Plans for 2008

Marc Winter (IPHC-Strasbourg)

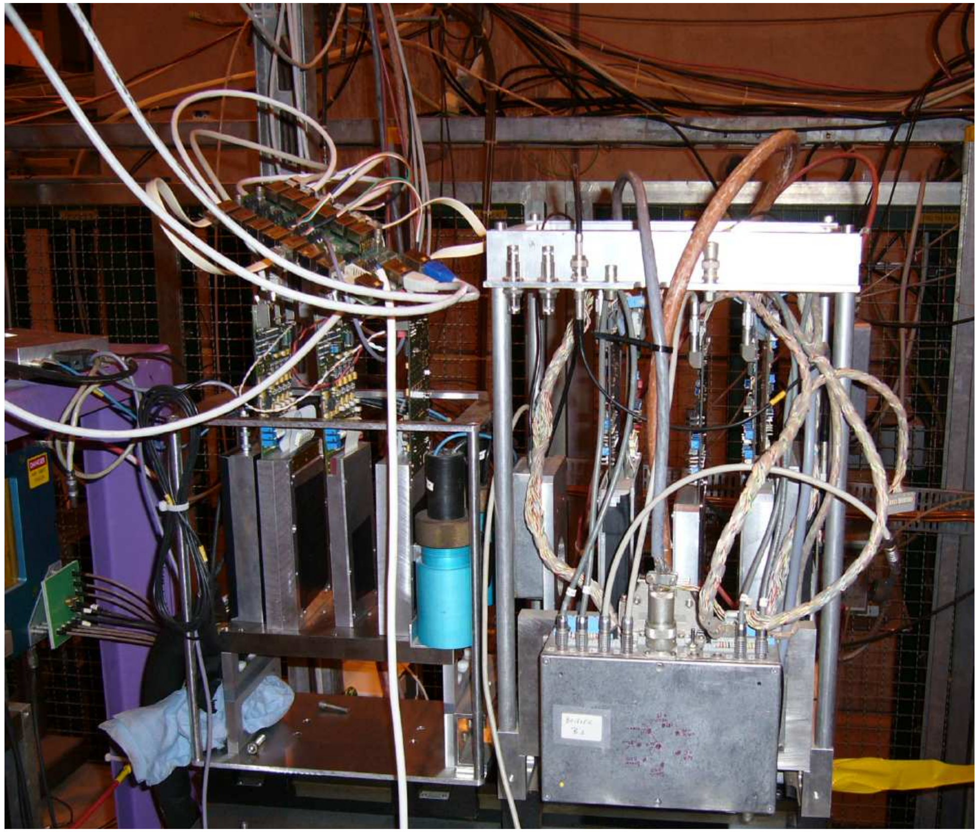
contributions from DAPNIA-Saclay, LPSC-Grenoble

▷ **More info. on IPHC Web site : http://wwwires.in2p3.fr/ires/web2/rubrique.php3?id_rubrique=63**

OUTLINE

- **Tests of sets of sensors in real experimental conditions :**
  - ⋇ **Beam telescopes : EUDET (European project), TAPI**
  - ⋇ **STAR HFT telescope**
- **Fast sensors with digitised outputs :**
  - ⋇ **Fast column // architecture with integrated discriminators : beam tests, new chips**
  - ⋇ **Zero-suppression micro-circuit : lab tests**
- **Summary & Plans for 2008**

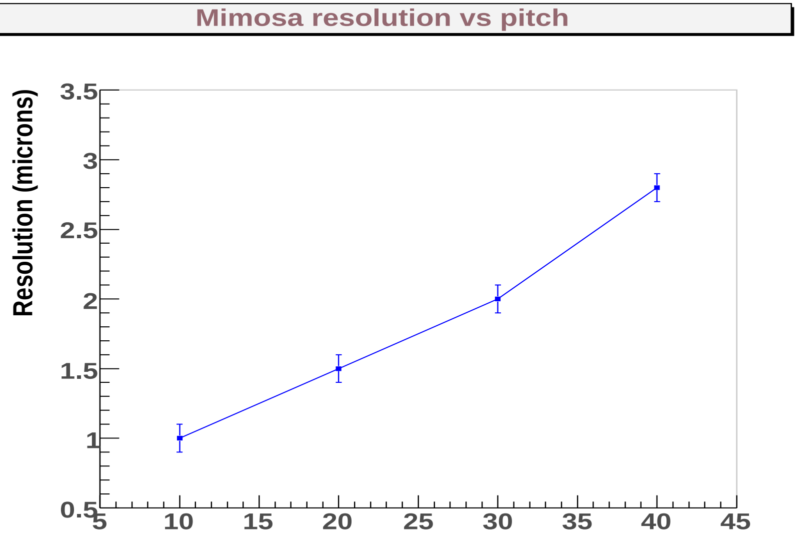
- **New beam telescope operated at DESY and CERN-SPS:**
  - ▷ **T.A.P.I.** ≡ **T**ELESCOPE **A** **P**IXELS DE L'**I**PHC
    - ◇ *3 or 4 MIMOSA-17 or/and -18 sensors (more in future)*
    - ◇ *Commissionning in June '07 at DESY*
    - ◇ *Real data taking in Sep. & Nov. '07 at CERN-SPS*
    - ◇ *R.o. freq. $\sim$ 10 (M-18) or 25 frames/s (M-17)*
    - ◇ *Running in front of Si-strip telescope ▷▷▷▷▷ ▷▷▷*



- **Several studies at CERN-SPS:**
  - *response of sensors to inclined tracks: 0 – 80°*
  - *performances of sensors exposed to non-ionising radiation*
  - *performances of thinned sensors*
  - *comparison of "14 μm" to "20 μm" epitaxy*

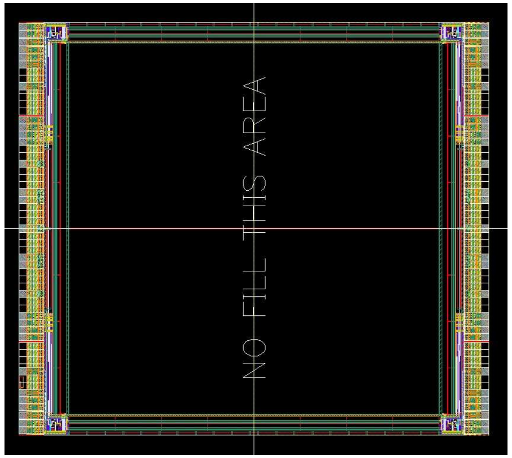
Beam test Results : Spatial Resolution

- **Single point resolution versus pixel pitch:**
  - clusters reconstructed with eta-function, exploiting charge sharing between pixels (12-bit ADC)
  - $\sigma_{sp} \sim 1\ \mu m$ (10 μm pitch) $\longrightarrow \lesssim 3\ \mu m$ (40 μm pitch)



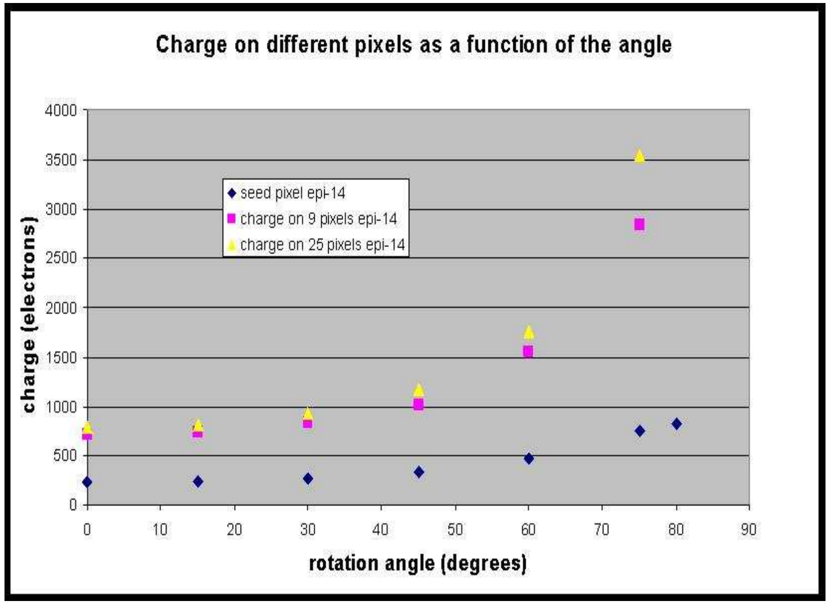
- **Recent result obtained with very small pitch :**
  - MIMOSA-18 : 512×512 pixels with 10 μm pitch, analog output, S/N $\sim$ 30
  - tested on Si-strip telescope at CERN-SPS (120 GeV π^-) in Nov. '07

  $\Rightarrow$ single point resolution observed (prelim.) $\lesssim$ 1 μm !!!
  $\hookrightarrow$ for EUDET telescope to allow $\lesssim$ 1 μm on DUT surface with few GeV e^- beam



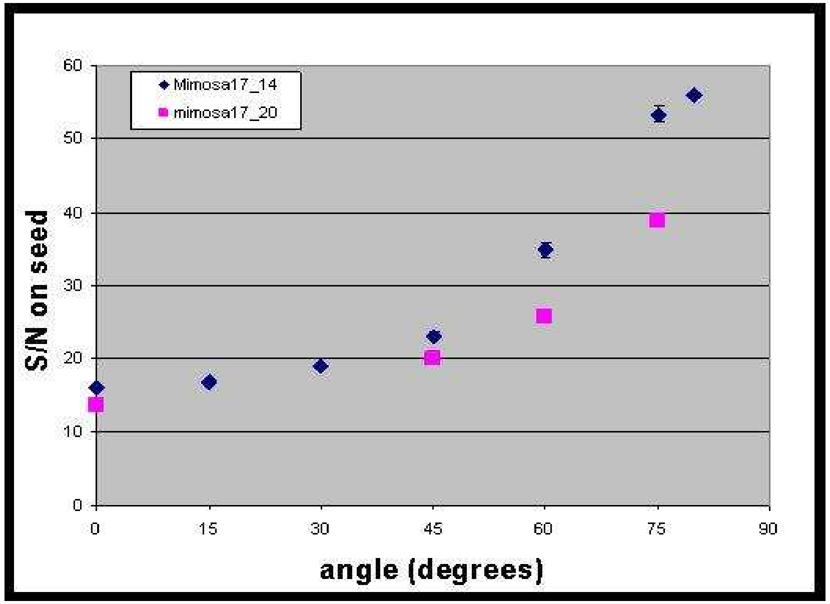
Motivation

- *simulate clusters from particules produced at shallow angle or from low $e^{\pm}_{BS}$ (low p $\rightarrowtail$ curling in ϕ)*
- *collect cluster data at various angles $\rightarrowtail$ data base*
- *adapt signal processing μcircuits and cluster rec. algo. to inclined tracks : 2–3 seed pixels, large signal, large clusters, ...*



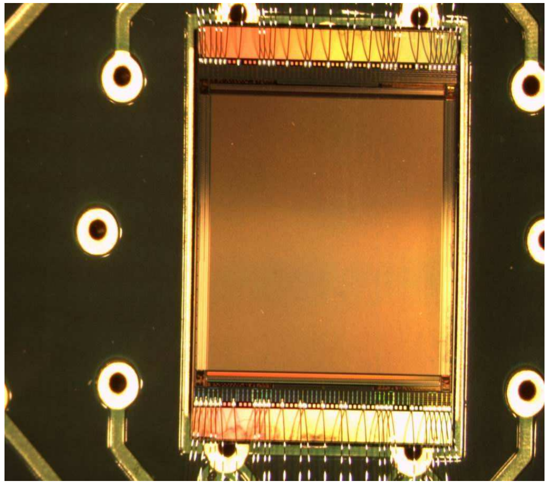
Measurements performed with TAPI at CERN-SPS

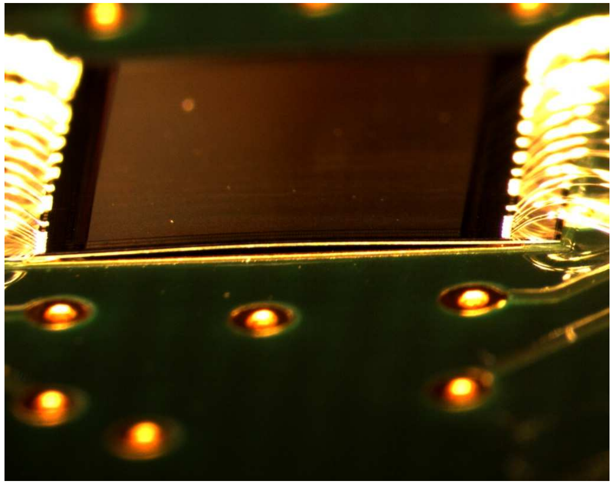
- *MIMOSA-17 (30 μm pitch, rad. tol. pixel), T_{room}*
- *measure Q, S/N, σ_{sp}, σ_{θ} at θ = 0, 15, 30, 45, 60, 75, $>$80°*
- *set-up data base for complete VD simulations (LoI)*
- *model cluster characteristics vs p & θ for "fast" VD simul.*
- *work performed together with Lukazc Maczewski (Warsaw)*
  (also: gyroscopic sensor support installed on DESY beam)



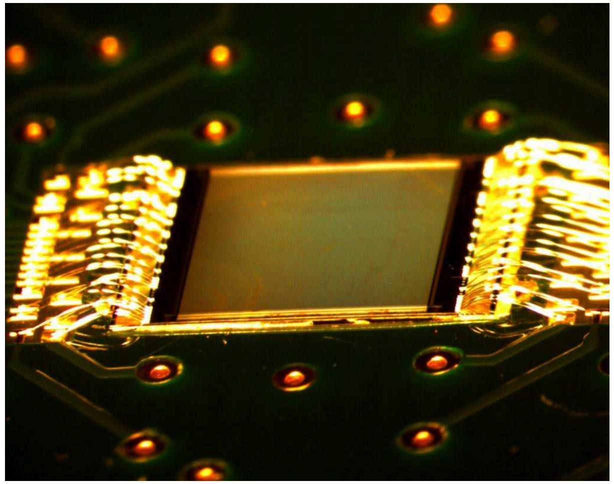
- **Thinning of AMS-0.35 engineering run reticles :**
  - *Thinning performed by APTEK (S.F. bay) via LBNL (STAR coll.)*
  - *Thickness claimed by provider : 50 μm $\rightarrowtail$ measured with IPHC bonding machine : $\sim$ 50–70 μm*
  - *MIMOSA-18 (5.5$\times$7.5 mm^2) & -17 (8$\times$9 mm^2) mounted on PCB for tests $\rightarrowtail$ keep them flat !*

MIMOSA-18: First gluing trial





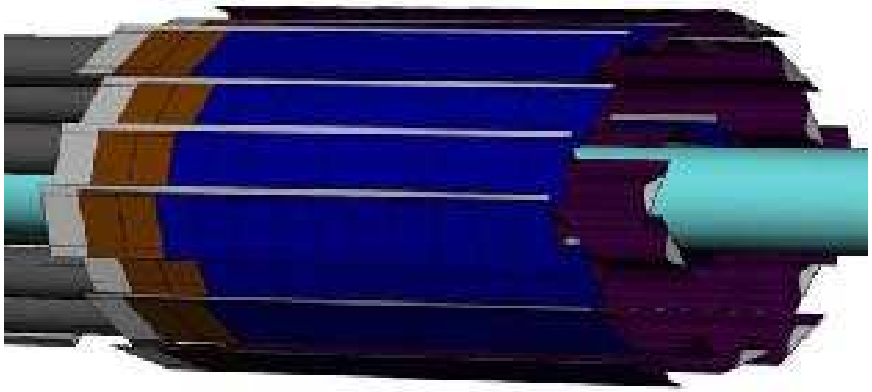
Second gluing trial



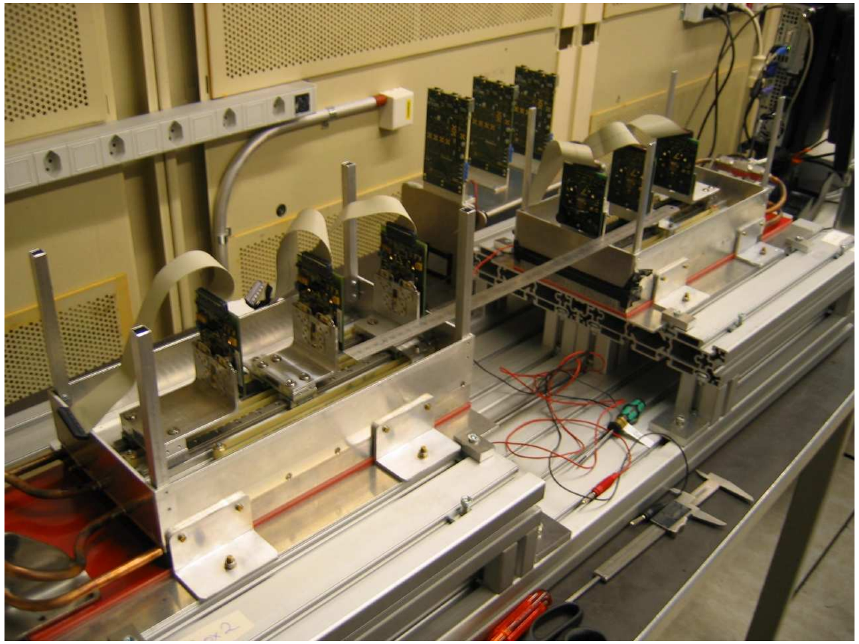
  - *Tests with ^{55}Fe source show no performance loss (noise, gain)*
  - *Tests of MIMOSA-18 mounted on TAPI with 120 GeV π^- at CERN-SPS (Nov. '07)*
    $\rightarrowtail$ *no performance loss observed* $\rightarrowtail$ $\epsilon_{\mathbf{det}}$ *= 99.79 $\pm$ 0.15 % (prelim.)*

- **Preliminary conclusion : Thinning down to $\sim$ 50 μm seems on a good track**

- **Vertex Detector upgrade for STAR expt at RHIC**
  - **2 cylindral layers : $\sim$ 1600 cm^2**
  - **$\gtrsim$ 160 million pixels ($\leq$ 30 μm pitch)**
  - **3 steps :**
  - ▷▷ **2007: telescope (3 MIMO-14) $\rightarrowtail$ BG meast, no pick-up !**
    - ◇ **2008/09: digital outputs without $\emptyset$ ($\leq$ 640 μs)**
    - ◇ **2010/11: digital outputs with integrated $\emptyset$ ($\leq$ 200 μs)**

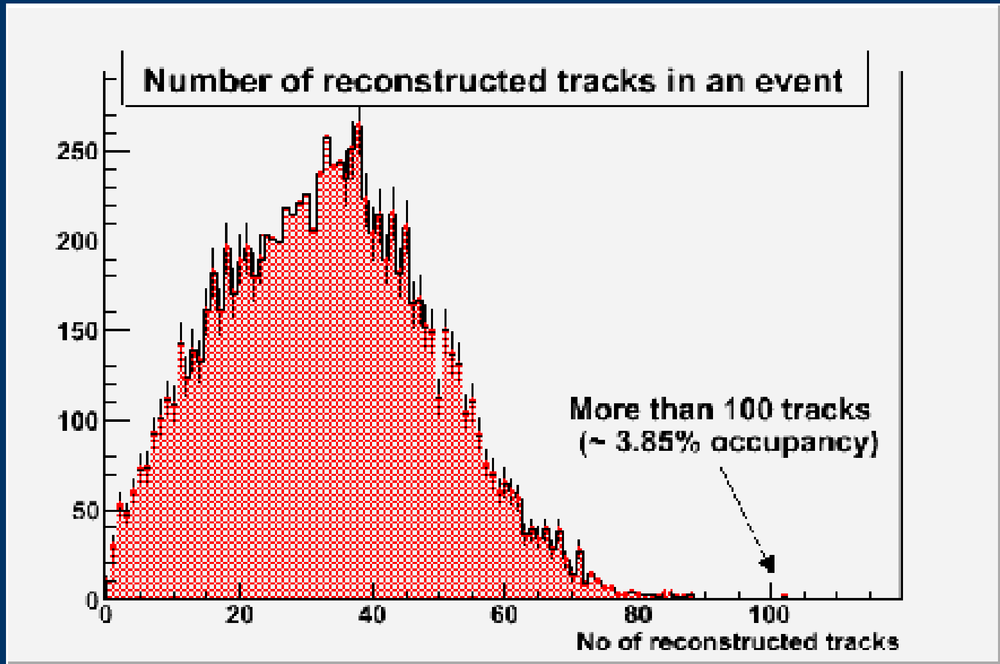


- **Beam telescope (FP6 project EUDET)**
  - **2 arms of 3 planes (plus 1 high resolution plane)**
  - **provide $\lesssim$ 1 μm resolution on 3 GeV e$^-$ beam (DESY)**
  - **2 steps :**
  - ▷▷ **2007: analog outputs**
    - $\rightarrowtail$ **telescope commissionned & running ($\lesssim$ 100 tracks / frame)**
    - $\rightarrowtail$ **used by non JRA-1 members at SPS (e.g. SILC)**
  - ◇ **2008/09: digital outputs with integ. $\emptyset$ ($\sim$ 100 μs)**



Performances...

- This impressive plot is showing the pretty mature development stage of the tracking software.



CERN large multiplicity data taken two weeks ago

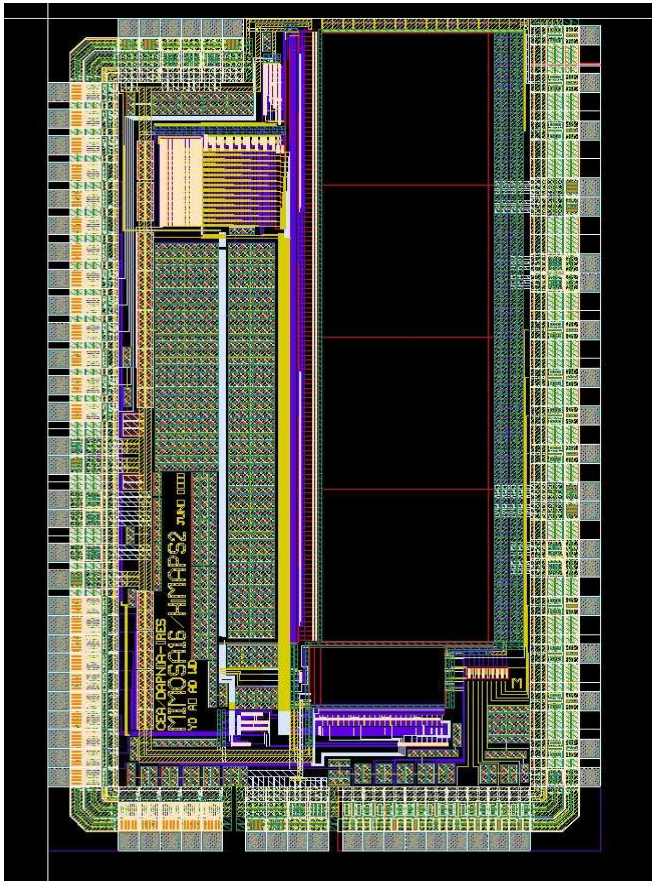
Integration of Signal Processing

Inside Pixels and on Chip Periphery

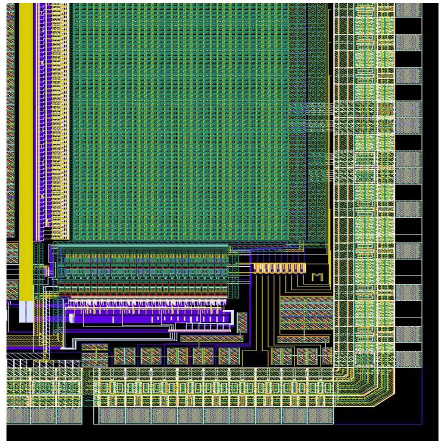
High R.-O. Speed Architecture : 2nd Prototype = MIMOSA-16

MIMOSA-16 design features :

- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–15 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (DS at end of each column)
- 24 columns ended with discriminator
- 4 sub-arrays :
  - S1 : like MIMOSA-8 (1.7x1.7 μm^2 diode)
  - S2 : like MIMOSA-8 (2.4x2.4 μm^2 diode)
  - S3 : S2 with ionising radiation tol. pixels
  - S4 : with enhanced in-pixel amplification (against noise of read-out chain)



$\Rrightarrow$



Tests of analog part ("20" & "14" μm epitaxy) :

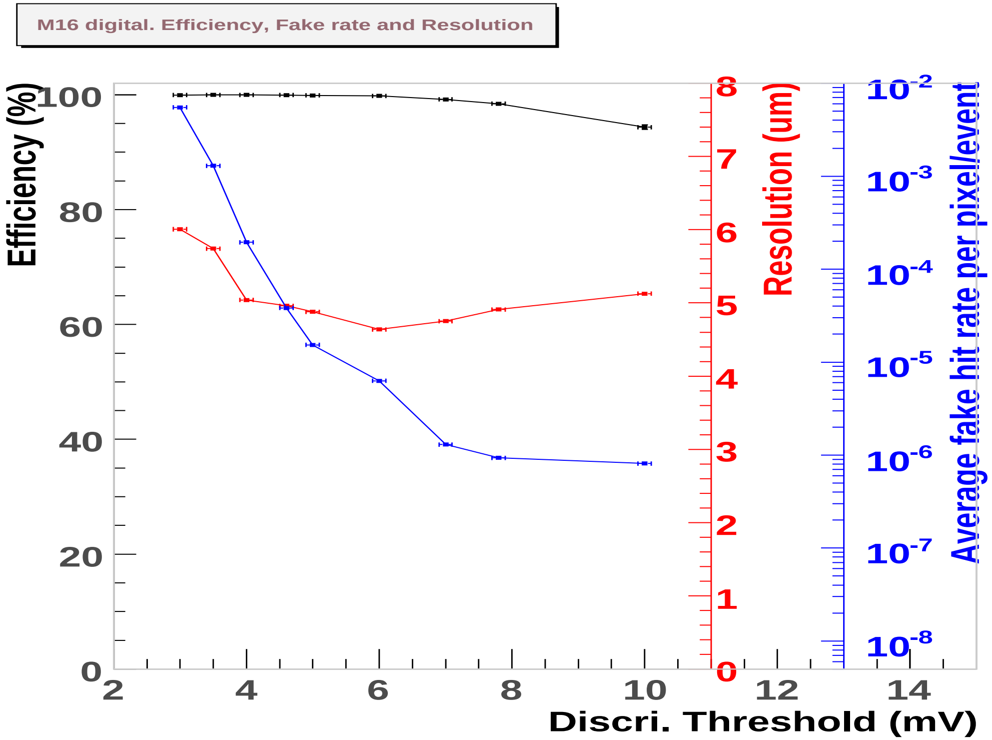
- sensors illuminated with ^{55}Fe source and $F_{r.o.}$ varied up to $\gtrsim$ 150 MHz
- measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs $F_{r.o.}$

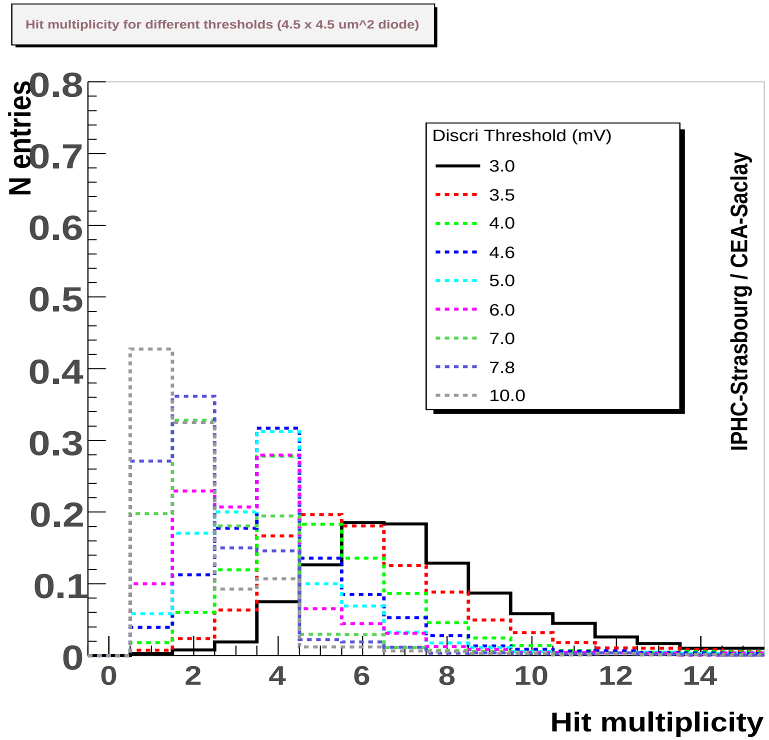
M.i.p. detection with Si-stip telescope studied at CERN in Sept. '07 $\longrightarrow$ characterisation of digital response :

- π^- beam of $\sim$ 180 GeV/c
- measurements of SNR, det. efficiency, fake rate, cluster characteristics, spatial resolution vs discri. threshold

MIMOSA-16 Beam Test Results (Digital Part)

- **CERN-SPS ($\sim$ 180 GeV π^-) $\longmapsto$ results of S4 ("14 μm" epitaxy)**
- **Read-out time $\sim$ 50 μs** ($\sim$ *1/4 of max. freq. due to DAS limitations)*

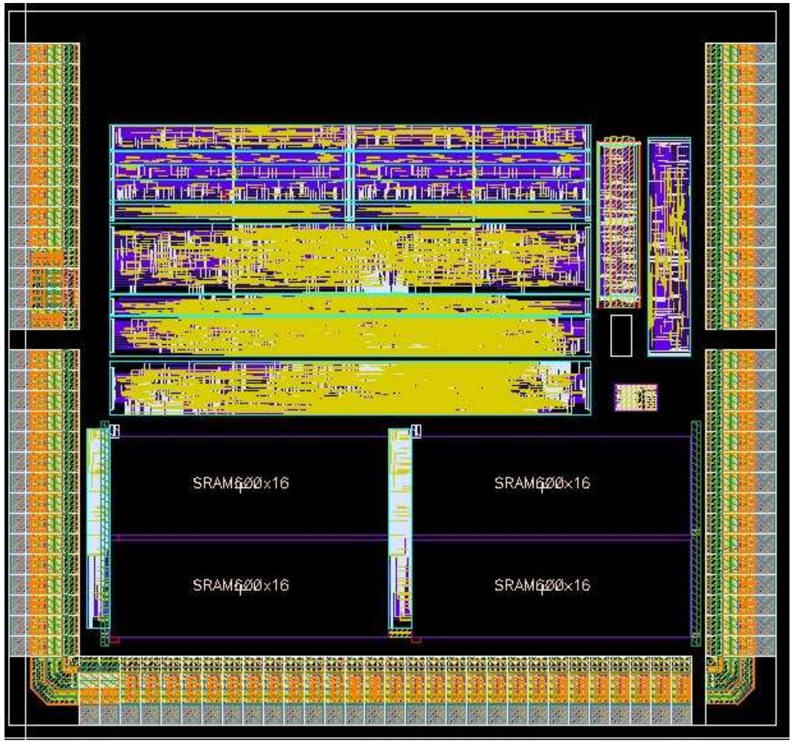




- **Major result $\longmapsto$ at least one pixel architecture validated for next steps : S4 (SNR $\sim$ 16)**

Discri. Threshold	*det. efficiency*	*fake rate*	*sgle pt resolution*
4 m V	*99.96 $\pm$ 0.03 (stat) %*	$\sim$ *2·10^{-4}*	$\sim$ *4.8–5.0 μm*
6 m V	*99.88 $\pm$ 0.05 (stat) %*	*<10^{-5}*	$\sim$ *4.6 μm*

■ **1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :**



⋇ 2 step, raw by raw, logic :

◇ step-1 (inside blocks of 64 columns) :

identify up to 6 series of $\leq$ 4 neighbour pixels per raw

delivering signal $>$ discriminator threshold

◇ step-2 : read-out outcome of step-1 in all blocks

and keep up to 9 series of $\leq$ 4 neighbour pixels

⋇ 4 output memories (512x16 bits) taken from AMS I.P. library

⋇ surface $\sim$ 3.9 $\times$ 3.6 mm^2

■ **Status :**

⋇ back from foundry end of Sept. '07 $\longrightarrow$ tests almost completed

⋇ design performances reproduced up to 1.15 $\times$ design read-out frequency (T$_{room}$) :

$\triangleright$ noise values as predicted, no pattern encoding error

Final prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 ⟶ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

■ Pixel characteristics (*optimal charge coll. diode size ?*) :

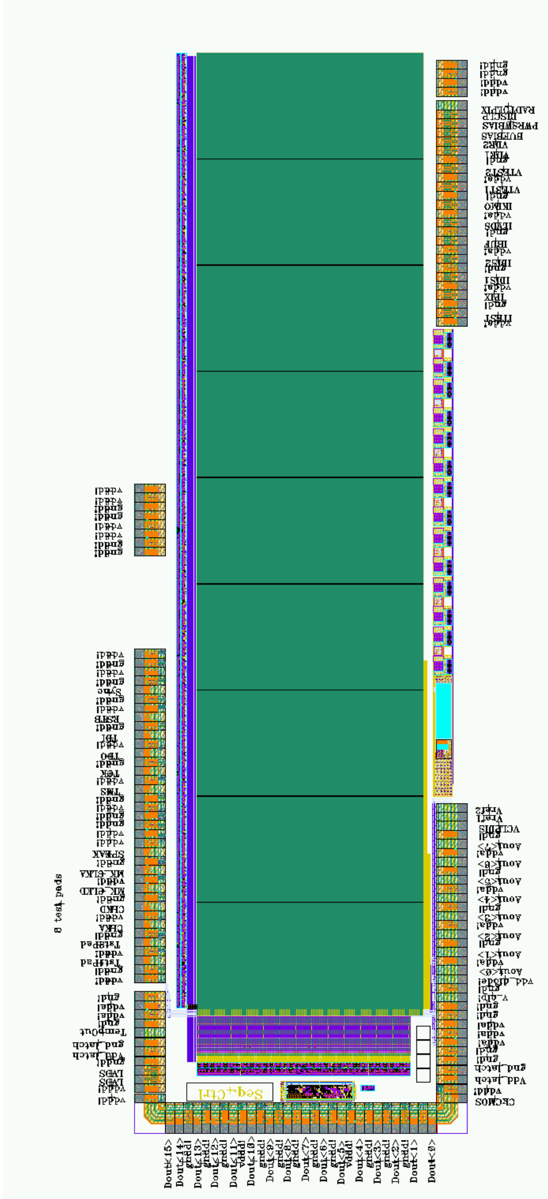
- ⋇ pitch : 18.4 μm (compromise resolution/pixel layout)
- ⋇ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ⋇ 128 columns ended with discriminator
- ⋇ 8 columns with analog output for test purposes
- ⋇ 9 sub-matrices of 64 rows :
  - 17 pixel designs w/o ionising rad. tol. diode
  - $\Rightarrow$ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)
- ⋇ read-out time $\sim$ 100 μs

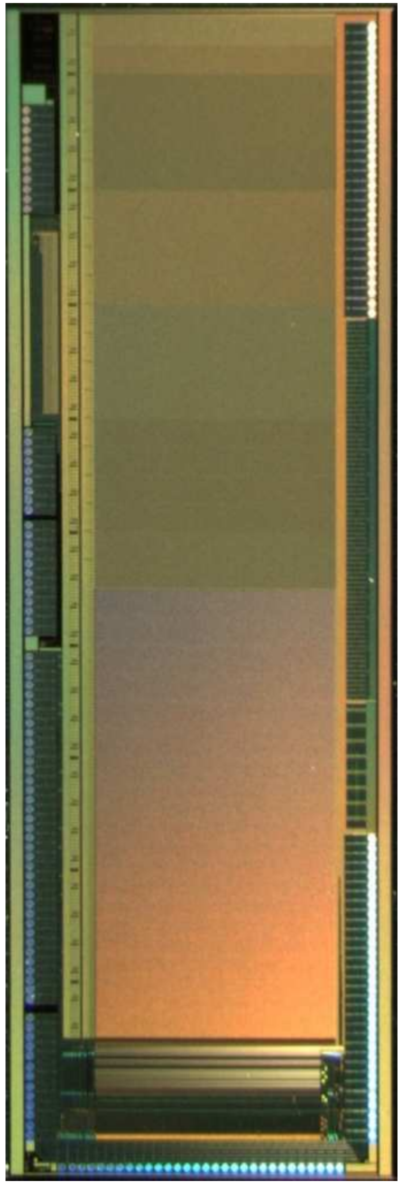
■ Testability :

- ⋇ JTAG + bias DAC ⟶ programmable chip steering
- ⋇ 2 additionnal DC voltages to emulate pixel's output
  for independent discriminator performance assessment
- ⋇ output frequency $\leq$ 40 MHz

■ Status :

- ⋇ Back from foundry ⟶ tests started in Feb.'08 (analog outputs)
  - ▷ ^{55}Fe source : chip active over whole surface (35°C, 92 μs)





SUMMARY

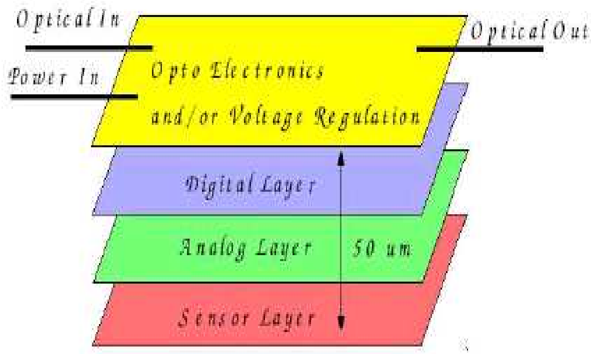
- **Steady progress towards perfo. adapted to running conditions with beam BG $>>$ MC simulations**

- **2007 :**
  - ⁂ *several achievements (beam tests) and progresses on sensor R&D :*
    fast col. // architecture with discri. output, μ-circuit, spatial resolution, inclined tracks etc.
  - ⁂ *successful 1st experimental use of small sets of sensors $\rightarrowtail$ telescopes: EUDET-JRA1, TAPI, STAR*
  - ⁂ *progress on syst. integration aspects : thinning, power cycling, ladder, etc.*

- **2008 :**
  - ⁂ **final EUDET telescope sensor fab.: 1$\times$2 cm^2; 0.6 Mpix; 100 μs; digital output with $\emptyset$; 50 μm thin**
  - ⁂ **STAR-HFT1 sensor fab.: 2$\times$2 cm^2; 0.4 Mpix; 640 μs; digital output; 50 μm thin $\rightarrowtail$ D^0 phys. in 2010**
  - ⁂ *several other R&D lines: fast archi. with ADC, new fab. proc., system integ., etc. $\rightarrowtail$ FP-7*
  - ⁂ *vertex detector design optimisation with physics processes $\rightarrowtail$ LoI*

- *$>$ 2008 :*
  - ⁂ *proto-ladder for outer/inner layers in 2010/2011 ($\lesssim$ 0.2 % X$_0$), based on STAR-HFT ladder ($\lesssim$ 0.28 % X$_0$)*
  - ⁂ *final sensor designs for outer/inner layers in 2010/2011*
  - ⁂ *STAR-HFT2 sensor (data taking starting in 2011)*

- *Perspective : 3DIT MIMOSA $\equiv$ 4 chip sandwich*
  $\hookrightarrow$ *optimal technology for each tier*



BACK-UP SLIDES

Pixel design :

- ✳ adapt existing pixel architectures from 25 μm to $<$ 20 μm pitch
- ✳ adapt sensing diode dimensions to maximise CCE (surface $\nearrow$) & gain (surface $\searrow$) : optimum $\sim$ 10–15 μm^2
- ▶ find optimal pixel pitch : single point resolution (pitch $\searrow$) against reliable design (pitch $\nearrow$)

Column read-out architecture :

- ✳ adapt existing S&H and discriminators from 25 μm to $<$ 20 μm pitch
- ✳ integrate $\emptyset$ and output memories

Row and pixel steering (consequences of large surface) :

- ✳ adapt pixel steering (speed) inside column to avoid capacitance due to large nb of switches $\rightarrowtail$ pixel design
- ✳ adapt row steering to their length (2 cm)

Sensor autonomy and testability :

- ✳ JTAG + bias DAC $\rightarrowtail$ programmable chip steering
- ✳ 2 or 3 additionnal DC voltages to emulate pixel's output for independent discriminator performance assessment

Major R&D Milestones in Next 5 Years

- **Developments simultaneously oriented towards well focussed applications and towards generic objectives useful to several applications**

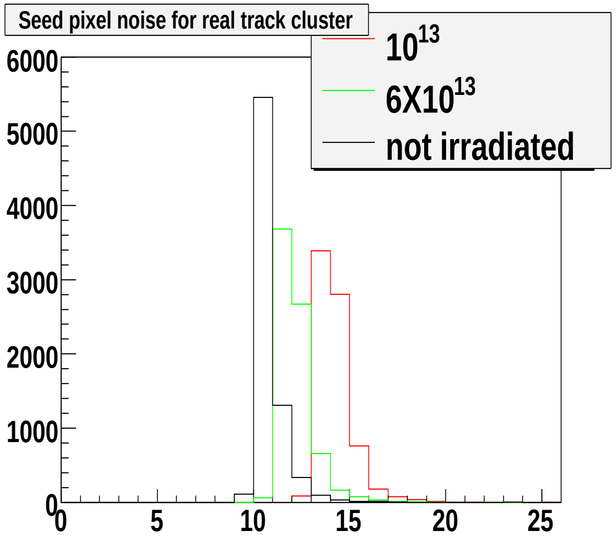
Application	version	2006	2007	2008	2009	2010	2011
STAR	HFT-1	R&D	final proto.	Prod.			
	HFT-2	R&D	R&D	R&D	proto final	Prod.	
EUDET	BT-1	2 Prod.	commissioned				
	BT-2	R&D	final proto	Prod.			
Imaging		R&D	final proto	Prod. ?			
Generic topics							
Fast sensors :	○ architecture	R&D	R&D	R&D +	R&D ++	ILC proto	CBM proto
	○ ADC	R&D	R&D	final proto	↗		
	○ digital	pre-study	R&D	final proto	↗		
Radiation tolerance		R&D	R&D	R&D	R&D	↗	
Fabrication technologies		R&D	R&D	R&D	R&D	↗ ???	
Thinning		R&D	D	D	OK ???		

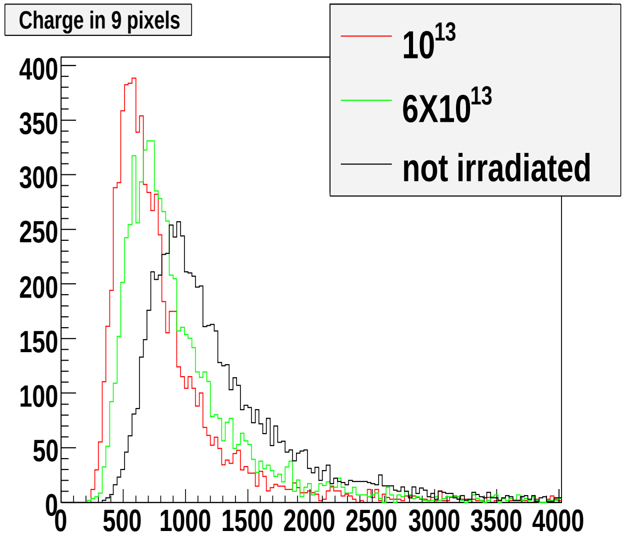
- Established ionising radiation tolerance (reminder): **1 MRad – $2{\cdot}10^{12}$ n_{eq}/cm^2 – 10^{13} $e^-_{10\ MeV}$/cm^2 OK**

- Non-ionising radiation tolerance (Summer / Autumn 2007):

  ⋇ **MIMOSA-18 irradiated with $\lesssim 10^{13}$ O(1 MeV) n/cm^2 (+ 100–200 kRad γ gas) $\Rrightarrow$ tested on $\sim$ 120 GeV π^- beam (SPS)**

  ▷ **Preliminary results:** • T = -20°C • $t_{r.o.} \sim$ 3 ms • cuts at 5N (seed) & 2N (crown)





Fluence (n_{eq}/cm^2)	0	$6{\cdot}10^{12}$	$1{\cdot}10^{13}$
Noise (e^- ENC) (-20°C, 3 ms, 5N/2N)	10.8 $\pm$ 0.3	12.2 $\pm$ 0.3	14.3 $\pm$ 0.3
Q_{clust} (e^-)	1026	680	560
S/N (MPV)	28.5 $\pm$ 0.2	20.4 $\pm$ 0.2	14.7 $\pm$ 0.2
Det. Eff. (%)	99.93 $\pm$ 0.03	99.85 $\pm$ 0.05	99.5 $\pm$ 0.1

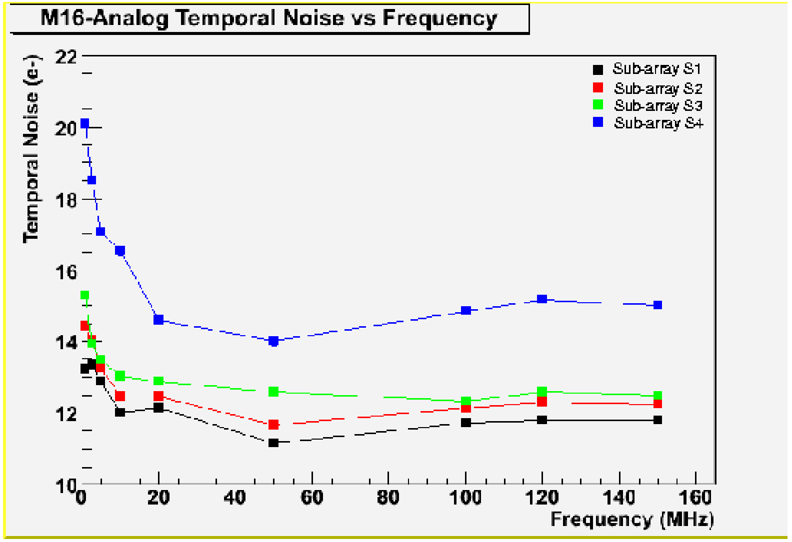
- $\sim 10^{13}$ n/cm^2/s affordable at T $<$ 0°C & $t_{r.o.} \sim$ O(1) ms & 10 μm pitch

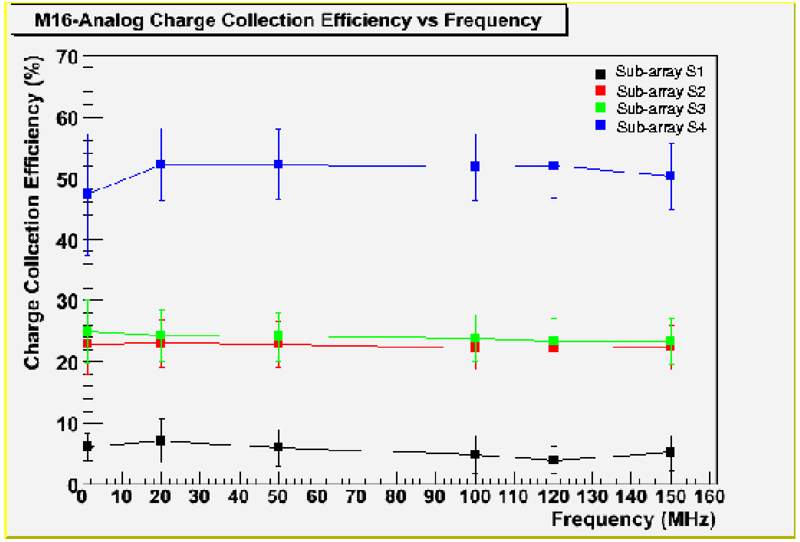
  $\hookrightarrow$ **study tolerance vs pitch, diode size, r.o. speed, digital output, ... , annealing ?????**

Integration of Signal Processing

Inside Pixels and on Chip Periphery

Pixel noise and charge collection efficiency (*"20 μm" epitaxy*) :





08/01/07 Résumé résultats Mimosa-16 chip#0 08/01/07 Résumé résultats Mimosa-16 chip#0

$\Rrightarrow$ **Noise performance satisfactory (**like MIMOSA-8 and -15**)**

$\Rrightarrow$ *CCE: very poor for S1* (1.7x1.7 μm^2) *& poor for S2/S3* (2.4x2.4 μm^2)

$\rightarrowtail$ *already observed with MIMOSA-15 but more pronounced for "20 μm" option*

$\hookrightarrow$ suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 μm^2 diode)

- **Next steps :**
  - Mid-term : *EUDET, STAR $\rightarrowtail$ real experimental conditions*
  - Long-term *full sensor prototyping : CBM (and ILC)*

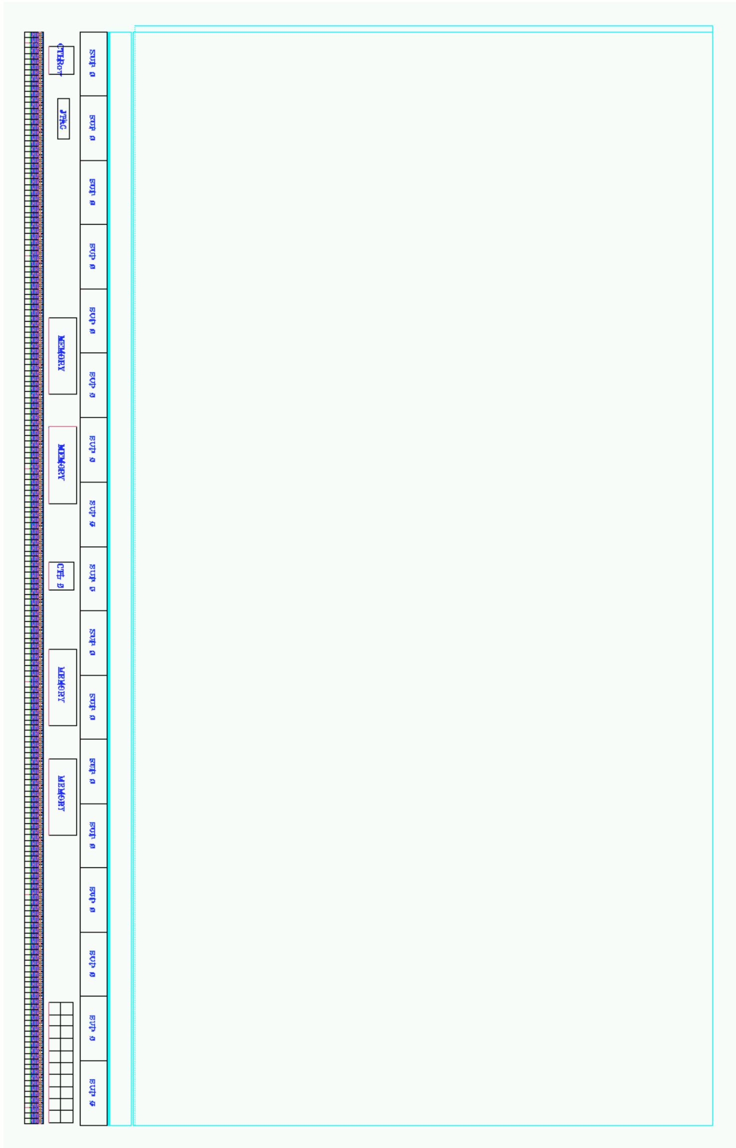
- **Integrated $\emptyset$ $\rightarrowtail$ real scale sensors without ADC ($\sigma_{sp} \sim$ 4–6 μm) :**
  - ⋇ *EUDET telescope (2008)*
  - ⋇ *STAR-HFT1/2 (2010/11)*
  - ⋇ *CBM-MVD ($\gtrsim$ 2012)*

- **Increasing read-out speed and replacing discriminators with 4-5 bit ADC (ILC) :**
  - ⋇ *read-out speed $\rightarrowtail$ CBM-MVD ($\gtrsim$ 2012)*

Autumn 2008 : MIMOSA-22^{+} = Final EUDET Sensor

- **MIMOSA-22 complemented with $\emptyset$ (SUZE-01)**
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm^2)
- Read-out time $\sim$ 100 μs
- Chip dimensions : $\sim$ 20 x 12 mm^2

▷ Opportunity for an engineering run combining various chips (N.I. rad. tol. ?)



Devts performed in // :

- June 2008 : submission of final STAR-HFT1 sensor
  - ▷ $\sim$ 2 $\times$ 2 cm^2 ⁕ 400 kpix/sensor ⁕ $\leq$ 640 μs ⁕ 50 μm thin
  - $\hookrightarrow$ equip 2 or 3 sectors of 1 + 3 ladders (10 chips/ladder)
- explore new tracks : XFAB, IBM-0.18 OPTO, 3DIT, ...

Beyond 2008:

- **design sensor for STAR-HFT2** $\rightarrowtail$ extension of MIMOSA-22^{+}
- **increase r.o. frequency** by $\sim$ 50 % (new $\emptyset$ & memory design)

System Integration Studies

- Thinning
- Ladder design
- Data Flow

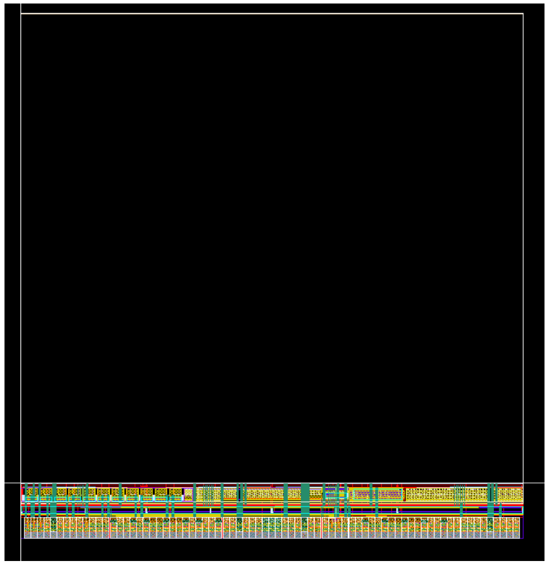
Thinning

Thinning motivations and constraints :

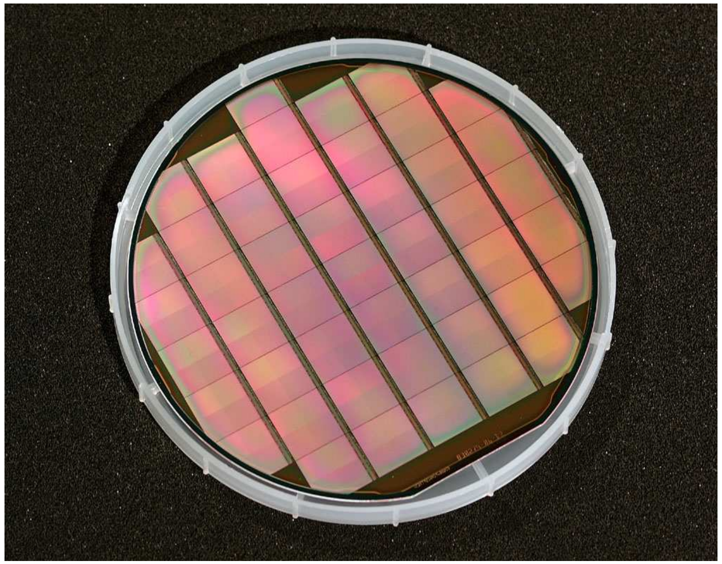
- *thin sensors to $\lesssim$ material budget of "mechanical support"*
- *minimal thickness of CMOS sensors :*

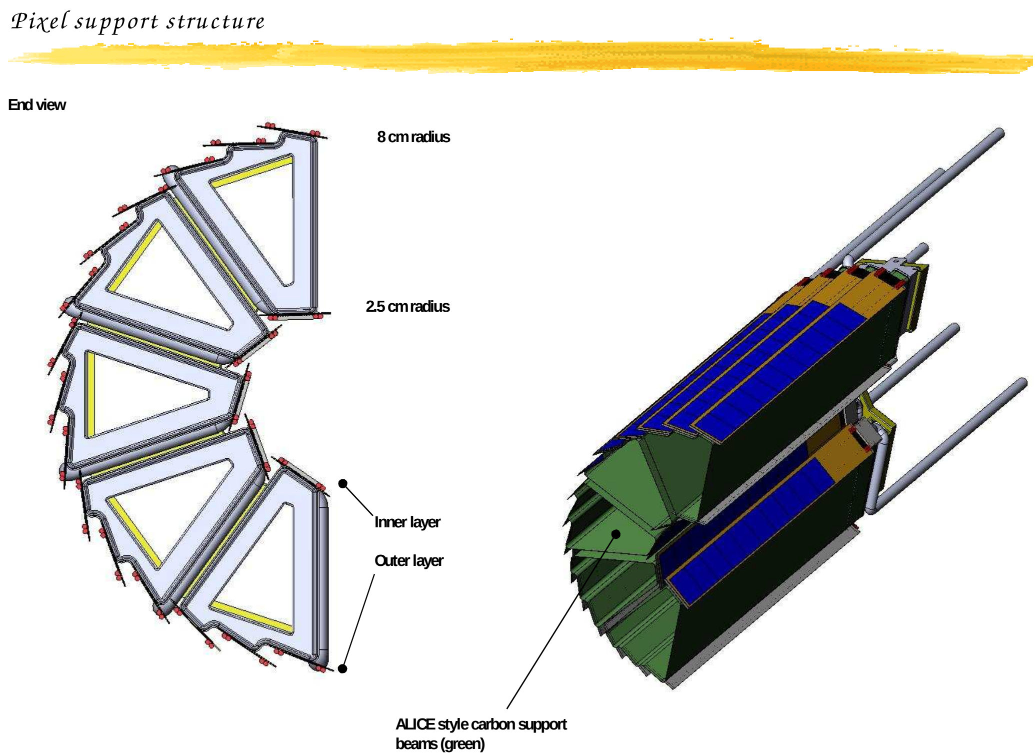
  10–15 μm (metal layers and SiO_2) + 15 μm (T + epitaxy) + 5–10 μm (substrate) $\approx$ 30–40 μm
- *thinned sensors should be "easy" to handle*
- *thinning procedure should have high mechanical yield and preserve detection performances*
- *CMOS technology fab. yield $\rightarrowtail$ foster diced sensors (despite few 10^{-4} X_0 add. mat. budget / ladder)*
- *thinning of individual sensors seems preferable to full wafer thinning : cheaper but same quality ?*

MIMOSA-17 : 8 x 9 mm^2



MIMOSA-5 : 6" wafer

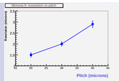




- **Predominantly driven by STAR HFT project at LBNL**

- **Thinning of MIMOSA-5 wafers :**
  - *3 wafers thinned via LBNL to 50 $\pm$ 5 μm*
  - *result satisfactory (after pre-dicing):*
    sensors can be manipulated and mounted on support
  - *3 ladder prototypes fabricated at LBL ($\gtrsim$ 0.25 % X_0)*
    $\rightarrowtail$ up to 9 sensors mounted on ladder and tested

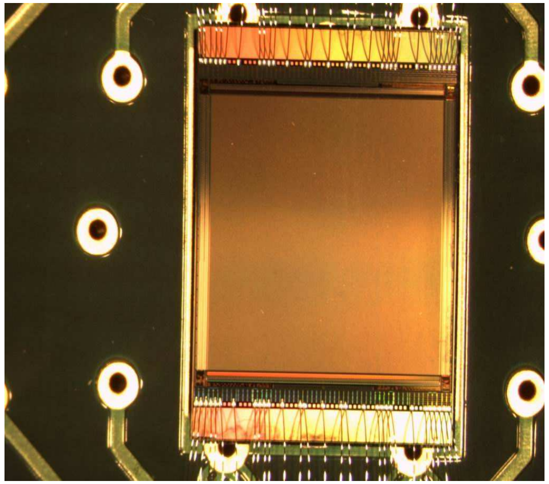
- **Thinning of individual sensors to $\sim$ 50 μm:**
  - *several chips of $\sim$ 0.2 – 3.5 cm^2 (MIMOSA-5, -10, -14, -17, -18, -20, etc.) thinned individually via LBNL*
  - *recent result: MIMOSA-18 prototype thinned to 50 μm was successfuly tested with ^{55}Fe at IPHC*
    $\rightarrowtail$ no change of performances (e.g. noise, gain, det.eff, ...) $\rightarrowtail$ next slide
  - *Plans :*
    - *replace present (thick) sensors (MIMOSA-17, -18) equipping telescopes (EUDET, TAPI, ...)*
    - *equip STAR-HFT1 with thinned sensors (2008/09) $\rightarrowtail$ 0.25 – 0.3 % X_0*
    - *extend ladder devt to ILC Vertex Detector (LBNL-ILC team ?) $\rightarrowtail$ goal $\leq$ 0.2 % X_0*

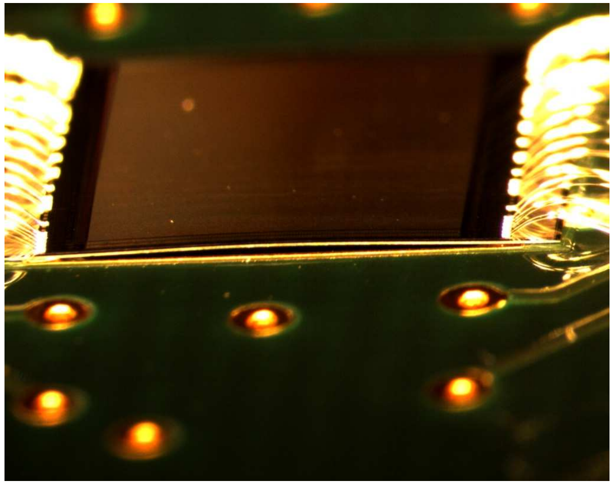


Thinning of Diced Sensors

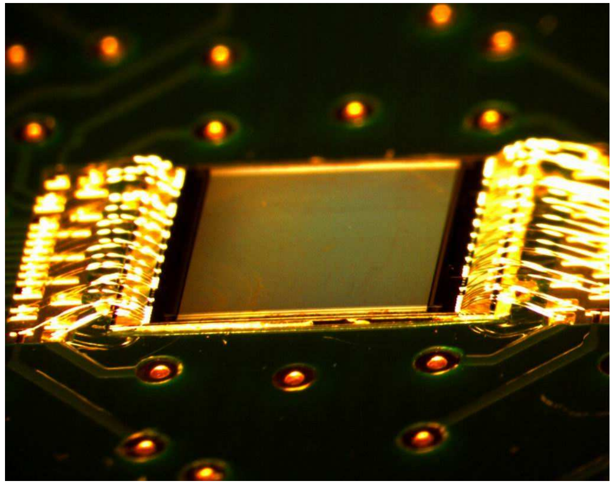
- **Thinning of AMS-0.35 engineering run reticles :**
  - *Thinning performed by APTEK (S.F. bay) via LBNL (STAR coll.)*
  - *Thickness claimed by provider : 50 μm $\rightarrowtail$ measured with IPHC bonding machine : $\sim$ 50–70 μm*
  - *MIMOSA-18 (5.5$\times$7.5 mm^2) & -17 (8$\times$9 mm^2) mounted on PCB for tests $\rightarrowtail$ keep them flat !*

MIMOSA-18: First gluing trial





Second gluing trial



  - *Tests with ^{55}Fe source show no performance loss (noise, gain)*
  - *Tests of MIMOSA-18 mounted on TAPI with 120 GeV π^- at CERN-SPS (Nov. '07)*

    $\rightarrowtail$ *no performance loss observed* $\rightarrowtail$ $\epsilon_{\mathbf{det}}$ *= 99.79 $\pm$ 0.15 % (prelim.)*

- **Preliminary conclusion : Thinning down to $\sim$ 50 μm seems on a good track**

- **Data flow:**
  - *hundreds of millions of fast pixels $\Rrightarrow$ data flow is a MAJOR CONCERN !!!*
  - *U.L.M. Photonics : 250x250 μm^2 electro-optical converters $\rightarrowtail$ several Gbits/s*
  - *design of laser driver under study at IPHC*

- **New concept of mechanical support & heat extractor:**
  - *objective : mount, connect & operate $\sim$ 4 MIMOSA-18 (?) sensors, thinned to 50 μm, on 50–100 μm thin, aluminised, CVD diamond slabs $\equiv$ mech. support – heat extractor - cable support*
  - *status : 3 diamond 3" wafers fabricated $\rightarrowtail$ electroplating and lithography, etc.*

    $\rightarrowtail$ proto-ladders back at IPHC-Strasbourg before Summer

- **General remark :**
  - *CMOS sensors call for* CHALLENGING *system integration solutions : connexions (flex cable), data flow, ...*
  - **Lot of expertise and effort needed $\Rrightarrow$ Forces needed NOW !**

The Economy of Material Budget

- **Minimise multiple scattering inside detector material wherever possible** ($b \searrow$)

  ↪ *thickness, amount and choice of material for mechanical support, gluing, electrical connexions, thermal conductivity, power dissipation (avoid active cooling), ...*

- **Goal :** $<$ **0.2 % radiation length / layer** *(including chip + support + services)* *(* $\Leftrightarrow$ $<$ *200* μm *of silicon)*

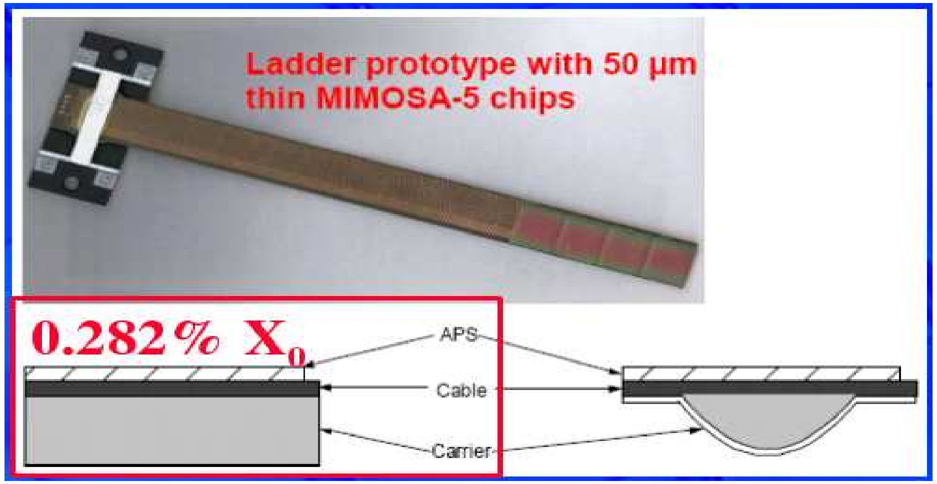
- **Presently** $<$ **0.3 % seems achievable** *(STAR vertex detector)*

- **STAR ladder : kapton cable contributes with 0.090 %**

  and carrier with 0.110 % of radiation length

  $\Rrightarrow$ **replace them with aluminised CVD diamond ?**

  ↪ *bonus in thermal transport*

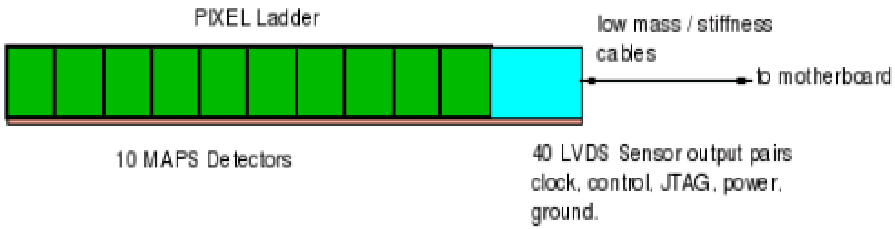


- **(CMOS) Sensor fabrication yield is a concern**

$\Rrightarrow$ **diced sensors prefered to stitched sets of 5–10 sensors**

↪ **inactive zones (**$\gtrsim$ **40** μm **wide) at sensor edge from dicing**

$\Rrightarrow$ **can these zones be reduced to** $\lesssim$ **few** μm **with plasma etching ?**



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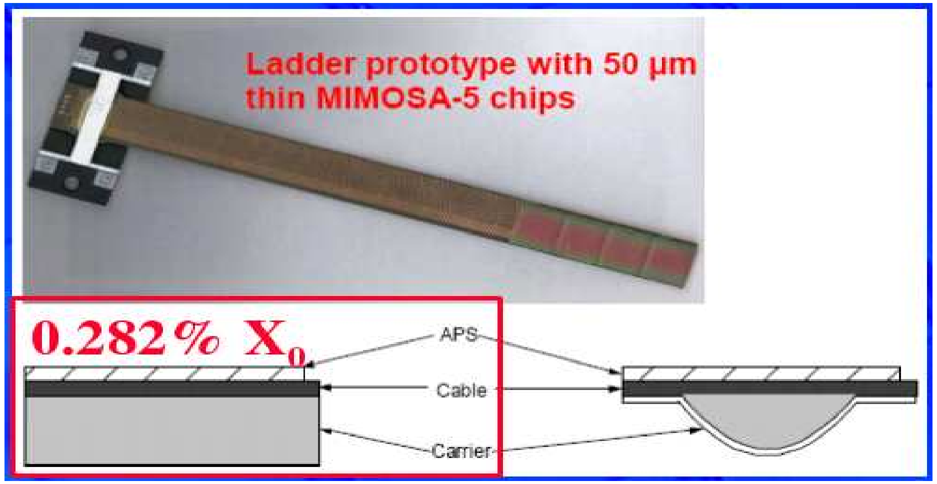

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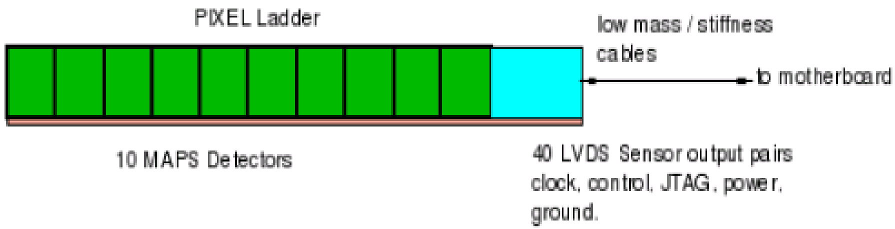

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► **3D Integ. Techno. include thinning and dicing capacities of great interest**