Silicon Strip Sensor R&D and results from HPK sensor measurements

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HEPHY-Vienna

Outline:
- SiLC “Sensor Baseline”
- Status of companies
- Results from HPK

March 5th, 2008

SilC Silicon Sensor Baseline

- **SilC sensor baseline**
  - FZ p-on-n sensors: n-bulk material, p+ implants for strips
  - high resistivity (5-10 kOhm cm)
  - Readout strip pitch of 50µm
    - Possibly intermediate strips in between (resulting 25µm pitch)
    - Smaller pitch becomes very complicated (Pitch adapter, bonding, charge sharing,…)
  - Thickness around 100-300µm
    - mostly limited by readout chip capabilities (S/N ratio)
  - **Low current:**<1nA per strip

  (Due to long integration time noise mostly defined by current and resistors)

- **Baseline for inner layers:**
  - 6” inch, Double sided, AC coupled

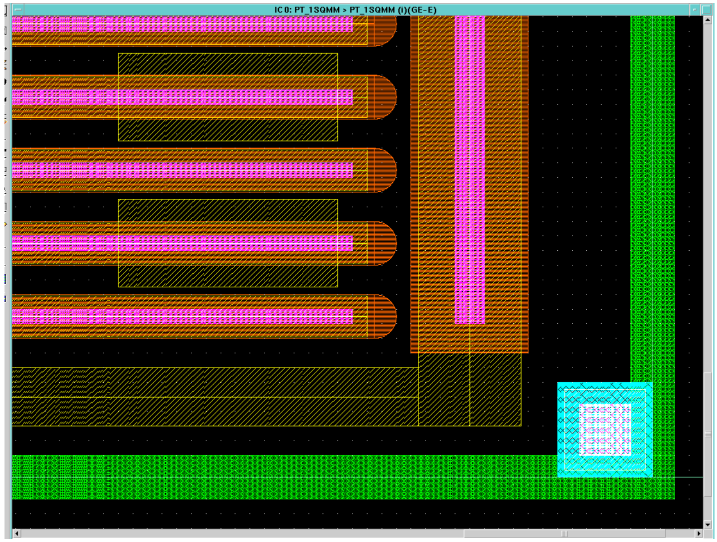
- **Baseline for outer layers:**
  - 8” (12”?) inch, Single sided, Preferably DC coupled (cheaper)

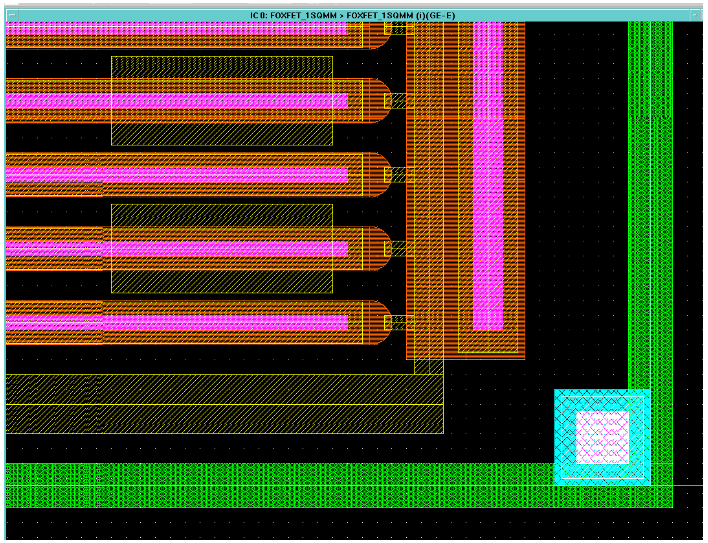
Sensor Baseline Details

Biasing Possibilities:

- bias resistor with **poly-silicon** (20 to 50 MOhm)

- **punch-through** (upper picture)
- or **FOXFET** biasing structure (lower picture)
  - Latter two have non-linear behavior
  - But are cheaper





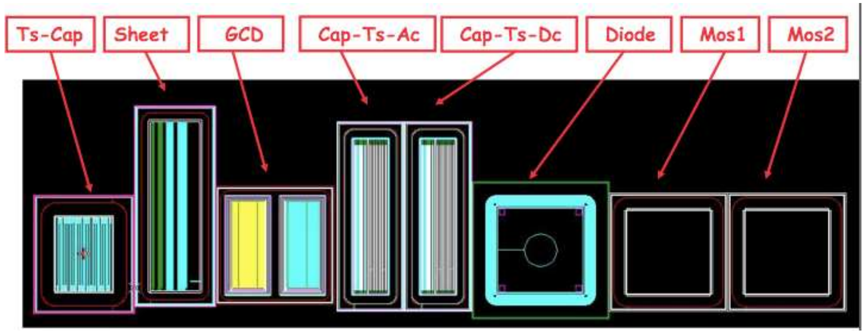
SiLC
Silicon for the Linear Collider

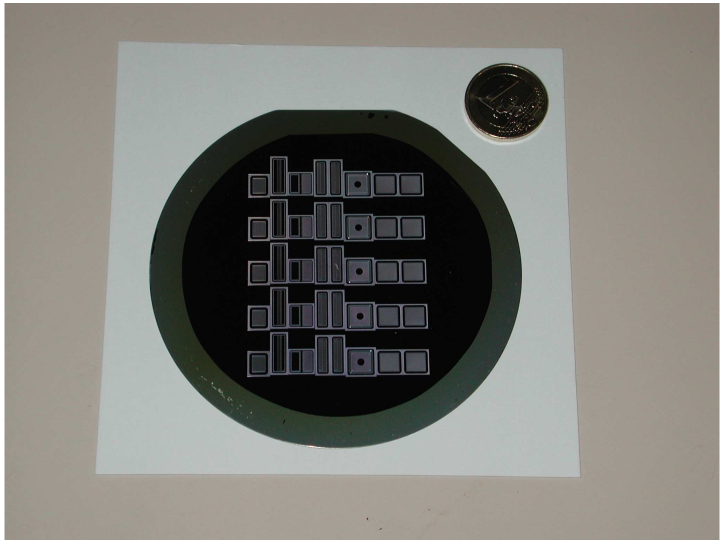
Status of the sensor producers

IET Warsaw

- Contact established with *Institute for Electron Technology* already three years ago
- They have experience with SOI and chip production, but not with fully depleted devices yet.
- Goal: develop test structures based on CMS ‘half-moon’, but improved

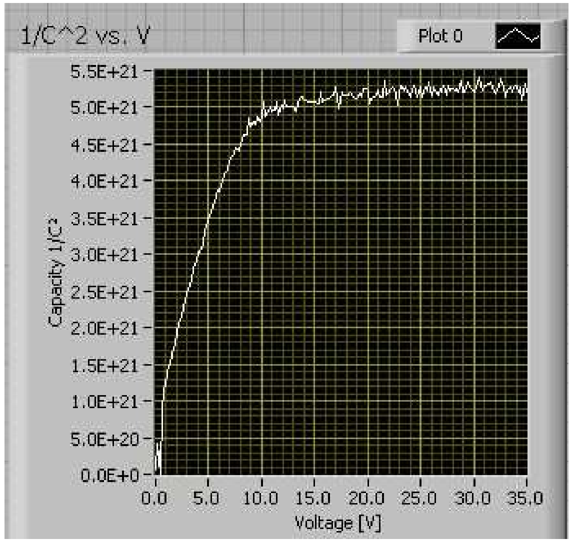
- **Three 4” wafers received from first processing batch**
- **Results look promising**



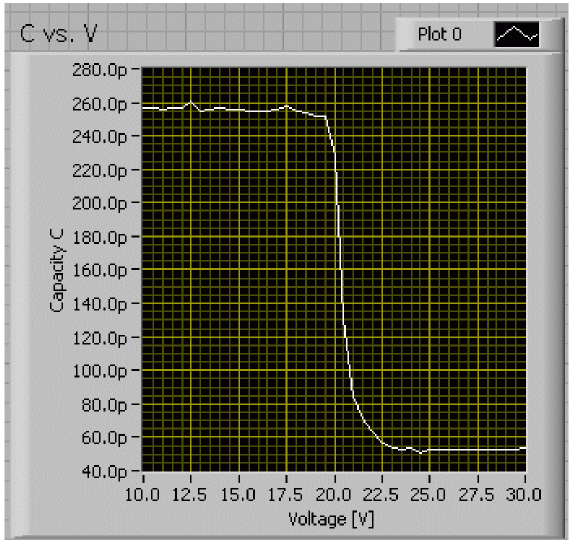


IET Warsaw Results

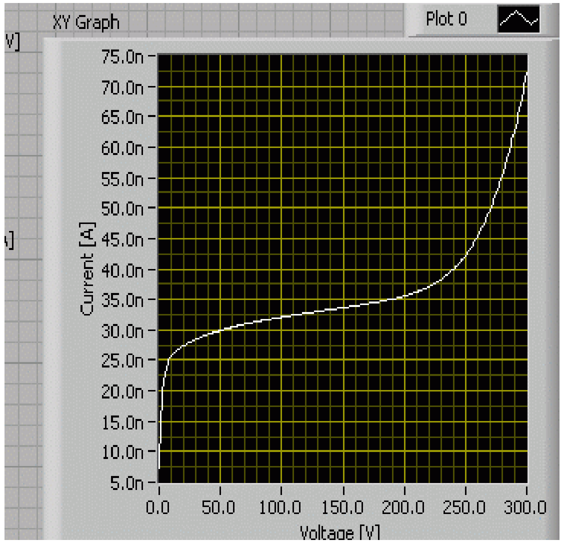
CV Diode:



CV MOS:



IV:



- CV Diode: $V_{depletion}$=8 V
- CV MOS: $V_{flatband}$=21V
- IV: I_{dark}@200V=35nA

Next step:

- Design and production of test structures for dual metal layer

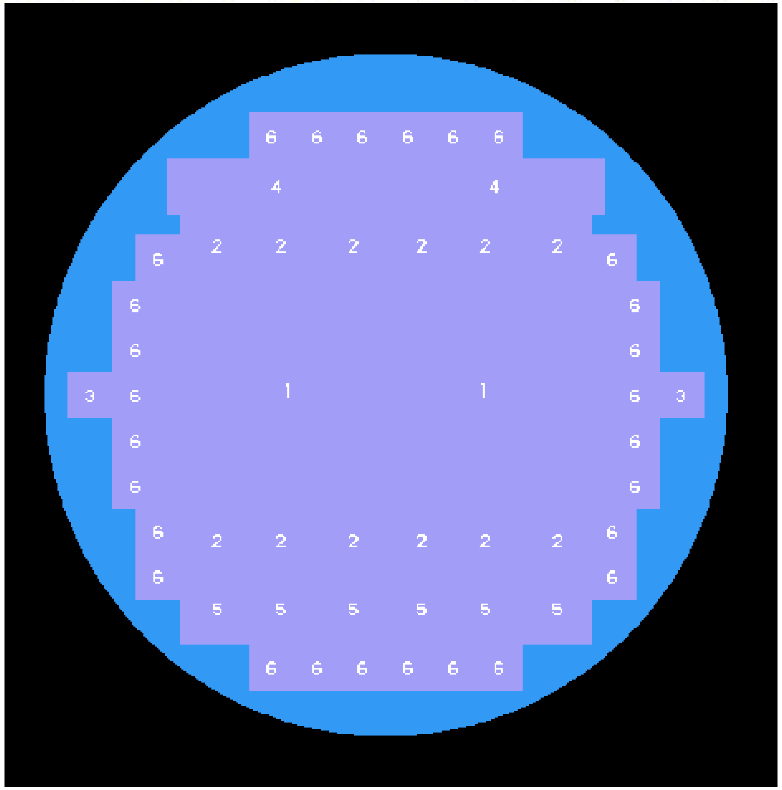
SiLC Silicon for the Linear Collider

VTT (Finland)

- VTT is a large Finnish national research center
- Start of collaboration in December 2007 with goal to develop detectors

Status:

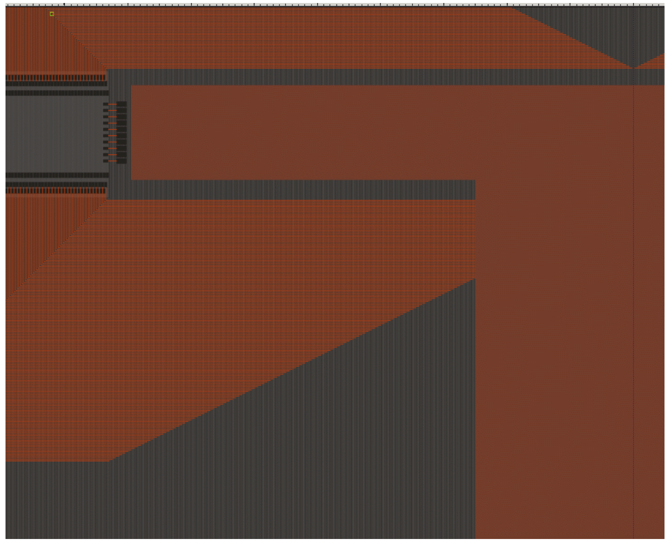
- Design ready
- Two main sensors on 4” wafer
  - One sensor DC coupled
  - Other AC coupled with FOXFET biasing
  - Vienna provided CMS-like test structures
- Processing ongoing
- We are waiting for the first wafers by end of the year
- **See talk by Simo Eraenen *(Torino SiLC meeting Dec 2008).***

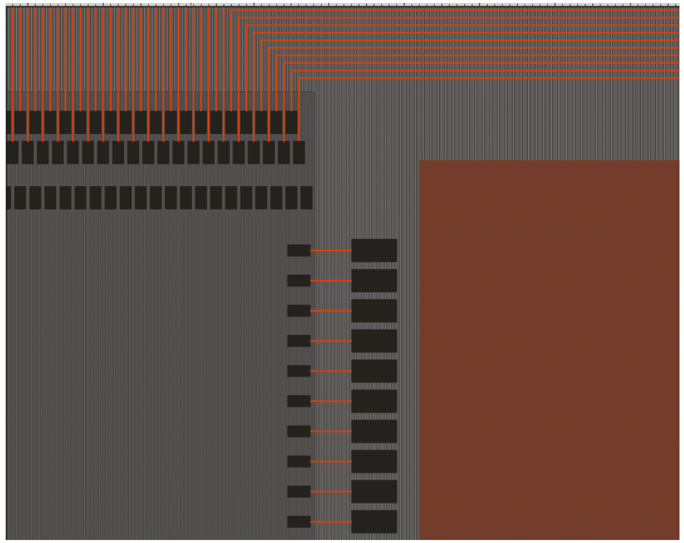


1. **MAIN DETECTOR, 5 X 5 SQCM**
2. *MEDIPIX2, 1.5 X 1.5 SQCM*
3. ALIGNMENT MARKS, 1 X 1 SQCM
4. **HALF MOON TEST STRUCTURE**
5. EDGELESS TEST STRUCTURES, 1.5 X 1.5 SQCM
6. BABY DETECTORS, 1 X 1 SQCM

ON Semiconductor

- Company located in Czech republic, former name “Tesla”
- High wafer throughput
  - 4” and 6” production line running
- Experience already with Delphi and Atlas Pixel detectors
- First contact established
- Agreement to design and build **dual-metal-layer test structures detectors** with them

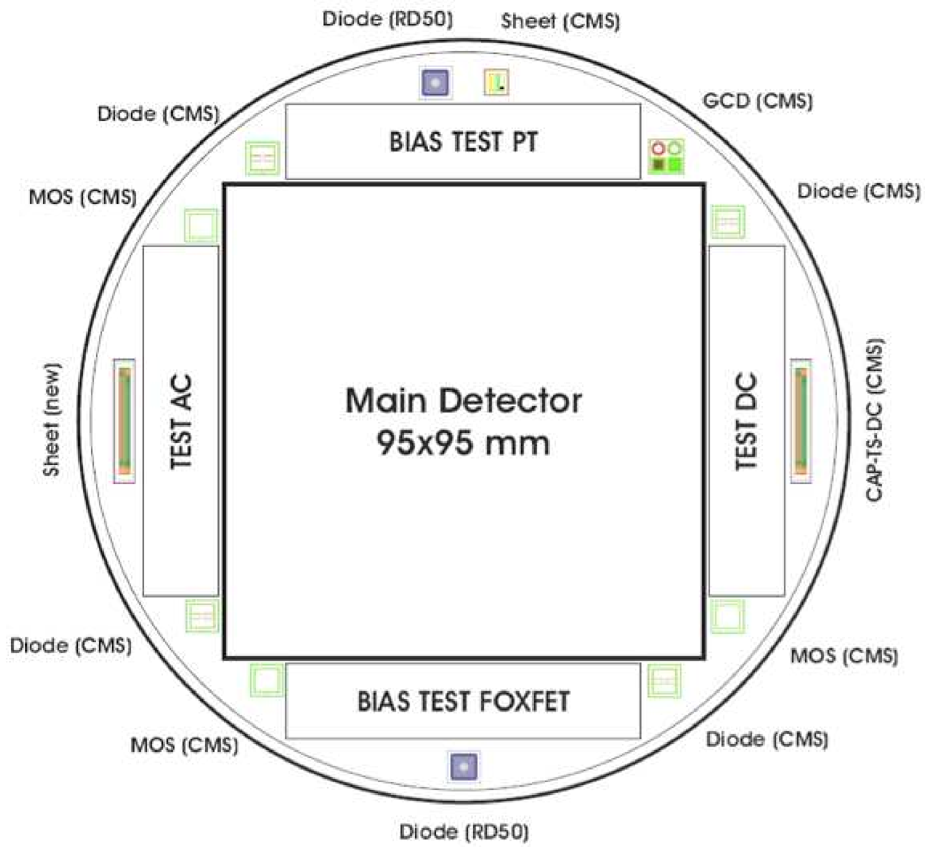




Measurement results on new SilC HPK sensors

HPK Sensors Order (1)

- Single-sided AC coupled SSD
- **Sensor size:** 91,5 x 91,5 mm² (± 0,04 mm)
- **Wafer thickness**: approx. 320 µm
- **Resistivity**: such that depletion voltage: 50 V < Vdepl < 100 Volt
- **Leakage current**: < 10 µA per sensor
- **Biasing scheme**: poly-Silicon Resistor with 20 MΩ (± 5 MΩ)
- **Number of strips:** 1792 (= 14 x 128)
- **Strip pitch:** 50 um pitch, without intermediate strips
- **Strip width:** 12.5 um
- **Dielectric Structure:** Oxide (SiO_2) + Nitride (Si_3N_4) between p+ and aluminium strips.
- 2 **bond pads** on each side of the strip
- 1 **probe pad** on each side of the strip (contact to p+)



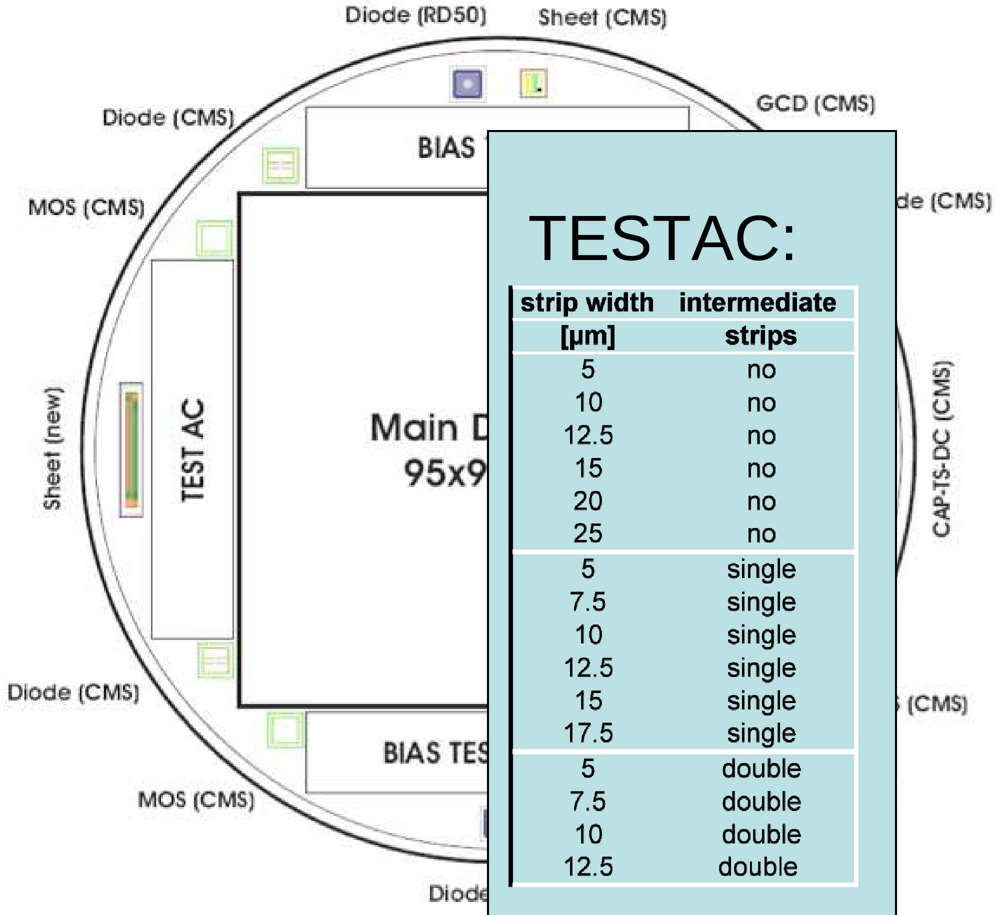
SiLC Silicon for the Linear Collider

HPK Sensors Order (2)

Test structures:

- BIASTEST FOXFET and punch-through
  - 128 channels with pitch=50um
  - with different biasing schemes

- TESTAC and TESTDC
  - 256 strips with pitch=50um
  - Multi-geometry test structures with different strip widths and different intermediate strips
  - Will be used to test coupling, C_int



TESTAC:

strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

SiLC Silicon for the Linear Collider

HPK Sensor Order (3)

We ordered:

- 30 “normal sensors”
- 5 “alignment sensors”
- Plus all associated test structures

Timeline:

- 1st discussion with HPK during VCI’07 in Vienna (February)
- 12 July 2007: Design ready
- October 2007: Delivery

What we got so far:

- 30 “normal sensor”
- 2 have been used for Testbeam in October

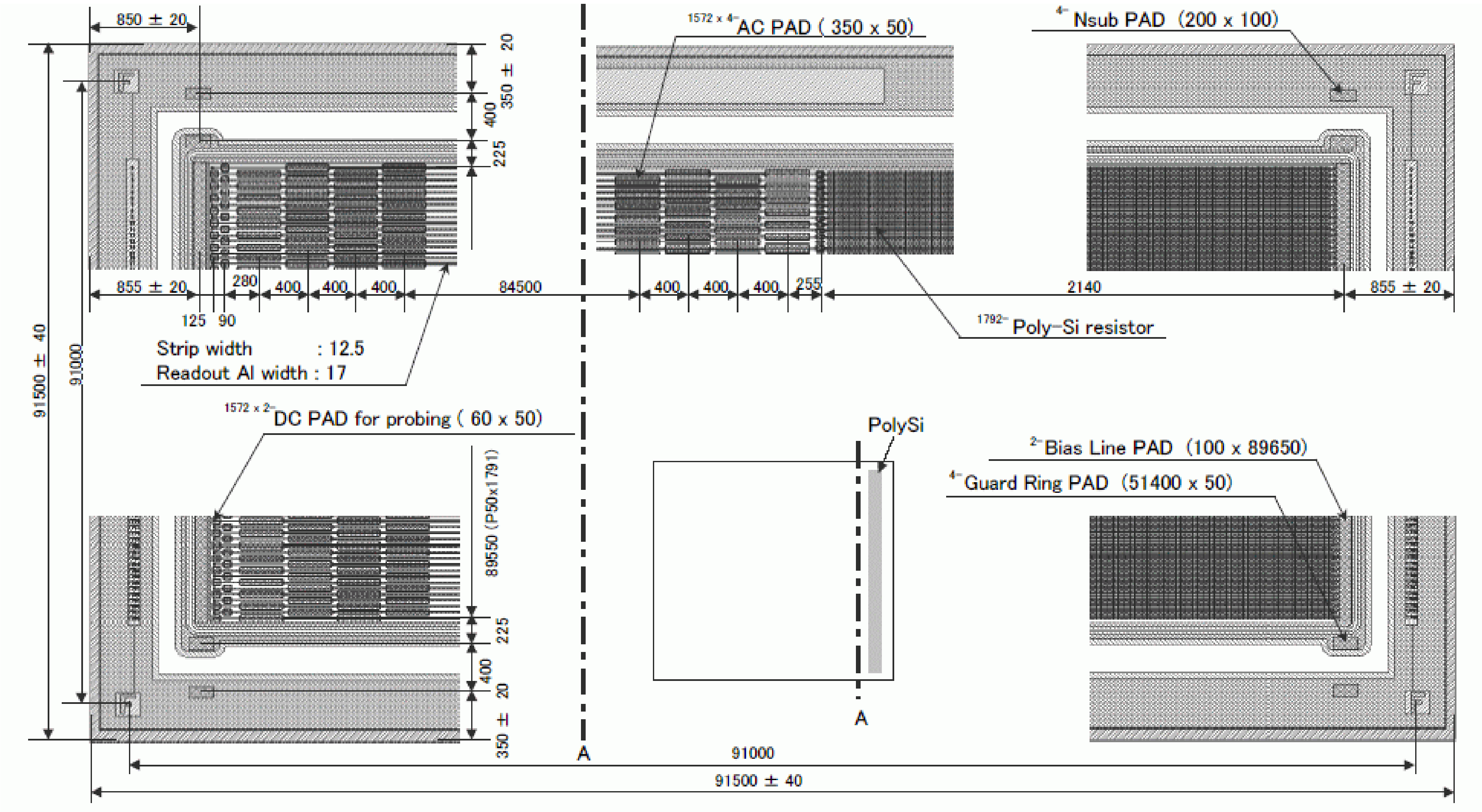
We tested:

- 28 sensors have been tested for IV and CV in Vienna,
- 10 have been shipped to Karlsruhe (IV, CV was repeated)
- Stripscan:
  - 1 sensor in Karlsruhe
  - 1 sensor in Vienna

- Strip Scan Parameters
  - strip leakage current I_{strip}
  - poly-silicon resistor R_{poly}
  - coupling capacitance C_{ac}
  - dielectric current I_{diel}

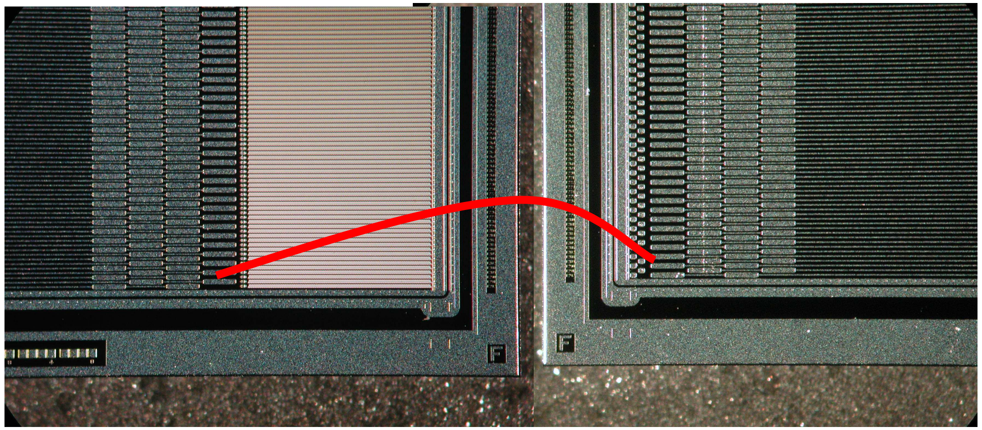
SiLC Silicon for the Linear Collider

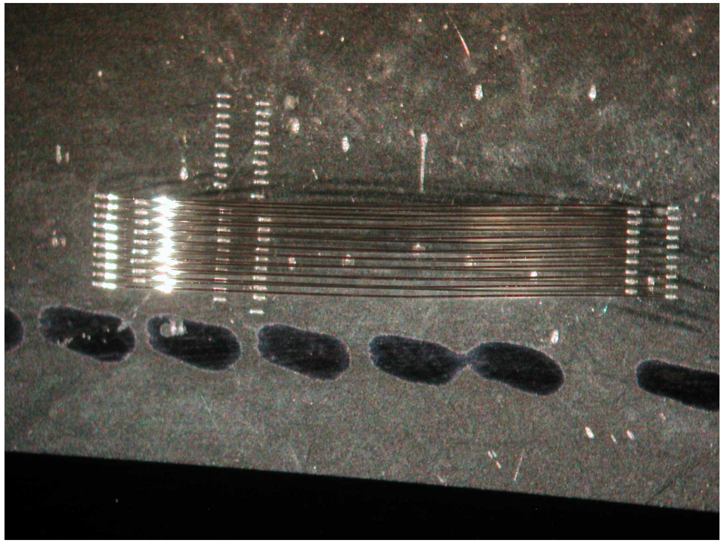
Main Sensor Layout for Reference



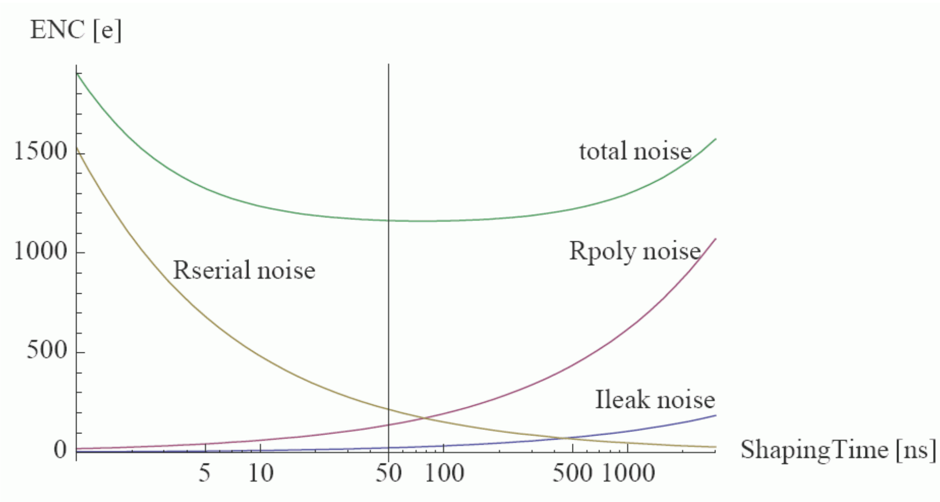
What we learned already: poly-Si

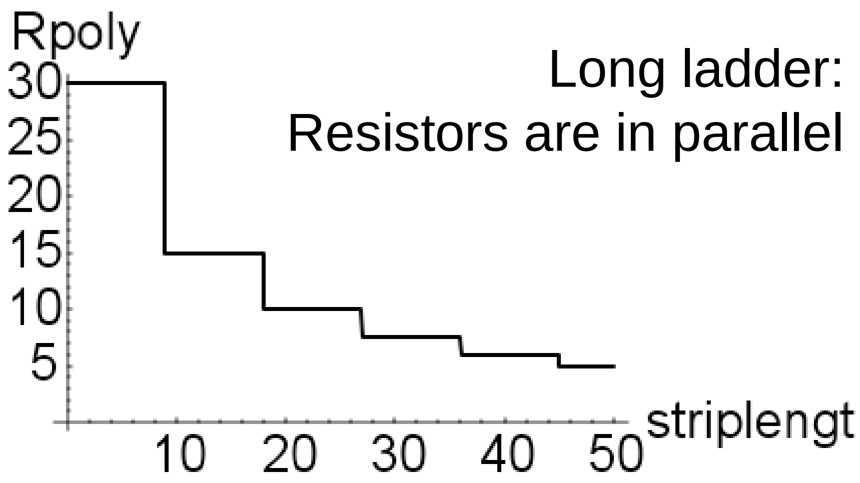
- Bonding problem for daisy-chained sensors
  - Because of the length of the poly-resistor the wire bonds connecting both sensors must be **5mm** long (at 50um pitch)
- We did some bonding tests and this seems to be a problem.
  - Bonds bend and touch each other
- Flipped sensors
  - No alternative since “near” sensor needs to be bonded on both sides
- Other alternative: use punch-through or FOXFEST biasing, since it requires less space (achievable resistor value still unclear)

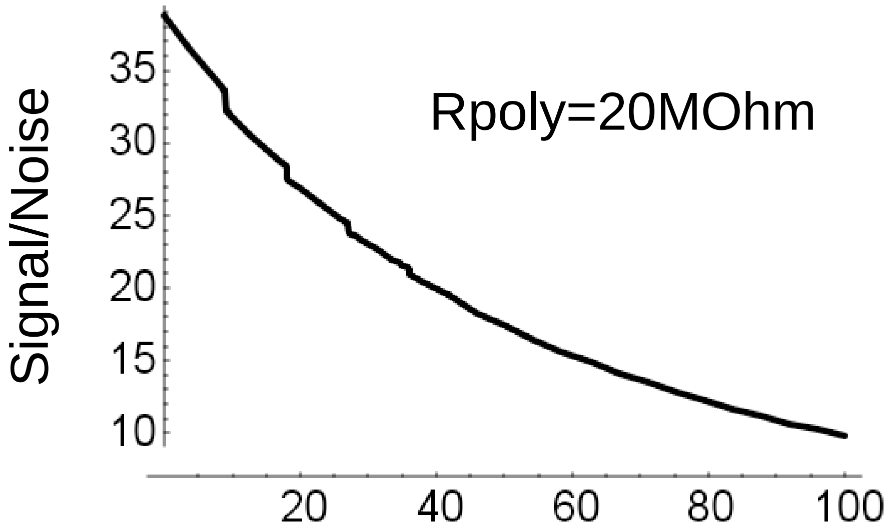


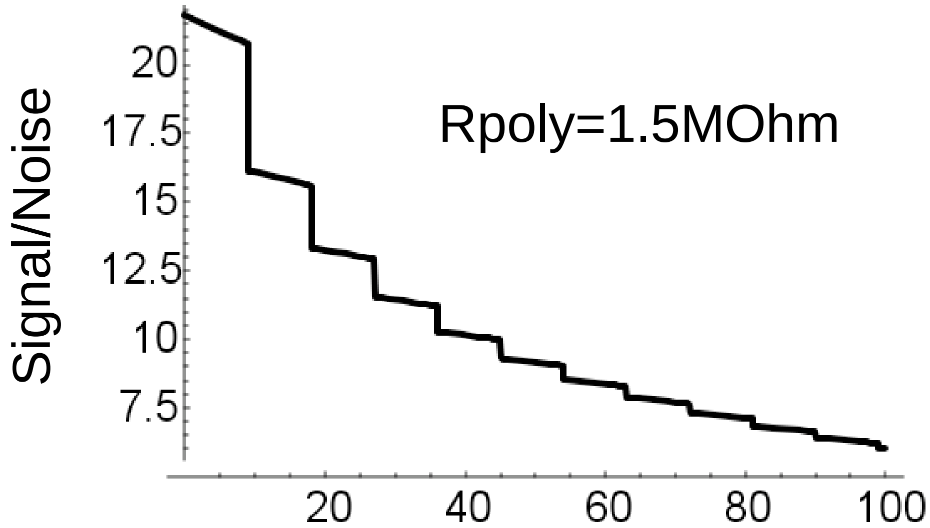


Noise considerations for different Resistors

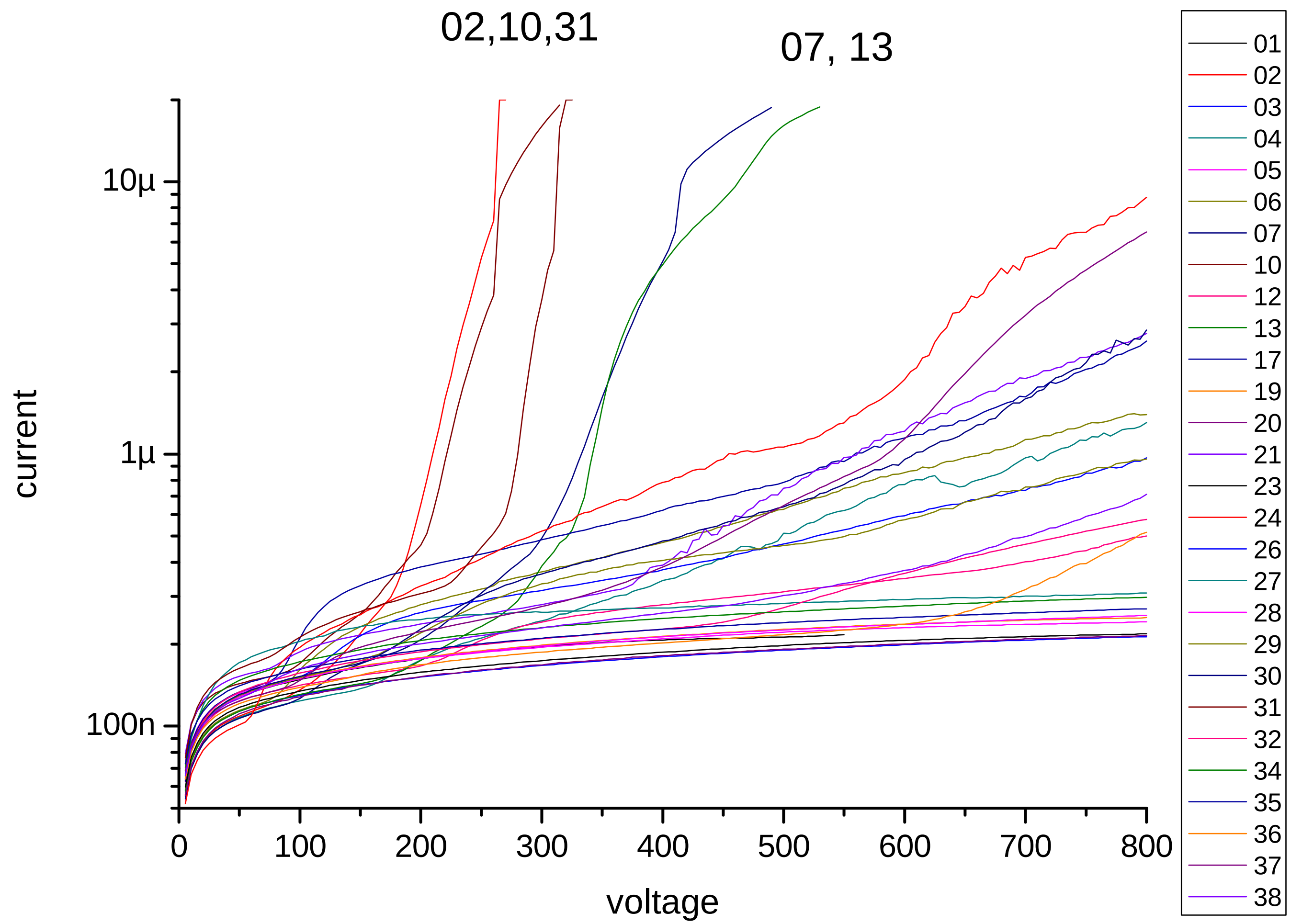








IV Results



Silicon for the Linear Collider

IV results for reference

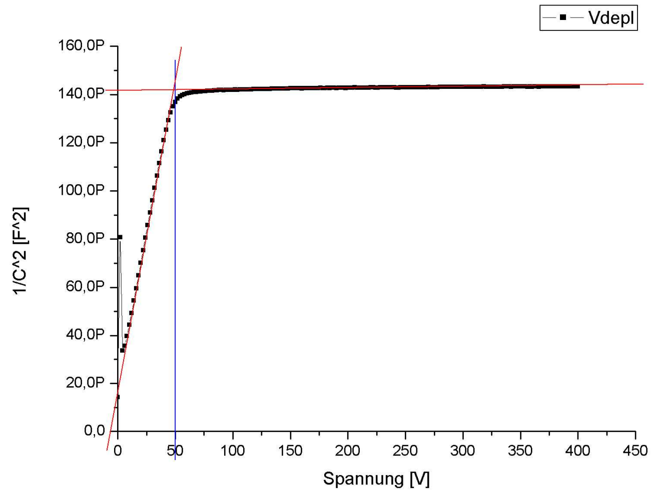
- IV tested up to 800V
- A large fraction of the sensors show some signs of breakthroughs
- Breakthroughs:
  - three sensors below 450V
  - one below 300V

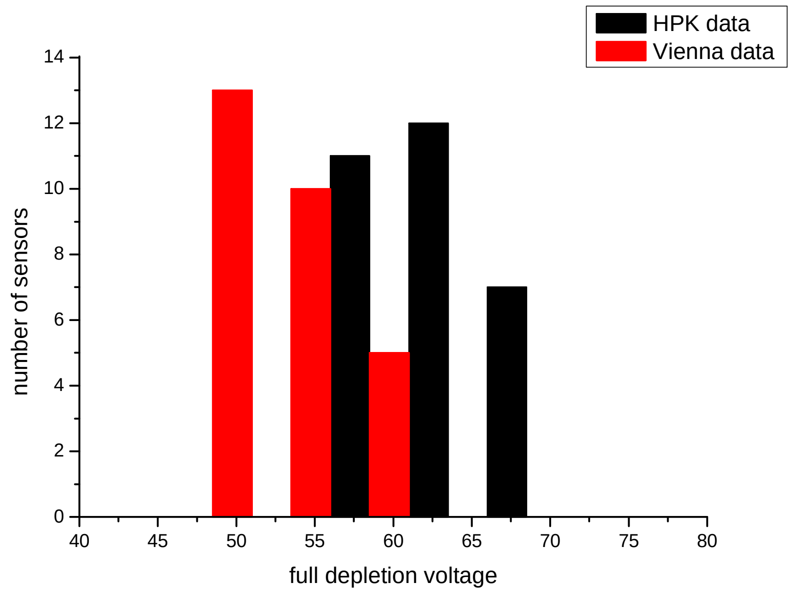
- No problem at all, since operating voltage<100V
- However, CMS sensors were (slightly) better

Object ID	Vdepl	I at 300V	I at 450V
ILC-6684-01	53	1.96E-07	2.10E-07
ILC-6684-02	50	xxxxxxxxx	xxxxxxxxxx
ILC-6684-03	47	1.67E-07	1.85E-07
ILC-6684-04	47	2.44E-07	4.12E-07
ILC-6684-05	53	1.95E-07	2.16E-07
ILC-6684-06	55	3.68E-07	5.41E-07
ILC-6684-07	53	4.91E-07	1.45E-05
ILC-6684-10	50	1.60E-05	xxxxxxxxxx
ILC-6684-12	57	2.41E-07	2.95E-07
ILC-6684-13	55	3.87E-07	8.58E-06
ILC-6684-17	50	4.83E-07	6.97E-07
ILC-6684-19	50	1.98E-07	2.21E-07
ILC-6684-20	50	1.68E-07	1.87E-07
ILC-6684-21	55	2.79E-07	5.45E-07
ILC-6684-23	50	1.74E-07	1.93E-07
ILC-6684-24	55	5.20E-07	9.58E-07
ILC-6684-26	50	3.15E-07	4.15E-07
ILC-6684-27	55	2.62E-07	2.77E-07
ILC-6684-28	55	1.97E-07	2.20E-07
ILC-6684-29	57	3.33E-07	4.33E-07
ILC-6684-30	57	3.63E-07	5.55E-07
ILC-6684-31	50	3.69E-06	xxxxxxxxxx
ILC-6684-32	47	2.09E-07	2.41E-07
ILC-6684-34	58	2.30E-07	2.56E-07
ILC-6684-35	55	2.10E-07	2.34E-07
ILC-6684-36	50	1.87E-07	2.09E-07
ILC-6684-37	50	2.75E-07	4.96E-07
ILC-6684-38	56	2.30E-07	2.77E-07

CV Results

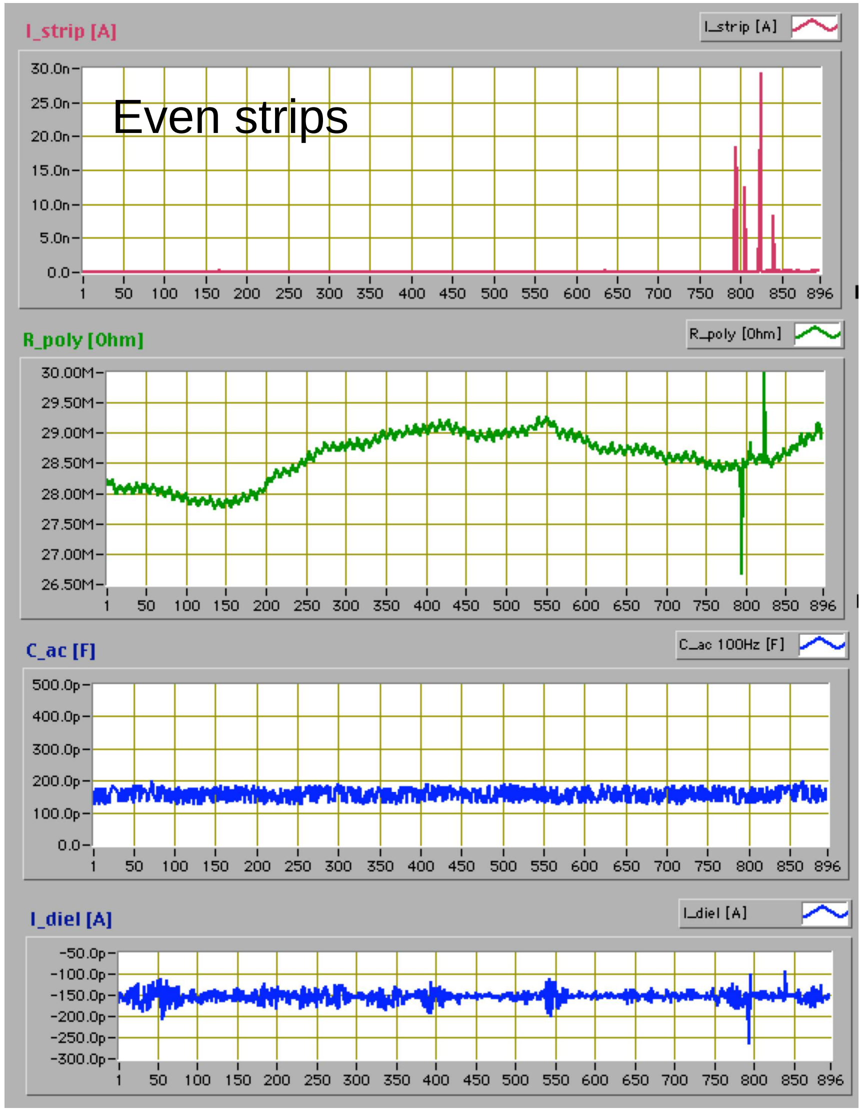
- We requested a resistivity such that depletion voltage is between 50 and 100V
- All sensors fully deplete between 47-58V, average at 52.5V
  - Resistivity is **6.7 kOhmcm** (rough estimate since more exact measurement on TS diode possible)
  - Safe operating voltage: 70-90V

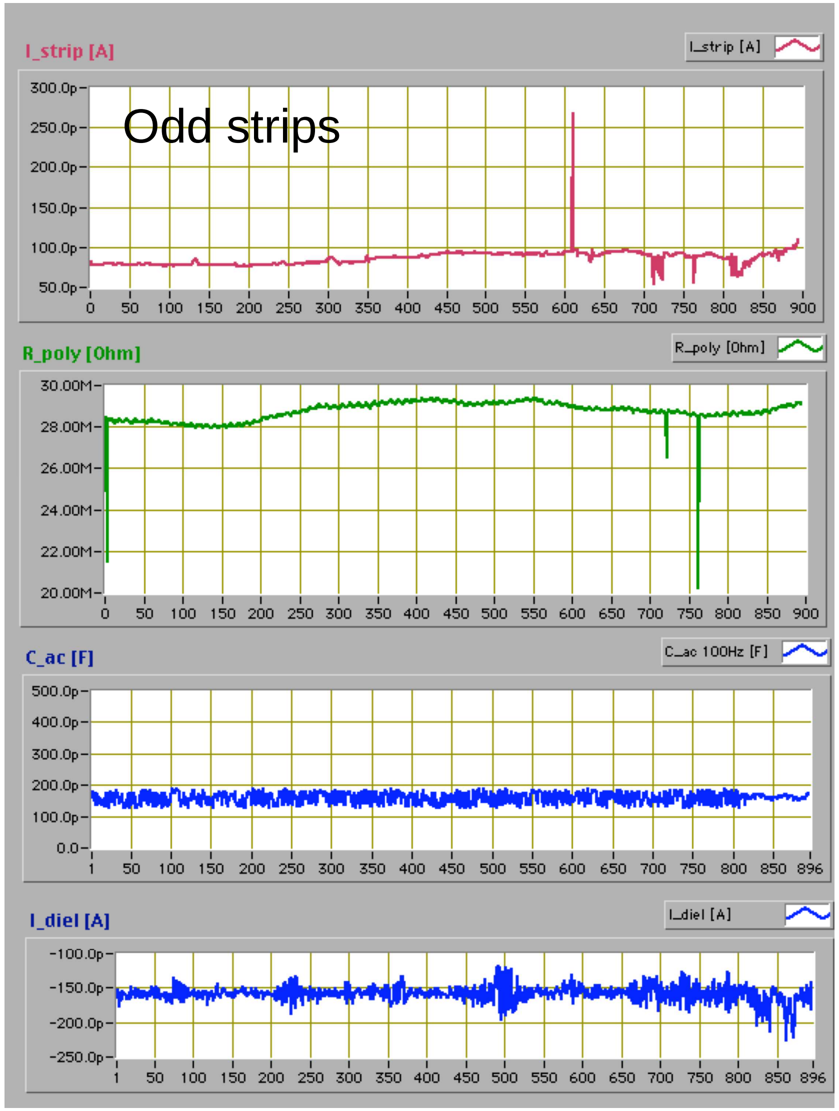




SiLC Silicon for the Linear Collider

Strip Scan Results (Vienna)

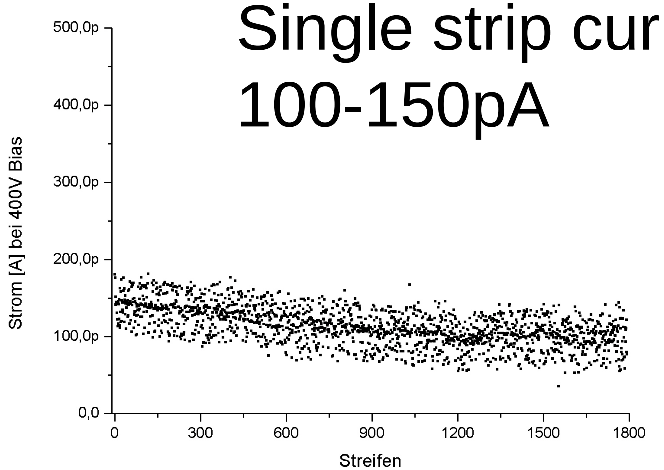




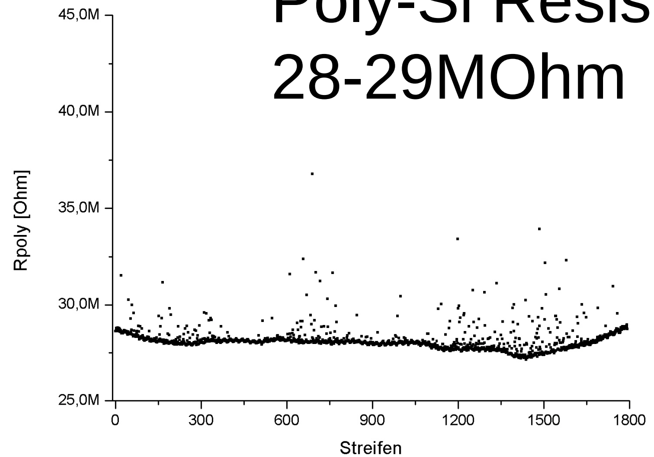
SiLC
Silicon for the Linear Collider

Strip Scan Results (Karlsruhe)

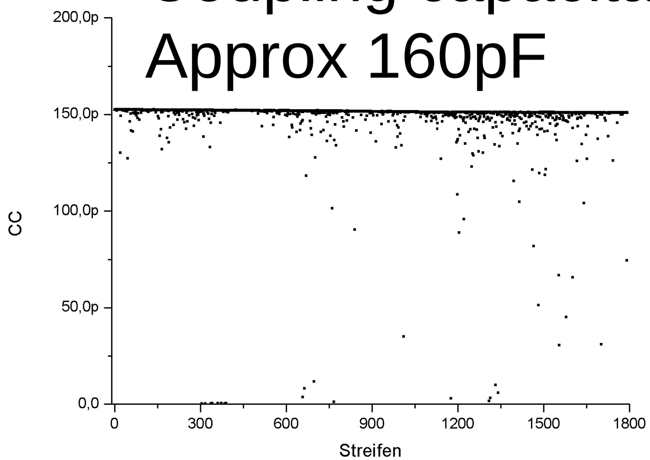
Single strip current
100-150pA



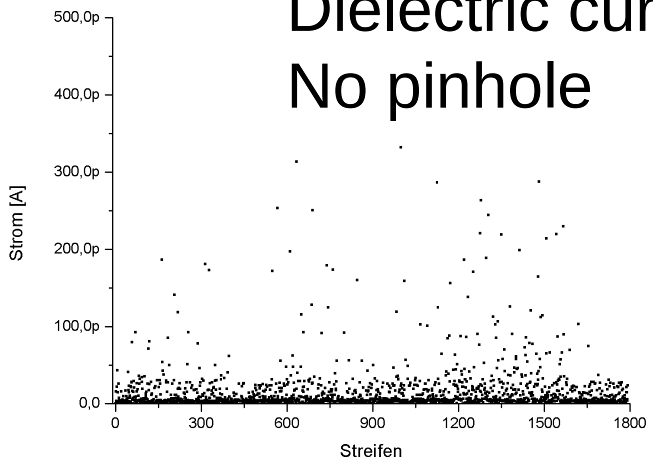
Poly-Si Resistor
28-29MOhm



Coupling capacitance
Approx 160pF



Dielectric current
No pinhole



Strip Scan Results (3)

- Measurements exactly identically between Karlsruhe and Vienna

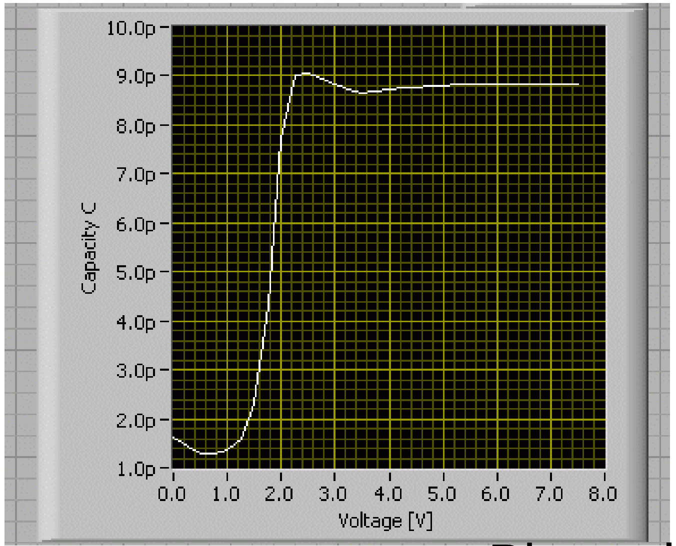
- I_strip = 137 pA
- R_poly = 28.65 MOhm
- C_ac = 156 pF
- I_diel< 160 pA

- Coupling Capacitance (C_ac)
  - SiLC: 1.42 pF/cm/um (on sensor)
  - CMS: 1.74 pF/cm/um (on TS)

  (from Sensor measurement oxide is 25% thicker than CMS; questionable to compare)

- Interstrip Capacitance
  - SilC: 0.94pF/cm
  - CMS: 0.84pf/cm
  - Larger because of narrower strips

Cint



Bias voltage

Proposal for a beam test

Proposal for a beam test

- TESTAC and TESTDC structures have
  - 256 strips with pitch=50um
  - Multi-geometry test structures with different strip widths and different intermediate strips
  - Could be used to test resolution in a testbeam

- What we need:
  - Beam time at SPS for 1 week
    - Has been requested for June 2008
    - Has been approved by SPSC May 30 to June4
  - EUDET Pixel Telescope + TLU Box
  - APV front end hybrid + 2 APV25 chips (available in Vienna)
  - APV readout system (available in Vienna)

- What we will learn
  - Which geometry is the ideal to reach best resolution

Summary/Outlook

- Sensor Producers
  - IET Warsaw: 1st wafers OK, 2nd iteration about to start; VTT: no news
  - ON Semi: collaboration just started, see next Talk
- Hamamatsu Results
  - Sensor electrically OK; as expected
  - Geometric problem with poly-Si resistor (too large to bond)
  - Test structures (and alignment sensors) still missing
- Vendor qualification procedure
  - HPK successfully qualified once all measurements finished
  - Other vendors have to comply with the same procedure
  - New vendors have to undergo the same procedure
    - At least one iteration of sample batch
    - Preproduction
    - Final production
- Once HPK test structures are available
  - In-depth measurements possible
  - Beam test at SPS testing resolution of different geometries

End.

Thanks for your attention.

SiLC work program for sensor R&D

- Step 1 (2007)
  - Use long strips (50 µm pitch)
  - Wafer thinning (100, 200, 300µm)
  - Test new readout chips (DC coupling, power cycling)
  - Improve standardized test structures and test setups
- Step 2a (2008-)
  - Move from pitch adapter to in-sensor-routing
  - Test crosstalk, capacitive load of those sensors
- Step 2b (2008-)
  - Test 6” double sided sensors
- Step 2c (2008-)
  - 8” (12”) single sided DC wafer

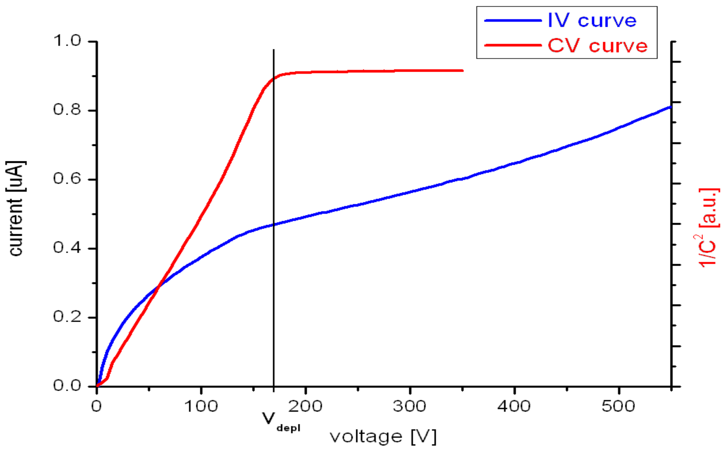
Step 1 and 2a:

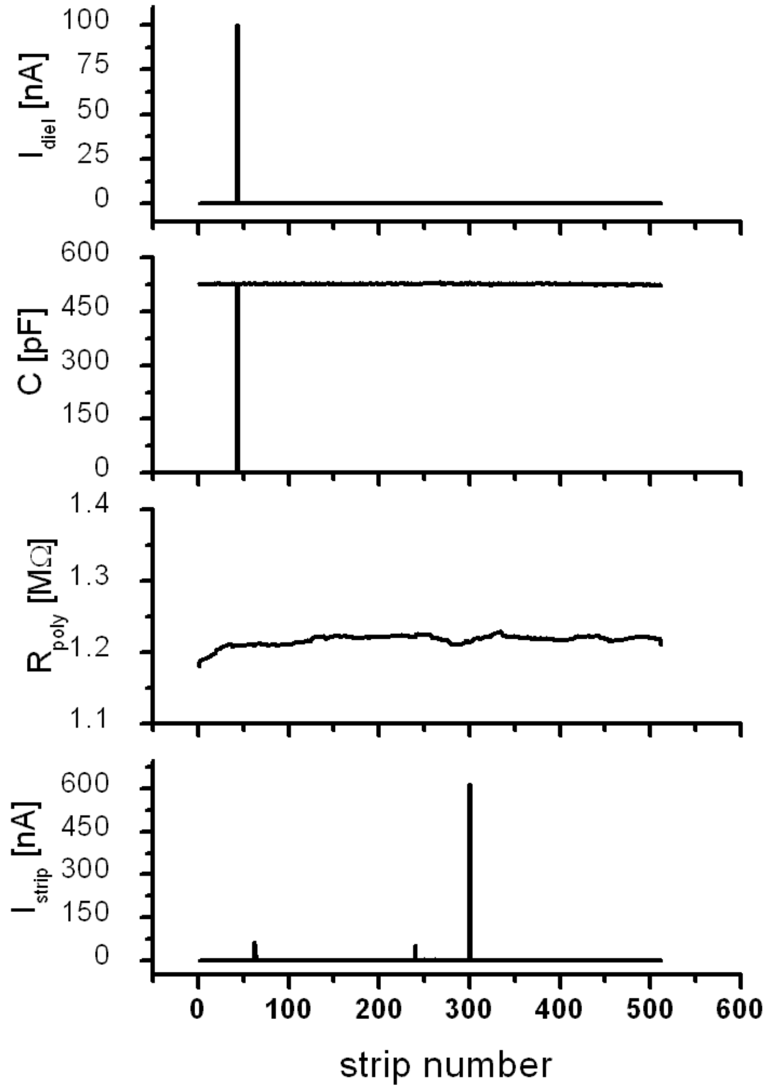
- Bump-bondable 128-channel chip available end 2007
- HPK agreed to provide a sensor design
- SiLC adapts strip to pad area
- HPK will process the sensor
- SiLC (Paris) provides chip
- HPK could bump bond chip to sensor
  - HPK is very interested to strengthen inhouse bumpbonding
    - In Bump
    - Flipchip
  - Stud-bonding (Jean-Francois)
- Testing begins 2008

Strip-by-Strip Characterization

What do we test?

- Global parameters:
  - **IV-Curve:** Dark current, Breakthrough
  - **CV-Curve:** Depletion voltage, Total Capacitance
- Strip Parameters e.g.
  - strip leakage current I_{strip}
  - poly-silicon resistor R_{poly}
  - coupling capacitance C_{ac}
  - dielectric current I_{diel}

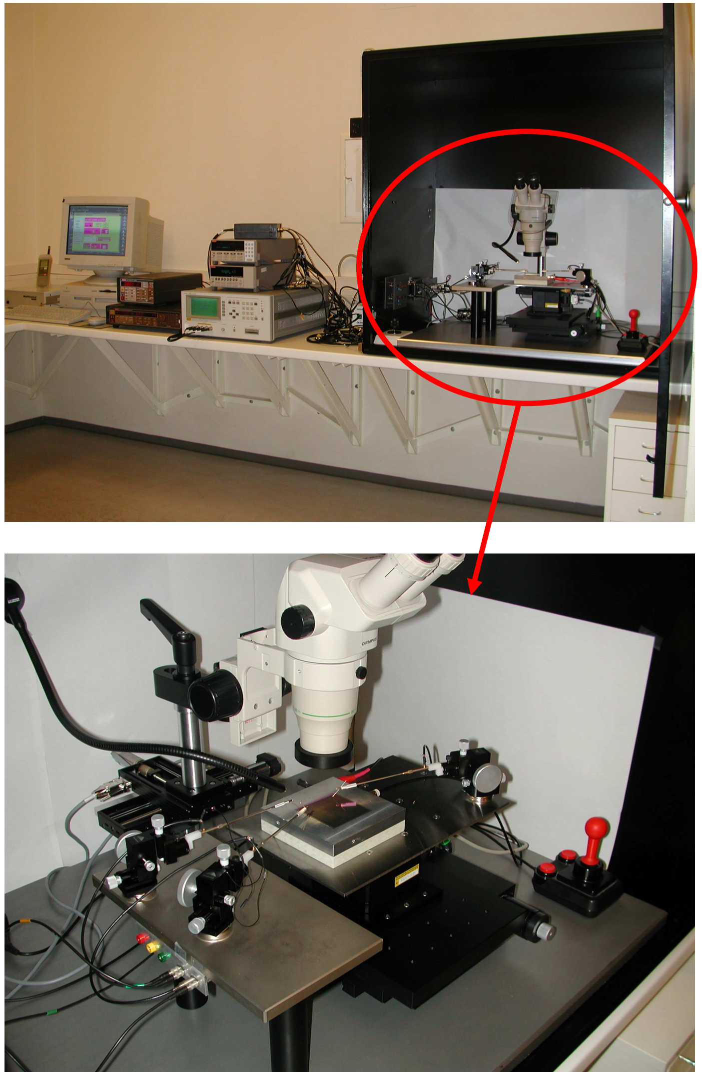




Strip-by-strip Test Setup

- Sensor in Light-tight Box
- Vacuum support jig is carrying the sensor
  - Mounted on freely movable table in X, Y and Z
- Cold chuck in Karlsruhe available

- Needles to contact sensor bias line
  - fixed relative to sensor
- Needles to contact:
  - DC pad (p^+ implant)
  - AC pad (Metal layer)
  - Can contact ever single strip while table with sensor is moving

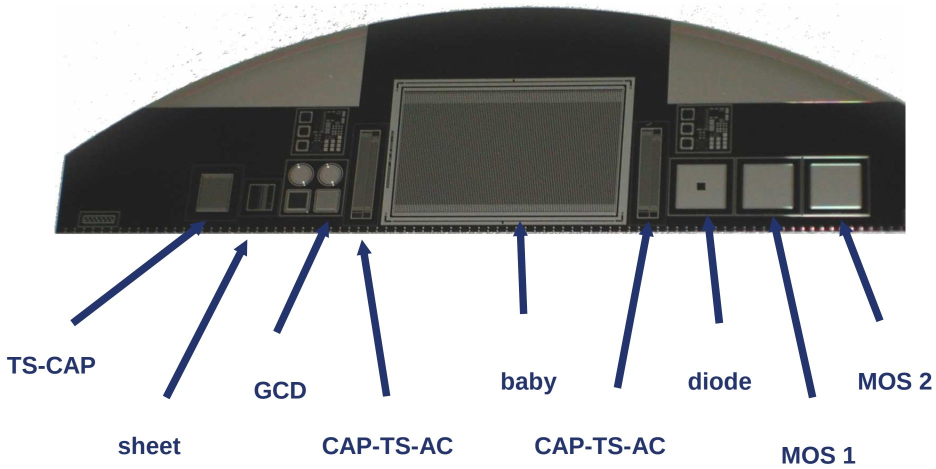


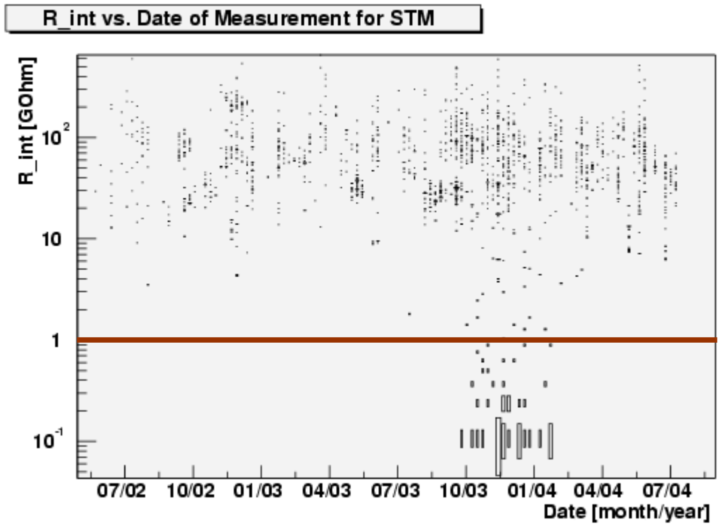
Process Monitoring on Test Structures

- **CMS "Standard Half moon"**
  - 9 different structures
  - Use to determine one parameter per structure

- Worked extremely well during CMS sensor production
  - Example of an identified problem can be seen in plot: low interstrip resistance

- Improved version for SiLC
  - overall size reduction
  - Structure design improvements (e.g.better sheet structure)



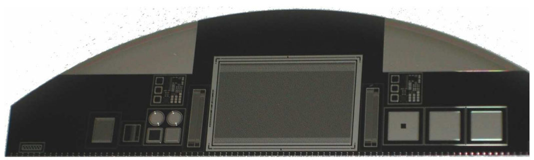


HEPHY Vienna

SiLC
Silicon for the Linear Collider

Test Structures Description

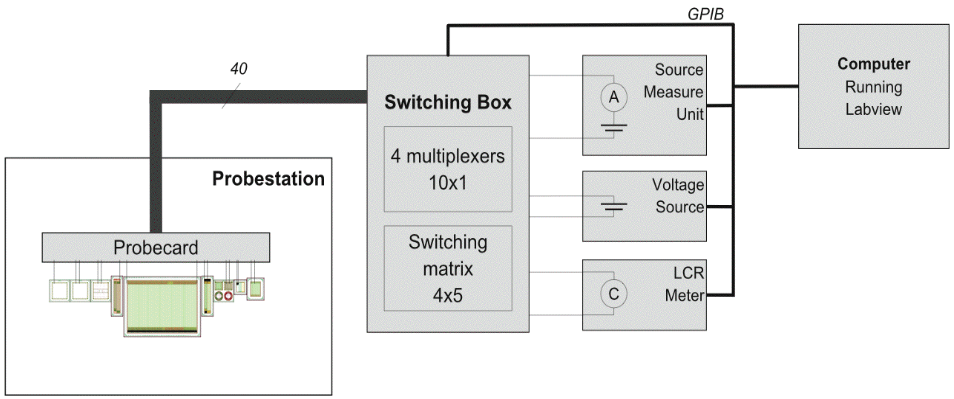
- **TS-CAP:**
  - Coupling capacitance C_{AC} to determine oxide thickness
  - IV-Curve: breakthrough voltage of oxide
- **Sheet:**
  - Aluminium resistivity
  - p^+-impant resistivity
  - Polysilicon resistivity
- **GCD:**
  - **G**ate **C**ontrolled **D**iode
  - IV-Curve to determine surface current $I_{surface}$
  - Characterize Si-SiO_2 interface

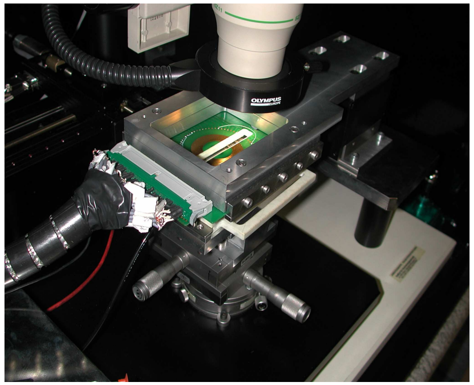


- **CAP-TS-AC:**
  - Inter-strip capacitance C_{int}
- **Baby-Sensor:**
  - IV-Curve for dark current
  - Breakthrough
- **CAP-TS-DC:**
  - Inter-strip Resistance R_{int}
- **Diode:**
  - CV-Curve to determine depletion voltage $V_{depletion}$
  - Calculate resistivity of silicon bulk
- **MOS:**
  - CV-Curve to extract flatband voltage $V_{flatband}$ to characterize fixed oxide charges
  - For thick interstrip oxide (MOS1)
  - For thin readout oxide (MOS2)

SiLC Silicon for the Linear Collider

Test structures Measurement Setup





- Probe-card with 40 needles contacts all pads of test structures in parallel
  - Half moon fixed by vacuum
  - Micropositioner used for Alignment
  - In light-tight box with humidity and temperature control
- Instruments
  - *Source Measurement Unit (SMU)*
  - Voltage Source
  - LCR-Meter (Capacitance)
- Heart of the system: Crosspoint switching box, used to switch instruments to different needles
- Labview and GPIB used to control instruments and switching system

SiLC
Silicon for the Linear Collider