A CCD Based Vertex Detector

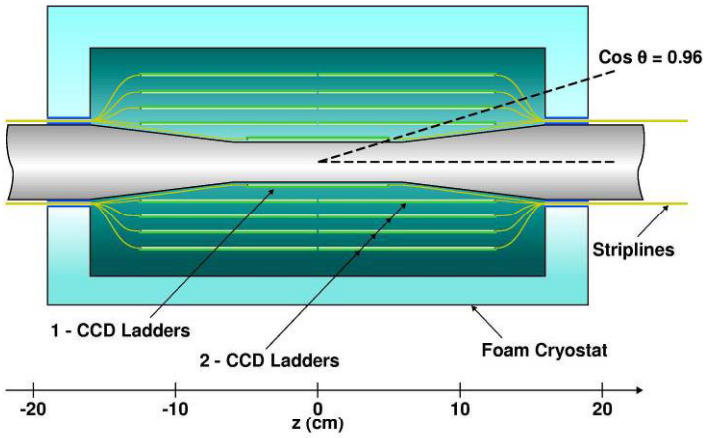
Konstantin Stefanov

STFC Rutherford Appleton Laboratory

On behalf of the Linear Collider Flavour Identification (LCFI) Collaboration

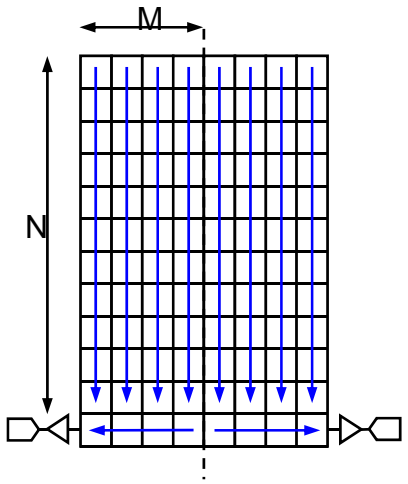
- **Introduction**
- **Vertex Detector R&D at LCFI**
  - **Column-Parallel CCDs**
  - **In-situ Storage Image Sensors**
  - **Low Mass Mechanical Support**
- **Conclusion**

Introduction

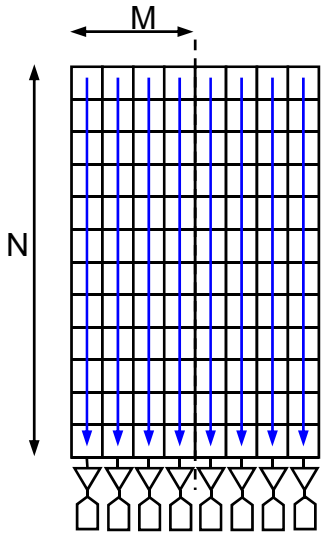


What is required for the vertex detector at ILC:

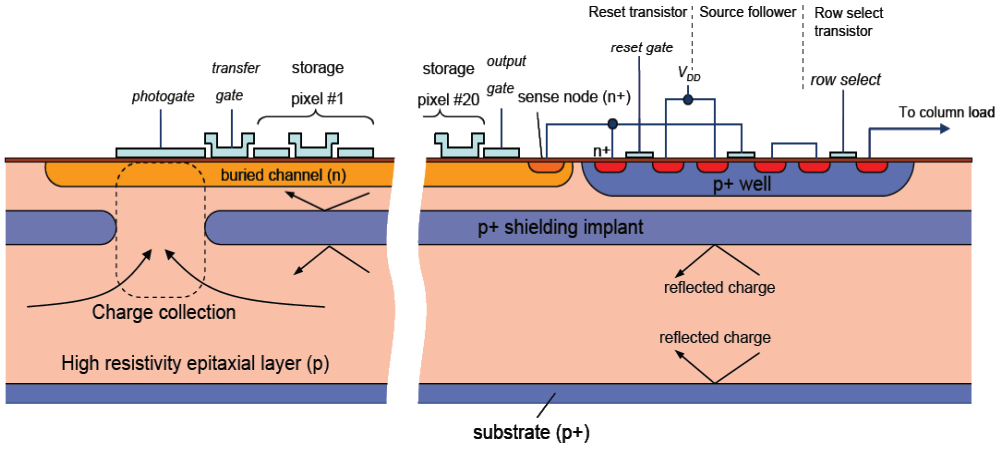
- **Excellent point resolution (3.5 μm), small pixel size = 20 μm, close to IP**
- **Low mass (≤ 0.1% X_0 per layer), low power dissipation**
- **Fast (low occupancy) readout – challenging, two main approaches**
- **Tolerates Electro-Magnetic Interference (EMI)**



"Classic CCD"
Readout time ≈ $N \times M / f_{out}$



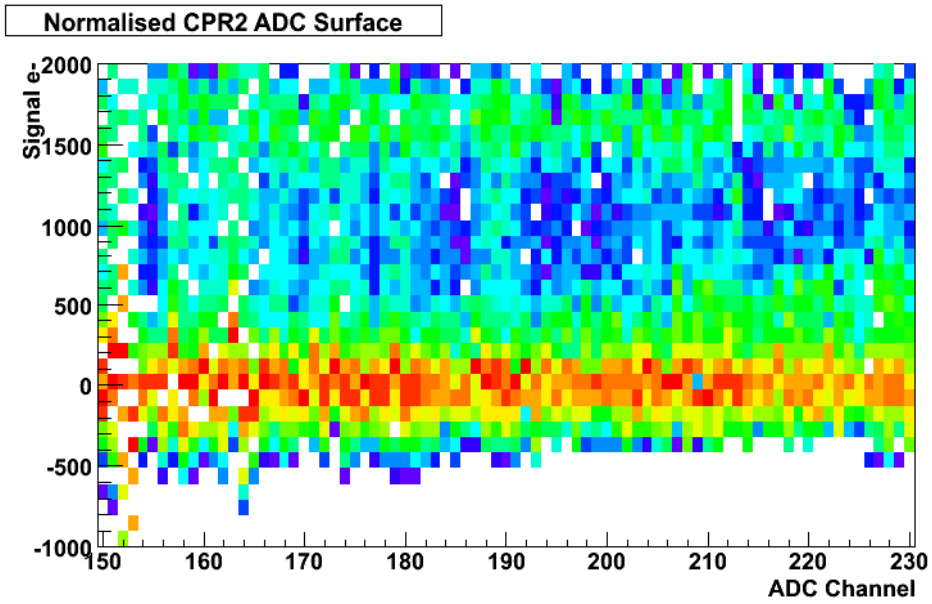
Column Parallel CCD
Readout time = N / f_{out}

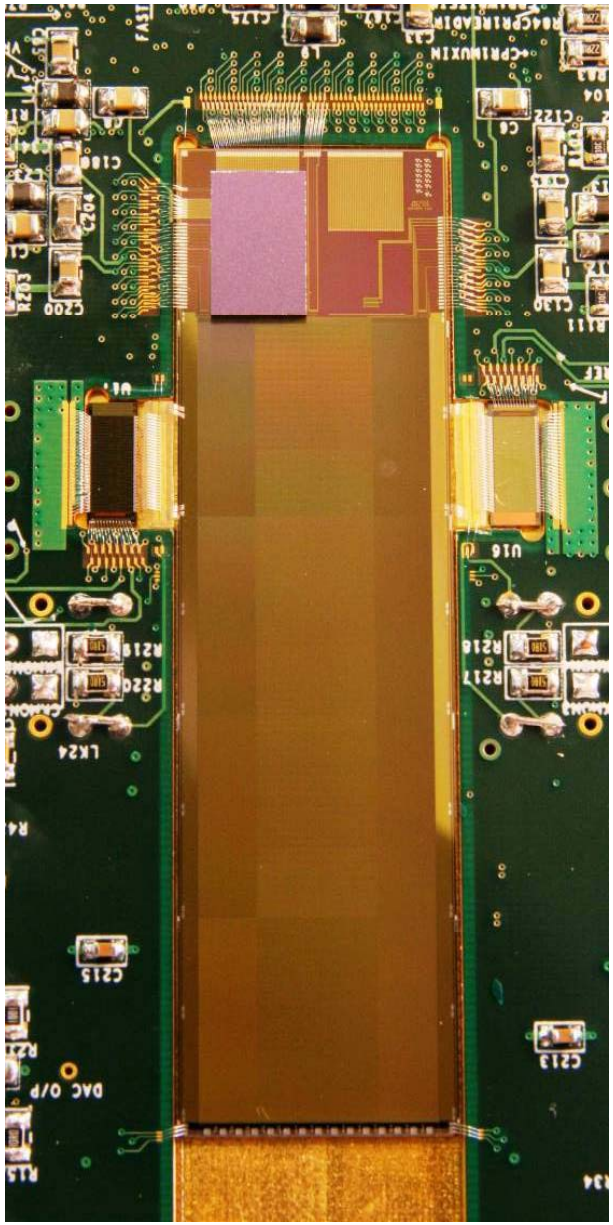


ISIS

CPCCD Programme: Bump-bonded CPC2/CPR2

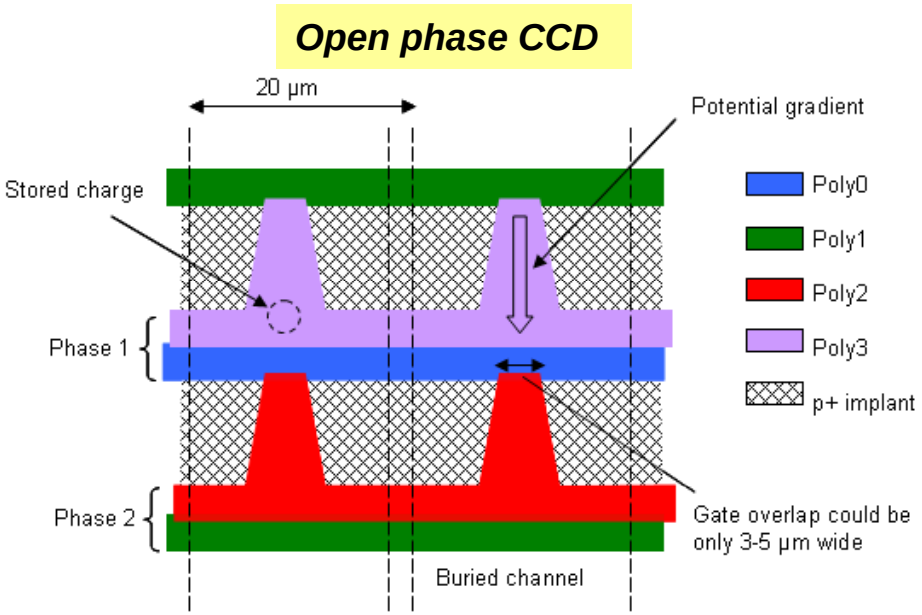
- Hybrid assembly CPC2/CPR2 fully tested
  - ❖ Results incorporated into CPR2A
- Bump-bonded CPC2-40/CPR2 driven by two CPD1 chips
  - ❖ Works up to 9 MHz
  - ❖ 5 cm long CCD, signals pass 5 “stitches”
  - ❖ Performance of the CPR2 is limiting factor, and gradually deteriorates at higher frequencies (missing and/or spurious codes)
  - ❖ Sparse readout (below) up to 6 MHz
- Stand-alone CPC2/CPD1 reached 45 MHz with transformer driver, 20 MHz with CPD1 and trying to improve

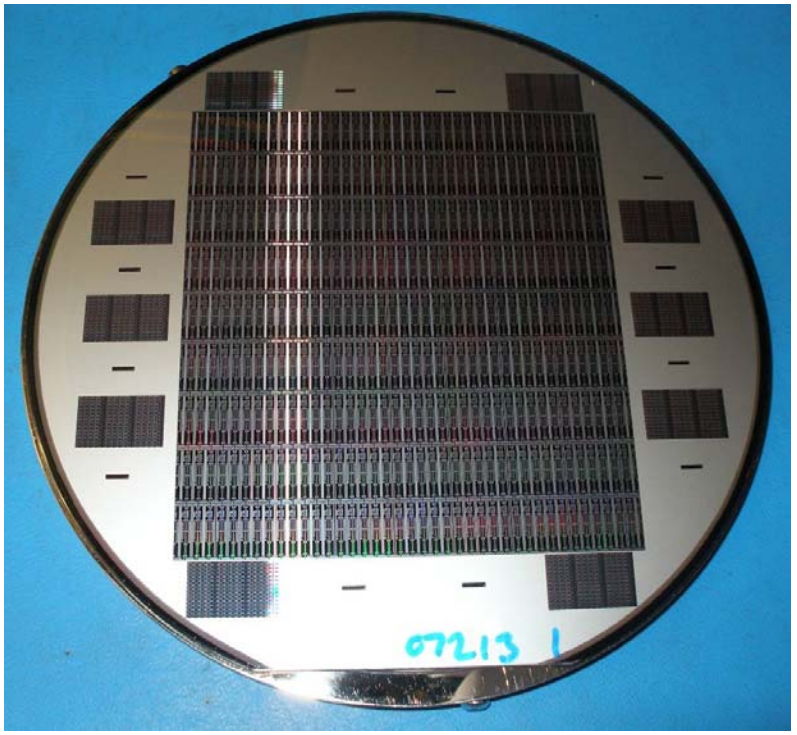




Tim Woolliscroft, Liverpool U

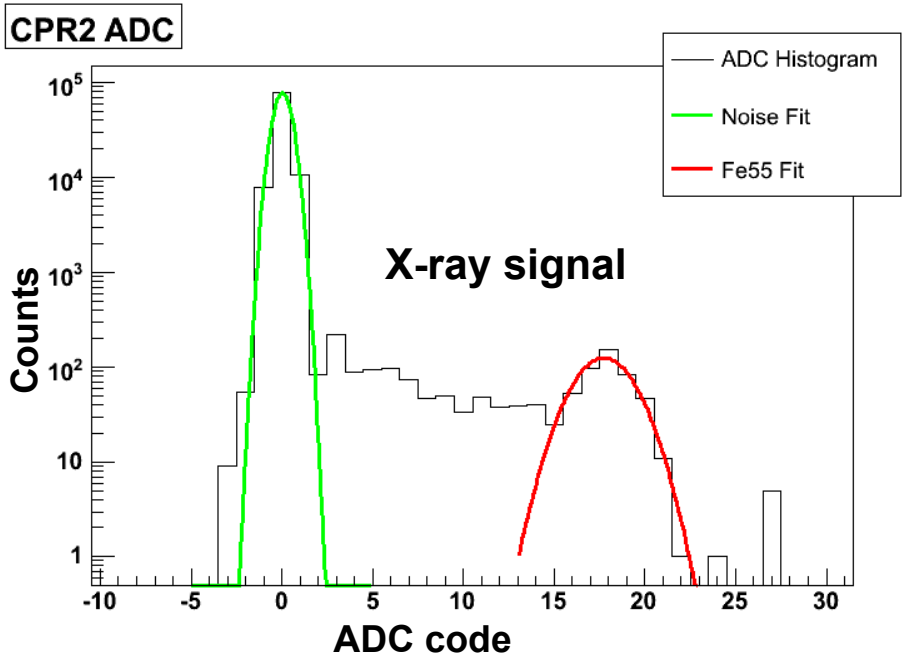
New Ideas: CCDs for Capacitance Reduction



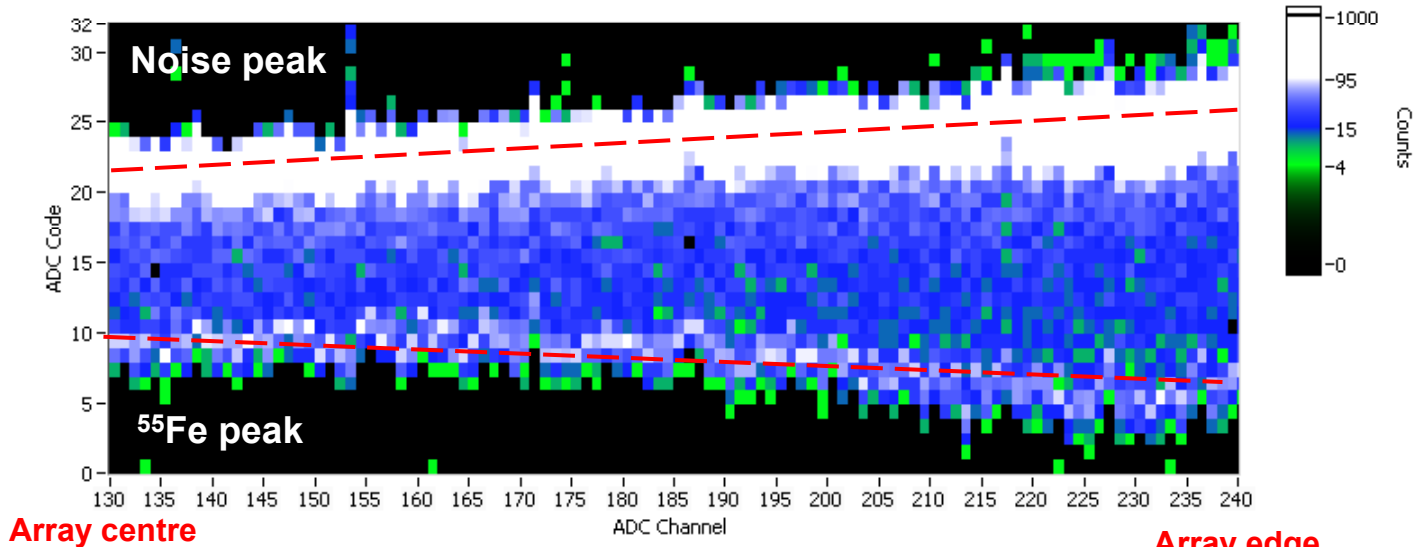


- High CCD capacitance is a challenge to drive because of the currents involved
  - ❖ New ideas to reduce the inter-gate capacitance C_{ig} (by a factor 2-4) and clock amplitude
  - ❖ Together with e2V Technologies designed 29 different types of small CCDs to test ideas
- 360 chips/wafer, first 6-inch wafers for LCFI

CPR2: Analogue Performance

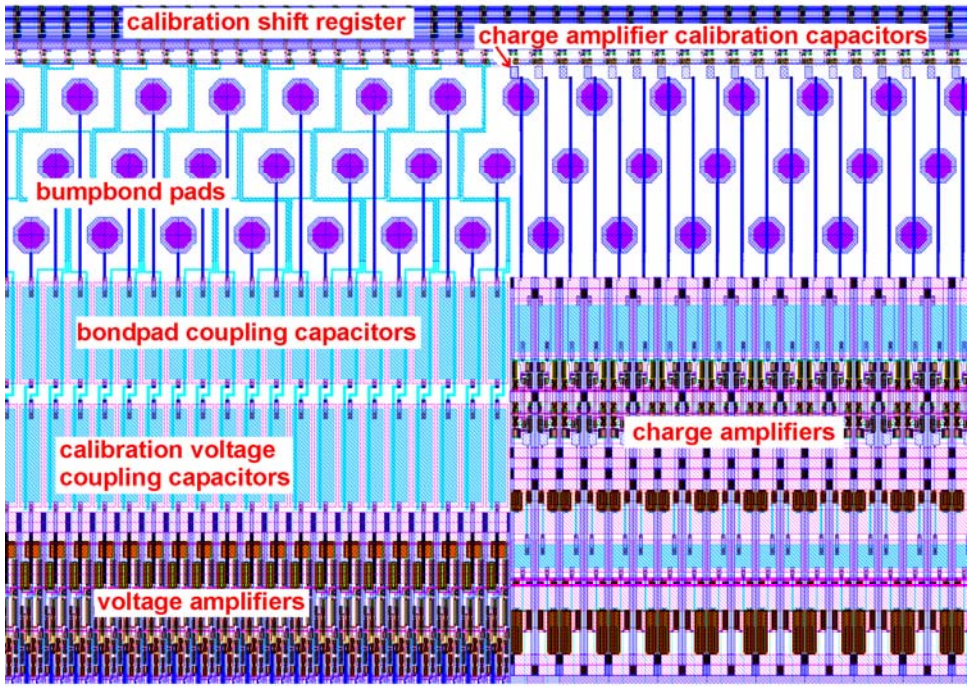


- Signals from all voltage channels observed (here at 2 MHz, 300 mV ADC range)
  - ❖ Gain decreases by 50% away from the chip edges (as in CPR1)
- Noise around 60-80 e-
- Bump bond yield appears to be 100%
- Charge channels did not work – swamped by digital crosstalk from the ADCs



The New Readout Chips CPR2A/B/C

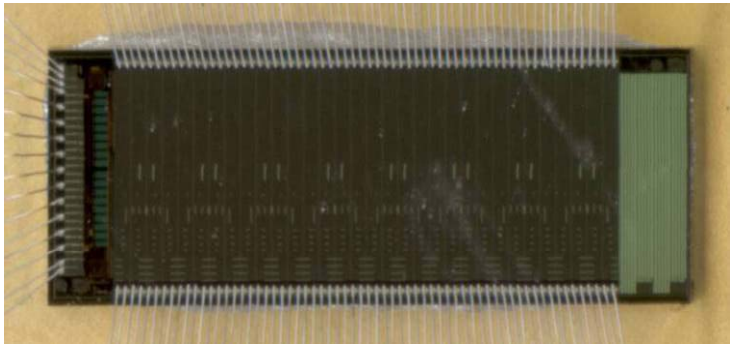
- Three variants: CPR2A, CPR2B and CPR2C submitted, delivery expected in mid-April
- The variants have different clock distribution – affects ADC performance;
- Expecting major improvements in functionality and performance:
  - ❖ Fully re-designed cluster finder and sparsification circuitry – should cope better with high peak hit densities; added individual column threshold;
  - ❖ Calibration circuit for both charge and voltage channels – allows analogue stand-alone testing of multiple channels;



- ❖ Near-constant power supply current in the ADCs (externally controlled) – should reduce interference to the charge channels
- ❖ Gain matching between voltage channels to per cent level, achieved by lower track resistance and more stable current sources

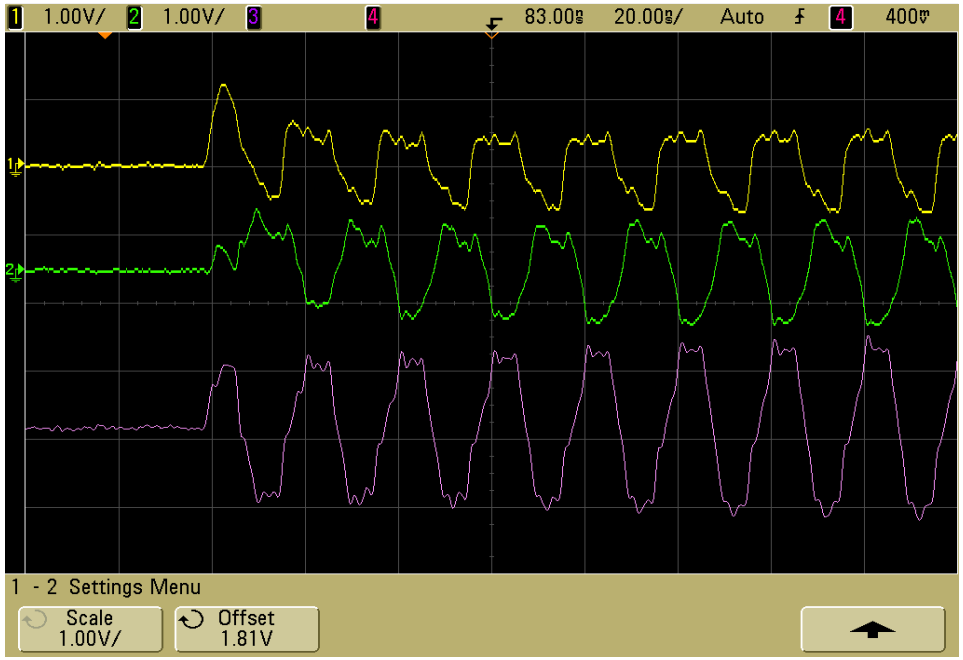
Steve Thomas, Peter Murray, RAL

Clock Driver for CPC2 : CPD1



Steve Thomas, Peter Murray, RAL

- Designed to drive:
  - ❖ Outer layer CCDs (127 nF/phase) at 25 MHz
  - ❖ L1 CCD (40 nF/phase) at 50 MHz
  - ❖ CPC2 requires ~21 Amps/phase!
- One chip drives 2 phases, up to 3.3 V clock swing
- 0.35 µm CMOS process, chip size 3×8 mm^2
- Careful layout on- and off-chip to cancel inductance



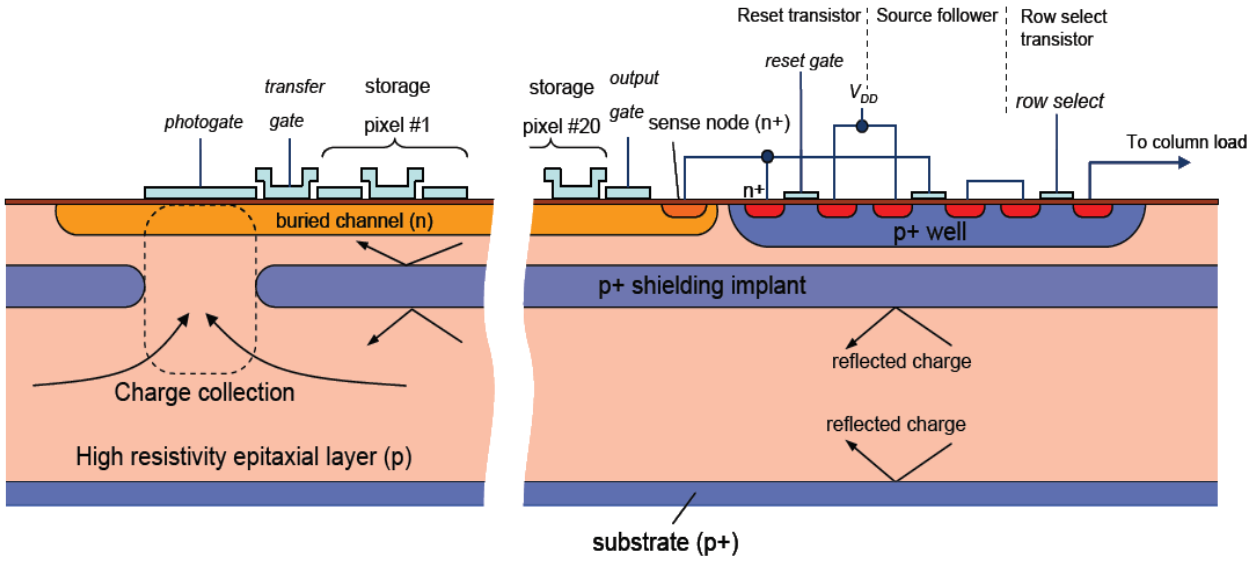
2 $V_{pk\text{-}pk}$ differential clocks

Tests:

- CPD1 driving 32 nF-equivalent internal load at 50 MHz
- Hope to maintain the same performance when bump-bonded to a CCD

Rui Gao, Andrei Nomerotski, Oxford U

In-situ Storage Image Sensor (ISIS)



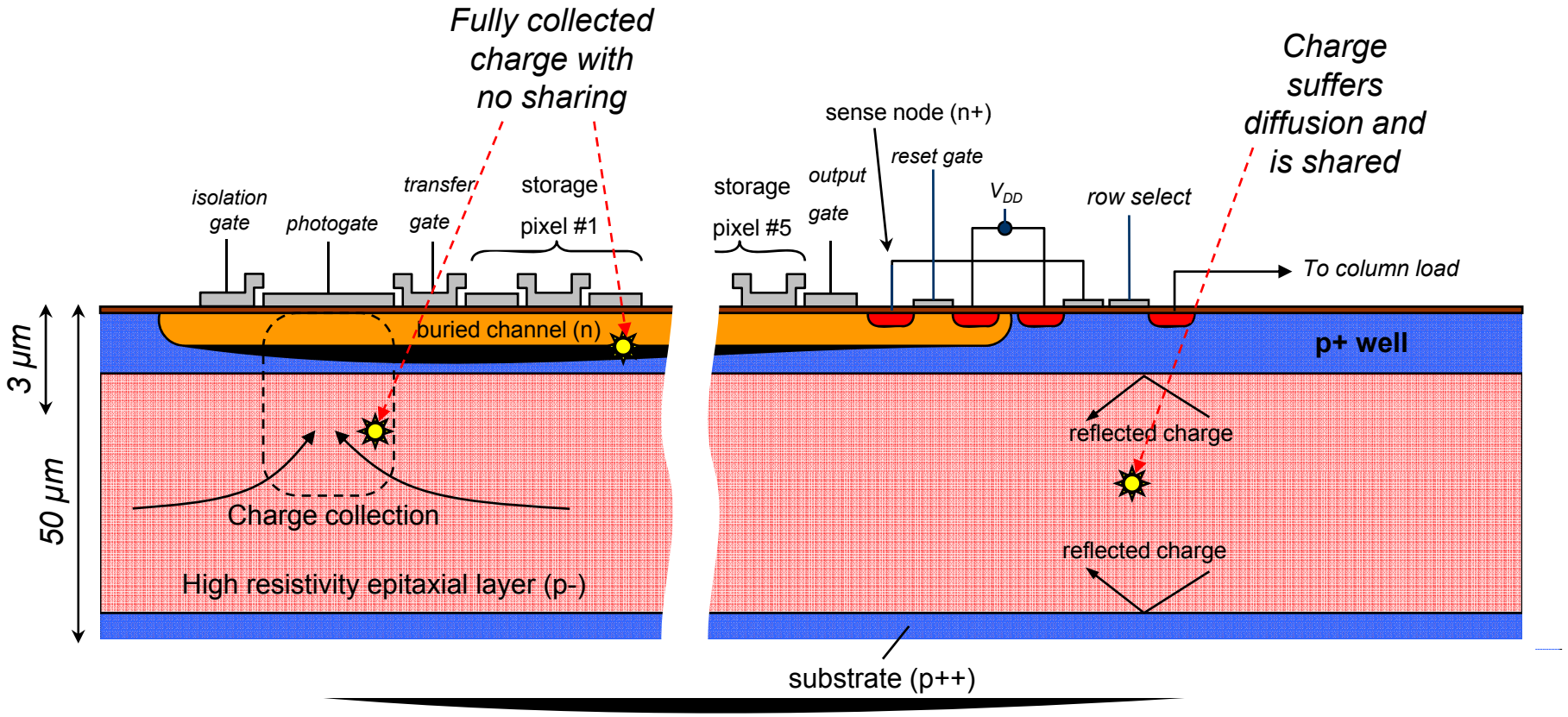
Chris Damerell, RAL

Operating principles of the ISIS:

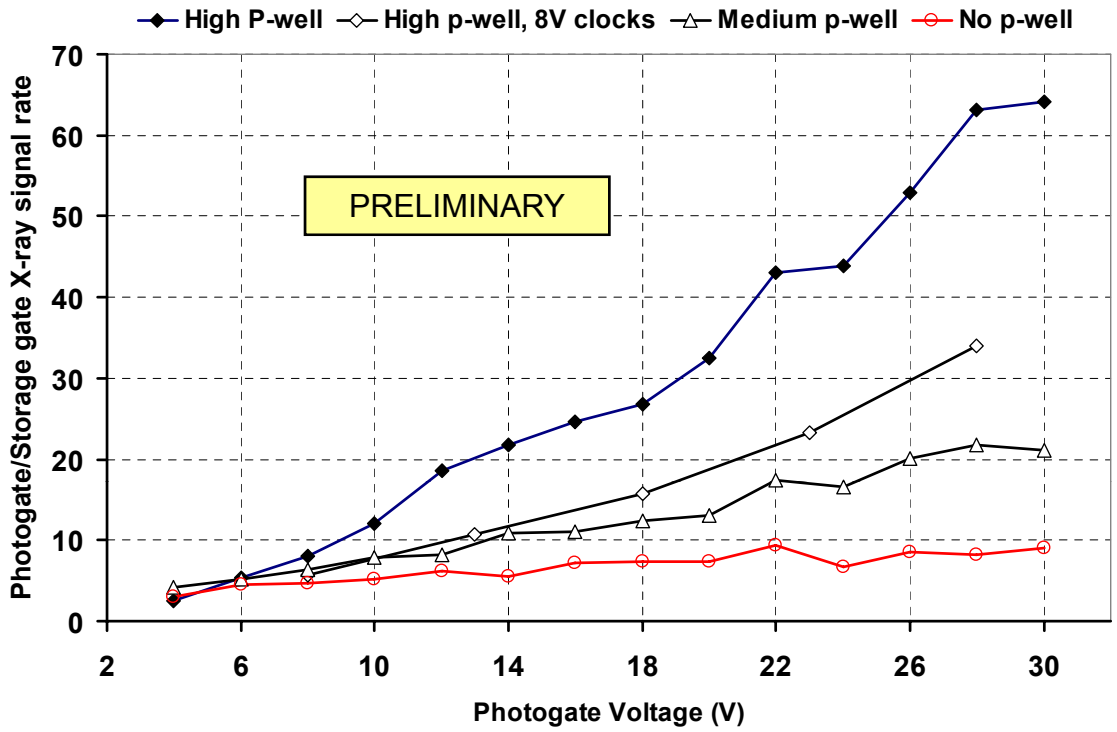
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup);**
4. **1 MHz column-parallel readout is sufficient;**

ISIS1 (p-well) – Experimental Results

- In the new, revised p-well ISIS1 we studied :
  - ❖ Is the p-well reflecting charge as intended?
  - ❖ When and where is the p-well punched through?
- Using 5.9 keV X-rays (30 μm attenuation length in Si, converted charge in ≈1 μm sphere)



ISIS1 (p-well)



Plotting the ratio *R*:

$$R = \frac{\text{Charge collected on the photogate}}{\text{Charge collected on a storage pixel}}$$

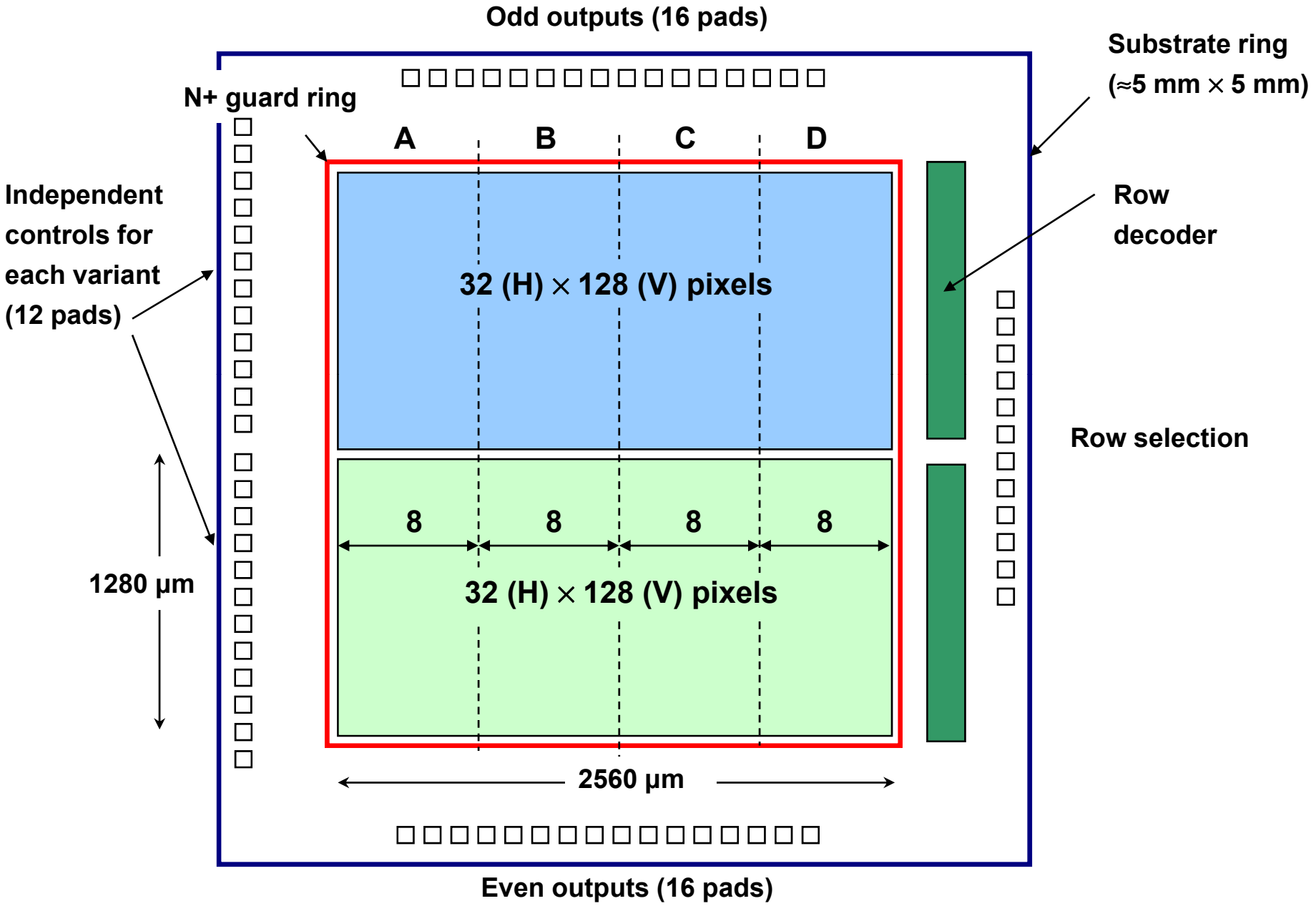
Gary Zhang, RAL

- "High p-well" – good protection of the storage register due to charge reflection
- The p-well works!
  - ❖ The p-well under the storage gates can be punched through by higher clock amplitudes – *R* drops
- Lower ratio with the medium-doped p-well due to lower potential barrier
- "No p-well" – only gate geometry and bias play role, *R* is the lowest

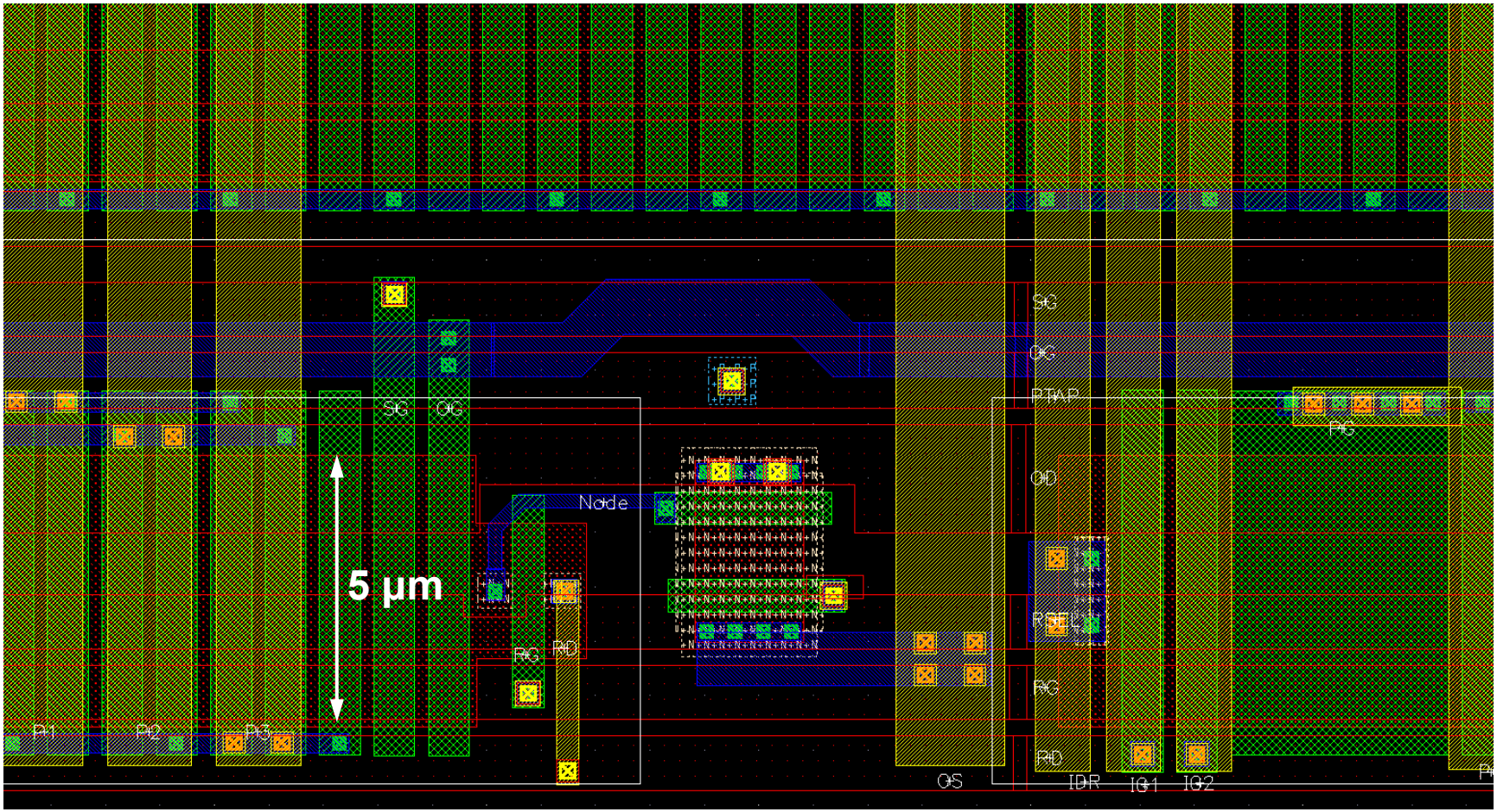
Development of the New ISIS2

- Jazz Semiconductor agreed to develop the CCD buried channel implant and the deep p+ implant
  - We supply our custom doping profiles
- The process is 0.18 µm dual gate oxide (1.8 V/5 V)
- Wafers with custom epitaxial layer: 25 µm, ≥100 Ω.cm on p++ substrate
- Will use ¼ of the mask set + 2 additional masks on MPW to reduce costs
- Option to process 5 or 10 wafers, each with process variations, e.g. different doping levels
- Our wafers will be processed independently from the other customers'
- Area = 1 cm^2
- Design is well advanced!
  - 40% complete: pixel layout and logic for row selection done

ISIS2 – Chip Layout



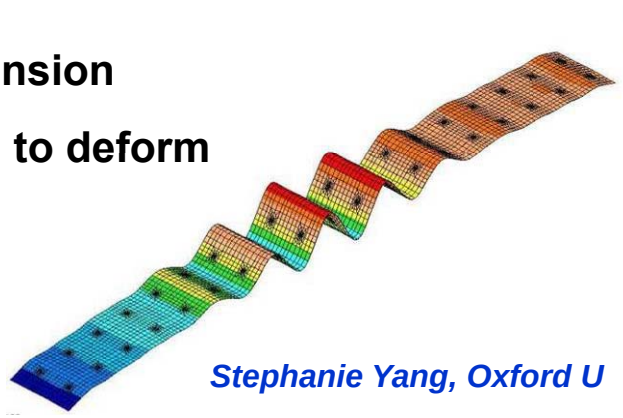
ISIS2 – Preliminary Pixel Layout



- 80 µm × 10 µm pixels, 5 µm wide buried channel, 3 metal layers
- Consulting with CCD and CMOS experts
- Target tape-out date = 8 April 2008

Mechanical Support Studies

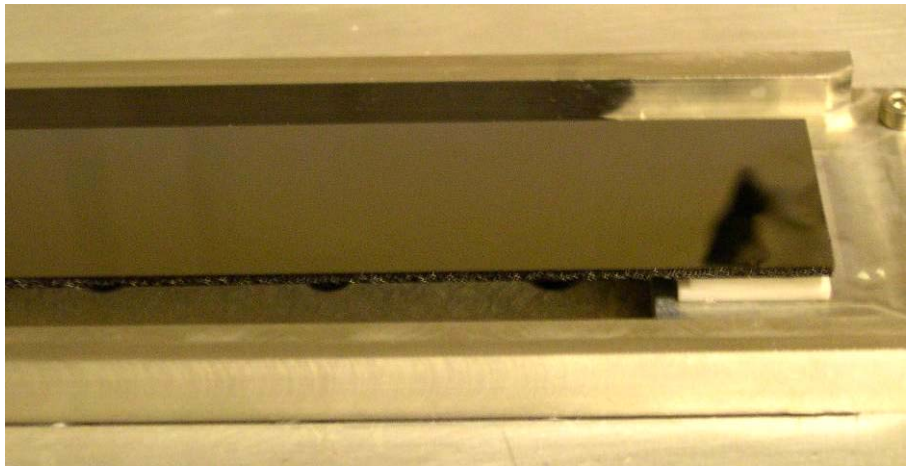
- Goal is 0.1% X_0 per ladder or better, while allowing low temperature operation (~170 K)
- Active detector thickness is only 20 μm
- Unsupported silicon
  - ❖ Stretched thin sensor (50 μm), prone to lateral deformation
  - ❖ Fragile, practically abandoned
- Silicon on thin substrates
  - Sensor glued to semi-rigid substrate held under tension
  - Thermal mismatch is an issue – causes the silicon to deform
  - Many studies done for Be substrate
- Silicon on rigid substrates
  - Shape maintained by the substrate
  - Materials with good thermal properties available
  - Foams offer low density and mass while maintaining strength



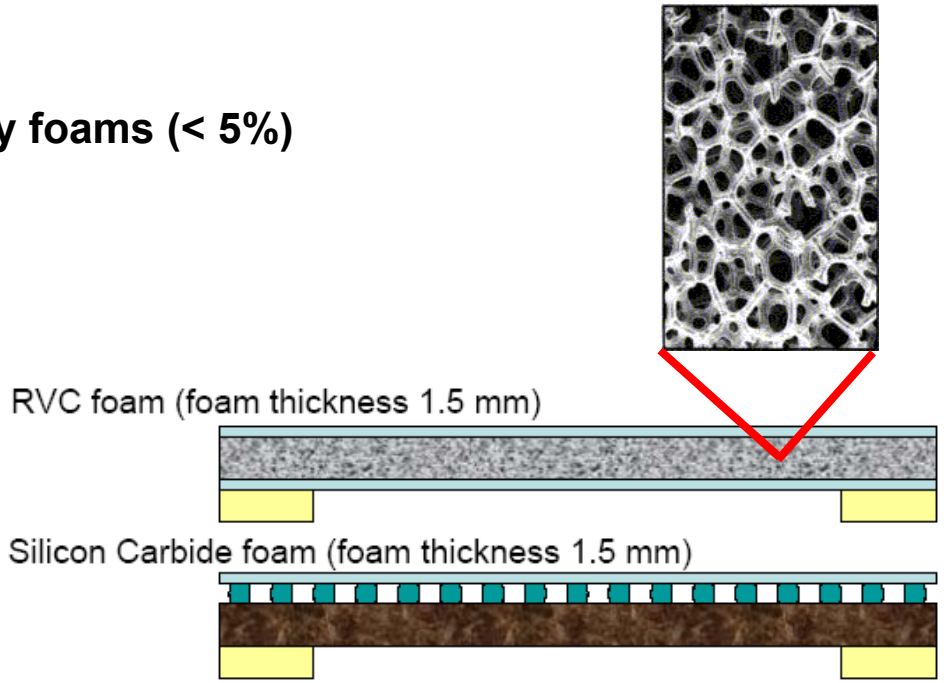
Stephanie Yang, Oxford U

Mechanical Support Studies

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~ 3% density)
  - Foam (1.5mm thick), sandwiched between two 25 μm silicon pieces – required for rigidity
  - Achieves 0.09% X_0
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 μm) on SiC foam (1.5mm);
  - Achieves 0.16% X_0
  - 0.09% X_0 possible with lower density foams (< 5%)



Thanks to Erik Johnson, RAL



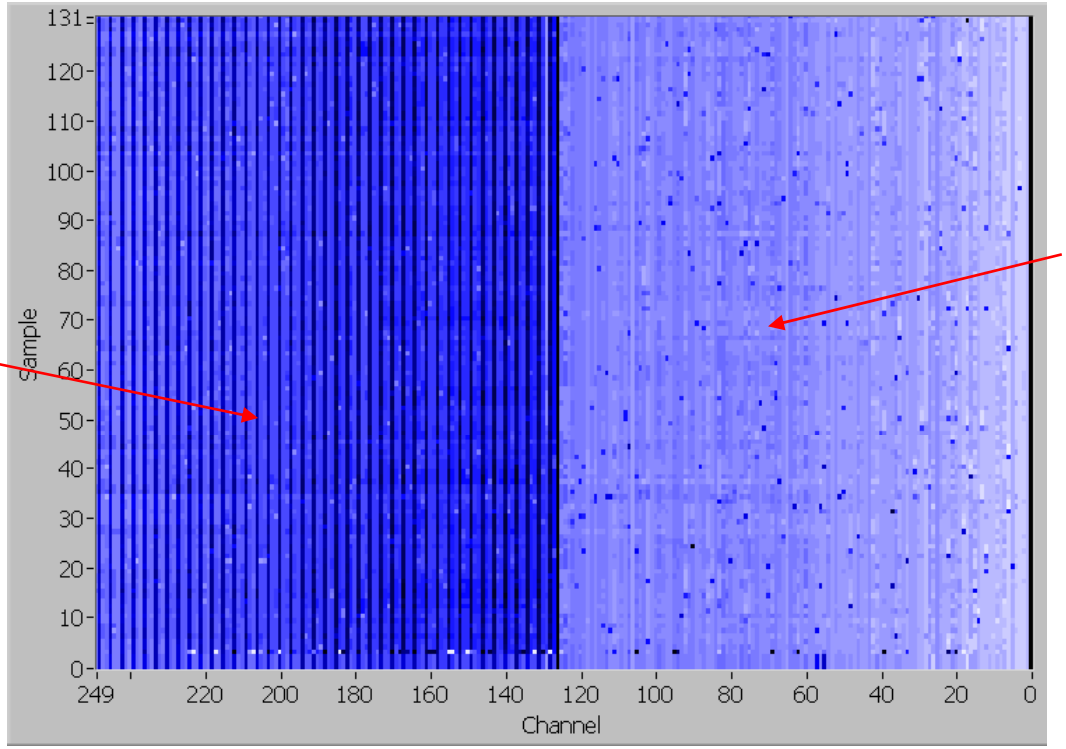
Conclusion

- Detector R&D is progressing very well
- CPCCD programme:
  - ❖ Bump-bonded assemblies CPC2-40/CPR2 reach 9 MHz
  - ❖ Programme for capacitance and clock amplitude reduction underway
  - ❖ Driver system with CMOS ASICs or transformers
  - ❖ Third generation readout chip CPR2A to be delivered in April
- ISIS development:
  - ISIS1 with p-well shows good protection from parasitic charge collection
  - Now designing ISIS2 in CMOS process
- Mechanical support aims at $\leq 0.1\%\ X_0$ using modern materials

Extra Slides

CPC1/CPR1 Performance

5.9 keV X-ray hits, 1 MHz column-parallel readout



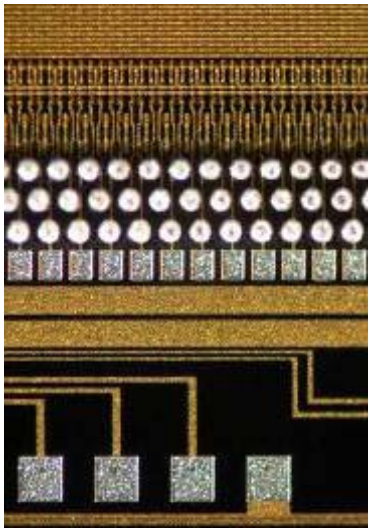
Charge outputs, inverting (positive signals)

Noise ≈100 e-

Voltage outputs, non-inverting (negative signals)

Noise ≈60 e-

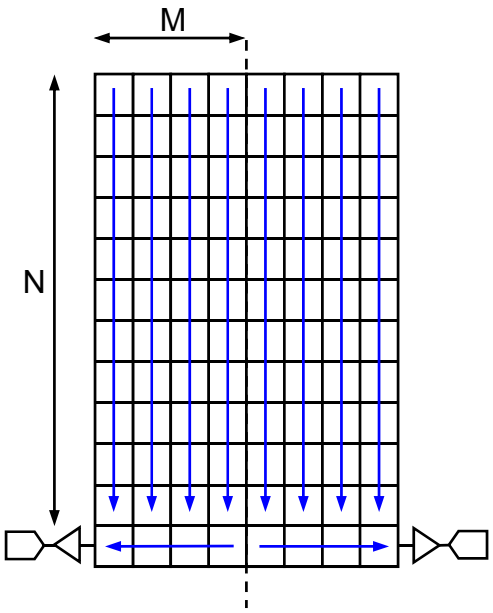
- **First time e2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% : mechanical damage during compression suspected**
- **Differential non-linearity in ADCs (100 mV full scale) : addressed in CPR2**



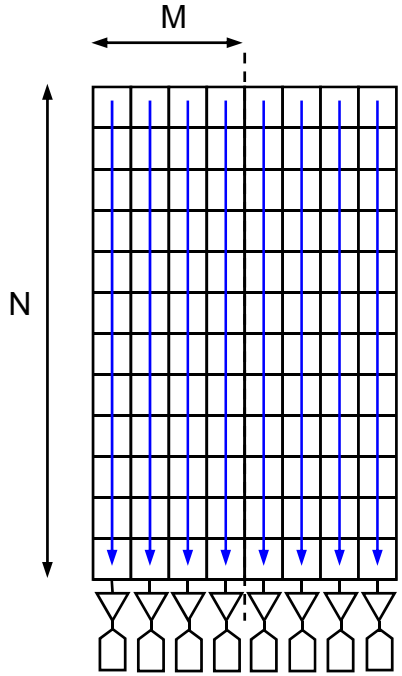
Bump bonds on CPC1 under microscope

The Column Parallel CCD

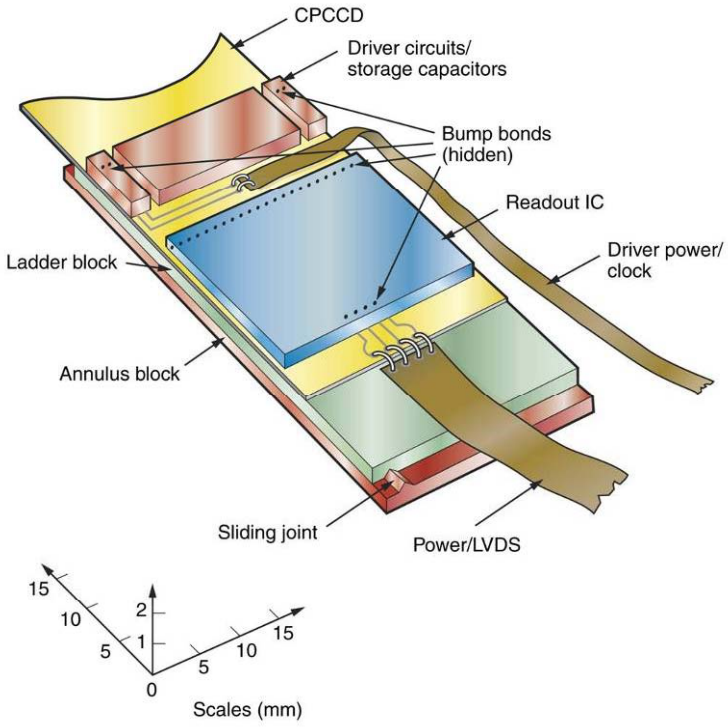
- Main detector work at LCFI
- Every column has its own amplifier and ADC – requires readout chip
- Readout time shortened by orders of magnitude
- All of the image area clocked, complicated by the large gate capacitance
- Optimised for low voltage clocks to reduce power dissipation



"Classic CCD"
Readout time ≈
$N \times M / f_{out}$

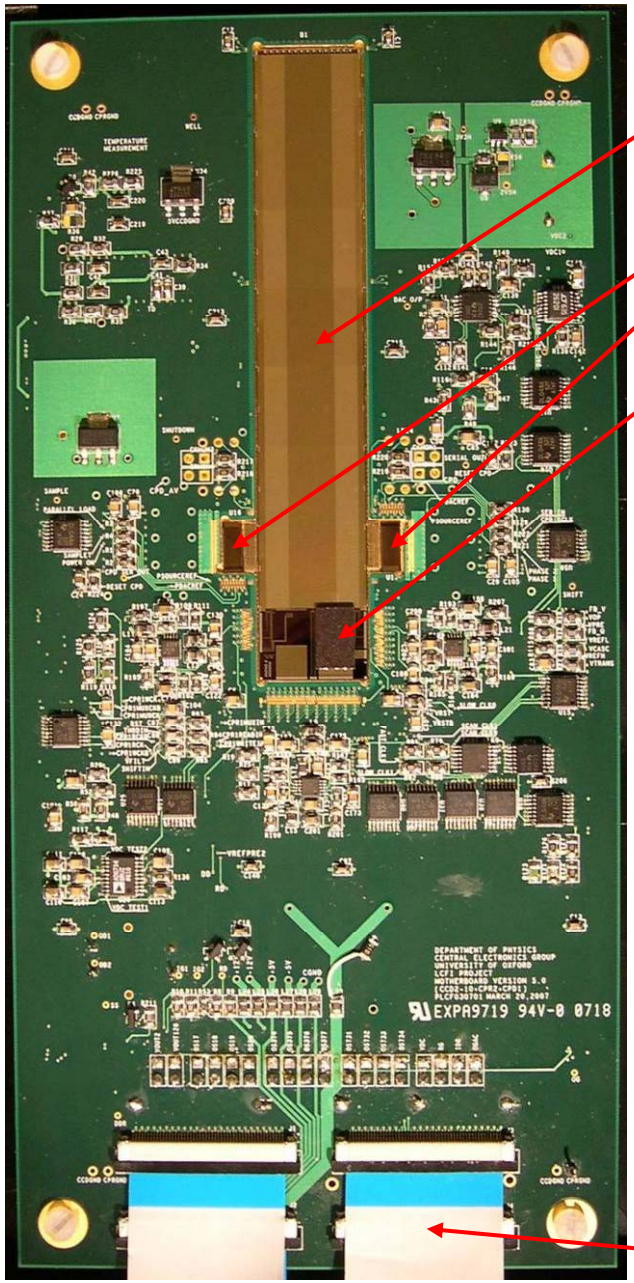


Column Parallel CCD
Readout time = N / f_{out}



CPC2, CPR2 and CPD1 All Together

104 mm

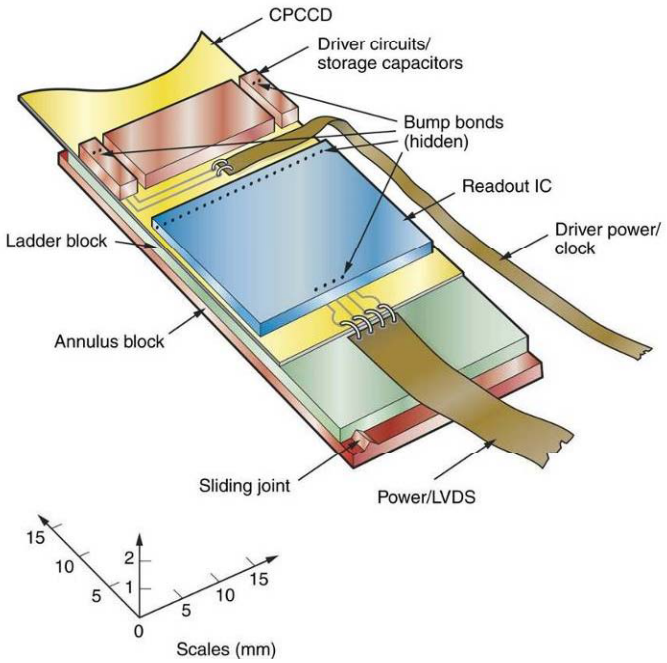


CPC2-70

Two driver chips CPD1

Bump-bonded CPR2

Flexible cables



Getting closer to a prototype detector ladder!