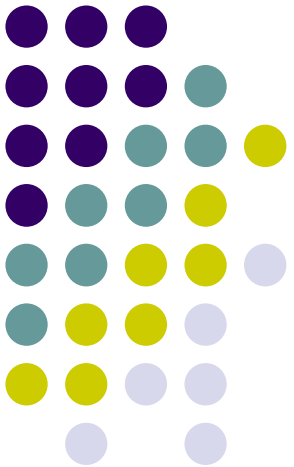
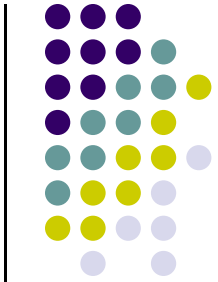
FPCCD Vertex Detector for ILC

Yasuhiro Sugimoto
KEK
@TILC08



- Concept of FPCCD VTX
- FPCCD prototype
- VTX inner radius

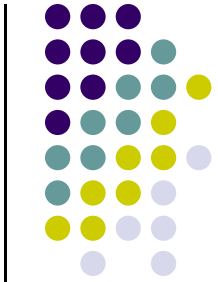
Basic concept



- Pair background at small R
  - ~5000 hits/cm^2/train with B=3T and R=20mm
  - Pixel occupancy ~10% for 25μm pixel (several pixels are fired for one track hit)
  - In order to keep the occupancy small (<1%),
    - read out 20 times per train (1ms), or
    - 20 times finer pixel ➔ Fine Pixel CCD (FPCCD)

    is necessary

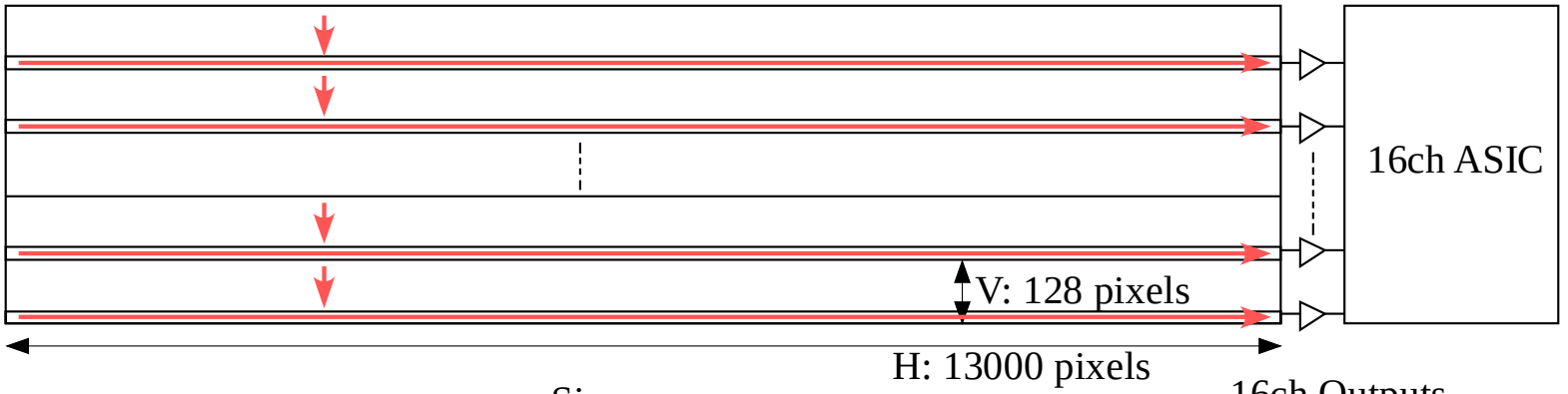
Advantages of FPCCD VTX



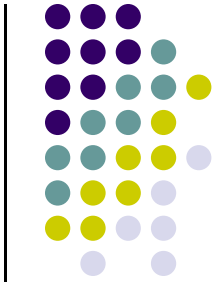
- Completely free from beam-induced RF noise (EMI)
- Excellent spatial resolution of σ_x~1.4μm even with digital readout
- Excellent two-track separation capability because of fine pixels and fully depleted epitaxial layer
- Capability of low-energy pair-background rejection by making use of hit-cluster shape
- Simple structure which enables large wafer size with high yield rate
- No heat source in the image area
- No need for very high readout speed

Schematic design

- Sensor and ASIC
  - ~5μm square pixel
  - Multi-port readout to reduce readout time (<200ms) with moderate readout speed (~10Mpixels/s)
  - Small number of V-shift and large number of H-shift to reduce effect of radiation damage (CTI)
  - 15 – 20 μm thick fully depleted epitaxial layer



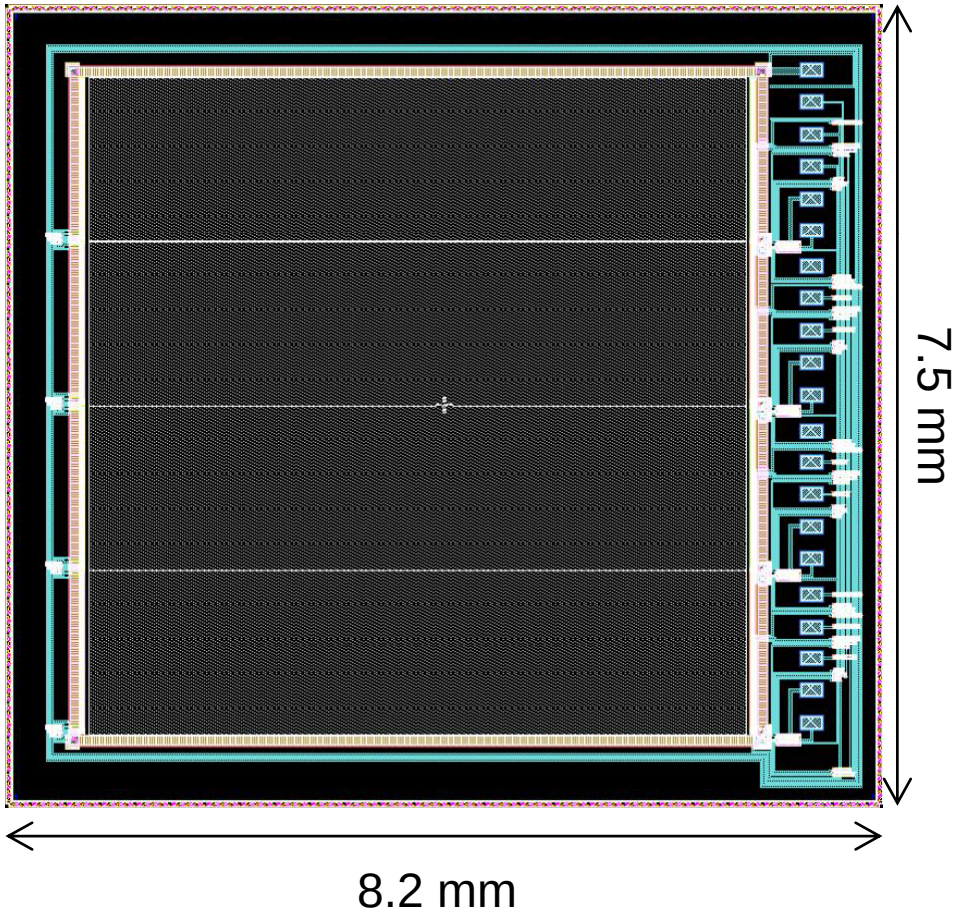
R&D for FPCCD sensor



- Challenges of FPCCD
  1. Small pixel size ~5 μm
  2. Readout speed > 10 MHz
  3. Noise < 50 electrons (preferably <30 electrons)
  4. Power consumption < 10 mW/ch
  5. Horizontal register (same size as pixel) in the image area
  6. Wafer thickness ~50 μm
  7. Multi-channel low power readout ASIC ➔ Takubo's talk
- Prototype sensor in FY2007
  - Tackle issues 2, 3, 4, and 5

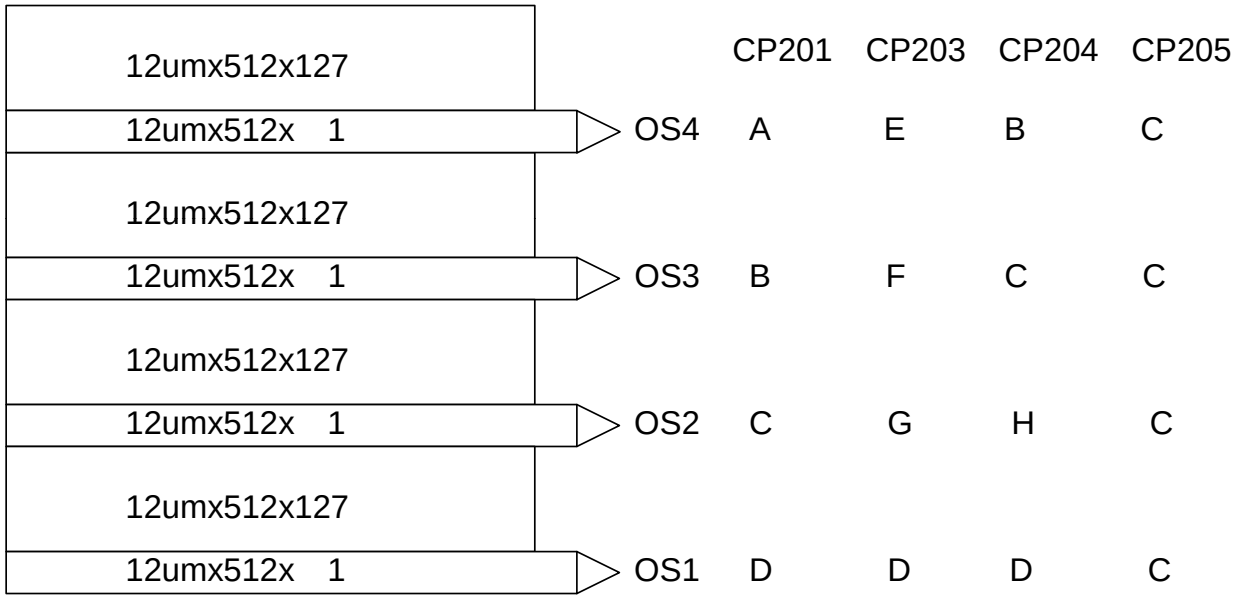
Prototype of FPCCD

- 12μm pixel size
- 512x512 pixels
- 6.1x6.1 mm^2 image area
- 4ch /chip
- 128(V)x512(H) pixels for each channel
- Several different designs of output amp
- Chips have been made and are being tested by HPK
- To be delivered in few weeks



Types of Prototype

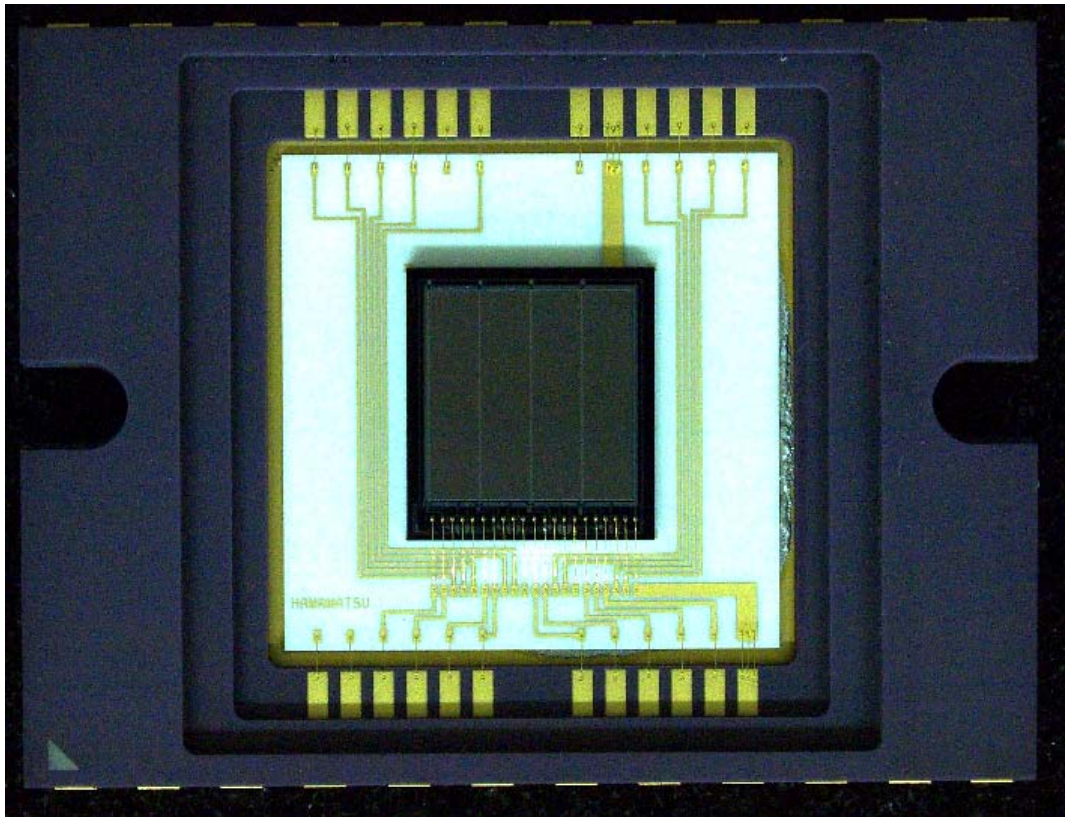
- Output amp: type A – H

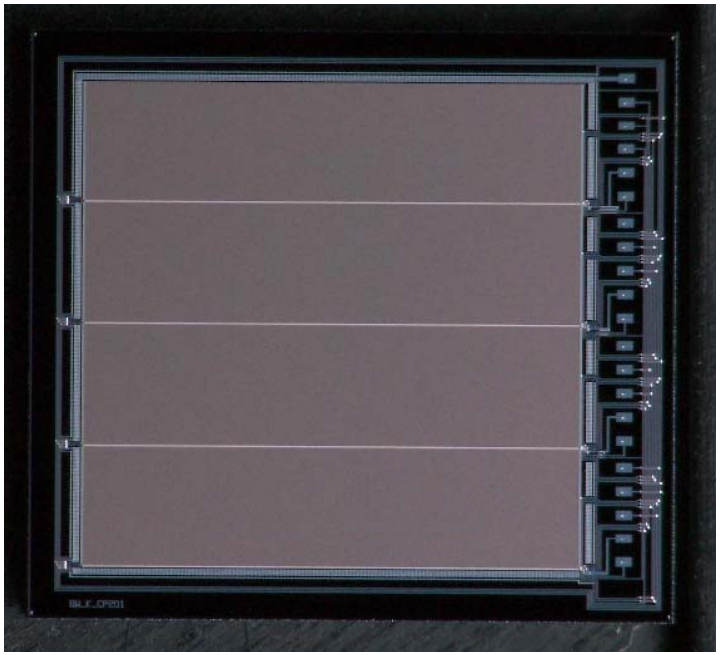


	CP201	CP203	CP204	CP205
OS4	A	E	B	C
OS3	B	F	C	C
OS2	C	G	H	C
OS1	D	D	D	C

- Process / Device type
  - Wafer: epitaxial layer 24 / 15 μm
  - Gate SiO_2 for output Tr: standard (all) / thin (CP204, 205)
  - Device type: package / bare chip

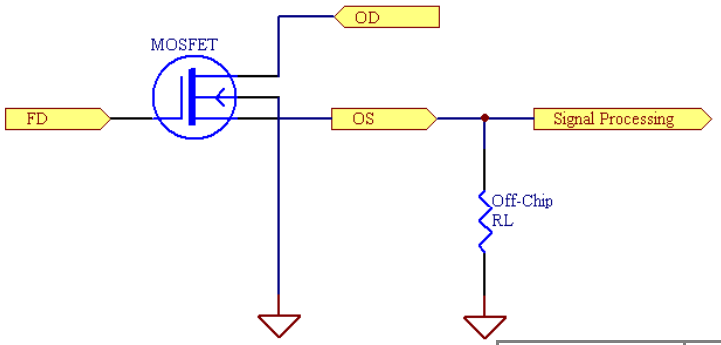
Packaged and bare chip



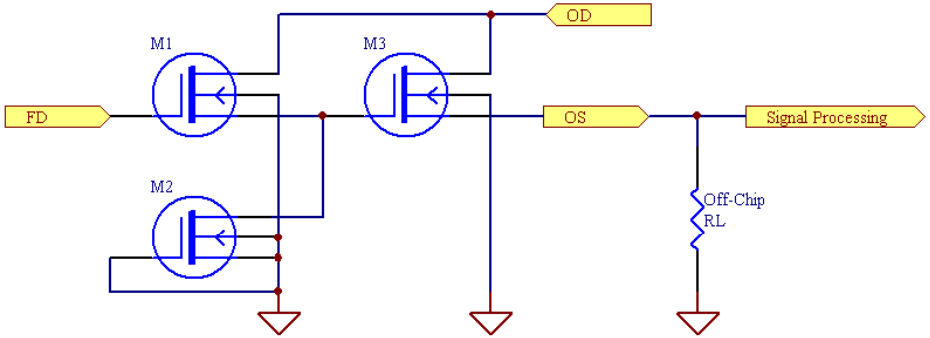


Output amp

- Type D

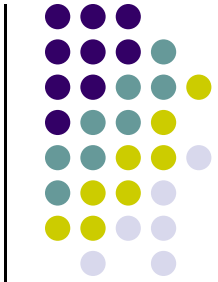


- Others



Type	M1	M2	M3
A	M1-Type1	M2-Type1	M3-Type1
B			M3-Type2
C			M3-Type3
E		M2-Type2	M3-Type2
F			M3-Type3
G			M3-Type4
H		M2-Type1	M3-Type4
Remark		Type1 > Type2 at drain current	Type1 > Type2 > Type3 > Type4 at drain current

Characteristics of Prototype



- Preliminary results given by HPK

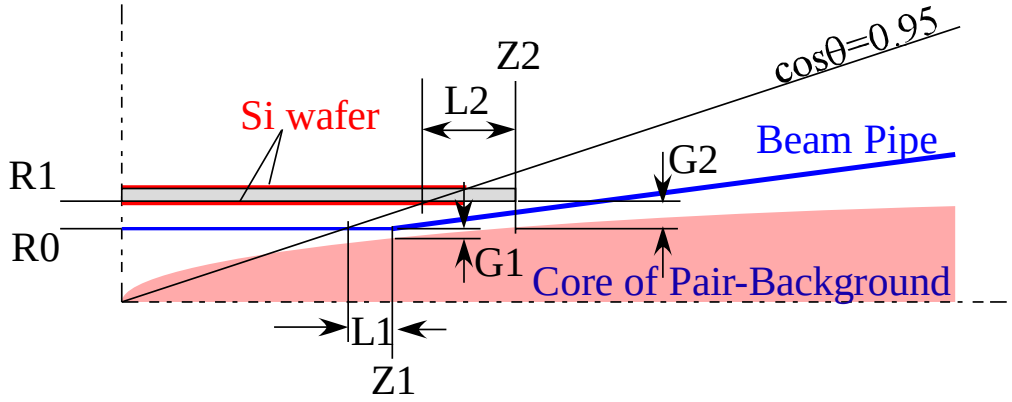
Device type	Package		Bare chip	
Epi thickness (μm)	15	24	15	24
V-register gate capacitance (pF)	1600	550	1600	550
H-register gate capacitance (pF)	40	40	40	40
Output source capacitance (pF)	<4	<4	<2	<2

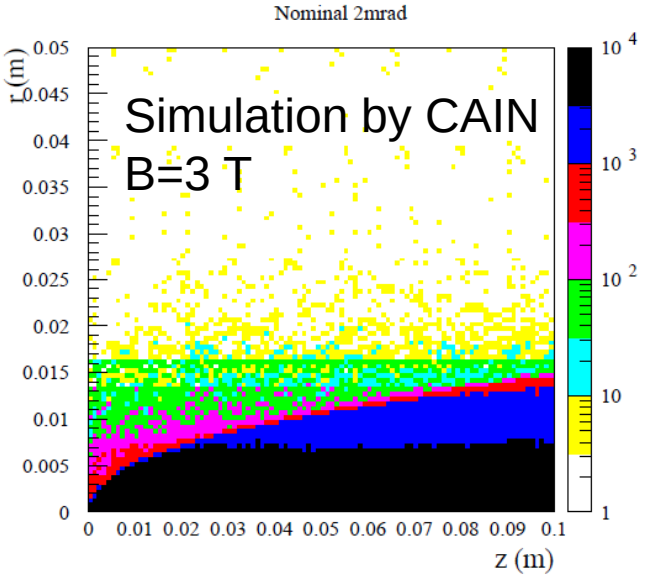
Amp type		A	B	C	E	F	G
Output gain (μV/e)	Epi:15 μm	5.4	5.3	5.2	6.9	6.2	5.6
	Epi:24 μm	5.8	5.3	5.0	6.6	5.9	5.4
Id (mA)	Epi:15 μm	1.57	1.55	1.50	1.28	1.22	1.14
	Epi:24 μm	1.48	1.44	1.38	1.15	1.09	0.99

V_{OD}=10V, R_L=10kΩ, 10MHz, RT

Study on inner radius

- Design criteria
  - Reasonable clearance between pair-background core and beam pipe, and between beam pipe and ladder





G1=2mm, G2=4mm, L1=5mm, L2=20mm

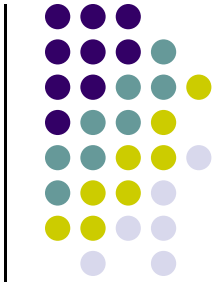
B (T)	E_{CM} (GeV)	Option	R_0(mm)	R_1(mm)
3	500	Nominal	13	17.5
3	500	Low P	17	22

Strong dependence on machine parameters

(500GeV Nominal)

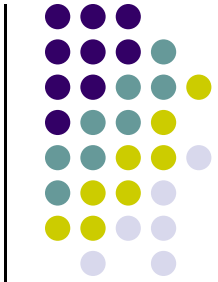
B (T)	R_0(mm)	R_1(mm)
3	13	17.5
3.5	12	16
4	11.5	15

Summary and outlook

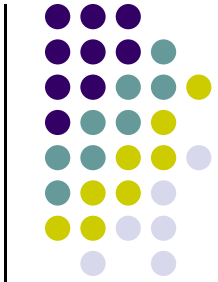


- The first prototype FPCCDs have been made by HPK and will be delivered soon
  - Pixel size: 12μm
  - H-register same size as pixels in image area
  - 4ch/chip
  - Several types of output circuit
  - Two different epitaxial layer thickness (15 / 24 μm)
  - Two different gate oxide thickness for output transistors
- Detailed study on the prototype FPCCDs will be done in FY2008
- Radius of innermost layer Rin of VTX was studied for 3, 3.5, and 4T magnetic field, and Rin=17.5, 16, and 15 mm are proposed, respectively

Backup slide



Collaboration



- KEK
  - A. Miyamoto, K. Nakayoshi, Y. Sugimoto
- JAXA/ISAS
  - H. Ikeda
- Tohoku University
  - T. Nagamine, Y. Takubo, H. Yamamoto
- Tohoku Gakuin University
  - K. Abe

FPCCD VTX

- Vertex detector
  - Two CCD layers make a ladder in order to make mini-vector of tracks and reject pair-background tracks
  - 3 ladders make the vertex detector
  - Operation at ~-50 degrees
  - Ladders are confined in a cryostat
  - Angular coverage:
    - $|\cos\theta|<0.95$ with inner 4 layers
    - $|\cos\theta|<0.9$ with all 6 layers