DHCAL
PCB STUDY
For RPC

1 m² PCB SOLUTION

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Collaboration with LAPP and LAL

1 m² PCB MAIN SPECIFICATIONS

ASU PCB Design
- 24 x 64 1 sq cm pads
- 24 Hardrocs Asics chained

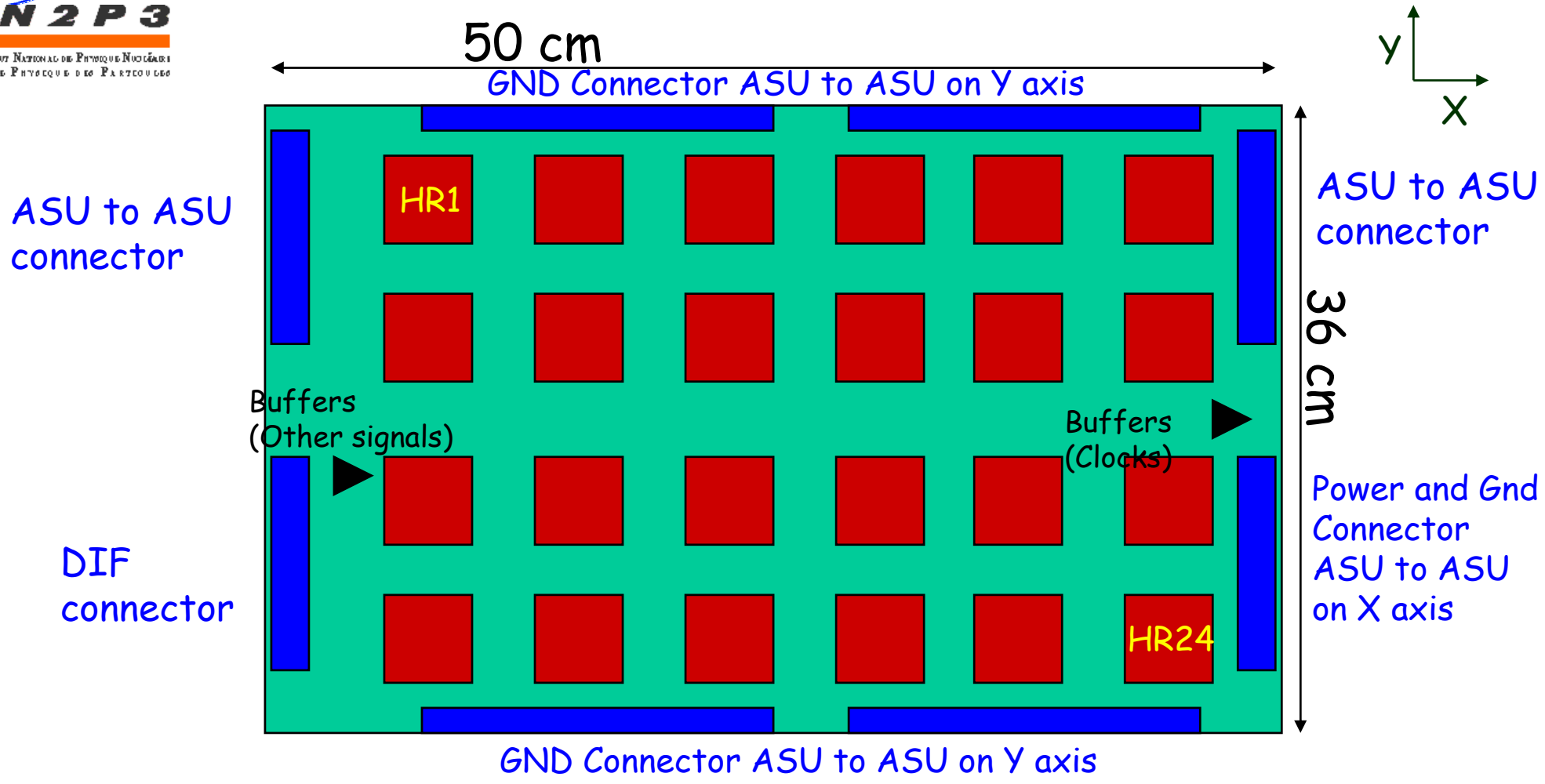
1 m2 PCB board :
- 6 ASUs
- 144 Hardroc Asics

DIF boards :
- 1 DIF for 1 ASU : 6 DIFs
- 1 DIF for 2 ASU : 3 DIFs

Buffered Signals
(Long Lines 1 m for Clock on 1 ASU):
- Slow Control
- Power_on
- Control for Analog Readout
- Digital Readout

Analog Readout :
- All OUT_Q are connected together
- EN_OTAQ switch on or off using DIF board and decoder

ASU PCB DESIGN



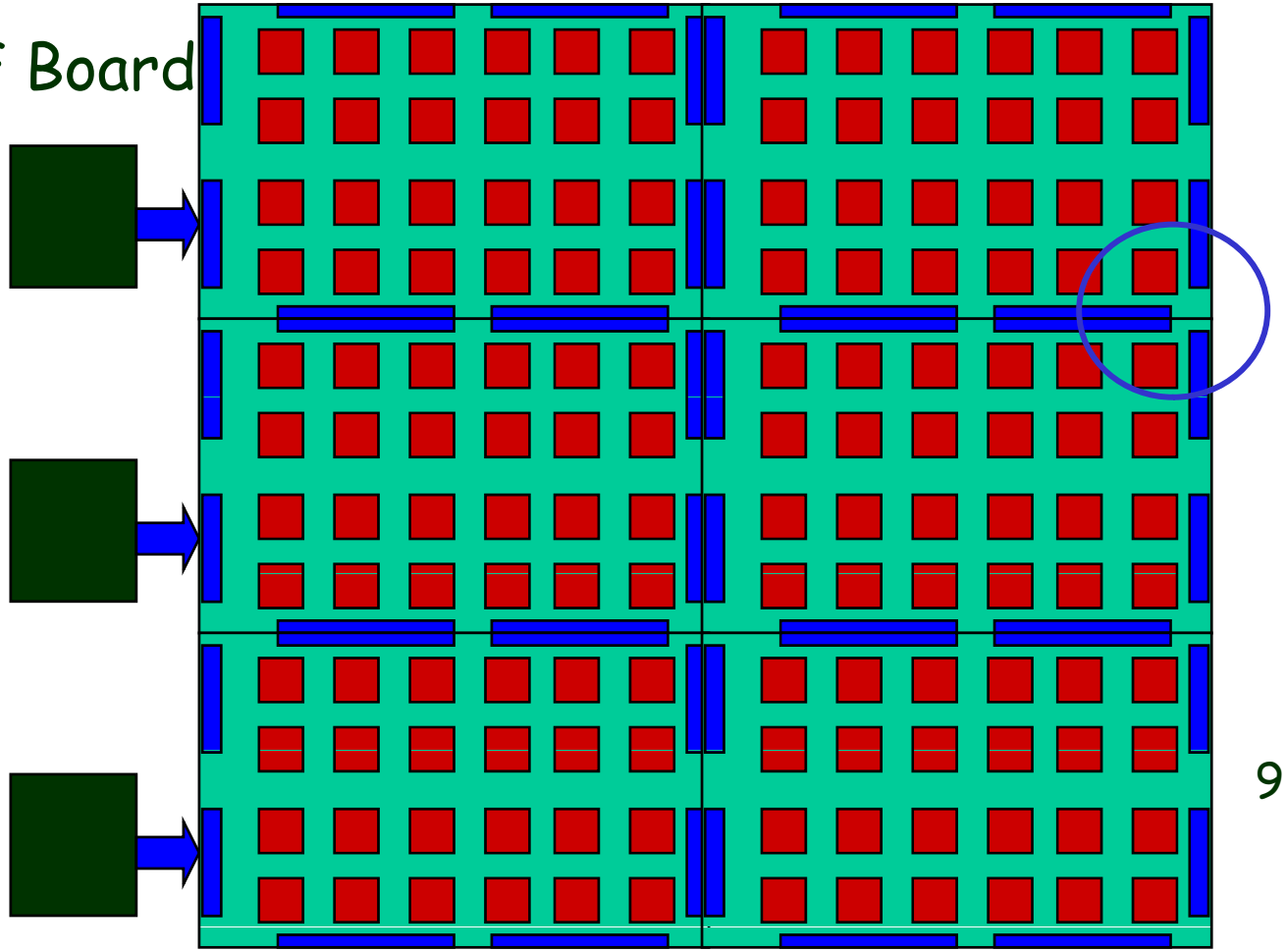
1536 pads on Bottom Layer

Buried and Blind Vias (Same as the last PCB with 4 HR)

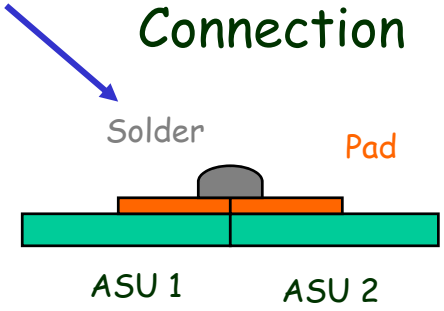
1 m² PCB DESIGN

1 DIF for 2 ASUs

DIF Board



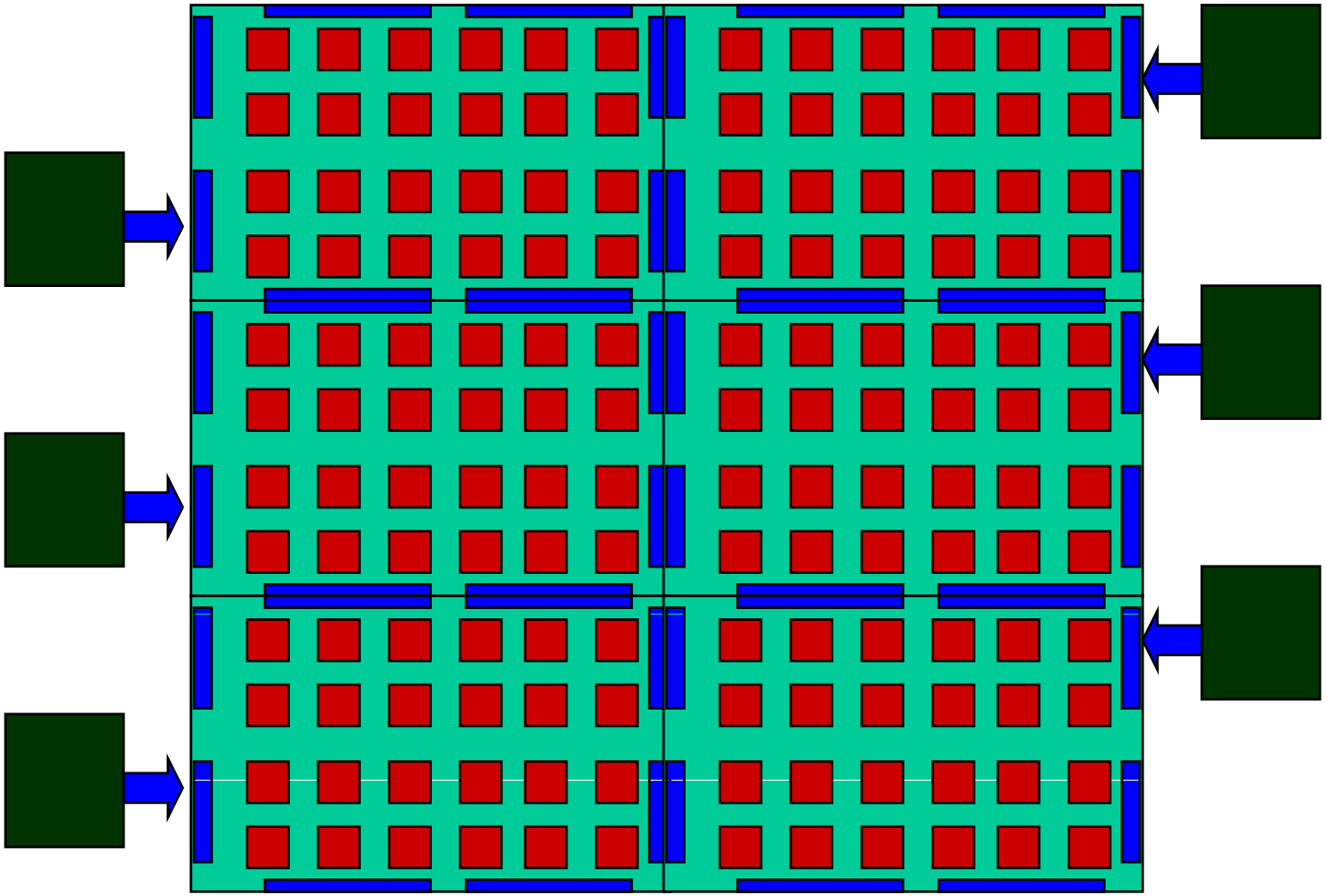
ASU to ASU Connection



9216 pads on Bottom Layer

1 m^2 PCB DESIGN

1 DIF for 1 ASUs



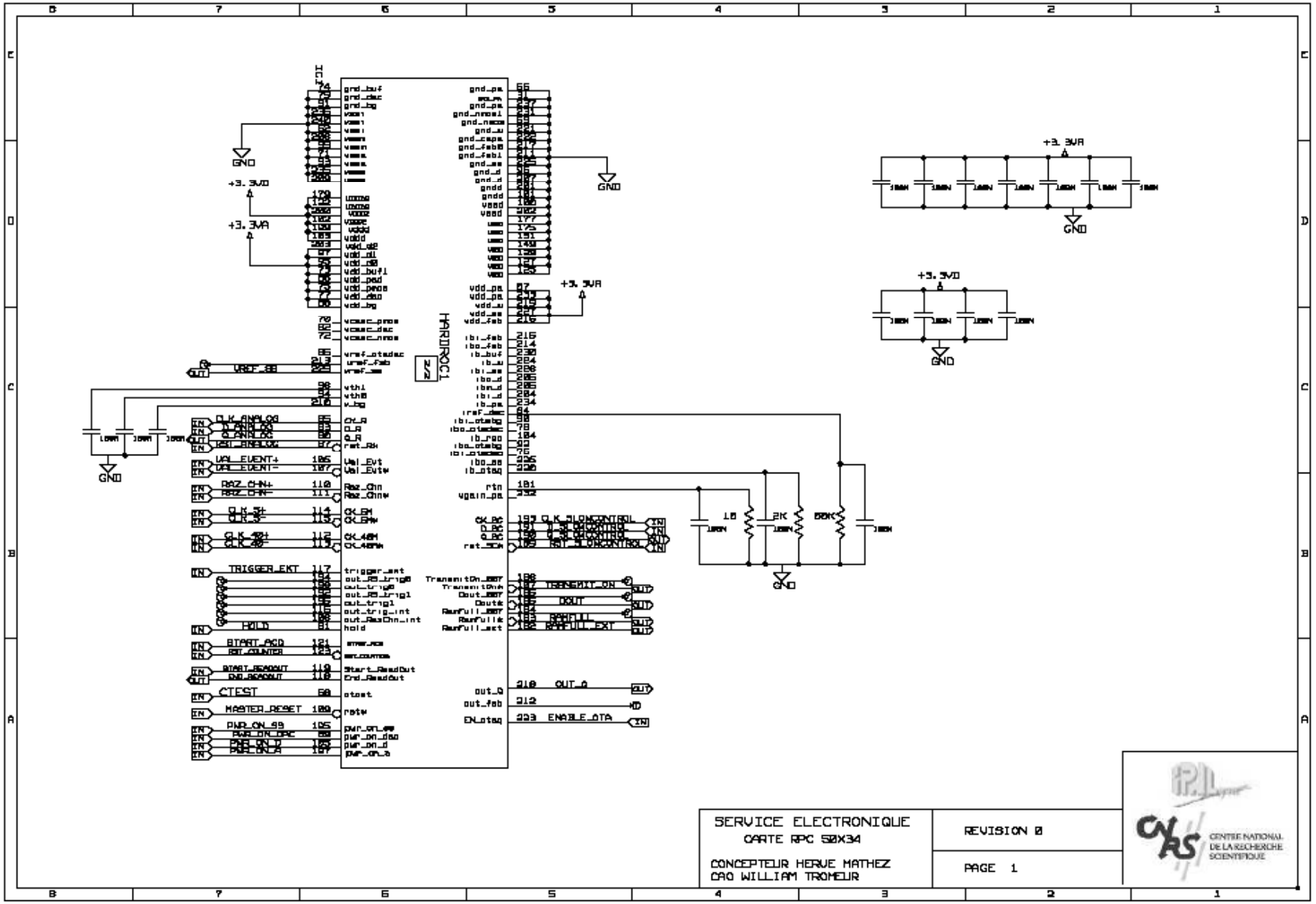
1 m^2 PCB DESIGN (Layers)

- Layer 1 (TOP) : interconnect
- Layer 2 : interconnect
- Layer 3 : 3.3V Digital
- Layer 4 : GND
- Layer 5 : 3.5V Analog
- Layer 6 : PADs to Hardroc
- Layer 7 : GND
- Layer 8 (BOTTOM) : PADs

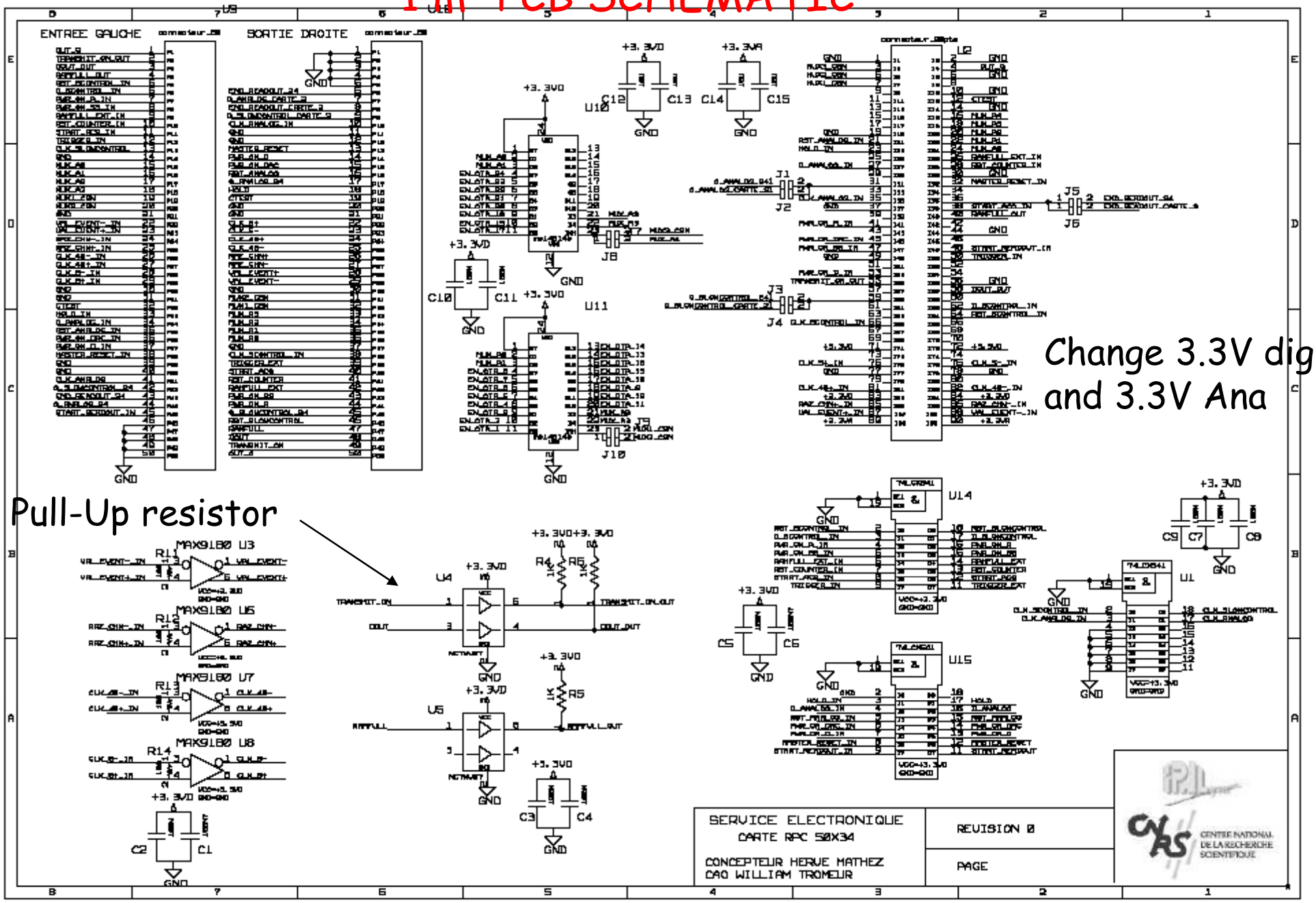
Pads to Hardroc interconnects are the same for the entire PCB (hierarchical design)

Send the Layout to Fab next week

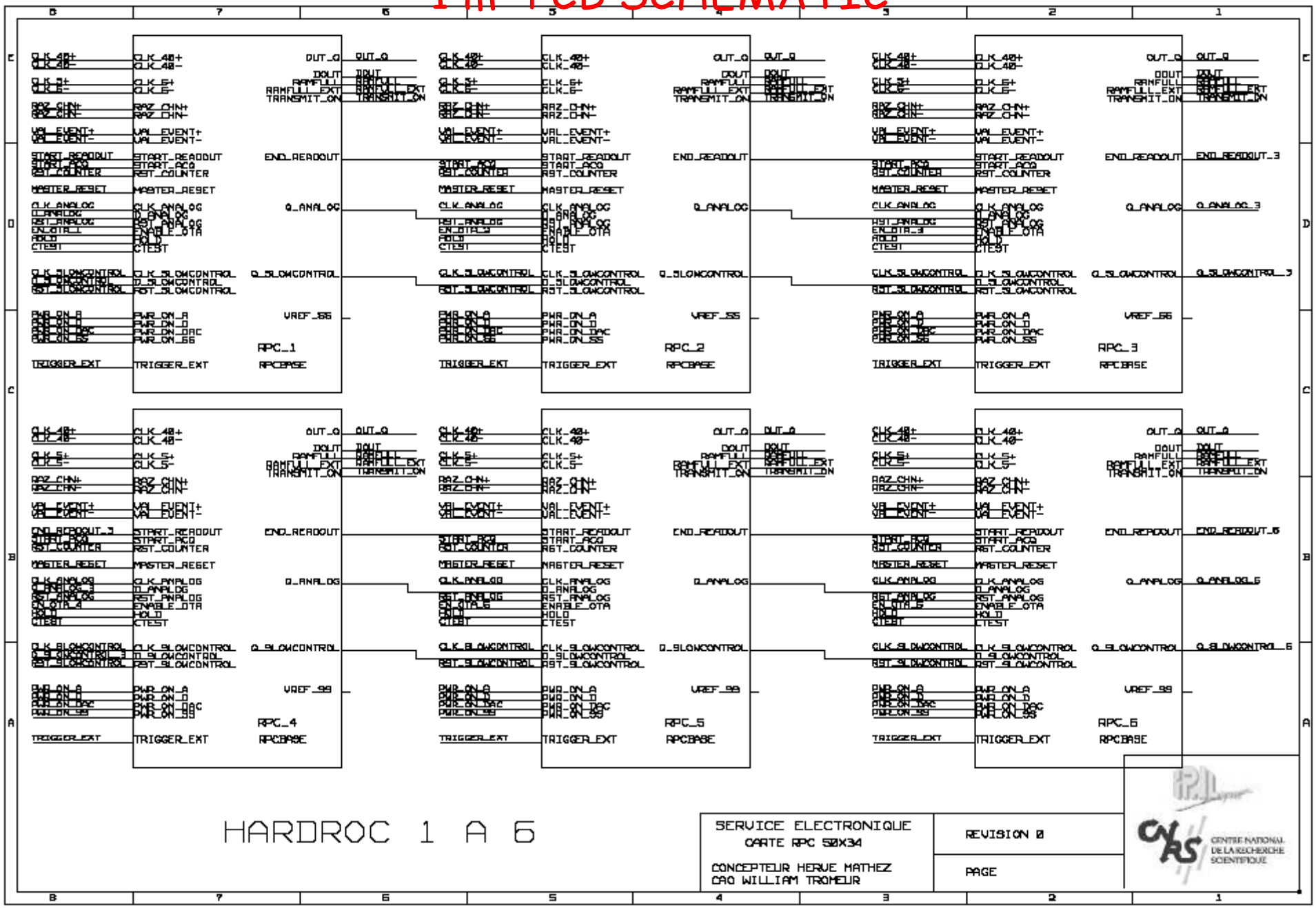
1 m² PCB SCHEMATIC



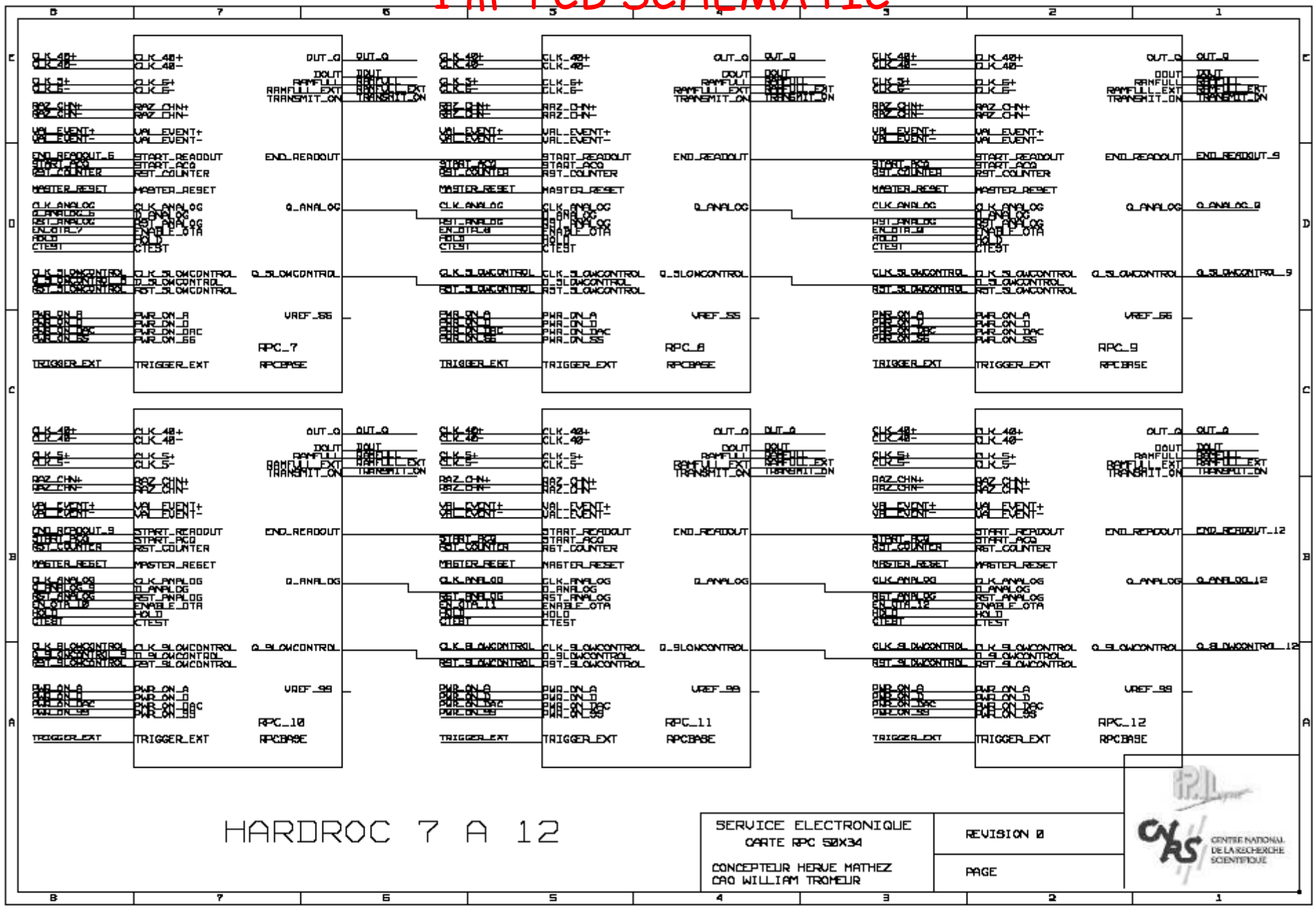
1 m² PCB SCHEMATIC



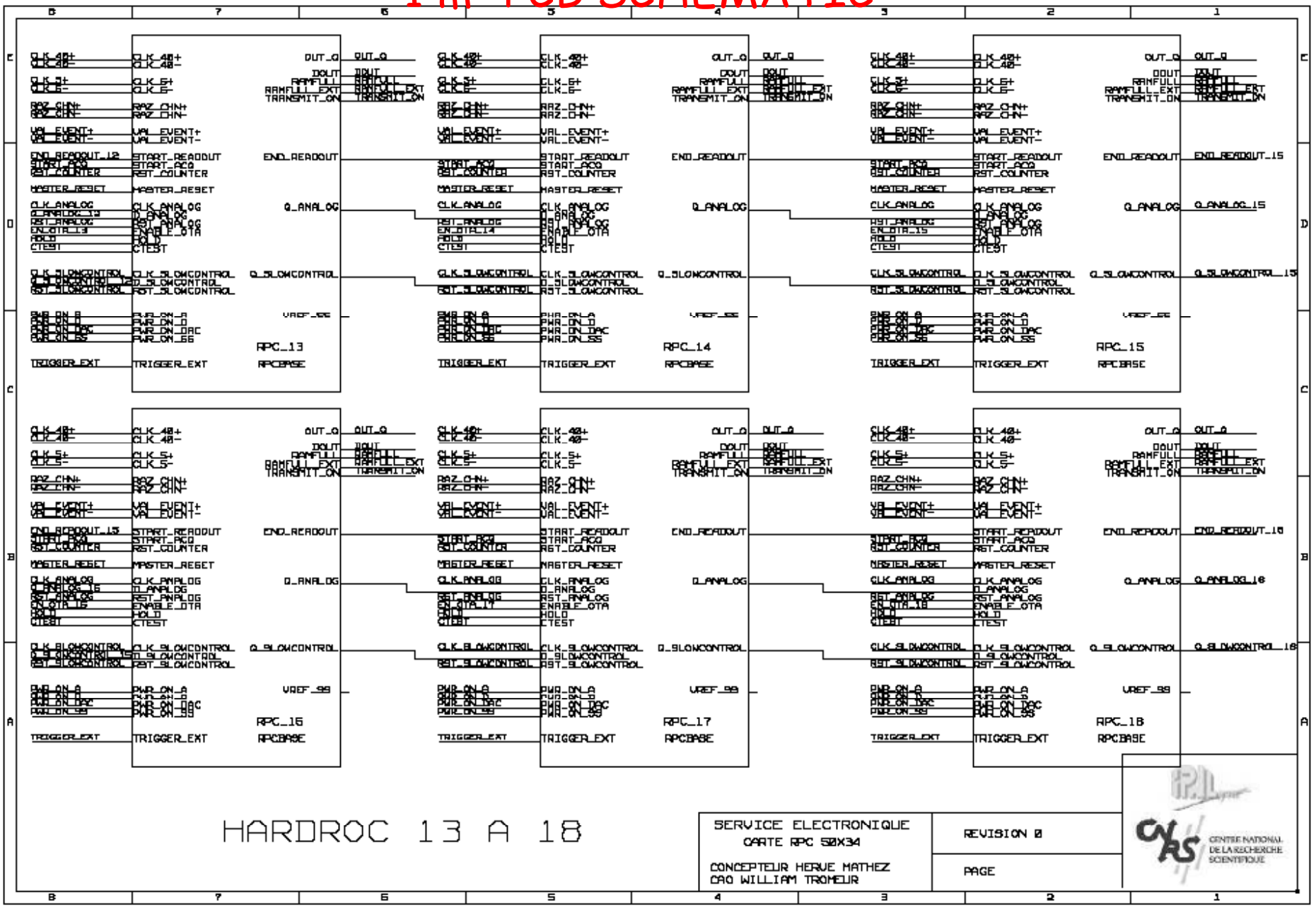
1 m² PCB SCHEMATIC



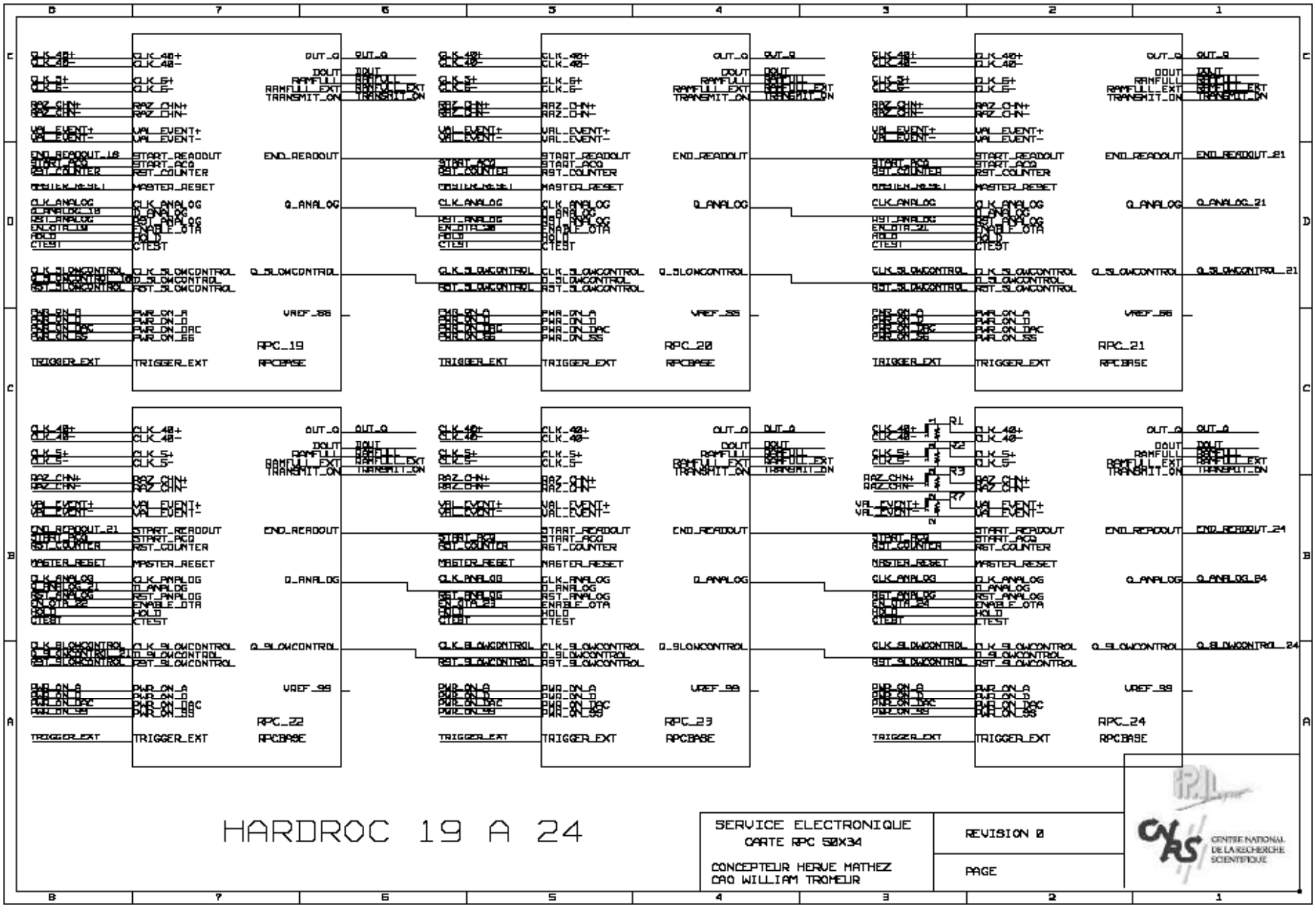
1 m² PCB SCHEMATIC



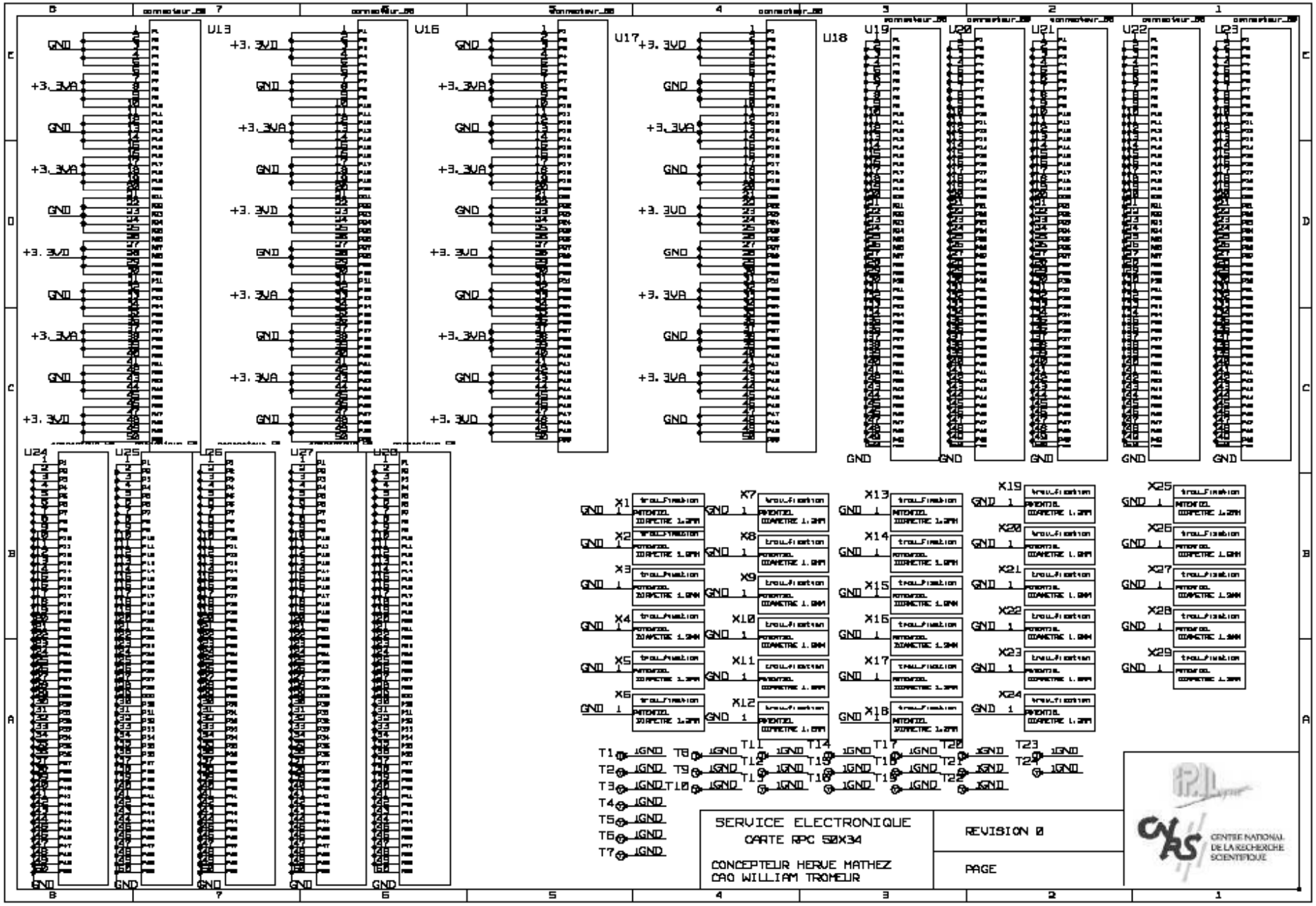
1 m² PCB SCHEMATIC



1 m² PCB SCHEMATIC



1 m² PCB SCHEMATIC



1 m² PCB SCHEMATIC